VIDEO PRODUCTS

DATABOOK

2nd EDITION

FEBRUARY 1994

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

This new, single-volume edition of the Video ICs Databook covers SGS-THOMSON's extensive dedicated video product range for television monitor, VCR and related applications. The voluminous datasheets on microcontrollers are now published in a separate book on Video Dedicated Microcontrollers, Another format change is that products are classified by function rather than being listed in alphanumerical order.

Included in this edition is information on a number of important new product families:

Advanced devices for analog satellite receivers and a complete new range of color TV cores covering PAL and SECAM applications - from the most basic, cost-effective solutions to the most competitive mid-range color TV.

For monitors there is a new family of wideband and vertical deflection amplifiers conforming to the industry standards of TDA1675 and TDA1170 and which demonstrate unparallelled performance in voltage and current ranges.

New video and audio matrices meet the increasing demand of connecting various devices to television sets (satellite, decoder, video games, VCRs and Camcorders). And responding to the need for low cost drums, is a new range of video head amplifiers.

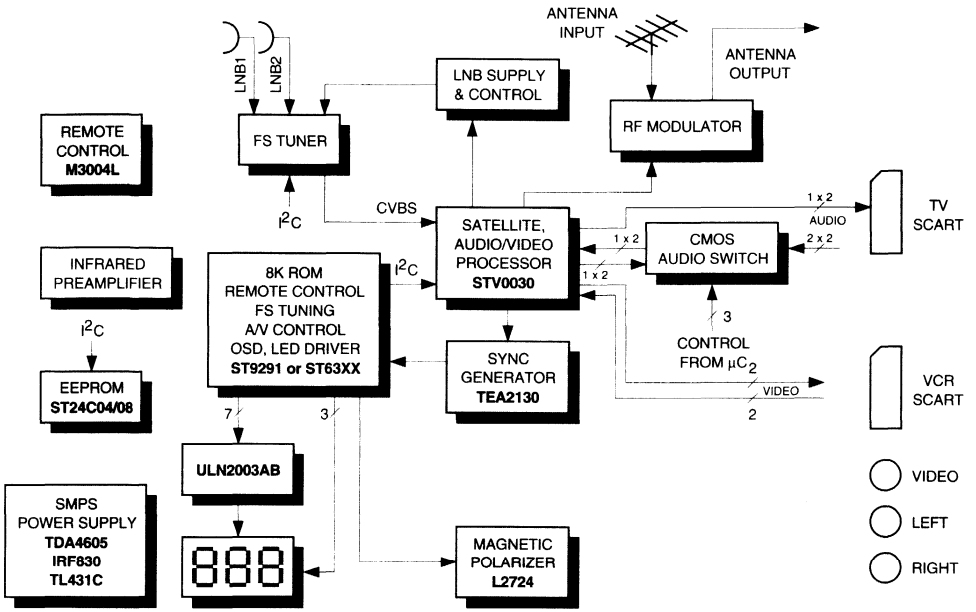
Finally, in answer to the emerging requirement for video phones, there are new graphics devices with LCD capability.

Should this volume not contain information on the product you are looking for, please contact your nearest SGS-THOMSON office. The product may be included in other Databooks covering micros, memories, standard ICs or discretes.

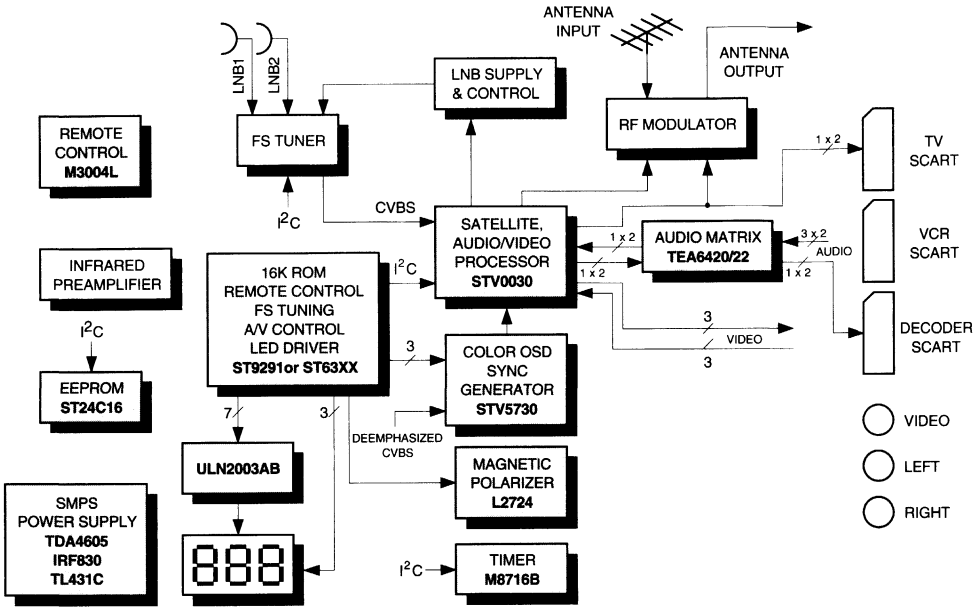
Complementing this Video ICs Databook is a Video Products Application Manual, part of the comprehensive technical support offered by SGS-THOMSON to help make application design fast and productive. It includes information on PC design aids and evaluation boards.

TYPICAL CONFIGURATION BLOCK DIAGRAMS

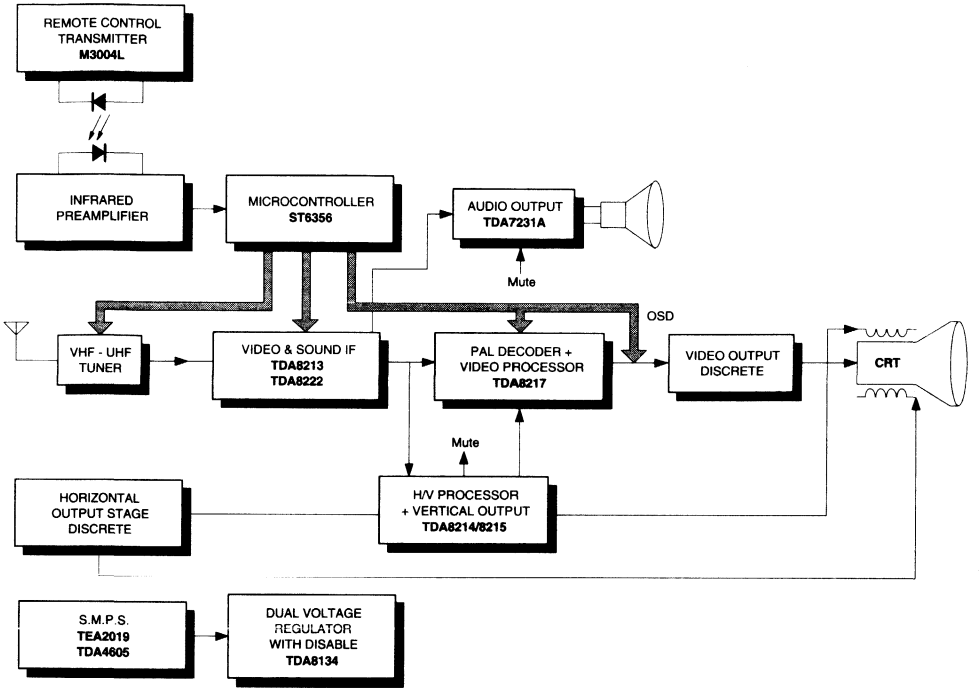
ANALOGUE MEDIUM / LOW END SATELLITE RECEIVER



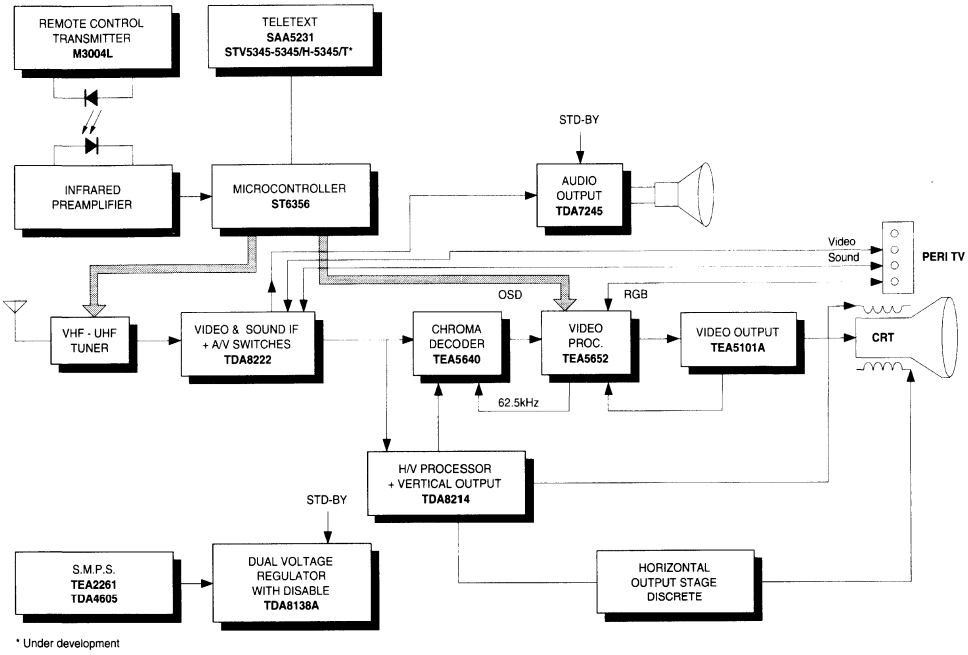
ANALOGUE HIGH END SATELLITE RECEIVER



LOW-COST 3 CHIPS PAL CHASSIS

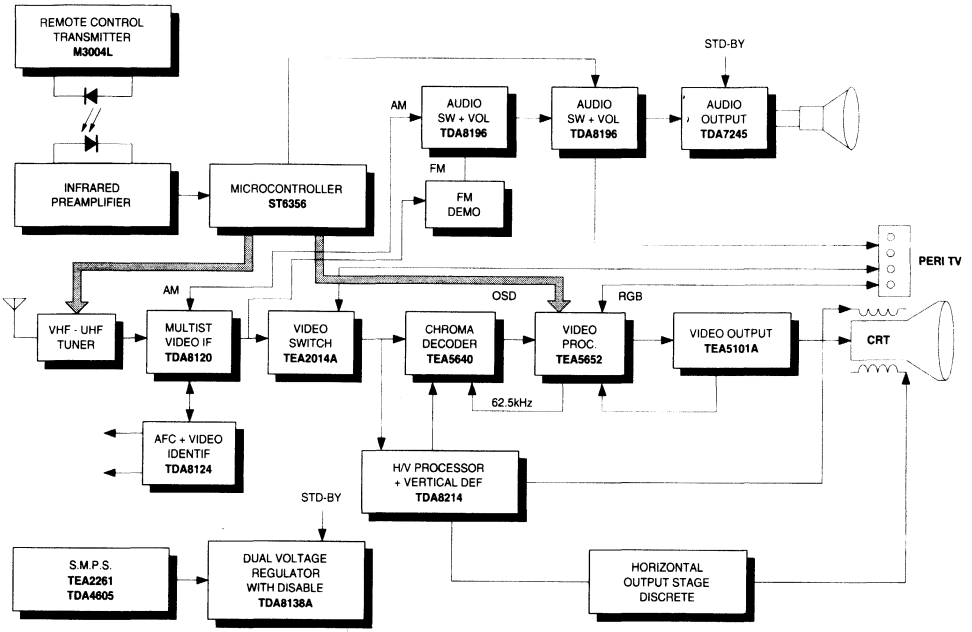


PAL/SECAM LOW-COST CHASSIS (BG/DK standards)

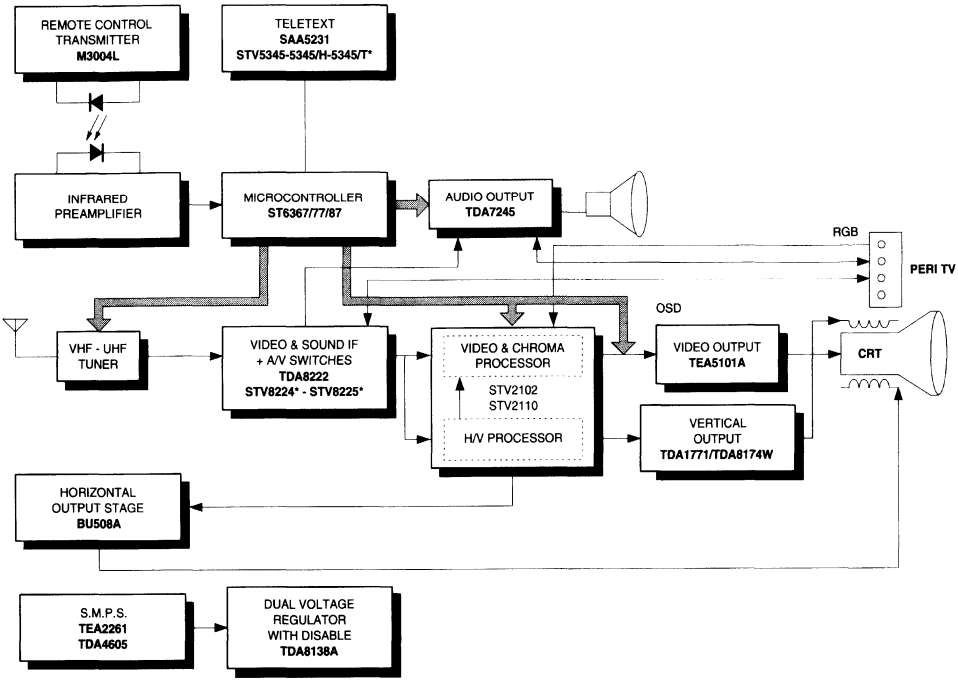


* Under development

PAL/SECAM MONOSOUND LOW-COST CHASSIS (BG/L standards)

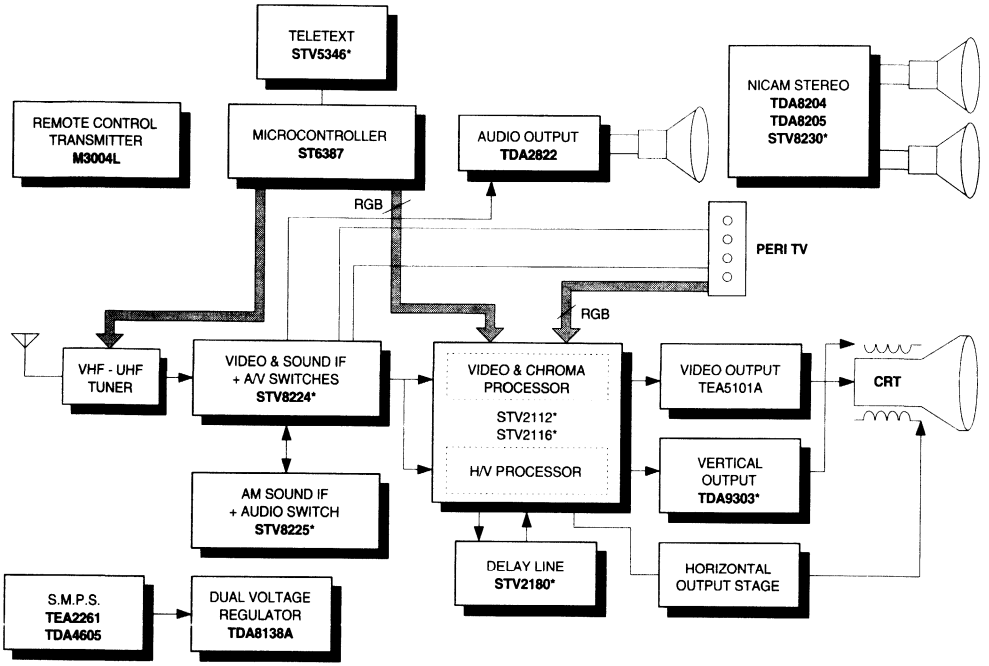


PAL OR PAL/SECAM CTV BASED ON STV2102/STV2110 (BG/DK/L standards)



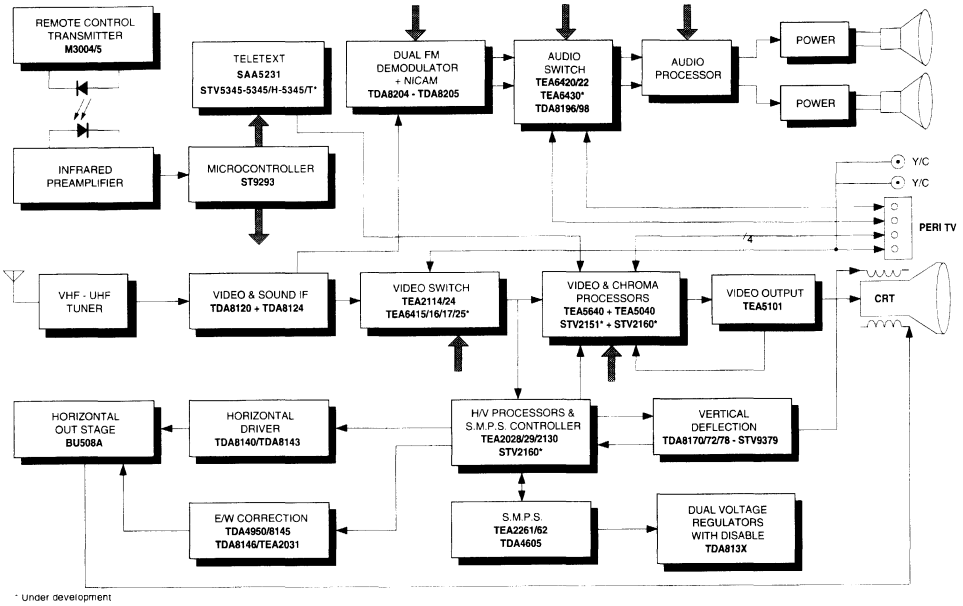
* Under development

PAL/SECAM or PAL/NTSC 90 Deg CTV BASED ON STV2112/STV2116



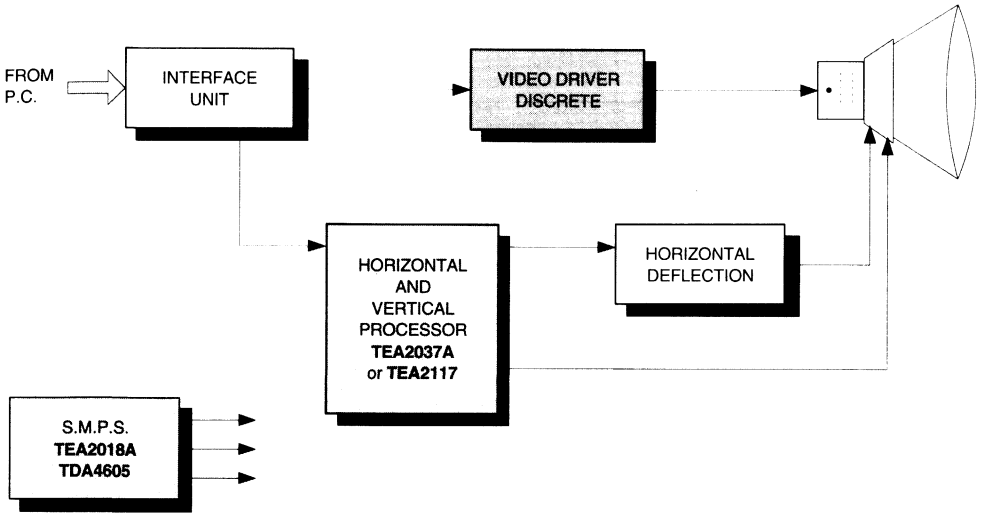
* Under development

FLEXIBLE MULTISTANDARD CTV

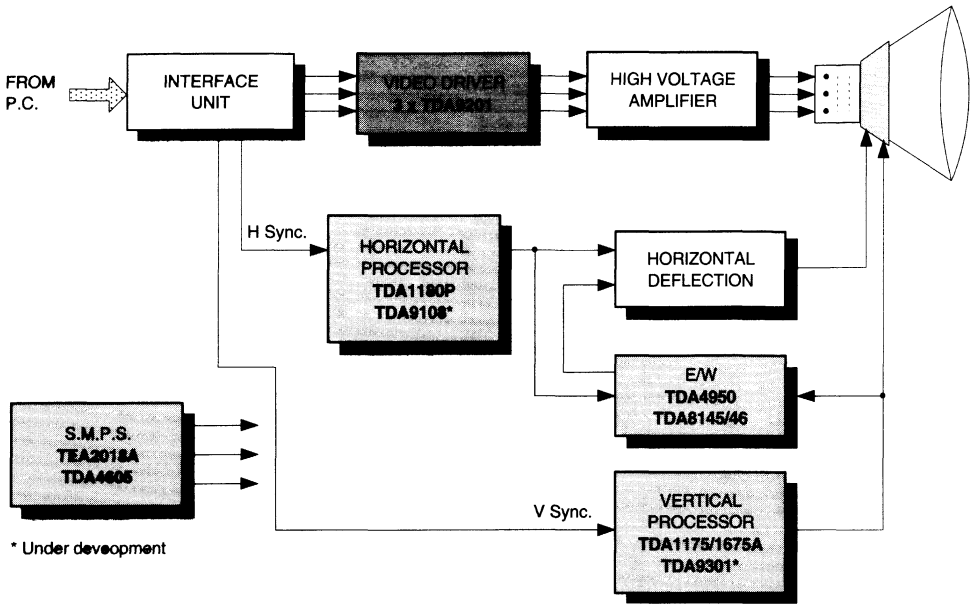


* Under development

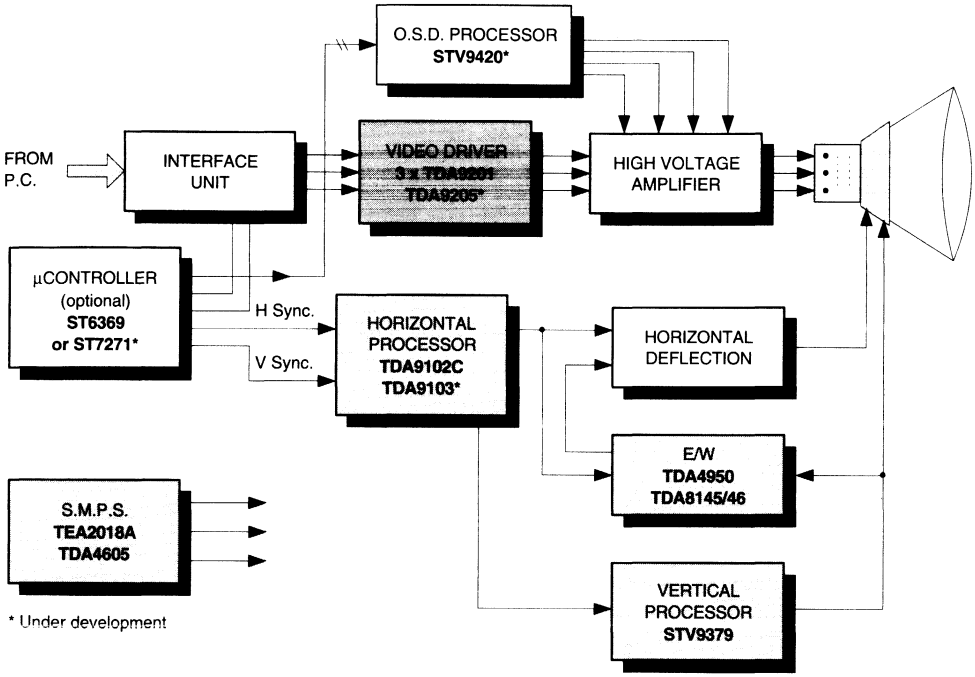
LOW-COST 14" VGA MONITOR (B & W color)



MULTI-MODE MONITOR COLOR UP TO 56k HORIZONTAL DEFLECTION

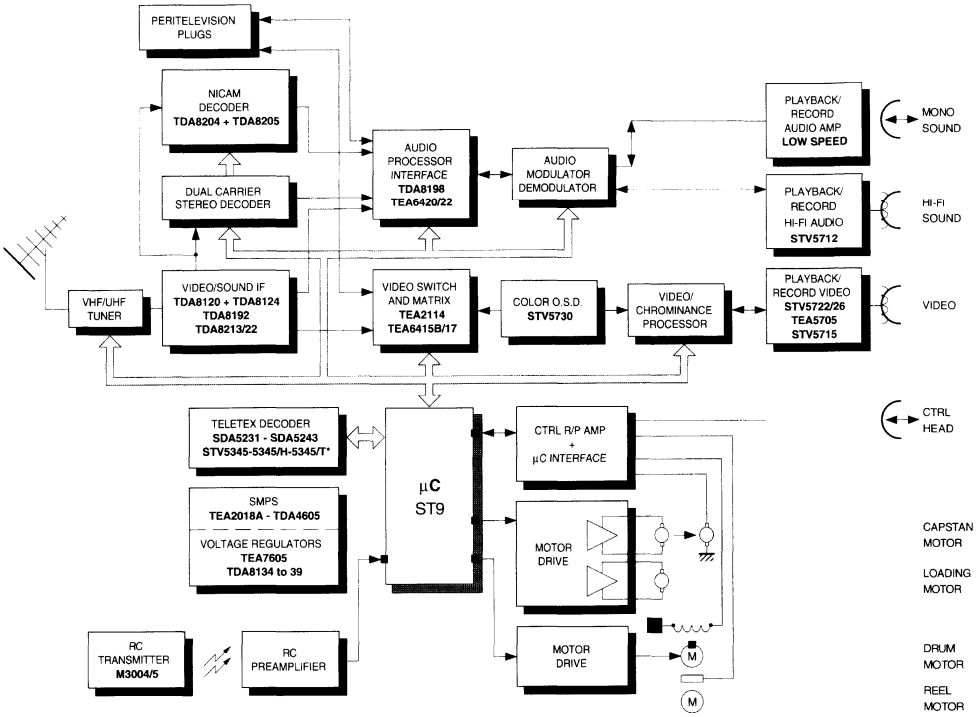


ADVANCED MULTI SYNC COLOR MONITOR 14 TO 21



* Under development

VCR APPLICATIONS



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SELECTION GUIDE

For detailed information on products referred to in the selection guide but not included as datasheet in this book, please refer to the databook indicated in colum "DB"

SGS-THOMSON DATABOOKS

DB	DESCRIPTION	ORDER CODE
a	4 BIT MCU FAMILY ET9400	DBET9400ST/1
b	16 BIT MPUs & ASSOCIATED PERIPHERALS	DB6800ST/1
c	AUDIO POWER and PROCESSING ICs	DBAUDIOPROST/1
d	AUTOMOTIVE PRODUCTS	DBAUTOMOTIVEST/2
e	CB12000 SERIES STANDARD CELLS	DBCB12/1
f	CB12000 SERIES STANDARD CELL MODULE GENERATORS	DBCB12GEN/1
g	ANALOG CELLS AND ARRAYS	DBANACA/1090
h	HIGH SPEED CMOS (Q1'94)	DBHSCMOSST/2
i	IMAGE PROCESSING	DBIMAGEPROST/2
j	INDUSTRIAL and COMPUTER PERIPHERAL ICs	DBINCOMPEST/2
k	INDUSTRY STANDARD ANALOG ICs	DBSTANDANAST/2
l	CB22000 SERIES STANDARD CELLS	DBCB22KST/1
m	ISB12000 SERIES CONTINUOUS ARRAYS	DBISB12KST/1
n	ISB24000 SERIES CONTINUOUS ARRAYS	DBISB24KST/1
o	LINE CARD ICs (Q1'94)	DBLINCARDST/2
p	LOW POWER SCHOTTKY TTL ICs	DBLPSST/1
q	VOLTAGE REGULATORS	BKVOLTAREST/1
r	POWER BIPOLAR TRANSISTORS	DBBIPTRANST/1
s	POWER MODULES	DBPOMODULEST/1
t	POWER MOS DEVICES	DBPOWERMOSST/3
u	GAL PROGRAMMABLE LOGIC DEVICES	DBPROLOGICST/1
v	PROTECTION DEVICES	DBPROTECST/2
w	RF & MICROWAVE POWER TRANSISTORS	DBRFST/2
y	SMALL SIGNAL TRANSISTORS	DBSMSIGST/1
z	CMOS B SERIES	DBCMOSBST/1
aa	CMOS LINEAR	BKCMOSLINST/3
ab	POWER SCHOTTKY DIODES	DBPOSCHODIOST/1
ac	ISDN & DATACOM PRODUCTS	DBISDNICST/1
ad	TELEPHONE SET ICs	DBTELSETST/2
ae	DEDICATED MCU FAMILY FOR TELEPHONE SET APPLICATIONS	DBTELMCUST/1
af	COMPUTER GRAPHICS	DBGRAPHICST/2
ag	THE L4970 SWITCHING REGULATOR IC FAMILY	BKL4970FA/0489
ah	THE TRANSPUTER DATABOOK	DBTRANST/3
ai	THE TRANSPUTER DEVELOPMENT AND iq SYSTEMS DATABOOK	72TRN21901
aj	SCRs & TRIACS	DBSCRTRIST/2
ak	VIDEO PRODUCTS	DBVIDEOST/2
al	DEDICATED MCU FAMILY FOR TV/MONITOR APPLICATIONS	DBVIDEMCUST/1
am	Z80 MICROPROCESSOR FAMILY	DBZ80ST/1
an	SCHOTTKY & RECTIFIER DIODES (Q1'94)	DBDIODEST/1
ao	MEMORY DATABOOK (Q1'94)	DBMEMORYST/3
ap	ST6210/ST6215/ST6220/ST6225	DBST6ST/3
aq	ST624X Family LCD DISPLAY CONTROL	DBST624XFST/1
ar	ST9 FAMILY 8/16 BIT MCU	DBST9ST/1
as	ST9040 FAMILY 8/16 BIT MCU	DBST9040FAST/1
at	ST6 FAMILY SOFTWARE TOOLS AST6, LST6, SIMST6	DBST6SOFTOST/1
au	SUBSYSTEMS PRODUCT PROFILE	BKSUBST/1
av	ST10 USER MANUAL	UMST10ST/1
(*)	NOT INCLUDED IN CURRENT DATABOOKS CONTACT YOUR NEAREST SGS-THOMSON SALES OFFICE	

DEFLECTION - ICs

VERTICAL DEFLECTION

Type Number	Description	Package	Page Number
STV9303	Ramp Generator & Vertical Output	CLIPWATT11/SIP10	55
STV9379	Vertical Deflection Booster	HEPTAWATT	59
TDA1175	Low-Noise Vertical Deflection System	FINDIP	63
TDA1675A	Vertical Deflection System	MULTIWATT15	71
TDA1771	Ramp Generator & Vertical Output	SIP10	81
TDA8170	Vertical Deflection Booster	HEPTAWATT	85
TDA8172	Vertical Deflection Booster	HEPTAWATT	91
TDA8173	Vertical Deflection Booster	DIP16	95
TDA8175	Vertical Deflection Booster	HEPTAWATT	99
TDA8178FS	Vertical Deflection Booster	HEPTAWATT	101
TDA8178S	Vertical Deflection Booster	HEPTAWATT	107
TDA8179FS	Vertical Deflection Booster	HEPTAWATT	113
TDA9302H	Vertical Deflection Booster	HEPTAWATT	119

HORIZONTAL DRIVER

Type Number	Description	Package	Page Number
TDA8140	Horizontal Deflection Power Driver	POWERDIP (8+8)	123
TDA8143	Horizontal Deflection Power Driver	SIP9	133

HORIZONTAL AND VERTICAL DEFLECTION PROCESSORS

Type Number	Description	Package	Page Number
TDA1180P	Horizontal Delection Processor	DIP16	141
TDA2593	Horizontal Delection Processor	DIP16	153
TDA8128	Sync. Separator and Video Signal Identification	DIP8	159
TDA8185I	Horizontal & Vertical Deflection Processor	DIP24	163
TDA8214B	Horizontal & Vertical Deflection Circuit	POWERDIP (16+2+2)	171
TDA8215B	Horizontal & Vertical Deflection Circuit	POWERDIP (16+2+2)	179
TDA8218	Horizontal & Vertical Deflection Circuit	POWERDIP (16+2+2)	187
TDA9102C	H/V Processor for TTL V.D.U.	DIP20	195
TDA9108	Monitor Horizontal Processor	DIP14	201
TEA2029C	Color TV Scanning and Power Supply Processor	DIP28	209
TEA2037A	Horizontal & Vertical Delection Monitor	POWERDIP (8+8)	217
TEA2117	Horizontal & Vertical Delection Monitor	MULTIWATT15	225
TEA2130	Color TV Scanning Processor	DIP20	233

DEFLECTION - ICs (continued)

ORIZONTAL DEFLECTION DIODE

Type Number	Description	Package	Page Number
MTV32-400A	Diode for Horizontal Deflection Circuits for High-End Monitors and TV	DO27	241
MTV32-600A	Diode for Horizontal Deflection Circuits for High-End Monitors and TV	DO27	243
DTV32-1000A	High Voltage Diode for Horizontal Deflection Circuits for High-End Monitors and TV	DO27	243
DTV32(F)-1200/1500A	High Voltage Diode for Horizontal Deflection Circuits for High-End Monitors and TV	TO-220AC/ ISOWATT220AC	245
DTV32(F)-1200/1500B	High Voltage Diode for Horizontal Deflection Circuits for High-End Monitors and TV	TO-220AC/ ISOWATT220AC	247
DTV64(F)-1200C	High Voltage Diode for Horizontal Deflection Circuits for High-End Monitors and TV	TO-220AC/ ISOWATT220AC	249

EAST/WEST CORRECTION

Type Number	Description	Package	Page Number
TDA4950	E/W Correction Circuit	DIP8	251
TDA8145	E/W Correction Circuit (Square Tube)	DIP8	255
TDA8146	E/W Correction Circuit (Universal)	DIP14	259
TEA2031A	E/W Correction Circuit	DIP8	263

SMPS & DEFLECTION TRANSISTORS

Type Number	V_{CBO}/ V_{CES}	IC	$V_{CE(sat)}$ @ I_C I_B			t_s	t_f	Dissipation @ - I_{B2}		Packages	Page Number
	(V)	max (A)	max (V)	(A)	(A)	max (ms)	(ms)	@ 16 KHz (W)	(A)		
BU806*	400	8	1.5	5	0.5	0.55•	0.2•	–	–	TO-220	269
BU806 FI*	400	8	1.5	5	0.5	0.55•	0.2•	–	–	ISOWATT220	269
BU807*	330	8	1.5	5	0.5	0.55•	0.2•	–	–	TO-220	269
BU807 FI*	330	8	1.5	5	0.5	0.55•	0.2•	–	–	ISOWATT220	269
BU808FI*	1400	10	1.6	5	0.5	3	0.8	–		ISOWATT218	275
BU808DFI*	1400	10	1.6	5	0.5	3	0.8	–	–	ISOWATT218	275
BU810*	600	7	2.5	4	0.2	1.5	0.4	–	–	TO-220	279
BUH313▲	1300	5	1.5	3	0.75	–	–	1	1.35	ISOWATT218	283
BUH313D	1300	5	1.5	3	0.75	–	–	1.9	1.65	ISOWATT218	289
BUH315▲	1500	5	1.5	3	0.75	–	–	1	1.35	ISOWATT218	295
BUH315D	1500	5	2	3	1	–	–	1.9	1.65	ISOWATT218	301
BUH417	1700	7	1.5	4	1	–	–	1.6	1.8	ISOWATT218	307
BUH515▲	1500	8	1.5	5	1.25	–	–	2.1	2.2	ISOWATT218	313
BUH515D	1500	8	1.5	5	1.25	–	–	3.1	2.2	ISOWATT218	319
BUH517	1700	8	1.5	5	1.25	–	–	1.7	2.5	ISOWATT218	325
BUH715▲	1500	10	1.5	7	1.5	–	–	2.5	3.5	ISOWATT218	331
BUH1015T▲	1500	16	1.5	10	2	–	–	–	–	TO-218	337
BUH1215T▲	1500	19	1.5	12	2.4	–	–	–	–	TO-218	339
BUL48	800	7	1.5	4	1.0	1.0	0.10	–	–	TO-220	341
BUL410	1000	7	1.5	3	0.6	2.0	0.11	–	–	TO-220	345
BUL510	1000	8	1.0	4	0.8	3.4	0.15	–	–	TO-200	349
SGSF664	1200	20	1.5	12	2.4	3	0.25	–	–	TO-3	353
SGSF665	1300	20	1.5	10	2	3	0.25	–	–	TO-3	357

* Darlington • Typical Value ▲ Also Ideal for SMPS

CHROMA

CHROMA VIDEO CIRCUITS

Type Number	Description	Package	Page Number
TDA8217	PAL Decoder & Video Processor	DIP20	363
TEA5040S	Bus Controlled Video Processor	SHRINK42	371
TEA5640/E	PAL/SECAL/NTSC 3.58/NTSC 4.53 Decoder	DIP28	383
TEA5640F	PAL/SECAM Decoder	DIP28	395
TEA5652	Wide Band Video Processor	SHRINK30	405

RGB HIGH VOLTAGE OUTPUT STAGE

Type Number	Description	Package	Page Number
TEA5101A	RGB Video Output Amplifier	MULTIWATT15	415

VIDEO CHROMA & DEFLECTION PROCESSOR

Type Number	Description	Package	Page Number
STV2102A	PAL Luma-Chroma & Deflection Processor	SHRINK42	421
STV2110A	PAL/SECAM Luma-Chroma & Deflection Processor	SHRINK42	433

INTERMEDIATE FREQUENCY (IF)

SOUND IF CIRCUITS

Type Number	Description	Package	Page Number
TDA8190	TV Sound Channel with DC Control	DIP20	449
TDA8191	TV Sound Channel with DC Control	DIP20	459
TDA8192	Multistandard AM & FM Sound IF	DIP20	465

VIDEO AND SOUND IF

Type Number	Description	Package	Page Number
TDA8120B	Multistandard Video and Sound IF System	DIP24	469
TDA8124	Multistandard Video IF Interface	DIP20	475
TDA8213	Video & Sound IF System	DIP20	479
TDA8222	Video and Sound IF System with Video and Sound Switches	SHRINK24	487

AUDIO, VIDEO AND SOUND SWITCHES

Type Number	Description	Package	Page Number
TDA8196	Audio Switch & DC Volume Control	DIP8	497
TDA8198	Double Audio Switch & DC Volume Control for TV	DIP8	501
TDA8199	Stereo Amplifier & DC Volume Control for TV	DIP14	505
TEA2014A	Video Switch	DIP8	509
TEA2114	Large Bandwidth Video Switch	DIP8	513
TEA2124	Large Bandwidth Video Switch	DIP8	517
TEA5114A	RGB Switch Circuit	DIP16	521
TEA5115	5 Channel Video Switch	DIP18	525
TEA5116	5 Channel Video Switch	DIP18	535
TEA6415B	Bus Controlled Video Matrix Switch	DIP20	543
TEA6416	Bus Controlled Video Matrix Switch	DIP20	551
TEA6417	Enhanced Bus Controlled Video Matrix Switch	DIP20	557
TEA6420	Bus Controlled Video Matrix Switch (5 x 4 stereo)	SHRINK24	563
TEA6422	Bus Controlled Video Matrix Switch (6 x 3 stereo)	SHRINK24	567
TEA6425	Video Cellular Matrix	DIP20	571
TEA6430	Audio Cellular Matrix	SHRINK24	577

REMOTE CONTROL

Type Number	Description	Package	Page Number
M3004AB1	Remote Control Transmitter	DIP20	583
M3004LAB1	Remote Control Transmitter	DIP20	591
M3004LD	Remote Control Transmitter	SO20L	591
M3005AB1	Remote Control Transmitter	DIP20	599
M3005LAB1	Remote Control Transmitter	DIP20	607
M3005LD	Remote Control Transmitter	SO20L	607
M3006LAB1	Remote Control Transmitter	DIP16	615
M145026	Remote Control Encoder/Decoder Circuit	DIP16/SO16	623
M145027	Remote Control Encoder/Decoder Circuit	DIP16	623
M145028	Remote Control Encoder/Decoder Circuit	DIP16/SO16L	623

AUDIO POWER AMPLIFIERS

Type Number	Description	Package	Page Number
TDA1904	4W Audio Amplifier	POWERDIP (8+8)	635
TDA1905	5W Audio Amplifier + Mute	POWERDIP (8+8)	637
TDA2006	12W Audio Amplifier	PENTAWATT	639
TDA2007A	6+6W Stereo Amplifier	SIP9	641
TDA2009A	10+10W Quality Stereo Amplifier	MULTIWATT 11	643
TDA2030	14W Hi-Fi Audio Amplifier	PENTAWATT	645
TDA2040	20W Hi-Fi Audio Amplifier	PENTAWATT	647
TDA2050	20W Hi-Fi Audio Amplifier	PENTAWATT	649
TDA2052	65W Hi-Fi Audio Amplifier With Mute/Stand-By	HEPTAWATT	651
TDA2822	Dual 1.7W Amplifier	DIP16	653
TDA7231A	1.6W Audio Amplifier	DIP8	655
TDA7233/D	1W Audio Amplifier + Mute	SO-8	657
TDA7233S	1W Audio Amplifier + Mute	SIP9	659
TDA7245	5W Audio Amplifier	POWER DIP (9+9)	661
TDA7262	20+20W High-Quality TV Amplifier	MULTIWATT 11	663
TDA7263	12+12W Stereo Amplifier With Mounting	CLIPWATT 11	665
TDA7265	25+25W Stereo Amplifier With Mute & ST-By	MULTIWATT 11	667
TDA7294	100V-100W DMOS Amplifier With Mute/ST/By	MULTIWATT15V/15H	669

VIDEO RECORDER CIRCUITS

Type Number	Description	Package	Page Number
M8716B	Clock Calendar with Serial I^2C Bus	DIP8	673
STV5712	FM Audio Playback & Record Amplifier for VCR	SO16	677
STV5715	2-Head Playback & Record Amplifier for VCR	SO20L	685
STV5722	2-Head Playback & Record Amplifier for VCR	SO16	693
STV5726	4-Head Playback & Record Amplifier for VCR	SO20L	695
STV5730	On-Screen Display	SO28L	697
TEA5702A	Playback & Record 2-Head Amplifier for VCR	SO20L	701
TEA5703	Playback & Record 3-Head Amplifier for VCR	SO20L	709
TEA5705	Playback & Record 4-Head Amplifier for VCR	SO28L version B	717
TEA5706A	Playback & Record 4-Head Amplifier for VCR	SO28L	727

TELETEXT DECODER

Type Number	Description	Package	Page Number
SAA5231	Data Slicer for Teletext Processor	DIP28	739
SDA5243	Computer-Controlled Teletext Decoder	DIP40	747
SDA5243/H	Computer-Controlled Teletext Decoder	DIP40	747
STV5345	Teletext Decoder with 8 Integrated Pages	DIP40	767
STV5345/H	Teletext Decoder with 8 Integrated Pages	DIP40	767
STV5345/T	Teletext Decoder with 8 Integrated Pages	DIP40	767

SWITCH MODE POWER SUPPLY

Type Number	Description	Package	Page Number
TDA4601	Switch Mode Power Supply	SIP9	793
TDA4601B	Switch Mode Power Supply	POWERDIP(9+9)	793
TDA4605	Switch Mode Power Supply Processor	DIP8	799
TEA2018A	Current Mode S.M.P.S. Controller	DIP8	803
TEA2019	Current Mode S.M.P.S. Controller	DIP14	809
TEA2260	Primary S.M.P.S. Controller (Slave)	BATWING DIP16	815
TEA2261	Primary S.M.P.S. Controller (Slave)	BATWING DIP16	815
TEA2262	Primary S.M.P.S. Controller (Slave)	BATWING DIP16	823
TEA5170	Secondary S.M.P.S. Controller (Master)	DIP8	831

GRAPHIC CIRCUITS

Type Number	Description	Package	Page Number
STG1700	True Color Palette-DAC With 16-Bit Pixel Port	PLCC44	841
STG1702	Enhanced True Color Palette-DAC With 16-Bit Pixel Port	PLCC44	843
STG1703	Dual Clock Synthesis Palette-DAC With 16-Bit Pixel Port	PLCC68	845
STV9410	CRT and LCD Semi-graphic Display Processor	DIP20 / SO24	847
TS9347	Single-Chip Semi-Graphic Display Processor	DIP40	871

VOLTAGE REGULATORS

Type Number	Description	Package	Page Number
TDA8134	Dual Voltage Regulator with Disable (+5.1V, +12V)	HEPTAWATT	907
TDA8135	Dual Voltage Regulator with Disable (+5.1V, Adjustable Voltage)	HEPTAWATT	911
TDA8136	Dual Voltage Regulator with Disable (+12V)	HEPTAWATT	915
TDA8137	Dual Voltage Regulator with Disable & Reset (+5.1V)	HEPTAWATT	919
TDA8138	Dual Voltage Regulator with Disable & Reset (+5.1V, +12V)	SIP9	923
TDA8138A	Dual Voltage Regulator with Disable & Reset (+5.1V, +12V)	HEPTAWATT	923
TDA8138B	Dual Voltage Regulator with Disable & Reset (+5.1V, +12V)	HEPTAWATT	923
TDA8139	Dual Voltage Regulator with Disable & Reset (+5.1V, Adjustable Voltage)	SIP9	927
TEA7605	Low Dropout Voltage Regulator (+5V)	TO220	931

AUTOMATIC VOLTAGE SWITCH

Type Number	Description	Package	Page Number
AVS08	Automatic Mains Selector (110/220V AC) for SMPS < 200W	TO-220AB	937
AVS10	Automatic Mains Selector (110/220V AC) for SMPS < 300W	TO-220AB	943
AVS12	Automatic Mains Selector (110/220V AC) for SMPS < 500W	TO-220AB	949
AV20/200	Automatic Voltage Switch for SMPS < 300W	DIP8/TO-220AB	955

LED DISPLAY DRIVERS

Type Number	Description	Package	Page Number
M5450	LED Display Driver	DIP40	965
M5451	LED Display Driver	DIP40/PLCC44	965
M5480	LED Display Driver	DIP28	971
M5481	LED Display Driver	DIP20	977
M5482	LED Display Driver	DIP20	983

NICAM

Type Number	Description	Package	Page Number
TDA8204	NICAM Decoder	SHRINK42	991
TDA8205	NICAM QSPK Demodulator	SHRINK42	1003

SPECIAL FUNCTION

Type Number	Description	Package	Page Number
L6720/21	Minitel Interfaces	POWERDIP(16+2+2)	1013
STV1389AQ	Cable Driver for Digital Transfer	QFP32	1021
STV1601A	Serial Interface Transmission Decoder	PGA37	1027
STV1602A	Serial Interface Transmission Encoder	PGA37	1043

WIDE BAND VIDEO AMPLIFIER

Type Number	Description	Package	Page Number
TDA9201	Wide Band Video Amplifier	POWERDIP20	1067

ANALOGUE SATELLITE RECEIVERS

Type Number	Description	Package	Page Number
STV0030	Satellite Sound and Video Processor	PQFP64	1081
STV5730	On-Screen Display	SO28L	699

PROTECTION DEVICES

Type Number	Description	Package	Page Number
ITA6V1U1	6 × Unidirection Transil V_{BR} = 6.1 Volt	SO8	1107
ITA6V1U3	8 × Unidirectional Transil V_{BR} = 6.1 Volt	SO20	1109
ITA6V1M3	18 × Unidirectional Transil V_{BR} = 6.1 Volt	SO20	1111
ITA...B1	4 × Bidirectional Transil V_{BR} = 6.1 V → 25 Volt	SO8	1113
ITA...B3	8 × Bidirectional Transil V_{BR} = 6.1 V → 25 Volt	SO20	1115
SM4Txx	Uni and Bidirectional Surface Mount Transils P_P = 400W	SOD6	1117
SM6Txx	Uni and Bidirectional Surface Mount Transils P_P = 600W	SOD6	1119
SM15Txx	Uni and Bidirectional Surface Mount Transils P_P = 1500W	SOD15	1121

DEVICE NUMBER	DESCRIPTION	TECH	ELECTRICAL CHARACTERISTICS (25°C)								Page Num.
			V_{CC} (V) Min.	V_{CC} (V) Max.	V_{io} (mV) Max.	I_{ib} (nA) Typ.	I_{CC} (mA) Typ/amp	GBP (MHz) Typ.	SR (V/µS) Typ.	an (nV/√Hz) Typ.	
COMMERCIAL TEMPERATURE RANGE (0 to + 70°C)											
SINGLE OP-AMPs (0 to + 70°C)											
TSH150C	Very High Speed Bip Inputs	BiCMOS	6	12	5	100	23	150	190	7	1141
TSH151C	Very High Speed CMOS Inputs Single Supply	BiCMOS	6	12	10	0.025	23	150	200	20	1143
DUAL OP-AMPs (0 to + 70°C)											
MC4558C	General Purpose	BIPOLAR	4	44	5	50	1.1	5.5	2.2	12	1127
TL082C	General Purpose	JFET	8	36	10	0.02	1.4	4	16	15	1139
TL082AC	General Purpose	JFET	8	36	6	0.02	1.4	4	16	15	1139
TL082BC	General Purpose	JFET	8	36	3	0.02	1.4	4	16	15	1139
INDUSTRIAL TEMPERATURE RANGE (-40 to + 105°C)											
SINGLE OP-AMPs (-40 to + 105°C)											
MC33171	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1131
TSH150I	Very High Speed Bit Inputs	BiCMOS	6	12	5	100	23	150	190	7	1141
TSH151I	Very High Speed CMOS Inputs Single Supply	BiCMOS	6	12	10	0.025	23	150	200	20	1143
DUAL OP-AMPs (-40 to + 105°C)											
LM833	Very Low Noise Single Supply	BIPOLAR	4	36	5	300	2	15	7	4.5	1125
MC33078	Very Low Noise Single Supply	BIPOLAR	4	36	2	250	2	15	7	4.5	1129
MC33172	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1133
MC4558I	General Purpose	BIPOLAR	4	44	5	50	1.1	5.5	2.2	12	1127
TL082I	General Purpose	JFET	8	36	6	0.02	1.4	4	16	15	1139
TL082AI	General Purpose	JFET	8	36	6	0.02	1.4	4	16	15	1139
TL082BI	General Purpose	JFET	8	36	3	0.02	1.4	4	16	15	1139
TDA2320	Remote Control Pre-Amplifier	BIPOLAR	4	20	5	100	0.4	3	1.5	20	1137
QUAD OP-AMPs (-40 to + 105°C)											
MC33174	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1135
MILITARY TEMPERATURE RANGE (-55 to + 125°C)											
SINGLE OP-AMPs (-55 to + 125°C)											
MC35171	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1131
TSH150M	Very High Speed Bip Inputs	BiCMOS	6	12	5	100	23	150	190	7	1141
TSH151M	Very High Speed CMOS Inputs Single Supply	BiCMOS	6	12	10	0.025	23	150	200	20	1143
DUAL OP-AMPs (-55 to + 125°C)											
MC35172	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1133
TL082M	General Purpose	JFET	8	36	6	0.02	1.4	4	16	15	1139
TL082AM	General Purpose	JFET	8	36	6	0.02	1.4	4	16	15	1139
TL082BM	General Purpose	JFET	8	36	3	0.02	1.4	4	16	15	1139
QUAD OP-AMPs (-55 to + 125°C)											
MC35174	Low Consumption Single Supply	BIPOLAR	4	44	4.5	20	0.2	2.1	2	30	1135

CMOS UV EPROM and OTP ROM

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
64K	M27C64A-15F1	8K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1147
	M27C64A-20F1	8K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1147
	M27C64A-25F1	8K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1147
	M27C64A-30F1	8K x 8	300	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1147
	M27C64A-20F6	8K x 8	200	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1147
	M27C64A-25F6	8K x 8	250	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1147
	M27C64A-30F6	8K x 8	300	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1147
256K	M27C256B-70XF1	32K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-80XF1	32K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-10XF1	32K x 8	100	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-12XF1	32K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-15XF1	32K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-20XF1	32K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-25XF1	32K x 8	250	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-10F1	32K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-12F1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-15F1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-20F1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-25F1	32K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1149
	M27C256B-15XF6	32K x 8	150	5V ± 5%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-20XF6	32K x 8	200	5V ± 5%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-90F6	32K x 8	90	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-12F6	32K x 8	120	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-15F6	32K x 8	150	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-20F6	32K x 8	200	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-25F6	32K x 8	250	5V ± 10%	30mA / 100µA	-40 to 85	FDIP28W	1149
	M27C256B-15XF3	32K x 8	150	5V ± 5%	30mA / 100µA	-40 to 125	FDIP28W	1149
	M27C256B-20F3	32K x 8	200	5V ± 10%	30mA / 100µA	-40 to 125	FDIP28W	1149
	M27C256B-90B1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1149
	M27C256B-12B1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1149
	M27C256B-15B1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1149
	M27C256B-20B1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1149
	M27C256B-15B6	32K x 8	150	5V ± 10%	30mA / 100µA	-40 to 85	PDIP28	1149
	M27C256B-20B7	32K x 8	200	5V ± 10%	30mA / 100µA	-40 to 105	PDIP28	1149
	M27C256B-20B3	32K x 8	200	5V ± 10%	30mA / 100µA	-40 to 125	PDIP28	1149
	M27C256B-90C1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1149
	M27C256B-12C1	32K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1149
	M27C256B-15C1	32K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1149
	M27C256B-20C1	32K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1149
	M27C256B-12C6	32K x 8	120	5V ± 10%	30mA / 100µA	-40 to 85	PLCC32	1149
	M27C256B-15C6	32K x 8	150	5V ± 10%	30mA / 100µA	-40 to 85	PLCC32	1149
	M27C256B-20C6	32K x 8	200	5V ± 10%	30mA / 100µA	-40 to 85	PLCC32	1149
	M27C256B-90N1	32K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	TSOP28	1149
	M87C257-12XF1	32K x 8	120	5V ± 5%	30mA / 200µA	0 to 70	FDIP28W	1151
	M87C257-20XF1	32K x 8	200	5V ± 5%	30mA / 200µA	0 to 70	FDIP28W	1151
	M87C257-12F1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	FDIP28W	1151

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
256K	M87C257-20F1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	FDIP28W	1151
	M87C257-15F6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	FDIP28W	1151
	M87C257-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1151
	M87C257-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32	1151
	M87C257-20C6	32K x 8	200	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32	1151
	M87C257-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32	1151
512K	M27C512-70XF1	64K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-80XF1	64K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-12XF1	64K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-15XF1	64K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-20XF1	64K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-25XF1	64K x 8	250	5V ± 5%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-10F1	64K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-12F1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-15F1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-20F1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-25F1	64K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP28W	1153
	M27C512-15XF6	64K x 8	150	5V ± 5%	30mA / 100µA	–40 to 85	FDIP28W	1153
	M27C512-15F6	64K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W	1153
	M27C512-20F6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP28W	1153
	M27C512-12F3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	FDIP28W	1153
	M27C512-20F3	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	FDIP28W	1153
	M27C512-90B1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1153
	M27C512-12B1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1153
	M27C512-15B1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1153
	M27C512-20B1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP28	1153
	M27C512-15B6	64K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PDIP28	1153
	M27C512-20B6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	PDIP28	1153
	M27C512-12B3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	PDIP28	1153
	M27C512-20B3	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 125	PDIP28	1153
	M27C512-90C1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1153
	M27C512-12C1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1153
	M27C512-15C1	64K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1153
	M27C512-20C1	64K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1153
	M27V512-200K1	64K x 8	200	3 to 5.5V	10mA / 100µA	0 to 70	PLCC32	1153
	M27C512-12C6	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1153
	M27C512-20C6	64K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1153
	M27C512-12C3	64K x 8	120	5V ± 10%	30mA / 100µA	–40 to 125	PLCC32	1153
	M27C512-90N1	64K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	TSOP28	1153
	M27C512-12N1	64K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	TSOP28	1153
	M27V512-200N1	64K x 8	200	3 to 5.5V	10mA / 100µA	0 to 70	TSOP28	1155
1M	M27C1001-70XF1	128K x 8	70	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-80XF1	128K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-12F1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-12XF1	128K x 8	120	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-15XF1	128K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-20XF1	128K x 8	200	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1157

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
1M	M27C1001-25XF1	128K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-10F1	128K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-15F1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-20F1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-25F1	128K x 8	250	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1157
	M27C1001-20XF6	128K x 8	200	5V ± 5%	30mA / 100µA	–40 to 85	FDIP32W	1157
	M27C1001-12F6	128K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W	1157
	M27C1001-15F6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W	1157
	M27C1001-20F6	128K x 8	200	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W	1157
	M27C1001-10XF3	128K x 8	100	5V ± 5%	30mA / 100µA	–40 to 125	FDIP32W	1157
	M27C1001-10L1	Use M27V101-200L6					LCCC32W	1157
	M27C1001-15B1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP32	1157
	M27C1001-12B3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PDIP32	1157
	M27C1001-90C1	128K x 8	90	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1157
	M27C1001-10C1	128K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1157
	M27C1001-12C1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1157
	M27C1001-15C1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1157
	M27C1001-20C1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1157
	M27V101-200K1	128K x 8	200	3 to 5.5V	30mA / 100µA	0 to 70	PLCC32	1157
	M27C1001-90C6	128K x 8	90	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1157
	M27C1001-12C6	128K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1157
	M27C1001-15C6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1157
	M27V101-200L6	128K x 8	200	3.2 to 5.5V	30mA / 100µA	–40 to 85	LCCC32W	1159
	M27C1024-80XF1	64K x 16	80	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-12XF1	64K x 16	120	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-15XF1	64K x 16	150	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-20XF1	64K x 16	200	5V ± 5%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-10F1	64K x 16	100	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-12F1	64K x 16	120	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-15F1	64K x 16	150	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-20F1	64K x 16	200	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-25F1	64K x 16	250	5V ± 10%	35mA / 100µA	0 to 70	FDIP40W	1161
	M27C1024-12XF6	64K x 16	120	5V ± 5%	35mA / 100µA	–40 to 85	FDIP40W	1161
	M27C1024-10C1	64K x 16	100	5V ± 10%	35mA / 100µA	0 to 70	PLCC44	1161
	M27C1024-12C1	64K x 16	120	5V ± 10%	35mA / 100µA	0 to 70	PLCC44	1161
	M27C1024-15C1	64K x 16	150	5V ± 10%	35mA / 100µA	0 to 70	PLCC44	1161
	M27C1024-12C6	64K x 16	120	5V ± 10%	35mA / 100µA	–40 to 85	PLCC44	1161
2M	M27C2001-80XF1	256K x 8	80	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-15XF1	256K x 8	150	5V ± 5%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-10F1	256K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-12F1	256K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-15F1	256K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-20F1	256K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	FDIP32W	1163
	M27C2001-12F6	256K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	FDIP32W	1163
	M27C2001-10L1	Use M27V201-200L6					LCCC32W	1163
	M27C2001-10C1	256K x 8	100	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1163

CMOS UV EPROM and OTP ROM (cont'd)

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
2M	M27C2001-12C1	256K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1163
	M27C2001-15C1	256K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1163
	M27V201-200K1	256K x 8	200	3 to 5.5V	30mA / 100µA	0 to 70	PLCC32	1163
	M27C2001-12C6	256K x 8	120	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1163
	M27C2001-15C6	256K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1163
	M27V201-200L6	256K x 8	200	3.2 to 5.5V	30mA / 100µA	–40 to 85	LCCC32W	1165
4M	M27C4001-80XF1	512K x 8	80	5V ± 5%	50mA / 100µA	0 to 70	FDIP32W	1167
	M27C4001-10XF1	512K x 8	100	5V ± 5%	50mA / 100µA	0 to 70	FDIP32W	1167
	M27C4001-10F1	512K x 8	100	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W	1167
	M27C4001-12F1	512K x 8	120	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W	1167
	M27C4001-15F1	512K x 8	150	5V ± 10%	50mA / 100µA	0 to 70	FDIP32W	1167
	M27C4001-12F6	512K x 8	120	5V ± 10%	50mA / 100µA	–40 to 85	FDIP32W	1167
	M27C4001-95XL6	512K x 8	95	5V ± 5%	50mA / 100µA	–40 to 85	LCCC32W	1167
	M27C4001-10C1	512K x 8	100	5V ± 10%	50mA / 100µA	0 to 70	PLCC32	1167
	M27C4001-12C1	512K x 8	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC32	1167
	M27C4001-15C1	512K x 8	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC32	1167
	M27V401-200K1	512K x 8	200	3 to 5.5V	50mA / 100µA	0 to 70	PLCC32	1167
	M27C4001-12C6	512K x 8	120	5V ± 10%	50mA / 100µA	–40 to 85	PLCC32	1167
	M27V401-200L6	512K x 8	200	3.2 to 5.5V	50mA / 100µA	–40 to 85	LCCC32W	1169
	M27C4002-80XF1	256K x 16	80	5V ± 5%	50mA / 100µA	0 to 70	FDIP40W	1171
	M27C4002-10XF1	256K x 16	100	5V ± 5%	50mA / 100µA	0 to 70	FDIP40W	1171
	M27C4002-10F1	256K x 16	100	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W	1171
	M27C4002-12F1	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W	1171
	M27C4002-15F1	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	FDIP40W	1171
	M27C4002-12F6	256K x 16	120	5V ± 10%	50mA / 100µA	–40 to 85	FDIP40W	1171
	M27C4002-15F6	256K x 16	150	5V ± 10%	50mA / 100µA	–40 to 85	FDIP40W	1171
	M27C4002-12J6	256K x 16	120	5V ± 10%	50mA / 100µA	–40 to 85	JLCC44W	1171
	M27C4002-12C1	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC44	1171
	M27C4002-15C1	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44	1171
	M27C4002-12C6	256K x 16	120	5V ± 10%	50mA / 100µA	0 to 70	PLCC44	1171
	M27C4002-15C6	256K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44	1171
16M	M27C160-200F1	x8 / x16	200	5V ± 10%	50mA / 100µA	0 to 70	FDIP42W	1173

FLASH MEMORIES

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
256K	M28F256A-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1177
	M28F256-12B1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1175
	M28F256A-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1177
	M28F256-15B1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1175
	M28F256A-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1177
	M28F256-20B1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1175
	M28F256A-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32	1177
	M28F256-15B6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32	1175
	M28F256A-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32	1177
	M28F256-15B3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32	1175
	M28F256A-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1177
	M28F256-12C1	32K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1175
	M28F256A-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1177

FLASH MEMORIES (cont'd)

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	I_{CC} / Stdby	Temp. Range (°C)	Package	Page Number
256K	M28F256-15C1	32K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1175
	M28F256A-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1177
	M28F256-20C1	32K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1175
	M28F256A-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32	1177
	M28F256-15C6	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32	1175
	M28F256A-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32	1177
	M28F256-15C3	32K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32	1175
512K	M28F512-12B1	64K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1179
	M28F512-15B1	64K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1179
	M28F512-20B1	64K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PDIP32	1179
	M28F512-15B6	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PDIP32	1179
	M28F512-15B3	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PDIP32	1179
	M28F512-12C1	64K x 8	120	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1179
	M28F512-15C1	64K x 8	150	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1179
	M28F512-20C1	64K x 8	200	5V ± 10%	30mA / 200µA	0 to 70	PLCC32	1179
	M28F512-15C6	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 85	PLCC32	1179
	M28F512-15C3	64K x 8	150	5V ± 10%	30mA / 200µA	–40 to 125	PLCC32	1179
1M	M28F101-120P1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PDIP32	1181
	M28F101-150P1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PDIP32	1181
	M28F101-200P1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PDIP32	1181
	M28F101-150P6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PDIP32	1181
	M28F101-150P3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PDIP32	1181
	M28F101-120K1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1181
	M28F101-150K1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1181
	M28F101-200K1	128K x 8	200	5V ± 10%	30mA / 100µA	0 to 70	PLCC32	1181
	M28F101-150K6	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 85	PLCC32	1181
	M28F101-150K3	128K x 8	150	5V ± 10%	30mA / 100µA	–40 to 125	PLCC32	1181
	M28F101-120N1	128K x 8	120	5V ± 10%	30mA / 100µA	0 to 70	TSOP32	1181
	M28F101-150N1	128K x 8	150	5V ± 10%	30mA / 100µA	0 to 70	TSOP32	1181
	M28F101A-60N1	128K x 8	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP32	1183
	M28V101A-150N1	128K x 8	150	3.3V ± 0.3V	50mA / 100µA	0 to 70	TSOP32	1183
	M28F101B-60N1	128K x 8	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP32	1185
	M28V101B-150N1	128K x 8	150	3.3V ± 0.3V	50mA / 100µA	0 to 70	TSOP32	1185
	M28F102-150K1	64K x 16	150	5V ± 10%	50mA / 100µA	0 to 70	PLCC44	1187
	M28F102-150K6	64K x 16	150	5V ± 10%	50mA / 100µA	–40 to 85	PLCC44	1187
	M28F102-150K3	64K x 16	150	5V ± 10%	50mA / 100µA	–40 to 125	PLCC44	1187
2M	M28F201-60N1	256K x 8	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP32	1189
	M28V201-150N1	256K x 8	150	3.3V ± 0.3V	50mA / 100µA	0 to 70	TSOP32	1189
	M28F201A-60N1	256K x 8	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP32	1191
	M28V201A-150N1	256K x 8	150	3.3V ± 0.3V	50mA / 100µA	0 to 70	TSOP32	1191
4M	M28F410-60N1	x8 / x16	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP56	1193
	M28V410-150N1	x8 / x16	150	3V to 5.5V	50mA / 100µA	0 to 70	TSOP56	1193
	M28F411-60N1	512K x 8	60	5V ± 10%	50mA / 100µA	0 to 70	TSOP40	1195
	F28V411-150N1	512K x 8	150	3V to 5.5V	50mA / 100µA	0 to 70	TSOP40	1195
8M	M28F841-85N1	1M x 8	85	5V ± 10%	50mA / 100µA	0 to 70	TSOP40	1197
	M28V841-200N1	1M x 8	200	3V to 5.5V	50mA / 100µA	0 to 70	TSOP40	1197
16M	M28F161-100N1	2M x 8	100	3.3V ± 0.3V	50mA / 100µA	0 to 70	TSOP48	1199

EEPROM, I^2C Serial Access Bus

Size	Part Number	Organis.	Vcc min (V)	Feature	Temp. Range (°C)	Package	Page Number
1K	ST24C01B1	128 x 8	4.5	Byte/Page Write	0 to 70	PSDIP8	1201
	ST24W01B1	128 x 8	4.5	Write Control	0 to 70	PSDIP8	1201
	ST24C01CB1	128 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8	1201
	ST24W01CB1	128 x 8	3.0	Write Control	0 to 70	PSDIP8	1201
	ST25C01B1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8	1201
	ST25C01CB1	128 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8	1201
	ST25W01CB1	128 x 8	2.5	Write Control	0 to 70	PSDIP8	1201
	ST24C01B6	128 x 8	4.5	Byte/Page Write	–40 to 85	PSDIP8	1201
	ST24W01B6	128 x 8	4.5	Write Control	–40 to 85	PSDIP8	1201
	ST24C01CB6	128 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8	1201
	ST24W01CB6	128 x 8	3.0	Write Control	–40 to 85	PSDIP8	1201
	ST25C01B6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8	1201
	ST25C01CB6	128 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8	1201
	ST25W01CB6	128 x 8	2.5	Write Control	–40 to 85	PSDIP8	1201
	ST24C01M1	128 x 8	4.5	Byte/Page Write	0 to 70	SO8	1201
	ST24C01M1013TR	128 x 8	4.5	Byte/Page Write	0 to 70	SO8TR	1201
	ST24W01M1	128 x 8	4.5	Write Control	0 to 70	SO8	1201
	ST24W01M1013TR	128 x 8	4.5	Write Control	0 to 70	SO8TR	1201
	ST24C01CM1	128 x 8	3.0	Byte/Page Write	0 to 70	SO8	1201
	ST24C01CM1TR	128 x 8	3.0	Byte/Page Write	0 to 70	SO8TR	1201
	ST24W01CM1	128 x 8	3.0	Write Control	0 to 70	SO8	1201
	ST24W01CM1TR	128 x 8	3.0	Write Control	0 to 70	SO8TR	1201
	ST25C01CM1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8	1201
	ST25C01CM1TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR	1201
	ST25C01M1	128 x 8	2.5	Byte/Page Write	0 to 70	SO8	1201
	ST25C01M1013TR	128 x 8	2.5	Byte/Page Write	0 to 70	SO8TR	1201
	ST25W01CM1	128 x 8	2.5	Write Control	0 to 70	SO8	1201
	ST25W01CM1TR	128 x 8	2.5	Write Control	0 to 70	SO8TR	1201
	ST24C01M6	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8	1201
	ST24C01M6013TR	128 x 8	4.5	Byte/Page Write	–40 to 85	SO8TR	1201
	ST24W01M6	128 x 8	4.5	Write Control	–40 to 85	SO8	1201
	ST24W01M6013TR	128 x 8	4.5	Write Control	–40 to 85	SO8TR	1201
	ST24C01CM6	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8	1201
	ST24C01CM6TR	128 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR	1201
	ST24W01CM6	128 x 8	3.0	Write Control	–40 to 85	SO8	1201
	ST24W01CM6TR	128 x 8	3.0	Write Control	–40 to 85	SO8TR	1201
	ST25C01CM6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8	1201
	ST25C01CM6TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR	1201
	ST25C01M6	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8	1201
	ST25C01M6013TR	128 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR	1201
	ST25W01CM6	128 x 8	2.5	Write Control	–40 to 85	SO8	1201
	ST25W01CM6TR	128 x 8	2.5	Write Control	–40 to 85	SO8TR	1201
	ST24C01M3	128 x 8	4.5	Byte/Page Write	–40 to 125	SO8	1201

EEPROM, I²C Serial Access Bus (cont'd)

Size	Part Number	Organis.	V_{CC} min (V)	Feature	Temp. Range (°C)	Package	Page Number
2K	ST24C02AB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8	1203
	ST24C02AB1/AAB	256 x 8	3.0	Content all 00	0 to 70	PSDIP8	1203
	ST24C02CB1	256 x 8	3.0	Byte/Page Write	0 to 70	PSDIP8	1203
	ST24W02CB1	256 x 8	3.0	Write Control	0 to 70	PSDIP8	1203
	ST25C02AB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8	1203
	ST25C02CB1	256 x 8	2.5	Byte/Page Write	0 to 70	PSDIP8	1203
	ST25W02CB1	256 x 8	2.5	Write Control	0 to 70	PSDIP8	1203
	ST24C02AB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8	1203
	ST24C02CB6	256 x 8	3.0	Byte/Page Write	–40 to 85	PSDIP8	1203
	ST24W02CB6	256 x 8	3.0	Write Control	–40 to 85	PSDIP8	1203
	ST25C02AB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8	1203
	ST25C02CB6	256 x 8	2.5	Byte/Page Write	–40 to 85	PSDIP8	1203
	ST25W02CB6	256 x 8	2.5	Write Control	–40 to 85	PSDIP8	1203
	ST24C02CB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8	1203
	ST25C02CB3	256 x 8	2.5	Byte/Page Write	–40 to 125	PSDIP8	1203
	ST24C02AB3	256 x 8	3.0	Byte/Page Write	–40 to 125	PSDIP8	1203
	ST24C02AM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8	1203
	ST24C02AM1013TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR	1203
	ST24C02CM1	256 x 8	3.0	Byte/Page Write	0 to 70	SO8	1203
	ST24C02CM1TR	256 x 8	3.0	Byte/Page Write	0 to 70	SO8TR	1203
	ST24W02CM1	256 x 8	3.0	Write Control	0 to 70	SO8	1203
	ST24W02CM1TR	256 x 8	3.0	Write Control	0 to 70	SO8TR	1203
	ST25C02AM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8	1203
	ST25C02AM1013TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR	1203
	ST25C02CM1	256 x 8	2.5	Byte/Page Write	0 to 70	SO8	1203
	ST25C02CM1TR	256 x 8	2.5	Byte/Page Write	0 to 70	SO8TR	1203
	ST25W02CM1	256 x 8	2.5	Write Control	0 to 70	SO8	1203
	ST25W02CM1TR	256 x 8	2.5	Write Control	0 to 70	SO8TR	1203
	ST24C02AM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8	1203
	ST24C02AM6013TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR	1203
	ST24C02CM6	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8	1203
	ST24C02CM6TR	256 x 8	3.0	Byte/Page Write	–40 to 85	SO8TR	1203
	ST24W02CM6	256 x 8	3.0	Write Control	–40 to 85	SO8	1203
	ST24W02CM6TR	256 x 8	3.0	Write Control	–40 to 85	SO8TR	1203
	ST25C02AM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8	1203
	ST25C02AM6013TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR	1203
	ST25C02CM6	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8	1203
	ST25C02CM6TR	256 x 8	2.5	Byte/Page Write	–40 to 85	SO8TR	1203
	ST25W02CM6	256 x 8	2.5	Write Control	–40 to 85	SO8	1203
	ST25W02CM6TR	256 x 8	2.5	Write Control	–40 to 85	SO8TR	1203
	ST24C02AM3	256 x 8	3.0	Byte/Page Write	–40 to 125	SO8	1203
4K	ST24C04B1	512 x 8	4.5	Write Protection	0 to 70	PSDIP8	1205
	ST24C04CB1	512 x 8	3.0	Write Protection	0 to 70	PSDIP8	1205
	ST24W04CB1	512 x 8	3.0	Write Control	0 to 70	PSDIP8	1205
	ST25C04B1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8	1205

EEPROM, I^2C Serial Access Bus (cont'd)

Size	Part Number	Organis.	V_{CC} min (V)	Feature	Temp. Range (°C)	Package	Page Number
4K	ST25C04CB1	512 x 8	2.5	Write Protection	0 to 70	PSDIP8	1205
	ST25W04CB1	512 x 8	2.5	Write Control	0 to 70	PSDIP8	1205
	ST24C04B6	512 x 8	4.5	Write Protection	–40 to 85	PSDIP8	1205
	ST24C04CB6	512 x 8	3.0	Write Protection	–40 to 85	PSDIP8	1205
	ST24W04CB6	512 x 8	3.0	Write Control	–40 to 85	PSDIP8	1205
	ST25C04B6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8	1205
	ST25C04CB6	512 x 8	2.5	Write Protection	–40 to 85	PSDIP8	1205
	ST25W04CB6	512 x 8	2.5	Write Control	–40 to 85	PSDIP8	1205
	ST24C04CB3	512 x 8	3.0	Write Protection	–40 to 125	PSDIP8	1205
	ST24C04CM1	512 x 8	3.0	Write Protection	0 to 70	SO8	1205
	ST24C04CM1TR	512 x 8	3.0	Write Protection	0 to 70	SO8TR	1205
	ST24W04CM1	512 x 8	3.0	Write Control	0 to 70	SO8	1205
	ST24W04CM1TR	512 x 8	3.0	Write Control	0 to 70	SO8TR	1205
	ST25C04CM1	512 x 8	2.5	Write Protection	0 to 70	SO8	1205
	ST25C04CM1TR	512 x 8	2.5	Write Protection	0 to 70	SO8TR	1205
	ST25W04CM1	512 x 8	2.5	Write Control	0 to 70	SO8	1205
	ST25W04CM1TR	512 x 8	2.5	Write Control	0 to 70	SO8TR	1205
	ST24C04CM6	512 x 8	3.0	Write Protection	–40 to 85	SO8	1205
	ST24C04CM6TR	512 x 8	3.0	Write Protection	–40 to 85	SO8TR	1205
	ST24W04CM6	512 x 8	3.0	Write Control	–40 to 85	SO8	1205
	ST24W04CM6TR	512 x 8	3.0	Write Control	–40 to 85	SO8TR	1205
	ST25C04CM6	512 x 8	2.5	Write Protection	–40 to 85	SO8	1205
	ST25C04CM6TR	512 x 8	2.5	Write Protection	–40 to 85	SO8TR	1205
	ST25W04CM6	512 x 8	2.5	Write Control	–40 to 85	SO8	1205
	ST25W04CM6TR	512 x 8	2.5	Write Control	–40 to 85	SO8TR	1205
8K	ST24C08B1	1K x 8	4.5	Write Protection	0 to 70	PSDIP8	1207
	ST24C08CB1	1K x 8	3.0	Write Protection	0 to 70	PSDIP8	1207
	ST25C08CB1	1K x 8	2.5	Write Protection	0 to 70	PSDIP8	1207
	ST24C08B6	1K x 8	4.5	Write Protection	–40 to 85	PSDIP8	1207
	ST24C08CB6	1K x 8	3.0	Write Protection	–40 to 85	PSDIP8	1207
	ST25C08CB6	1K x 8	2.5	Write Protection	–40 to 85	PSDIP8	1207
	ST24C08CM1	1K x 8	3.0	Write Protection	0 to 70	SO8	1207
	ST24C08CM1TR	1Kx 8	3.0	Write Protection	0 to 70	SO8TR	1207
	ST25C08CM1	1K x 8	2.5	Write Protection	0 to 70	SO8	1207
	ST25C08CM1TR	1Kx 8	2.5	Write Protection	0 to 70	SO8TR	1207
	ST24C08CM6	1K x 8	3.0	Write Protection	–40 to 85	SO8	1207
	ST24C08CM6TR	1Kx 8	3.0	Write Protection	–40 to 85	SO8TR	1207
	ST25C08CM6	1K x 8	2.5	Write Protection	–40 to 85	SO8	1207
	ST25C08CM6TR	1Kx 8	2.5	Write Protection	–40 to 85	SO8TR	1207
16K	ST24C16CB1	2K x 8	3.0	Write Protection	0 to 70	PSDIP8	1209
	ST24E16DB1	2K x 8	3.0	XI^2C Bus & WC	0 to 70	PSDIP8	1211
	ST25C16CB1	2K x 8	2.5	Write Protection	0 to 70	PSDIP8	1209
	ST25E16DB1	2K x 8	2.5	XI^2C Bus & WC	0 to 70	PSDIP8	1211
	ST24C16CB6	2K x 8	3.0	Write Protection	–40 to 85	PSDIP8	1209
	ST24E16DB6	2K x 8	3.0	XI^2C Bus & WC	–40 to 85	PSDIP8	1211
	ST25C16CB6	2K x 8	2.5	Write Protection	–40 to 85	PSDIP8	1209

EEPROM, I²C Serial Access Bus (cont'd)

Size	Part Number	Organis.	V_{CC} min (V)	Feature	Temp. Range (°C)	Package	Page Number
16K	ST25E16DB6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	PSDIP8	1211
	ST24C16CB3	2K x 8	3.0	Write Protection	–40 to 125	PSDIP8	1209
	ST24C16CM1	2K x 8	3.0	Write Protection	0 to 70	SO8	1209
	ST24C16CM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR	1209
	ST24C16DM1	2K x 8	3.0	Write Protection	0 to 70	SO8	1209
	ST24C16DM1TR	2K x 8	3.0	Write Protection	0 to 70	SO8TR	1209
	ST24E16DM1	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8	1211
	ST24E16DM1TR	2K x 8	3.0	XI²C Bus & WC	0 to 70	SO8TR	1211
	ST25C16DM1	2K x 8	2.5	Write Protection	0 to 70	SO8	1209
	ST25C16DM1TR	2K x 8	2.5	Write Protection	0 to 70	SO8TR	1209
	ST25E16DM1	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8	1211
	ST25E16DM1TR	2K x 8	2.5	XI²C Bus & WC	0 to 70	SO8TR	1211
	ST24C16DM6	2K x 8	3.0	Write Protection	–40 to 85	SO8	1209
	ST24C16DM6TR	2K x 8	3.0	Write Protection	–40 to 85	SO8TR	1209
	ST24E16DM6	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8	1211
	ST24E16DM6TR	2K x 8	3.0	XI²C Bus & WC	–40 to 85	SO8TR	1211
	ST25C16DM6	2K x 8	2.5	Write Protection	–40 to 85	SO8	1209
	ST25C16DM6TR	2K x 8	2.5	Write Protection	–40 to 85	SO8TR	1209
	ST25E16DM6	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8	1211
	ST25E16DM6TR	2K x 8	2.5	XI²C Bus & WC	–40 to 85	SO8TR	1211
	ST24C16CML1	2K x 8	3.0	Write Protection	0 to 70	SO14	1209
	ST24C16CML1TR	2K x 8	3.0	Write Protection	0 to 70	SO14TR	1209
	ST25C16CML1	2K x 8	2.5	Write Protection	0 to 70	SO14	1209
	ST25C16CML1TR	2K x 8	2.5	Write Protection	0 to 70	SO14TR	1209
	ST24C16CML6	2K x 8	3.0	Write Protection	–40 to 85	SO14	1209
	ST24C16CML6TR	2K x 8	3.0	Write Protection	–40 to 85	SO14TR	1209
	ST25C16CML6	2K x 8	2.5	Write Protection	–40 to 85	SO14	1209
	ST25C16CML6TR	2K x 8	2.5	Write Protection	–40 to 85	SO14TR	1209

ZEROPOWER and TIMEKEEPER

Size	Part Number	Organis.	t_{ACC} (ns)	V_{CC} Range	Temp. Range (°C)	Package	Page Number
512	MK41T56N00	64 x 8	–	5V ± 10%	0 to 70	PSDIP8	1213
	MK41T56S00	64 x 8	–	5V ± 10%	0 to 70	SO8	1213
	MKI41T56S00	64 x 8	–	5V ± 10%	–40 to 85	SO8	1213
	MKI41T56S00TR	64 x 8	–	5V ± 10%	–40 to 85	SO8TR	1213

ST636x ROM Devices. MCU For TV Tuning with ON-Screen Display

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	COLOUR PINS	EMULATING DEVICES	Page Number
ST6365	8K	256	384	YES	YES	4	3	ST63E85, ST63T85	1217
ST6367	8K	256	384	YES	YES	6	3	ST63E87, ST63T87	1217
ST6375	14K	256	384	YES	YES	4	3	ST63E85, ST63T85	1217
ST6377	14K	256	384	YES	YES	6	3	ST63E87, ST63T87	1217
ST6385	20K	256	384	YES	YES	4	3	ST63E85, ST63T85	1217
ST6387	20K	256	384	YES	YES	6	3	ST63E87, ST63T87	1217

ST63E6x EPROM/OTP Devices. MCU For TV Tuning with ON-Screen Display

DEVICE	EPROM (Bytes)	OTPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	COLOUR PINS	TARGET ROM DEVICES	Page Number
ST63E85	20K		256	384	YES	YES	4	3	ST6365, 75, 85	1219
ST63T85		20K	256	384	YES	YES	4	3	ST6365, 75, 85	1219
ST63E87	20K		256	384	YES	YES	6	3	ST6367, 77 87	1219
ST63T87		20K	256	384	YES	YES	6	3	ST6367, 77, 87	1219

ST631xx ROM Devices. MCU For TV Frequency and Voltage Synthesis with On-Screen Display

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	VS	D/A	PACK.	EMUL. DEVICES	Page Number
ST63126	8K	256	128	12	3	4	YES	NO	4	PDIP40	ST63E126	1223
ST63156	8K	256	128	11	3	4	YES	YES	4	PDIP40	ST63E156	1223
ST63140	8K	256	128	6	3	3	YES	YES	1	PDIP28	ST63E140	1223
ST63142	8K	256	128	6	3	3	YES	NO	1	PDIP28	ST63E142	1223

ST631xx EPROM/OTP Devices. MCU For TV Frequency and Voltage Synthesis with On-Screen Display

DEVICE	EPROM (Bytes)	OTP ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	VS	D/A	PACK.	TARGET ROM DEVICES	Page Number
ST63E140	8K		256	128	6	3	3	YES	YES	1	PDIP28	ST63140	1225
ST63T140		8K	256	128	6	3	3	YES	YES	1	PDIP28	ST63140	1225
ST63E142	8K		256	128	6	3	3	YES	NO	1	PDIP28	ST63142	1225
ST631T42		8K	256	128	6	3	3	YES	NO	1	PDIP28	ST63142	1225
ST63E126	8K		256	128	12	3	4	YES	NO	4	PDIP40	ST63126	1225
ST63T126		8K	256	128	12	3	4	YES	NO	4	PDIP40	ST63126	1225
ST63E156	8K		256	128	11	3	4	YES	YES	4	PDIP40	ST63156	1225
ST63T156		8K	256	128	11	3	4	YES	YES	4	PDIP40	ST63156	1225

ST929x ROM Devices. With On-Screen Display and SPI

DEVICE	ROM (Bytes)	RAM (Bytes)	i/O	A/D	D/A Converter 8-bit	D/A Converter 14-bit	Data Slicer	Timer	Package	EMULATING DEVICES*	Page Number
ST9291N6	32K	640	42	1	8	1	–	2	PSDIP56	ST92E91N6	1233
ST9291J6	32K	640	32	1	8	1	–	2	PSDIP42	ST92E91J6	1233
ST9293J7	48K	768	31	1	–	–	–	2	PSDIP42	ST92E93J7	1235
ST9294N6	32K	640	42	1	8	–	1	2	PSDIP56	ST92E91N6	1237
ST9294J6	32K	640	31	1	8	–	1	2	PSDIP42	ST92E94J6	1237

ST92E9x EPROM Devices. With On-Screen Display and SPI

DEVICE	EPROM (Bytes)	RAM (Bytes)	i/O	A/D	D/A Converter 8-bit	D/A Converter 14-bit	Data Slicer	Timer	Package	EMULATING DEVICES*	Page Number
ST92E91N6	32K	640	42	1	8	1	–	2	CSDIP56W	ST9291N6	1233
ST92E91J6	32K	640	32	1	8	1	–	2	CSDIP42W	ST9291J6	1233
ST92E93J7	48K	768	31	1	–	–	–	2	CSDIP42W	ST9293J7	1239
ST92E94N6	32K	640	42	1	8	–	1	2	CSDIP56W	ST9291N6	1241
ST92E94J6	32K	640	31	1	8	–	1	2	CSDIP42W	ST9294J6	1241

ST90R5x, R9x ROMless Devices. With Bankswitch and A/D Converter

DEVICE	ROM (Bytes)	RAM (Bytes)	i/O Port	A/D	Timer	SPI	SCI	Package	Page Number
ST90R51	–	–	54	1	4	1	2	PQFP80	1243
ST90R91C1	–	1536	35	1	3	1	–	PLCC68	1245
ST90R91Q1	–	1536	40	1	3	1	–	PQFP80	1245

ST6369 ROM Device. MCU For Digital Controlled Multi-Frequency Monitor

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	A/D	14-bit D/A	6-bit D/A	EMULATING DEVICES	Page Number
ST6369	8K	256	384	1	1	6	ST63E69, ST63T69	1227

ST6369 EPROM/OTP Device. MCU For Digital Controlled Multi-Frequency Monitor

DEVICE	EPROM (Bytes)	OTPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	A/D	14-bit D/A	6-bit D/A	TARGET ROM DEVICE	Page Number
ST63E69	8K		256	384	1	1	6	ST6369	1229
ST63T69		8K	256	384	1	1	6	ST6369	1229

ST7271 ROM Device. MCU For Digital Controlled Multi-Frequency Monitor

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	D/A Converter 12-bit	D/A Converter 10-bit	Sync. Proc.	Timer	Package	EMULATING DEVICES*	Page Number
ST7271N5	16K	256	512	2	14	1	1	PSDIP56	ST72E71, ST72T71	1231
ST7271J1	16K	256	512	2	10	1	1	PSDIP42	ST72E71, ST72T71	1231

* Note. Contact SGS-THOMSON Marketing for further information.

DEFLECTION ICs

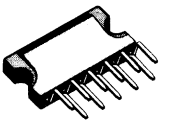
SGS-THOMSON MICROELECTRONICS

STV9303

PULSE DRIVEN VERTICAL BOOSTER

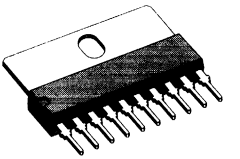
ADVANCE DATA

- OUTPUT CURRENT UP TO 2.5App
- 70V MAXIMUM FLYBACK VOLTAGE
- INTERNAL FLYBACK GENERATOR
- INTERNAL REFERENCE VOLTAGE GENERATOR
- INTERNAL RAMP GENERATOR
- SAWTOOTH STARTED BY THE END OF SYNC PULSE OR BY AN INTERNAL MONOSTABLE
- THERMAL PROTECTION



CLIPWATT 11
(Plastic Package)

ORDER CODE : STV9303W



SIP10
(Plastic Package)

ORDER CODE : STV9303

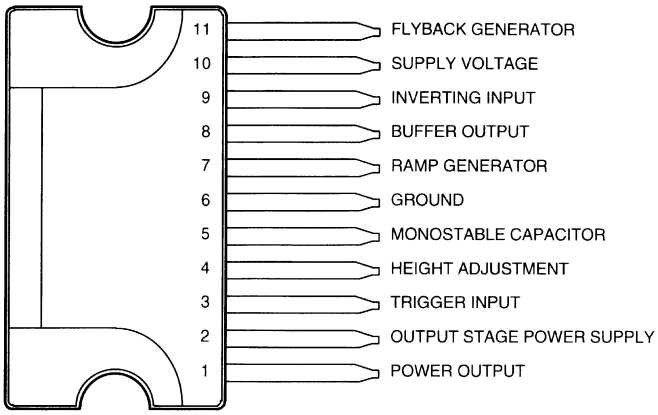
DESCRIPTION

The STV9303 is a pulse driven vertical booster intended for use in color TV. It includes a vertical ramp generator specially designed to fit with deflection processors like STV2102 or STV2110 which provide a 10.5 line lengh vertical pulse. The discharging of the sawtooth capacitor is triggerred by the trailing edge of the vertical sync and the charging by the leading edge.
During the sync pulse duration, the sawtooth will remains at its bottom value. Another possibility is to use the internal monostable (by connecting an external capacitor on Pin 5) to define the point where the sawtooth will restart. This second possibility is very usefull to avoid interlacing problems when using a conventional deflection processor delivering a small duration vertical pulse.
The STV9303 includes a very efficient power amplifier for direct driving of a TV picture tube in B & W or color television.
For power consumption saving, a flyback generator is also included. The current and voltage capabilities (2.5App max output current and 70V flyback peak voltage), make this IC also suitable for large screen TV sets.
Thermal protection is also provided.

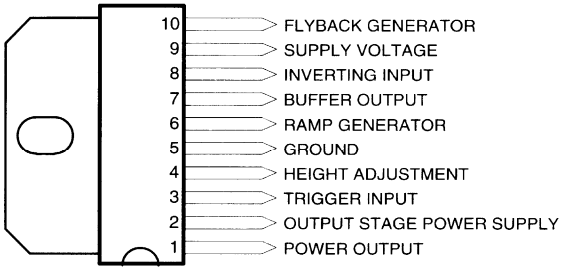
This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS

CLIPWATT11

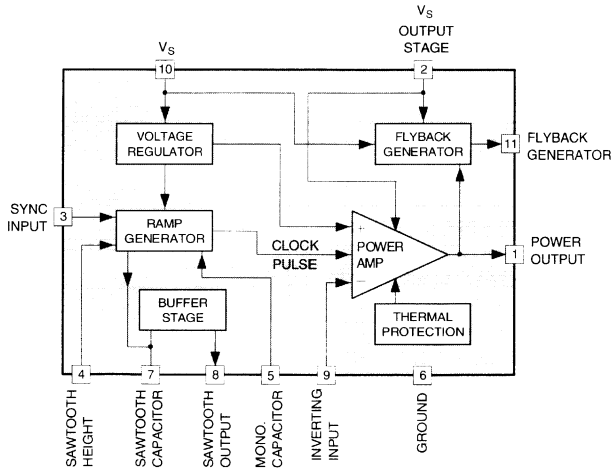


SIP10



9303V-02 EPS/9303V 01 EPS

BLOCK DIAGRAM (CLIPWATT)



9303V-03 EPS

ABSOLUTE MAXIMUM RATINGS (CLIPWATT Pin Connections)

Symbol	Parameter	Pins	Value	Unit
V_S	Supply Voltage	10	35	V
V_F, V_O	Flyback Voltage	1-2	70	V
V_{I-}	Amplifier Input Voltage	9	V_S	V
I_{OP}	Peak Output Current	1	1.5	A
I_{11}	Flyback DC Current at $V_O < V_S$	11	100	mA
I_{11}	Flyback Peak Current (f = 50 or 60Hz, T_{fly} < 1.5ms)	11	1.8	A
V_3	Trigger Input Voltage	3	V_S	V
T_{stg}	Storage Temperature		-40, +150	°C
T_j	Junction Temperature		Internally limited	

9303V-01 TBL

THERMAL DATA

Symbol	Parameter			Value	Unit
T_{pt}	Junction Temperature at Thermal Shutdown		Typ.	140	°C
T_{ph}	Thermal Protection Hysteresis		Typ.	25	°C
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	CLIPWAT11	Max.	3	°C/W
		SIP10	Max.	10	°C/W

9303V-02 TBL

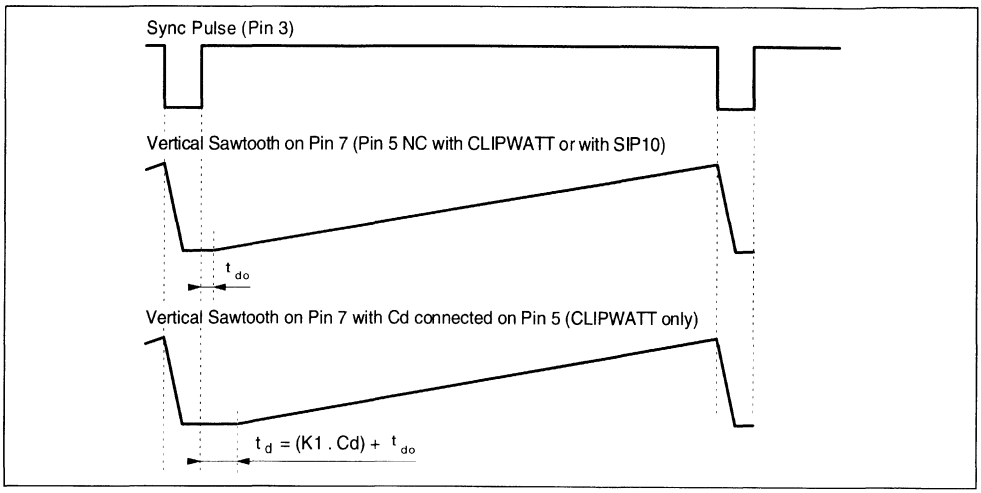
ELECTRICAL CHARACTERISTICS (CLIPWATT Pin Connections)

(V_S = 35V, T_{amb} = 25°C, unless otherwise specified)

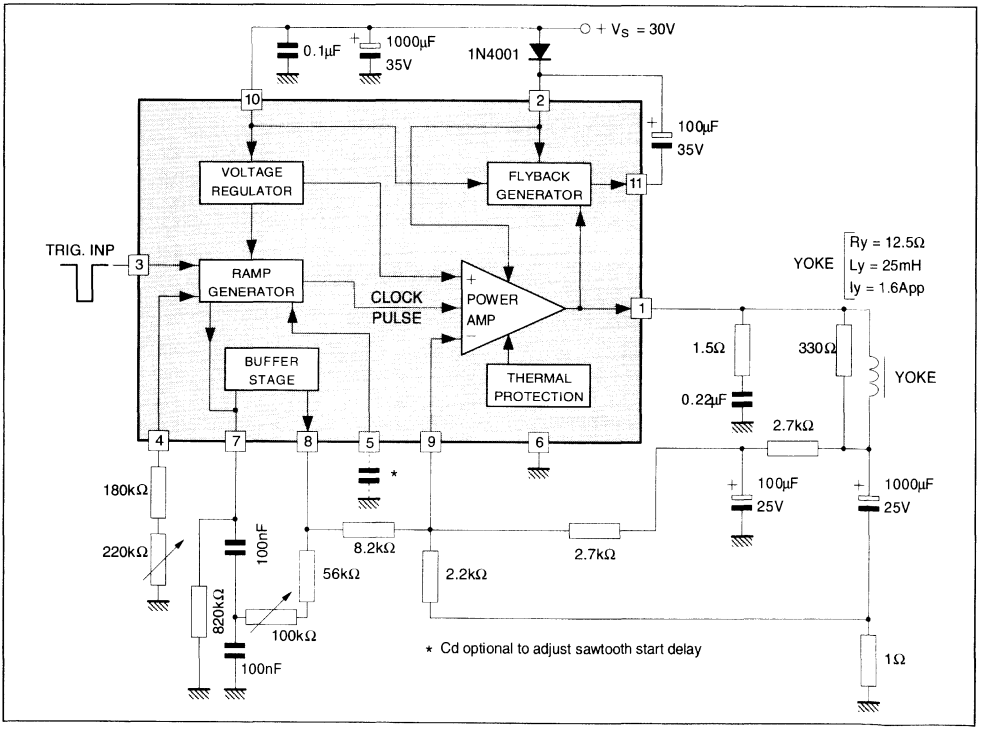
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I_1 = 0, I_{11} = 0		16	36	mA
I_{10}	Pin 10 Quiescent Current	I_1 = 0, I_{11} = 0		15	30	mA
$-I_7$	Ramp Generator Bias Current	V_7 = 0			1	µA
$-I_7$	Ramp Generator Current	V_7 = 0, $-I_4$ = 20µA	18.5	20	21.5	µA
dI_7/I_7	Ramp Generator Linearity	V_7 = 0 to 12V, $-I_4$ = 20µA		0.2	1	%
V_{1L}	Out Saturation Voltage to GND	I_1 = 0.1A I_1 = 1.25A		0.1 1.2	1 2.0	V V
V_{1H}	Out Saturation Voltage to V_S	$-I_1$ = 0.1A $-I_1$ = 1.25A		0.9 1.6	1.6 3.0	V V
V_4	Reference Voltage	$-I_4$ = 20µA	6.3	6.6	6.9	V
dV_4/V_S	Reference Voltage Drift versus V_S	V_S = 10V to 35V		1	2	mV/V
dV_4/dI_4	Reference Voltage Drift versus I_4	I_4 = 10µA to 30µA		0.1	1	mV/µA
V_R	Internal Reference Voltage		4.15	4.40	4.65	V
V_{D11-10}	Diode Fwd Voltage	I_D = 1.25A		1.5	3	V
V_{D1-2}	Diode Fwd Voltage	I_D = 1.25A		1.5	3	V
G_V	Output Stage Open Loop Gain	f = 100Hz		70		dB
V_{fs}	V10-11 Saturation Voltage	$-I_{11}$ = 1.25A		1.5	3.0	V
V_{11}	Pin 11 Saturation Voltage	I_{11} = 20mA		0.8	2	V
V_3	Trigger Input Threshold		2.6	3.0	3.4	V
V_8	Sawtooth Pedestall Voltage			1.85		V
I_1	Peak-to-peak Operating Current Range		0.4		2.5	A
V_{7M}	Max. Voltage on Pin 7		12			V
I_7	Min. Discharging Current		5			mA
K1	Delay between end of Sync Pulse and beginning of Sawtooth versus value of Capacitor on Pin 5			100		µs/nF
t_{do}	Max. Delay between end of Sync Pulse and beginning of Sawtooth Capacitor charging without Capacitor on Pin 5			2	10	µs

9303V-03 TBL

WAVEFORMS



APPLICATION CIRCUIT (CLIPWATT)



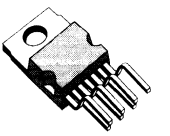
SGS-THOMSON MICROELECTRONICS

STV9379

VERTICAL DEFLECTION BOOSTER

PRELIMINARY DATA

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION
- OUTPUT CURRENT UP TO 2.0A_{PP}
- FLYBACK VOLTAGE UP TO 90V (on Pin 5)
- SUITABLE FOR DC COUPLING APPLICATION



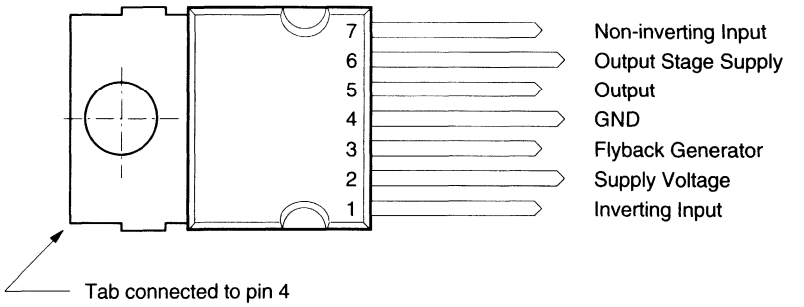
HEPTAWATT
(Plastic Package)

ORDER CODE : STV9379

DESCRIPTION

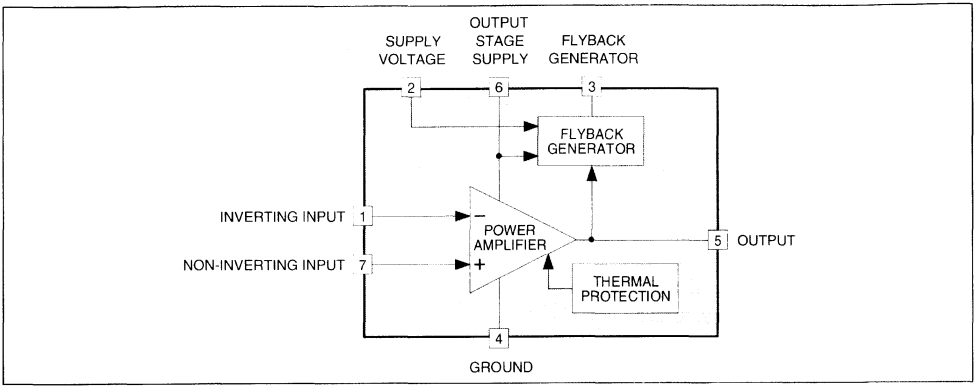
Designed for monitors and high performance TVs, the STV9379 vertical deflection booster delivers flyback voltages up to 90V.
The STV9379 operates with supplies up to 42V and provides up to 2App output current to drive the yoke.
The STV9379 is offered in HEPTAWATT package.

PIN CONNECTIONS



9379-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pin 2) (see note 1)	50	V
V_6	Flyback Peak Voltage (Pin 6) (see note 1)	100	V
V_1 , V_7	Amplifier Input Voltage (Pins 1-7) (see note 1)	- 0.3, + V_S	V
I_O	Maximum Output Peak Current (see notes 2 and 3)	1.5	A
I_3	Maximum Sink Current (first part of flyback) (t < 1ms)	1.5	A
I_3	Maximum Source Current (t < 1ms)	1.5	A
V_{ESD}	Electrostatic Handling for all pins (see note 4)	300	V
T_{oper}	Operating Ambient Temperature	- 20, + 75	°C
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	+150	°C

9379-01.TBL

Notes : 1. Versus GND.
2. The output current can reach 4A peak for t ≤ 10µs (up to 120Hz).
3. Provided SOAR is respected (see Figures 1 and 2).
4. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	3	°C/W
T_t	Temperature for Thermal Shutdown		150	°C
ΔT_t	Hysteresis on T_t		10	°C
T_{jr}	Recommended Max. Junction Temperature		120	°C

9379-02.TBL

ELECTRICAL CHARACTERISTICS

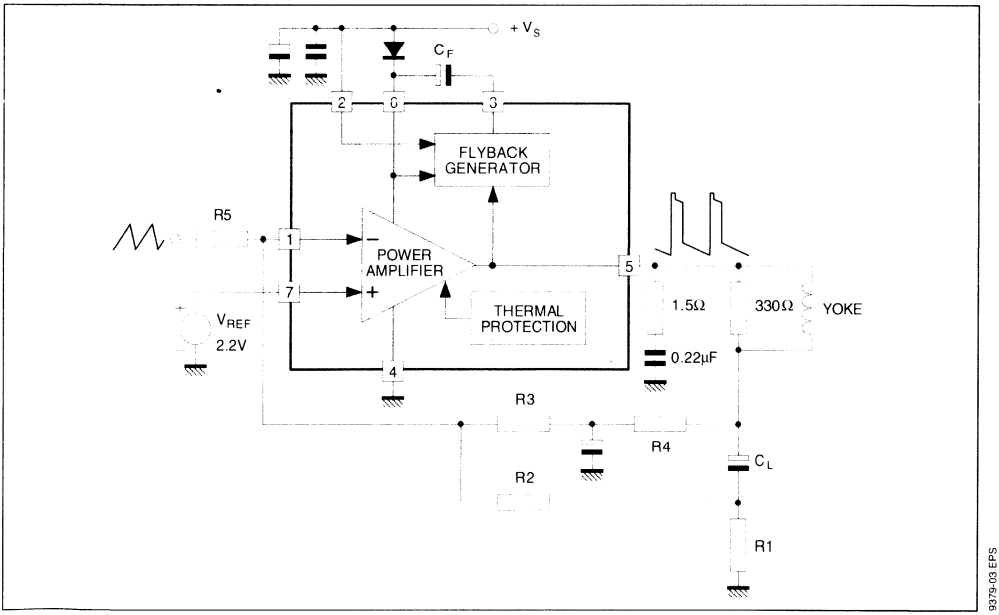
(V_S = 42V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	I_3 = 0, I_5 = 0		10	20	mA
I_6	Pin 6 Quiescent Current	I_3 = 0, I_5 = 0	5	10	30	mA
I_O	Max. Peak Output Current				1	A
I_1	Amplifier Bias Current	V_1 = 25V, V_7 = 26V		- 0.15	- 1	µA
I_7	Amplifier Bias Current	V_1 = 26V, V_7 = 25V		- 0.15	- 1	µA
V_{IO}	Offset Voltage				7	mV
$\Delta V_{IO}/dt$	Offset Drift versus Temperature			- 10		µV/°C
GV	Voltage Gain		80			dB
V_{5L}	Output Saturation Voltage to GND (Pin 4)	I_5 = 1A		1	1.5	V
V_{5H}	Output Saturation Voltage to Supply (Pin 6)	I_5 = - 1A		1.6	2.1	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_5 = 1A		1.5	2	V
V_{D3-2}	Diode Forward Voltage between Pins 3-2	I_3 = 1A		1.5	2	V
V_{3L}	Saturation Voltage on Pin 3	I_3 = 20mA		0.8	1.2	V
V_{3SH}	Saturation Voltage to Pin 2 (2nd part of flyback)	I_3 = - 1A		2.1	2.9	V

9379-03.TBL

APPLICATION CIRCUITS

AC COUPLING



9379-03.EPS

APPLICATION CIRCUITS (continued)
DC COUPLING

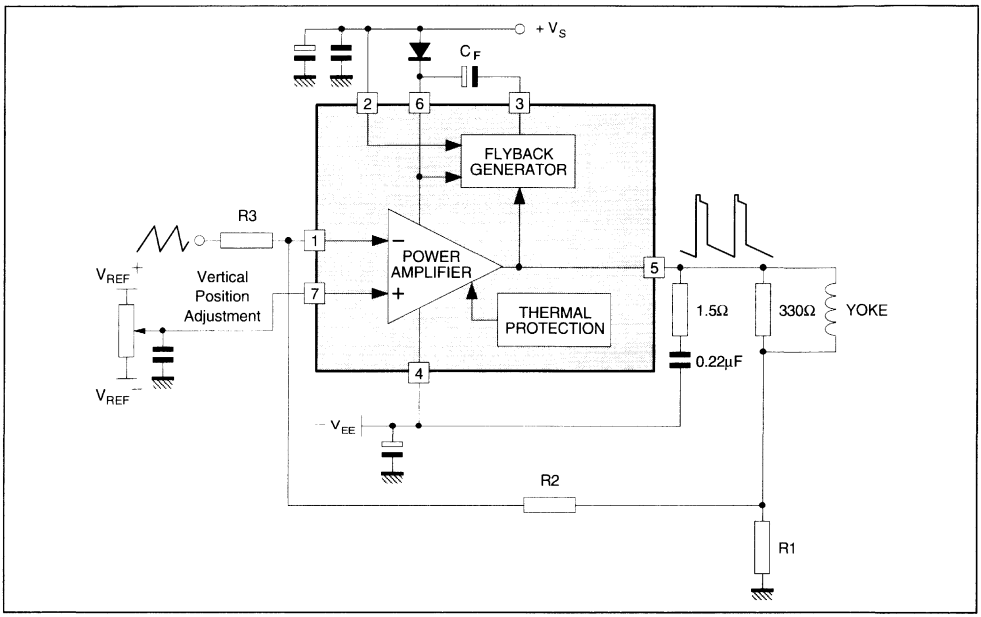


Figure 1 : Output Transistors SOA (for secondary breakdown)

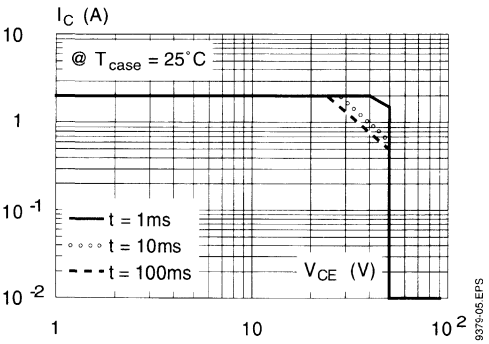
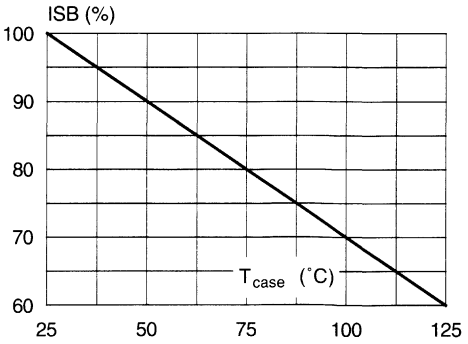


Figure 2 : Secondary Breakdown Temperature Derating Curve (ISB = secondary breakdown current)

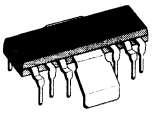


SGS-THOMSON MICROELECTRONICS

TDA1175

LOW-NOISE VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS
- ESD PROTECTED



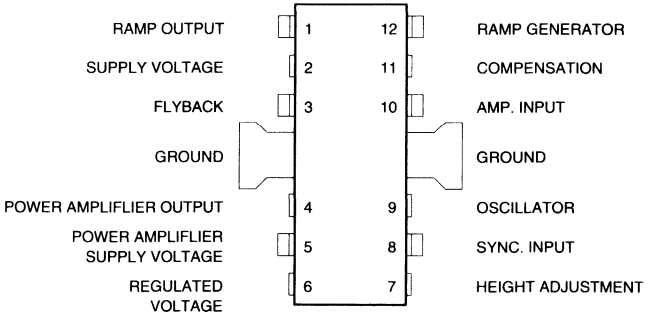
FINDIP
(Plastic Package)

ORDER CODE : TDA1175

DESCRIPTION

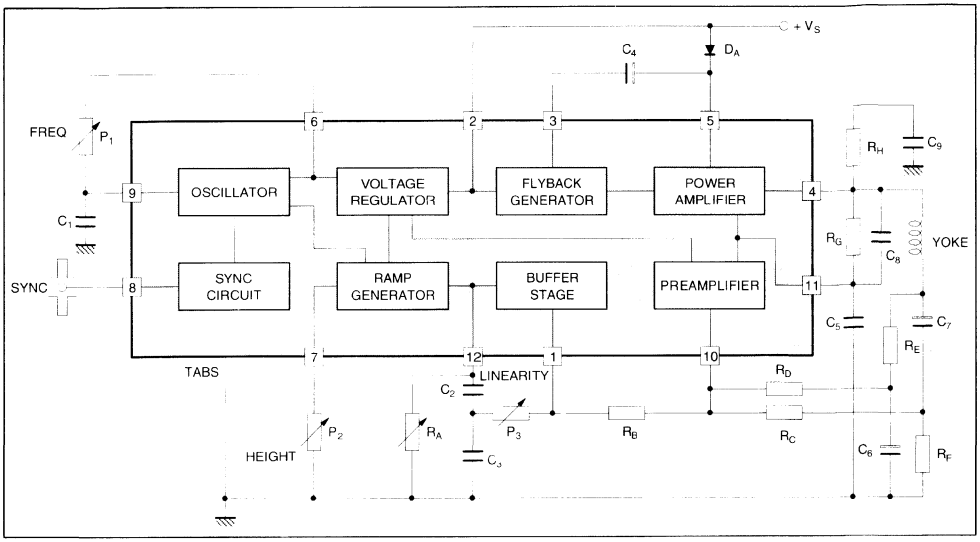
The TDA1175 is a monolithic integrated circuit in FINDIP plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors. The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

PIN CONNECTIONS



1175-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_4, V_5	Flyback Peak Voltage	60	V
V_{10}	Power Amplifier Input Voltage	+ 10 – 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2ms	2	A
I_o	Output Peak Current at f = 50Hz, t ≤ 10µs	2.5	A
I_o	Output Peak Current at f = 50Hz, t > 10µs	1.5	A
I_3	Pin 3 DC Current at $V_4 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50Hz, $t_{fly} \leq 1.5$ms	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{tot}	Power Dissipation : at T_{tab} = 90°C at T_{amb} = 80°C (free air)	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40, + 150	°C

1175-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}tab)}$	Thermal Resistance Junction-tab	Max.	12	°C/W
$R_{th\ (j\text{-}amb)}$	Thermal Resistance Junction-ambient	Max.	70	°C/W(1)

1175-02.TBL

(1) Obtaincd with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS (Refer to the test circuits, V_S = 35V)							
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	17	mA	1b
$-I_9$	Oscillator Bias Current	V_9 = 1V		0.1	1	µA	1a
$-I_{10}$	Amplifier Input Bias Current	V_{10} = 1V		1	10	µA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	µA	1a
$-I_{12}$	Ramp Generator Current	I_7 = 20µA, $V_{12} = 0$	18.5	20	21.5	µA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	ΔV_{12} = 0 to 12V, I_7 = 20µA		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	
V_1	Pin 1 Saturation Voltage to Ground	I_1 = 1mA		1	1.4	V	
V_3	Pin 3 Saturation Voltage to Ground	I_3 = 10mA		1.5	2.5	V	1a
V_4	Quiescent output Voltage	V_S = 10V, R1 = 1kΩ, R2 = 1kΩ V_S = 35V, R1 = 3kΩ, R2 = 1kΩ	4.1 8.2	4.4 8.8	4.7 9.4	V V	1a 1a
V_{4L}	Output Saturation Voltage to Ground	$-I_4$ = 0.1A $-I_4$ = 0.8A		0.9 1.8	1.2 2.2	V v	1c 1c
V_{4H}	Output Saturation Voltage to Supply	I_4 = 0.1A I_4 = 0.8A		1.4 2.8	2.1 3.1	V V	1d 1d
V_6	Regulated Voltage at Pin 6		6.5	6.7	6.9	V	1b
V_7	Regulated Voltage at Pin 7	I_7 = 20µA	6.6	6.8	7	V	1b
$\frlvert\frac{\Delta V_6}{\Delta V_S}\frrvert$, $\frlvert\frac{\Delta V_7}{\Delta V_S}\frrvert$	Regulated Voltage Drift with Supply Voltage	ΔVs = 10 to 35V		1	2	mV/V	1b
V_{10}	Amplifier Input Reference Voltage	$V_8 \leq 0.4$V	2.20	2.27	2.35	V	
AC CHARACTERISTICS (Refer to the AC test circuit, V_S = 22V, f = 50Hz)							
I_s	Supply Current	I_y = 1A_{PP}		140		mA	2
I_8	Sync. Input Current (positive or negative)		0.5		2	mA	2
V4	Flyback Voltage	I_y = 1A_{PP}		45		V	2
t_{fly}	Flyback Time	I_y = 1A_{PP}		0.7		ms	2
V_{ON}	Peak to Peak Output Noise	Pin 9 Connected to GND		18	30	mVpp	2
f_o	Free Running Frequency	(P1 + R1) = 300kΩ C9 = 0.1 µF	36	43.5		Hz	2
f_{OPER}	Operating Frequency Range		10		120	Hz	2
Δf	Synchronization Range	I_8 = 0.5mA, C9 = 0.1µF (P1+R1) = 300kΩ	14			Hz	2
$\frac{\Delta f}{\Delta V_S}$	Frequency Drift with Supply Voltage	V_s = 10 to 35V		0.005		Hz/V	2
$\frac{\lvert\Delta f\rvert}{\Delta T_{ab}}$	Frequency Drift with tab Temperature	T_{tab} = 40 to 120°C		0.01		Hz/°C	2

1175 03 TRI

Figure 1 : DC Test Circuits

Figure 1a

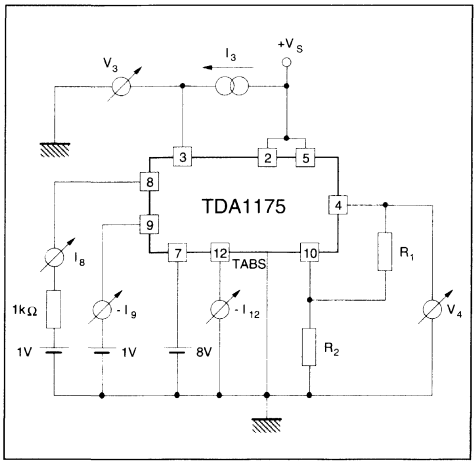


Figure 1b

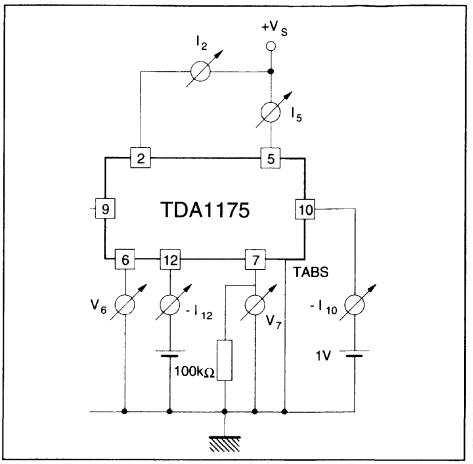


Figure 1c

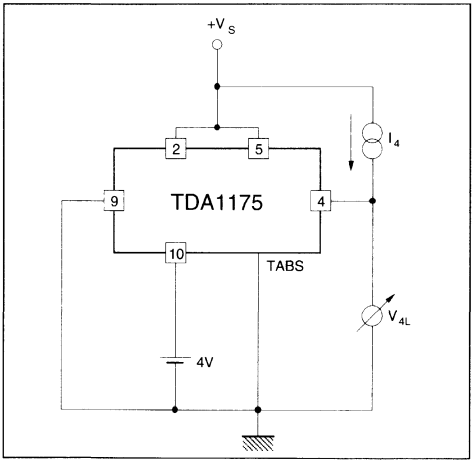


Figure 1d

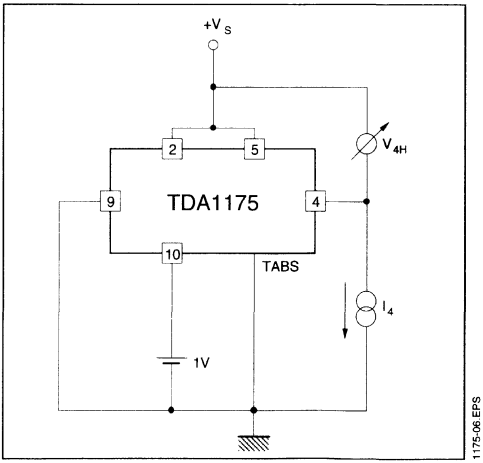


Figure 2 : AC Test and Application Circuit for Large Screen B/W TV Set 10Ω/20mH/1A$_{PP}$

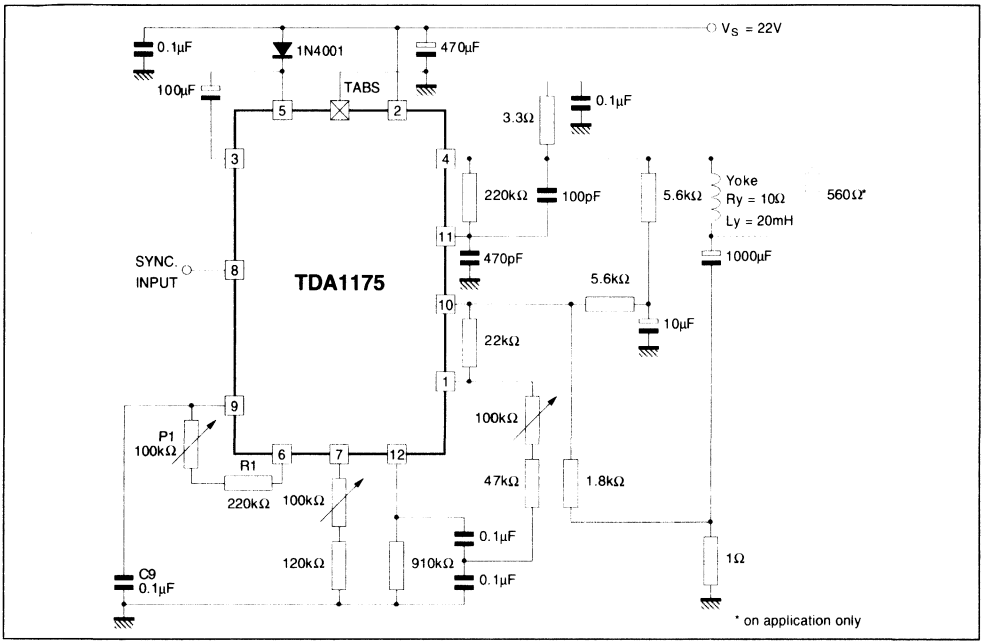


Figure 3 : Typical Application Circuit for Small Screen 90° CTV Set (R$_Y$ = 15Ω, L$_Y$ = 30mH, I$_Y$ = 0.82A$_{PP}$)

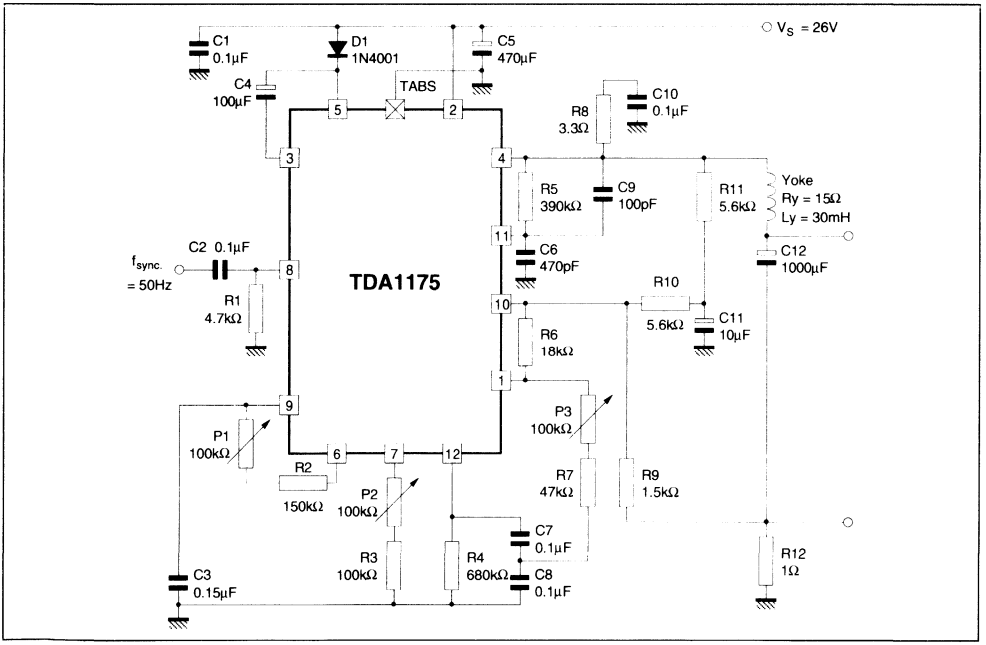
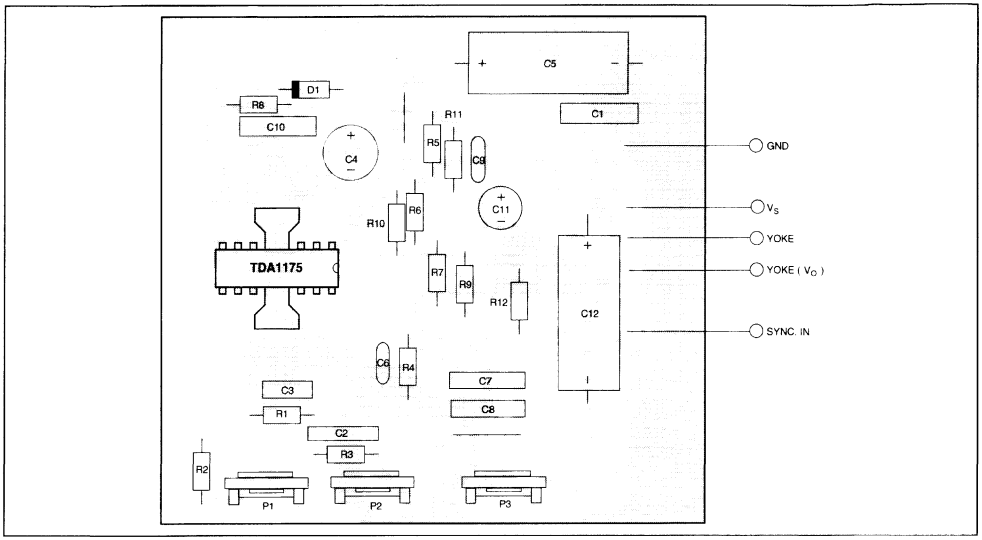


Figure 4 : P.C. Board and Components Layout of the Circuit of Figure 3 (1:1 scale)



MOUNTING INSTRUCTION

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

The junction to ambient thermal resistance can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (Figure 5) or to an external heatsink (Figure 6).

The diagram of Figure 7 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "e" of two equal square copper areas having a thicknessof 35 µ (1.4 mil).

Figure 5 : Example of P.C. Board Copper Area Used as Heatsink

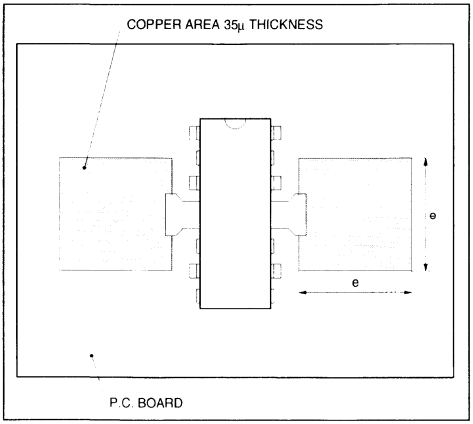


Figure 6 : Example of External Heatsink

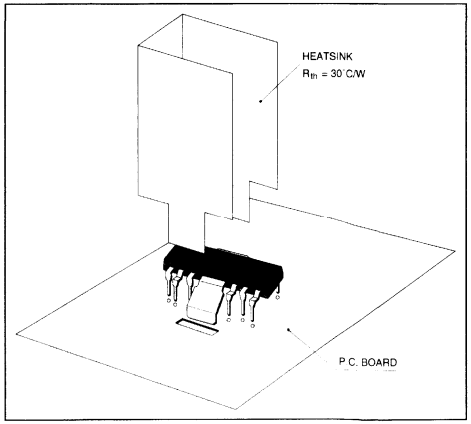


Figure 7 : Maximum Power Dissipation and Junction-ambient Thermal Resistance versus "e"

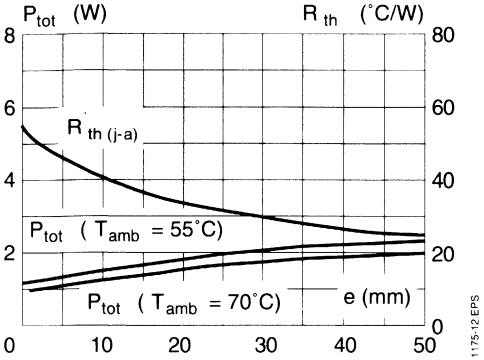
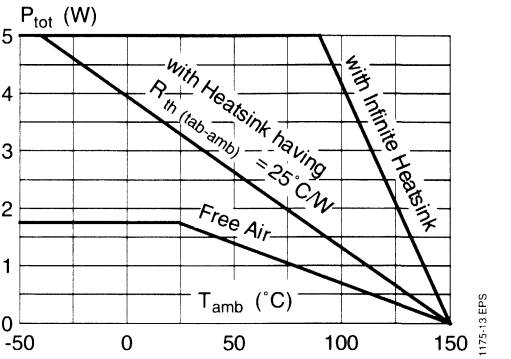


Figure 8 : Maximum Allowable Power Dissipation versus Ambient Temperature

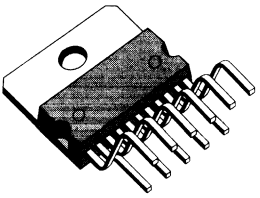


SGS-THOMSON MICROELECTRONICS

TDA1675A

VERTICAL DEFLECTION CIRCUIT

- SYNCHRONISATION CIRCUIT
- ESD PROTECTED
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER WITH HIGH CURRENT CAPABILITY
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT



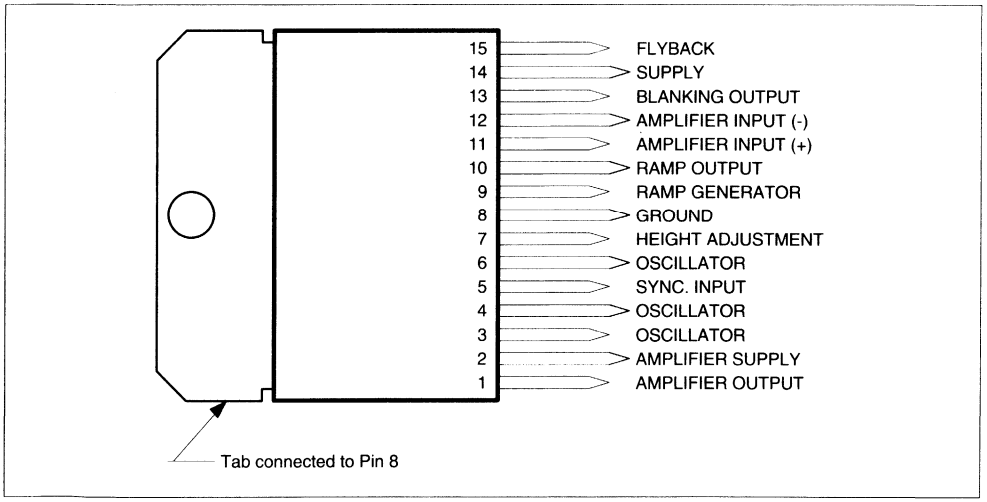
MULTIWATT 15
(Plastic Package)

ORDER CODE : TDA1675A

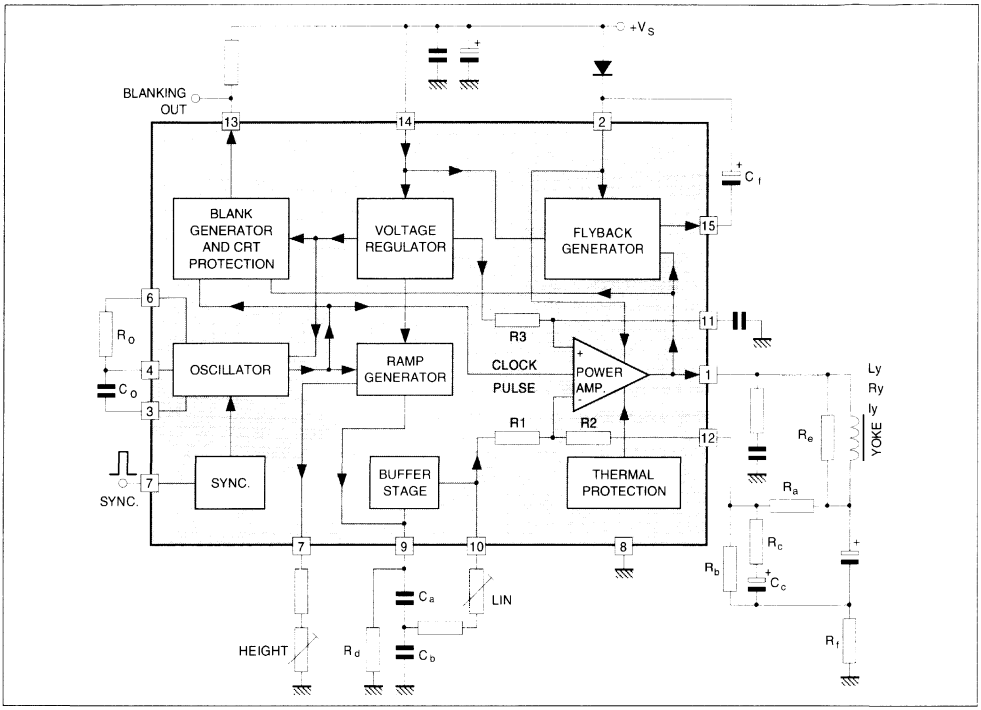
DESCRIPTION

The TDA1675A is a monolithic integrated circuit in 15-lead Multiwatt® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, B&W TVs, monitors and displays.

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 14	35	V
V_1, V_2	Flyback Peak Voltage	65	V
V_5	Sync. Input Voltage	20	V
V_{11}, V_{12}	Power Amplifier Input Voltage	V_S - 10	V
V_{13}	Voltage at Pin 13	V_S	
I_O	Output Current (non repetitive) at t = 2ms	3	A
I_O	Output Peak Current at f = 50Hz t > 10µs	2	A
I_O	Output Peak Current at f = 50Hz t ≤ 10 µs	3.5	A
I_{15}	Pin 15 Peak-to-peak Flyback Current at f = 50Hz, tfly ≤ 1.5ms	3	A
I_{15}	Pin 15 D.C. Current at V1 < V_{14}	100	mA
P_{tot}	Maximum Power Dissipation at $T_{case} \leq 60°C$	30	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	°C

1675A-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W
$R_{TH(j-a)}$	Thermal Resistance Junction-ambient	Max.	40	°C/W

1675A-02 TBL

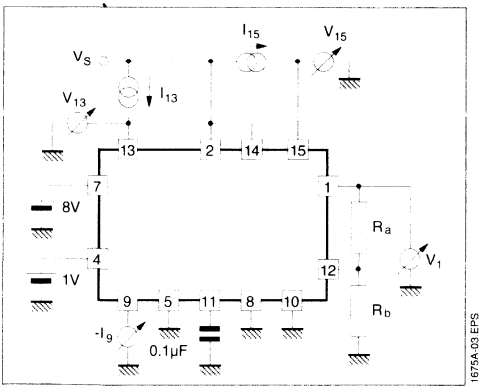
DC ELECTRICAL CHARACTERISTICS (V_S = 35V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 quiescent current	$I_1 = 0$		16	36	mA	1b
$-I_9$	Ramp generator bias current	$V_9 = 0$		0.02	1	µA	1b
$-I_9$	Ramp generator current	$V_9 = 0$; $-I_7 = 20\mu A$	18.5	20	21.5	µA	1b
$\frac{\lvert \Delta I_9 \rvert}{I_9}$	Ramp generator non linearity	$\Delta V_9 = 0$ to 15V, $-I_7 = 20\mu A$		0.2	1	%	1b
I_{14}	Pin 14 quiescent current			25	45	mA	1b
V_1	Quiescent output voltage	V_S = 35V, R_a = 2.2kΩ, R_b = 1kΩ V_S = 15V, R_a = 390Ω, R_b = 1kΩ	16.4 6.9	17.8 7.5	19.5 8.1	V V	1a
V_{1L}	Output saturation voltage to ground	I_1 = 1.2A,		1	1.4	V	1c
V_{1H}	Output saturation voltage to supply	$-I_1$ = 1.2A		1.6	2.2	V	1d
V_4	Oscillator virtual ground			0.45		V	1b
V_7	Regulated voltage at pin 7	$-I_7 = 20\mu A$	6.3	6.6	7	V	1b
$\frac{\Delta V_7}{\Delta V_S}$	Regulated voltage drift with supply voltage	ΔV_S = 15 to 35V		1	2	$\frac{mV}{V}$	1b
V_{11}	Amplifier input (+) reference voltage		4.1	4.4	4.7	V	1b
V_{13}	Blanking output saturation voltage	I_{13} = 10 mA		0.35	0.5	V	1a
V_{15}	Pin 15 saturation voltage to ground	I_{15} = 20 mA		1	1.5	V	1a

1675A-03.TBL

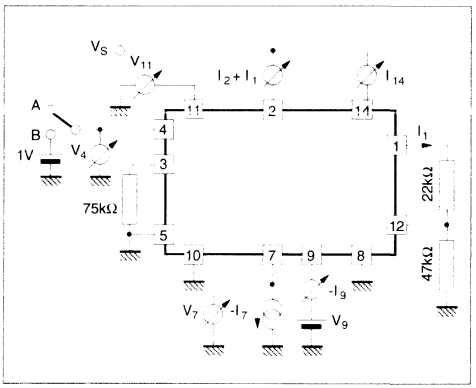
Figure 1 : DC Test Circuit.

Figure 1a



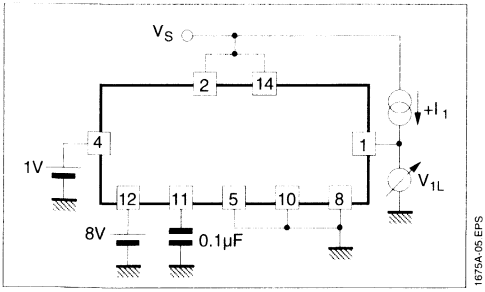
1675A-03.EPS

Figure 1b



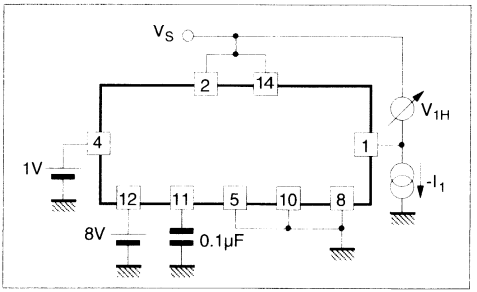
1675A-04.EPS

Figure 1c



1675A-05.EPS

Figure 1d



1675A-06.EPS

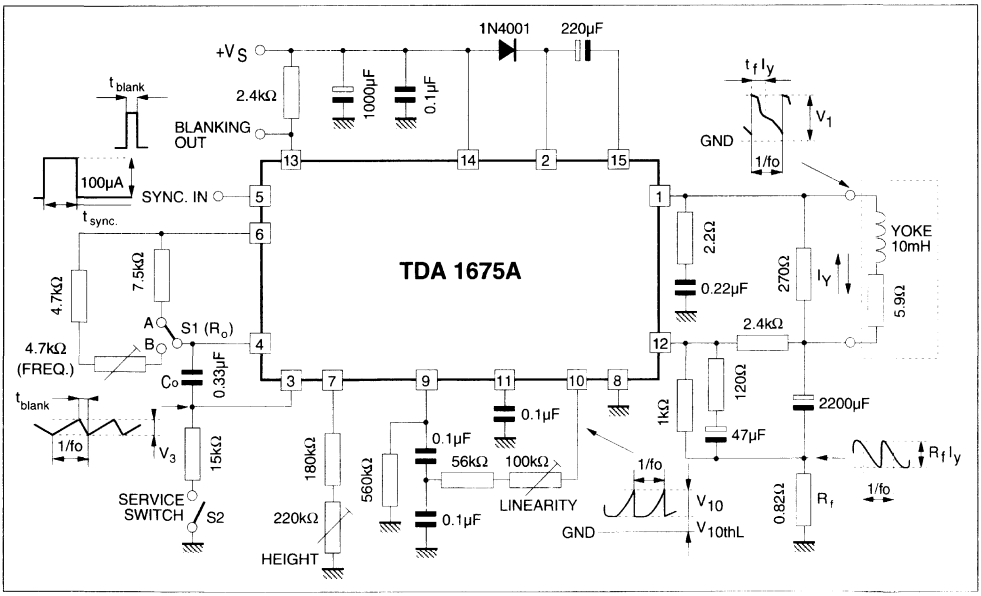
AC ELECTRICAL CHARACTERISTICS

(Refer to A.C. test circuit of fig. 2, T_{amb} = 25°C, V_S = 24V, f = 50Hz, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply Current	I_Y = 2A$_{PP}$		295		mA
I_5	Sync Input Current Required to Sync		100			µA
V_1	Flyback Voltage	I_y = 2App		50		V
V_3	Peak-to-peak Oscillator Sawtooth Voltage	I_5 = 0 I_5 = 100µA		3.6 3.4		V V
$V_{10TH(L)}$	Start Scan Level of the Input Ramp			1.85		V
t_{FLY}	Flyback Time	Iy = 2App		0.6		ms
t_{BLANK}	Blanking Pulse Duration	f_o = 50Hz, T_j = 75°C f_o = 60Hz, T_j = 75°C	1.33	1.4 1.17	1.47	ms ms
f_o	Free Running Frequency	R_o = 7.5kΩ, C_o = 330nF, T_j = 75°C R_o = 6.2kΩ, C_o = 330nF, T_j = 75°C	42	43.5 52.5	46	Hz Hz
Δf	Synchronization Range	I_5 = 100µA, T_j = 75°C	14	16		Hz
T_j	Junction Temperature for Thermal Shut-down			145		°C
V_{ON}	Peak-to-peak Output Noise				35	mV$_{PP}$

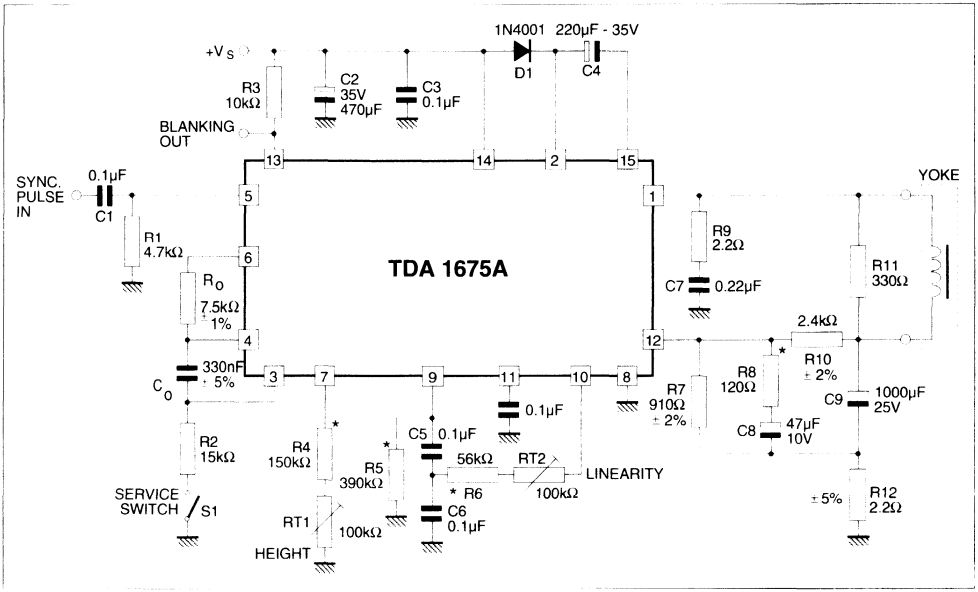
1675A-04.TBL

Figure 2 : AC Test Circuit



1675A-07.EPS

Figure 3 : Application Circuit for Small Scree 90° CTV Set (R_y = 15Ω ; L_y = 30 mH ; I_y = 0.82 A_{PP})



* The value depends on the characteristics of the CRT. The value shown is indicative only.

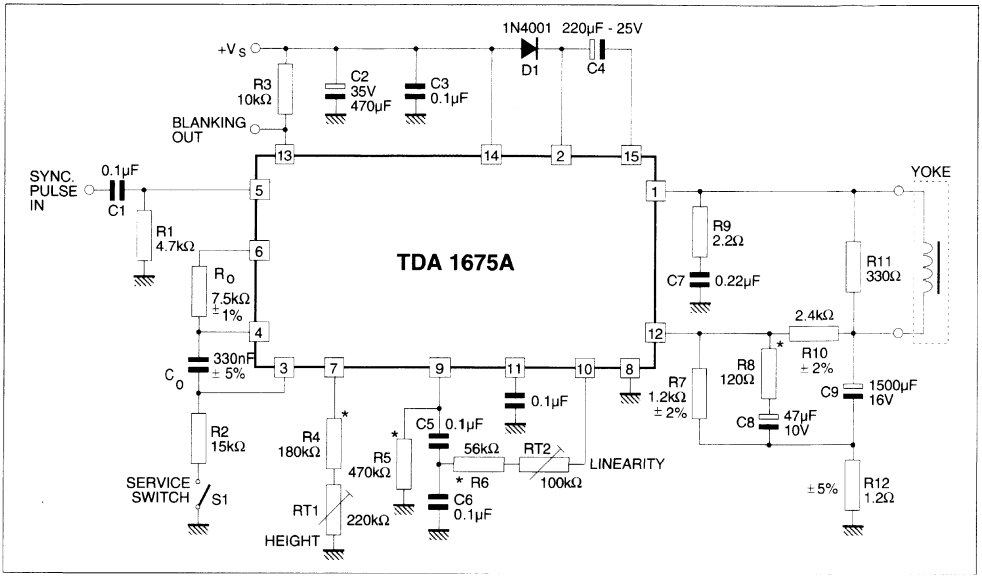
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	25	V
I_S	Supply current	140	mA
t_{FLY}	Flyback time	0.7	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.4	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for T_{amb} = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 13 16	 °C/W °C/W

1675A-05.TBL

* Worst case condition.

Figure 4 : Application Circuit for 110° CTV Set (R_y = 9.6Ω ; L_y = 24.6 mH ; I_y = 1.2 A_{PP})



1675A-09.EPS

* The value depends on the characteristics of the CRT. The value shown is indicative only.

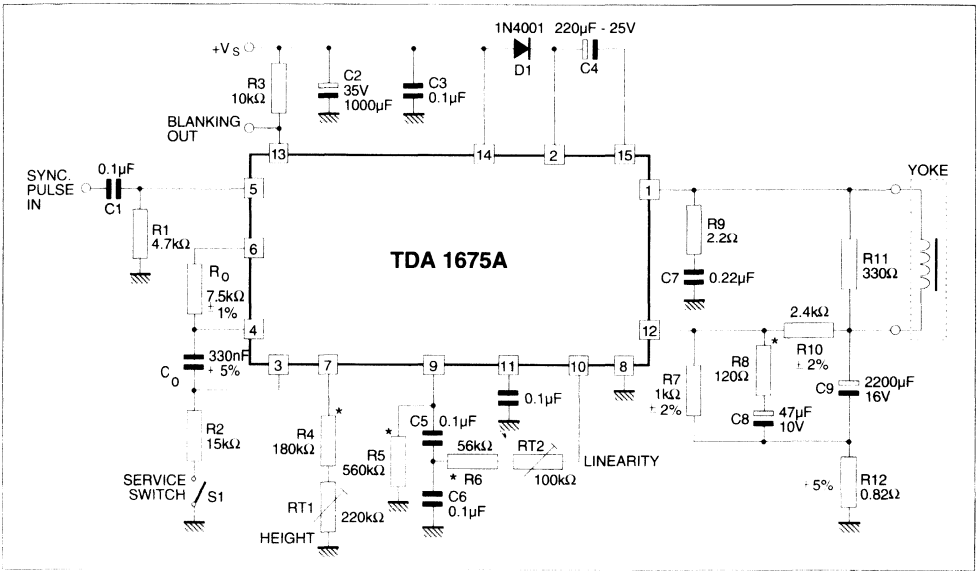
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	22.5	V
I_S	Supply current	185	mA
t_{FLY}	Flyback time	1	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	2.7	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 11.5 14.5	 °C/W °C/W

1675A-06.TBL

* Worst case condition.

Figure 5 : Application Circuit for 110° CTV Set (R_y = 5.9Ω ; L_y = 10 mH ; I_y = 1.95 App)



* The value depends on the characteristics of the CRT. The value shown is indicative only.

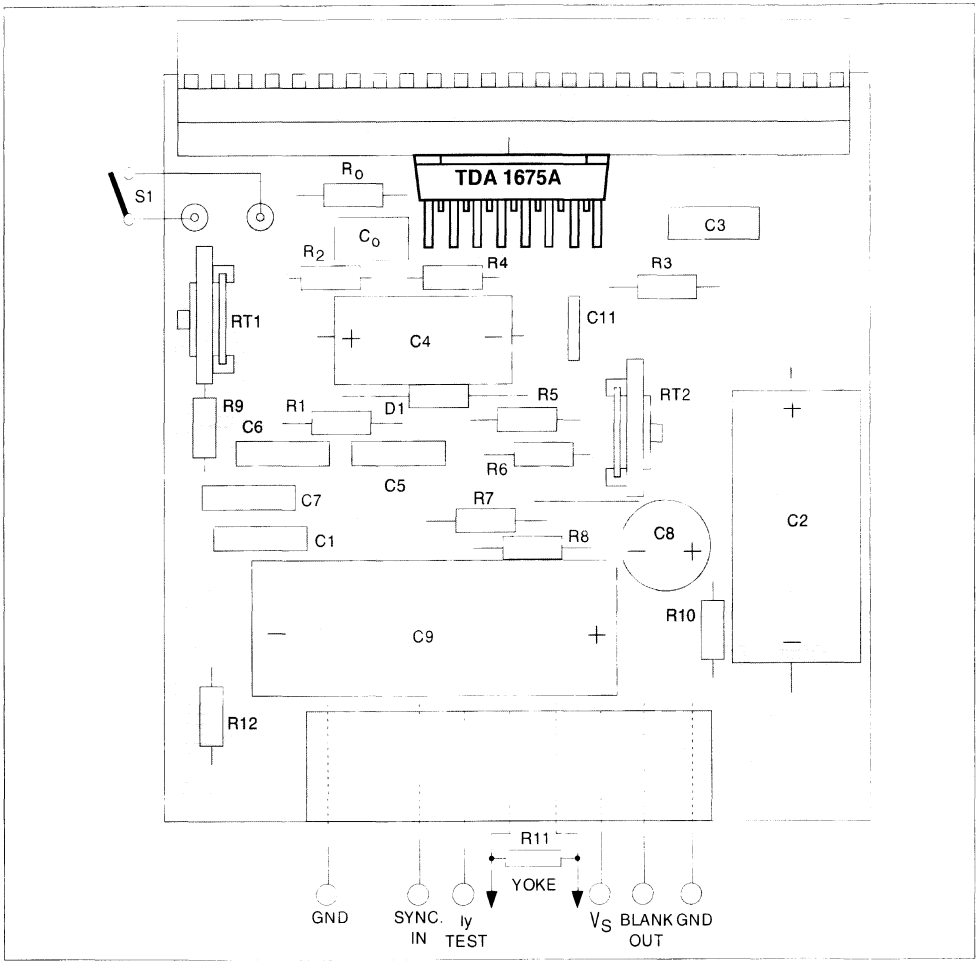
TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum supply voltage	24	V
I_S	Supply current	285	mA
t_{FLY}	Flyback time	0.6	ms
t_{BLKG}	Banking time	1.4	ms
f_O	Free running frequency	43.5	Hz
* P_{TOT}	Power dissipation	4.3	W
* $R_{TH(heatsink)}$	Thermal resistance of the heatsink for Tamb = 60°C and $T_{j\,max}$ = 110°C for T_{amb} = 60°C and $T_{j\,max}$ = 120°C	 6.5 8.5	 °C/W °C/W

1675A-07.TBL

* Worst case condition.

Figure 6 : PC Board and Components Layout for the Application Circuits of Figures 3, 4 and 5 (1 : 1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.

The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 4 is the inverting input of the amplifier used as integrator.

Pin 6 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 3 is the output of the amplifier.

Pin 5 is the input for sync pulses (positive)

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained by means of the series of two capacitors Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from C_a and C_b.

Pin 7 The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.

Pin 9 is the output of the current mirror that charges the series of C_a and C_b. This pin is also the input of the buffer stage.

Pin 10 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 12 is the inverting input of the amplifier. An external network, R_a and R_b, defines the DClevel across C_y so allowing a correct centering of the output voltage. The series network R_c and C_c, in conjunction with R_a and R_b, applies at the feedback input I_2 a small part of the parabola, available across C_y, and AC feedback voltage, taken across R_f. The external components R_c, R_a and R_d, produce the linearity correction on the output scanning currently and their values must be optimized for each type of CRT.

Pin 11 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured. A capacitor must be connected to increase the performances from the noise point of view.

Pin 1 is the output of the power amplifier and it drives the yoke by a negative slope current ramply. R_e and the Boucherot cell are used to stabilize the power amplifier.

Pin 2 The supply of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_S by a diode, while during the retrace time this pin is supplied from the flyback generator.

Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor C_f at the supply voltage pin of the power stage (pin 2).

When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power output amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 15 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor C_f transfers the jump to pin 2 (see pin 2).

Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time

when a flyback pulse has been generated. If the flyback pulse is absent (short cirucit or open cirucit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 13 is an open collector output where the blanking pulse is available.

Voltage regulator

The main supply voltage V_S, is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 14 is the main supply voltage input V_S (positive).

Pin 8 is the GND pin or the negative input of V_S

Figure 7 : Output Saturation Voltage to Ground vs. Peak Output Current

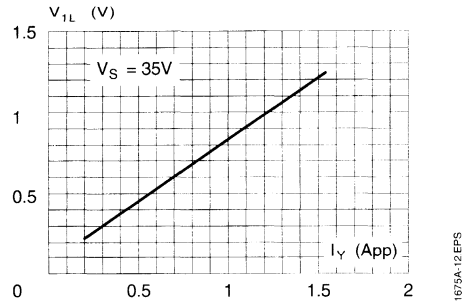


Figure 8 : Output Saturation Voltage to Supply versus Output Peak Current

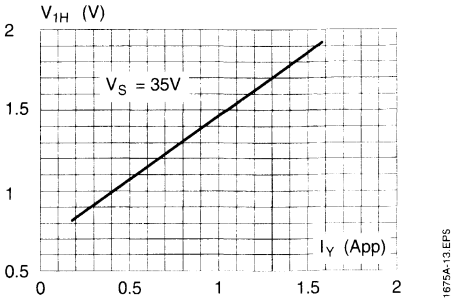
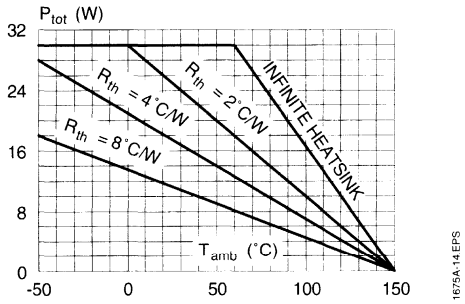


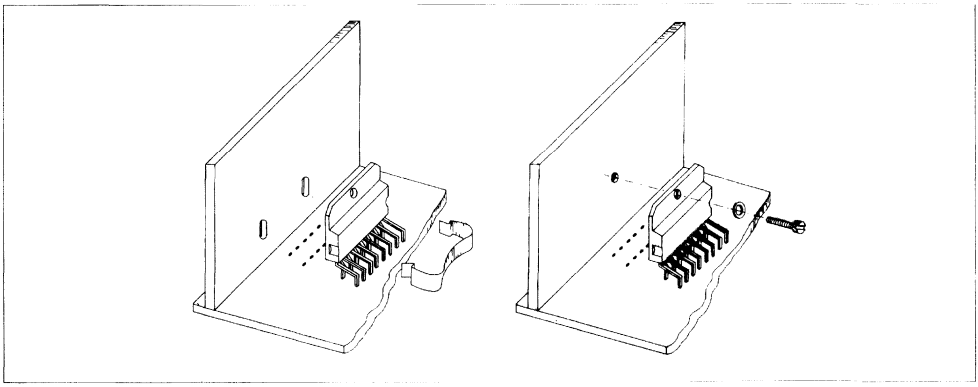
Figure 9 : Maximum allowable Power Dissipation vs. Ambient Temperature



MOUNTING INSTRUCTIONS

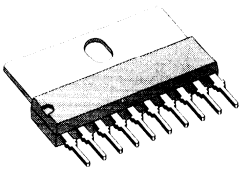
The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the MULTIWATT ® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package, it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Figure 10 : Mounting Examples



VERTICAL DEFLECTION CIRCUIT

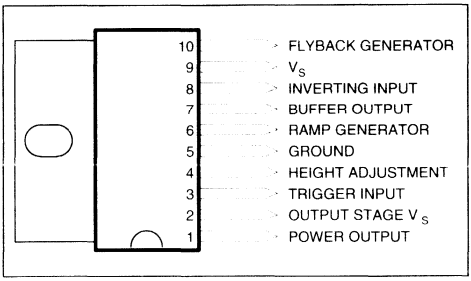
- RAMP GENERATOR
- INDEPENDENT AMPLITUDE ADJUSTEMENT
- BUFFER STAGE
- POWER AMPLIFIER
- FLYBACK GENERATOR
- INTERNAL REFERENCE VOLTAGE
- THERMAL PROTECTION



SIP10
(Plastic Package)

ORDER CODE : TDA1771

PIN CONNECTIONS (top view)



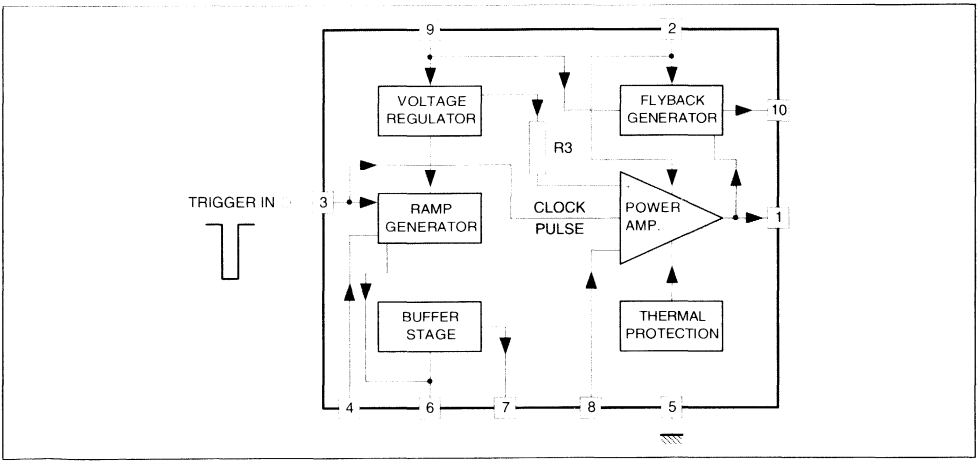
1771-01.EPS

DESCRIPTION

The TDA1771 is a monolithic integrated circuit in SIP10 package.

It is a full performance and very efficient vertical deflection circuit intended for direct drive of a TV picture tube in Color and B & W television as well as in Monitor and Data displays.

BLOCK DIAGRAM



1771-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	30	V
V_1 , V_2	Flyback Peak Voltage	65	V
V_3	Trigger Input Voltage	20	V
V_8	Amplifier Input Voltage	GND to V_S	V
I_0	Output Peak to Peak Current (non repetitive t = 2ms)	6	A
I_0	Output Peak to Peak Current t > 10µs	4	A
I_{10}	Pin 10 DC Current at $V_1 < V_9$	100	mA
I_{10}	Pin 10 Peak to Peak Current @ $t_{fly} < 1.5ms$	3	A
P_{tot}	Total Power Dissipation @ $T_{tab} = 60°C$	9	W
T_S, T_J	Storage and Junction Temperature	– 40, + 150	°C

1771-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}tab)}$	Thermal Resistance Junction-tab	Max.	10	°C/W
$R_{th\ (j\text{-}a)}$	Thermal Resistance Junction-ambient	Max.	70	°C/W

1771-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC (V_S = 30V)						
I_2	Pin 2 Quiescent Current	$I_1 = 0$, $I_{10} = 0$		16	36	mA
I_9	Pin 9 Quiescent Current	$I_1 = 0$, $I_{10} = 0$		15	30	mA
$-I_6$	Ramp Generator Bias Current	$V_6 = 0$			0.5	µA
$-I_6$	Ramp Generator Current	$V_6 = 0$, $-I_4 = 20µA$	18.5	20	21.5	µA
dI_6/I_6	Ramp Gener. Linearity	V_6 = 0 to 15V, $-I_4 = 20µA$		0.2	1	%
V_1	Quiescent Output Voltage	$R_a = 30k\Omega$, $R_b = 10k\Omega$, $V_S = 30V$	17.0	17.8	18.6	V
		$R_a = 6.8k\Omega$, $R_b = 10k\Omega$, $V_S = 15V$	7.2	7.5	7.8	V
V_{1L}	Out Saturation Voltage to GND	$I_1 = 0.5A$		0.5	1	V
		$I_1 = 1.2A$		1	1.4	V
V_{1H}	Out Saturation Voltage to V_S	$-I_1 = 0.5A$		1.1	1.6	V
		$-I_1 = 1.2A$		1.6	2.2	V
V_4	Reference Voltage	$-I_4 = 20µA$	6.3	6.6	6.9	V
dV_4/V_S	Reference Voltage Drift Versus V_S	V_S = 10V to 30V		1	2	mV/V
dV_4/dI_4	Reference Voltage Drift Versus I_4	I_4 = 10µA to 30µA		1.5	2	mV/µA
V_r	Internal Ref. Voltage		4.26	4.40	4.54	V
Gv	Ouput Stage Open Loop Gain	f = 100Hz		60		dB
V_{fs}	V_{9-10} Saturation Voltage	$-I_{10} = 1.2A$		1.5	2.5	V
V_{10}	Pin 10 Scanning Voltage	$I_{10} = 20mA$		1.7	3	V
V_3	Trigger Input Threshold	(see note 1)	2.6	3.0	3.4	V
I_3	Trigger Input Bias Current	$V_{IN} = V_3 - 0.2V$			30	µA
t_3	Trigger Input Width	(see note 2)	20	60	th	µS

1771-03.TBL

Notes : 1. The trigger input circuit can accept, with a metal option, positive and negative going input pulses.

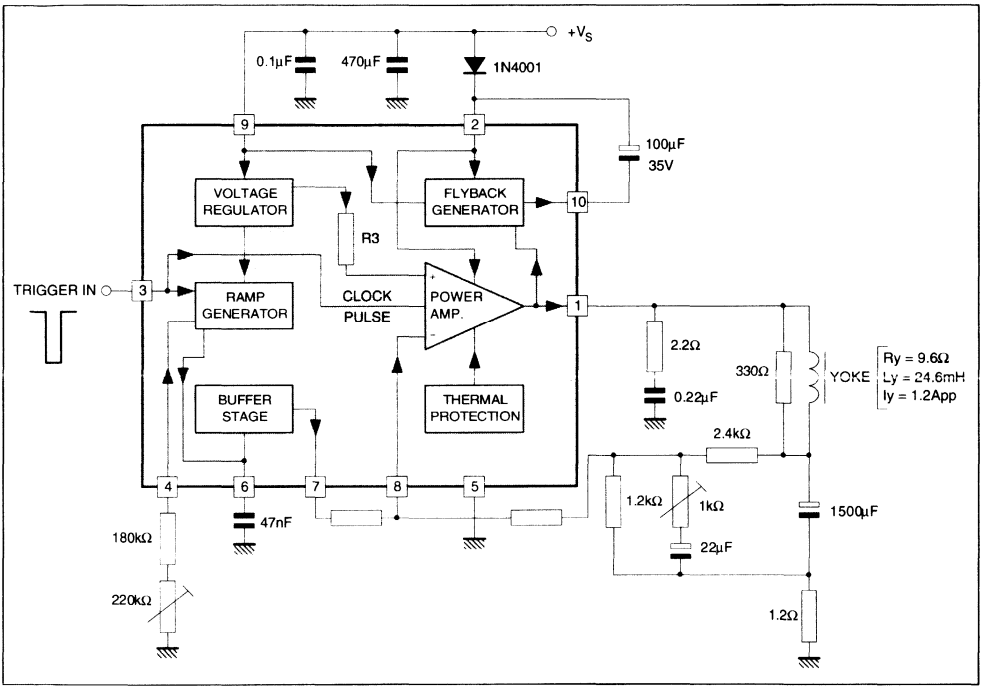
2. $th = \frac{1.2 \cdot t_S}{V_{PP}}$ where t_S is the vertical period and V_{PP} is ramp amplitude at Pin 6

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC (V_S = 24V)						
V_S	Operating Supply Voltage Range		10		30	V
I_1	Peak-to-peak Operating Current Range		0.4		2.5	A
I_S	Supply Current	I_Y = 2.4A_{pp}		315		mA
V_1	Flyback Voltage	I_Y = 2.4A_{pp}		51		V
V_7	Sawtooth Pedestall Voltage			1.85		V
T_{JS}	Junction Temp. for Thermal Shutdown			145		°C

1771-04.TBL

APPLICATION CIRCUIT



1771-03.EPS

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The functions incorporated are :
- POWER AMPLIFIER
- FLYBACK GENERATOR
- REFERENCE VOLTAGE
- THERMAL PROTECTION

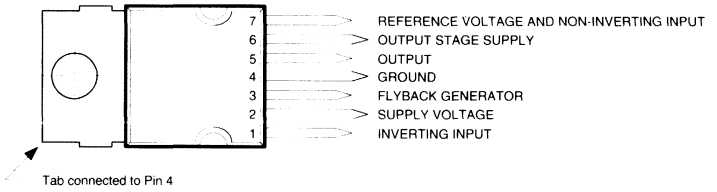
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8170

DESCRIPTION

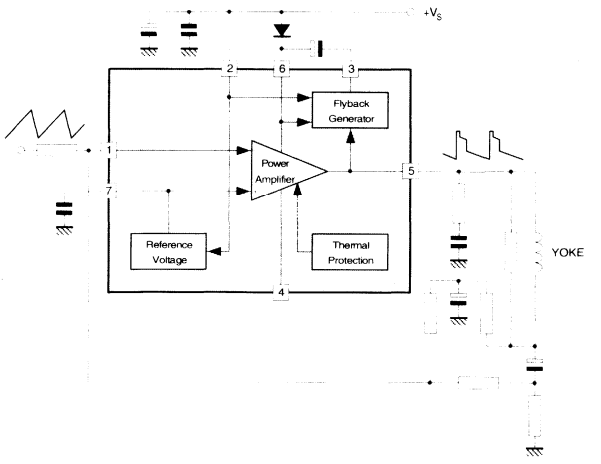
The TDA8170 is a monolithic integrated circuit in HEPTAWATT™ package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour and B & W television receivers as well as in monitors and displays.

PIN CONNECTIONS



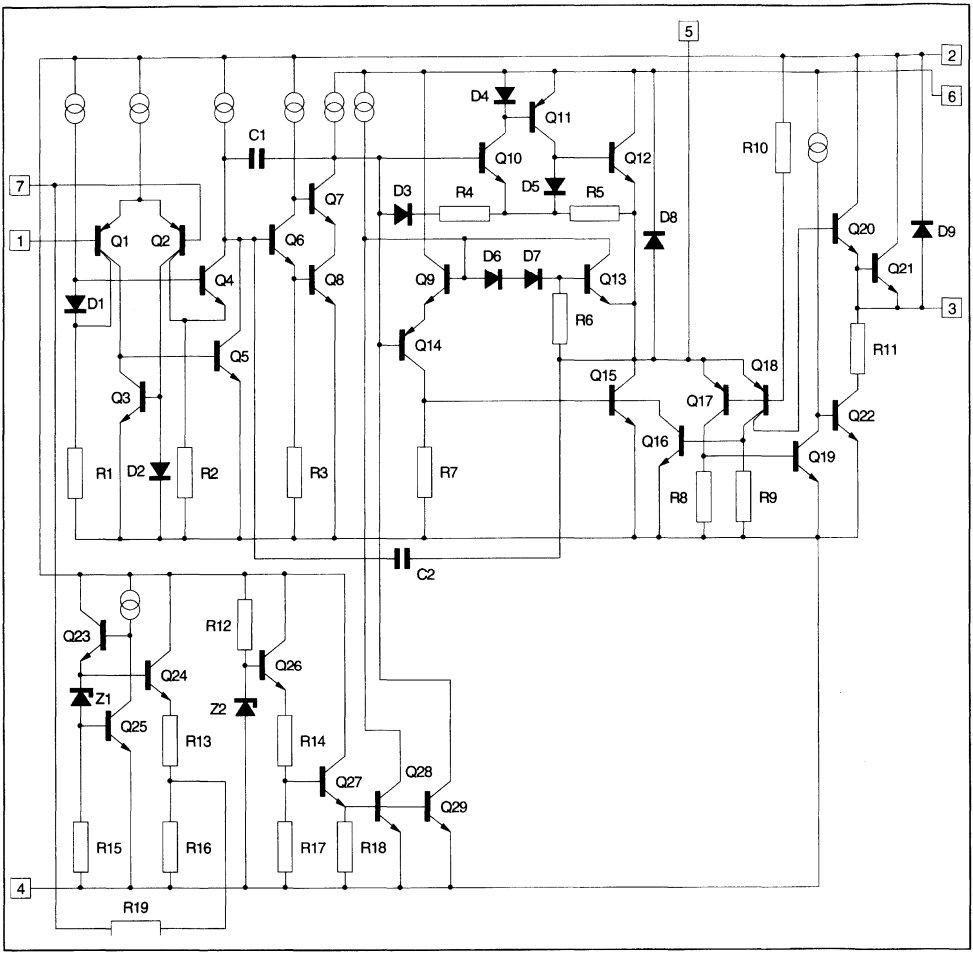
8170-01.EPS

BLOCK DIAGRAM



8170-02.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+ V_s$	
V_1, V_7	Amplifier Input Voltage	$+ V_s$ $- 0.5$	V
I_o	Output Peak Current (non repetitive, t = 2 msec)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, $t \leq 10$ µsec	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µsec	2	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current at f= 50 or 60 Hz, $t_{fly} \leq 1.5$msec	3	A
P_{tot}	Total Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

8170-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	°C/W

8170-02 TBL

ELECTRICAL CHARACTERISTICS

(refer to the test circuits, V_S = 35V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$, $I_5 = 0$		8	16	mA	1a
I_6	Pin 6 Quiescent Current	$I_3 = 0$, $I_5 = 0$		16	36	mA	1a
i_1	Amplifier input Bias Current	V_1 = 1 V		– 0.1	– 1	µA	1a
V_7	Reference Voltage			2.2		V	1a
$\frac{\Delta V_7}{\Delta V_S}$	Reference Voltage Drift versus Supply Voltage	V_s = 15 to 30 V		1	2	mV/V	1a
V_{3L}	Pin 3 Saturation Voltage to GND	I_3 = 20 mA		1		V	1c
V_5	Quiescent Output Voltage	V_s = 35 V , R_a = 39 kΩ		18		V	1d
		V_s = 15 V , R_a = 13 kΩ		7.5		V	1d
V_{5L}	Output Saturation Voltage to GND	I_5 = 1.2 A		1	1.4	V	1c
		I_5 = 0.7 A		0.7	1	V	1c
V_{5H}	Output Saturation Voltage to Supply	$- I_5$ = 1.2 A		1.6	2.2	V	1b
		$- I_5$ = 0.7 A		1.3	1.8	V	1b
T_j	Junction Temperature for Thermal Shut Down			140		°C	

8170-03 TBL

Figure 1a : Measurement of I_1, I_2, I_6, V_7, $\Delta V_7/\Delta V_S$

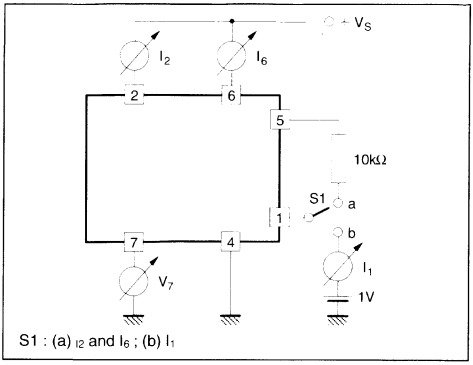


Figure 1b : Measurement of V_{5H}

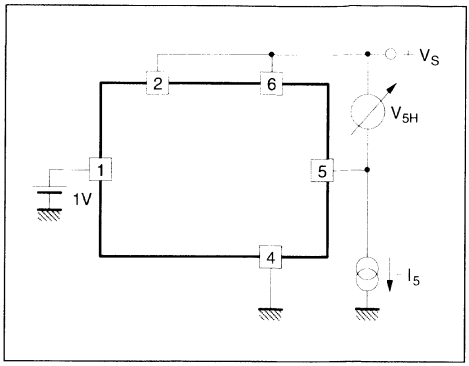


Figure 1c : Measurement of V_{3L}, V_{5L}

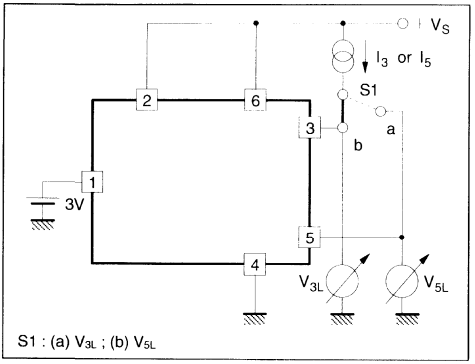


Figure 1d : M

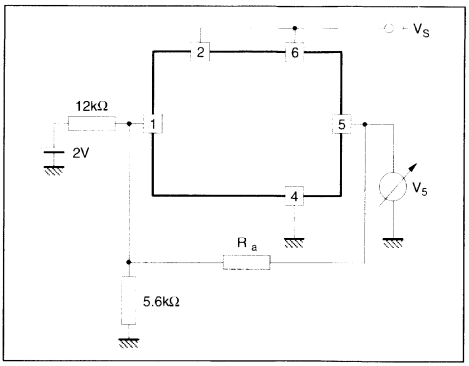


Figure 2 : AC Test Circuit

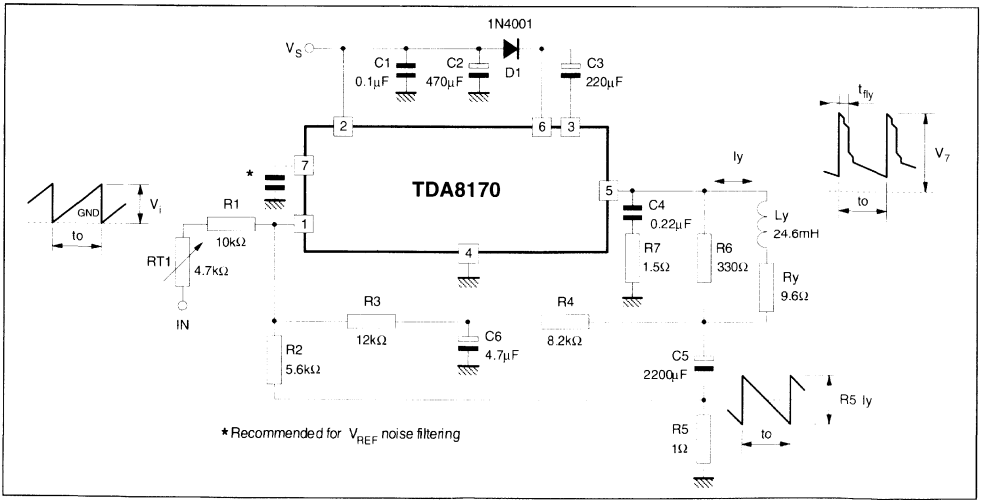
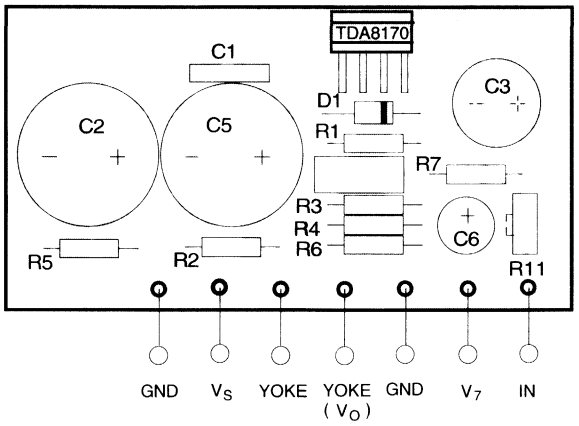


Figure 3 : PC Board and Component layout of the Circuit of fig. 2(1 : 1 scale)



8170-09.EPS

COMPONENTS LIST FOR TYPICAL APPLICATIONS

Component	110 ° TVC 5.9 Ω/10 mH 1.95 App	110 ° TVC 9.6 Ω/24.6 mH 1.2 App	90 ° TVC 15 Ω/30 mH 0.82 App	Unit
RT1	10	4.7	10	kΩ
R1	12	10	12	kΩ
R2	10	5.6	5.6	kΩ
R3	27	12	18	kΩ
R4	12	8.2	5.6	kΩ
R5	0.82	1	1	Ω
R6	270	330	330	Ω
R7	1.5	1.5	1.5	Ω
D1	1N 4001	1N 4001	1N 4001	–
C1	0.1	0.1	0.1	µF
C2 el.	1000/25 V	470/25 V	470/25 V	µF
C3 el.	220/25 V	220/25 V	220/25 V	µF
C4	0.22	0.22	0.22	µF
C5 el.	200/25 V	2200/25 V	1000/16 V	µF
C6 el.	4.7/16 V	4.7/16 V	10/16 V	µF

8170-04.TBL

TYPICAL PERFORMANCES

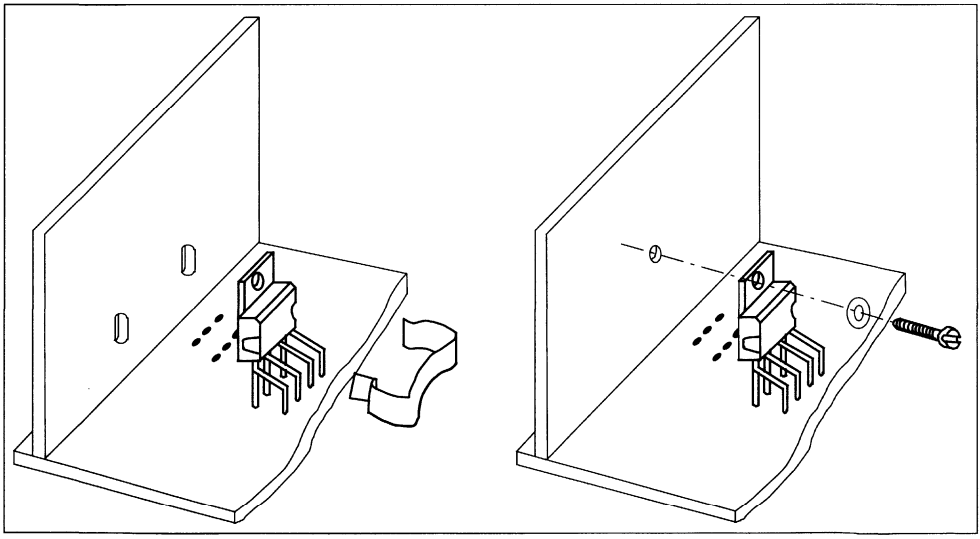
Parameter	110 ° TVC 5.9 Ω/10 mH	110 ° TVC 9.6 Ω/27 mH	90 ° TVC 15 Ω/30 mH	Unit
V_s - Supply Voltage	24	22.5	25	V
I_s - Current	280	175	125	mA
t_{fly} - Flyback Time	0.6	1	0.7	ms
P_{tot} - Power Dissip.	4.2	2.5	2.05	W
$R_{th\ o\text{-}a}$ - Heatsink	7	13	16	°C/W
T_{amb}	60	60	60	°C
$T_{j\ max}$	110	110	110	°C
T_o	20	20	20	ms
V_I	2.5	2.5	2.5	V_{pp}
V_7	2.5	2.5	2.5	V_p

8170-05.TBL

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the HEPTAWATT™ package attaching the heatsink is very simple, a screw a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

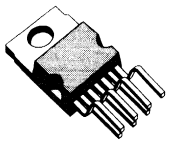
Figure 4 : Mounting Examples



8170-10.EPS

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION



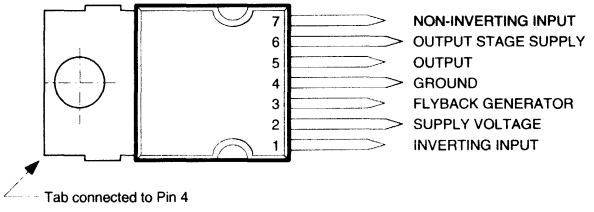
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8172

DESCRIPTION

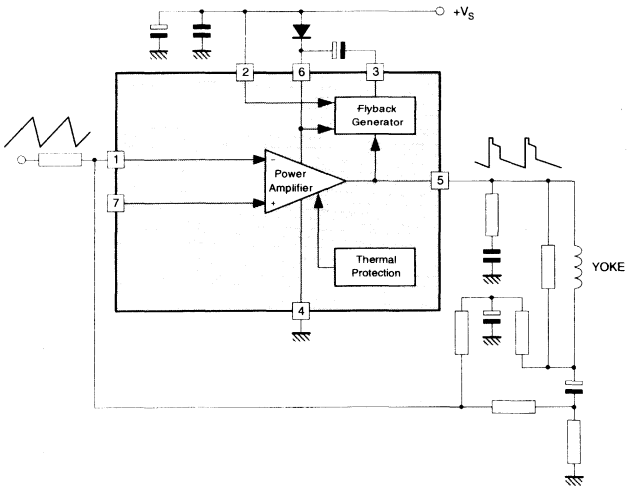
The TDA8172 is a monolithic integrated circuit in HEPTAWATT™ package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television as well as in monitors and displays.

PIN CONNECTIONS (top view)



8172-0 EPS

BLOCK DIAGRAM



8172-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+ V_s$	
V_1, V_7	Amplifier Input Voltage	$+ V_s$ $- 0.5$	V
I_o	Output Peak Current (non repetitive, t = 2 ms)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, $t \leq 10$ µs	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, $t > 10$ µs	2	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$ ms	3	A
P_{tot}	Total Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40, +150	°C

8172-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W

8172-02.TBL

ELECTRICAL CHARACTERISTICS

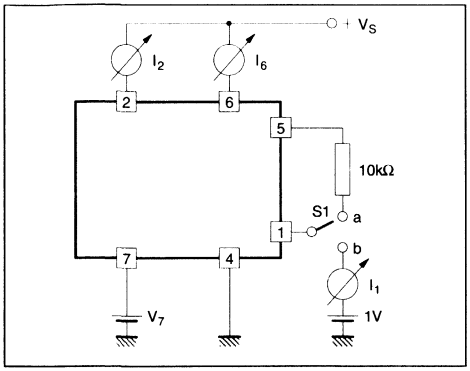
(refer to the test circuits, V_S = 35V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$, $I_5 = 0$		8	16	mA	1a
I_6	Pin 6 Quiescent Current	$I_3 = 0$, $I_5 = 0$		16	36	mA	1a
I_1	Amplifier Input Bias Current	V_1 = 1 V, V_7 = 2 V		– 0.1	– 1	µA	1a
		V_1 = 2 V, V_7 = 1 V		– 0.1	– 1	µA	1a
V_{3L}	Pin 3 Saturation Voltage to GND	I_3 = 20 mA		1	1.5	V	1c
V_5	Quiescent Output Voltage	V_s = 35V, R_a = 39 kΩ		18		V	1d
V_{5L}	Output Saturation Voltage to GND	I_5 = 1.2 A		1	1.4	V	1c
		I_5 = 0.7 A		0.7	1	V	1c
V_{5H}	Output Saturation Voltage to Supply	$- I_5$ = 1.2 A		1.6	2.2	V	1b
		$- I_5$ = 0.7 A		1.3	1.8	V	1b
T_j	Junction Temperature for Thermal Shut Down			140		°C	

8172-03.TBL

Figure 1 : DC Test Circuits.

Figure 1 a : Measurement of I_1 ; I_2 ; I_6



S_1 : (a) I_2 and I_6 ; (b) I_1

Figure 1 b : Measurement of V_{5H}

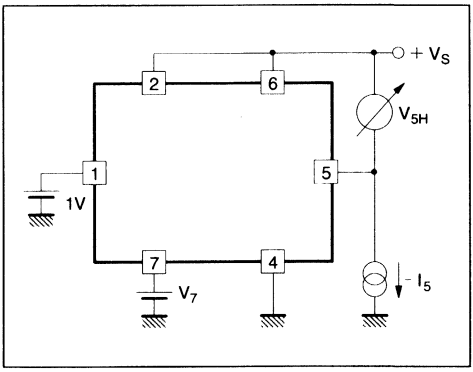
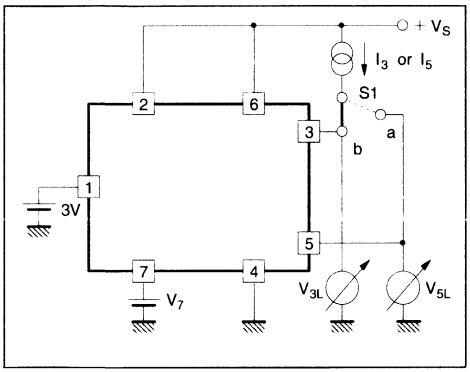


Figure 1 c : Measurement of V_{3L} ; V_{5L}



S_1 : (a) V_{3L} ; (b) V_{5L}

Figure 1 d : Measurement of V_5

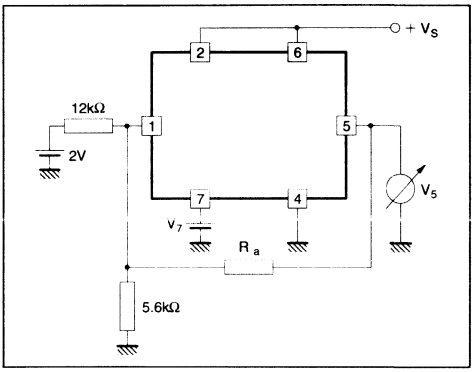
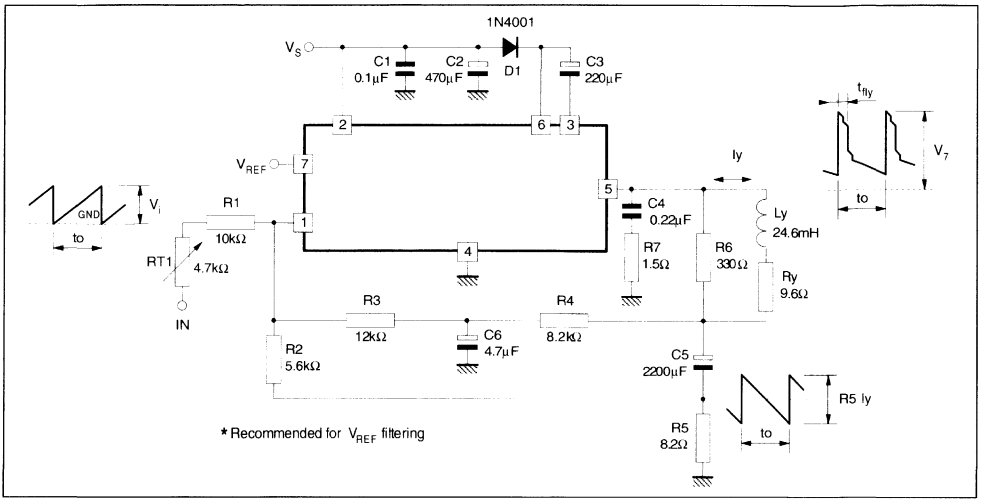


Figure 2 : AC Test Circuit



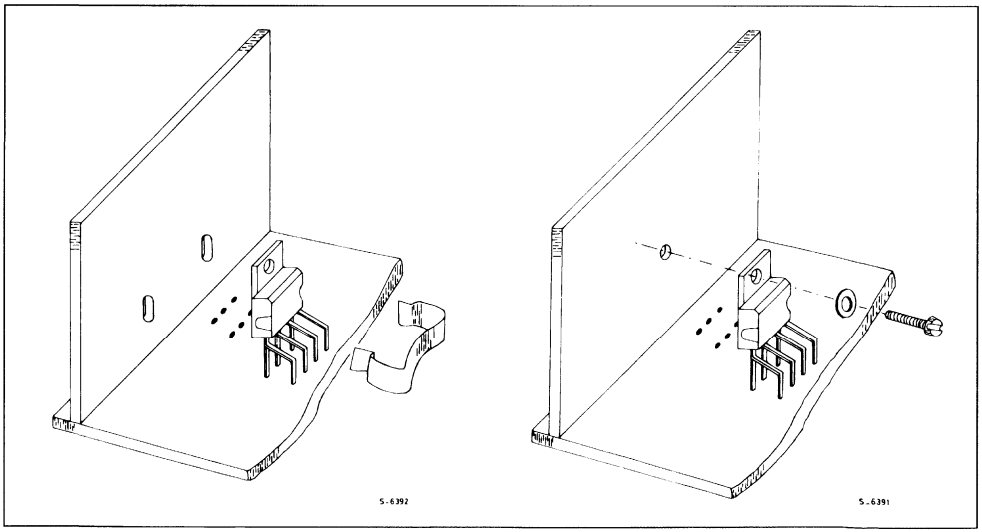
MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the HEPTAWATT™ package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient.

Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces, since the tab is connected to Pin 4 which is ground.

Figure 3 : Mounting Examples

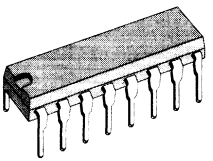


SGS-THOMSON MICROELECTRONICS

TDA8173

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION
- REFERENCE VOLTAGE



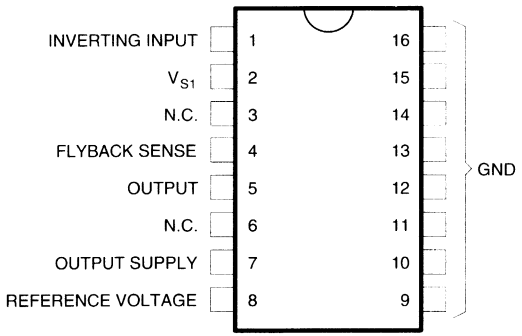
DIP16
(Plastic Package)

ORDER CODE : TDA8173

DESCRIPTION

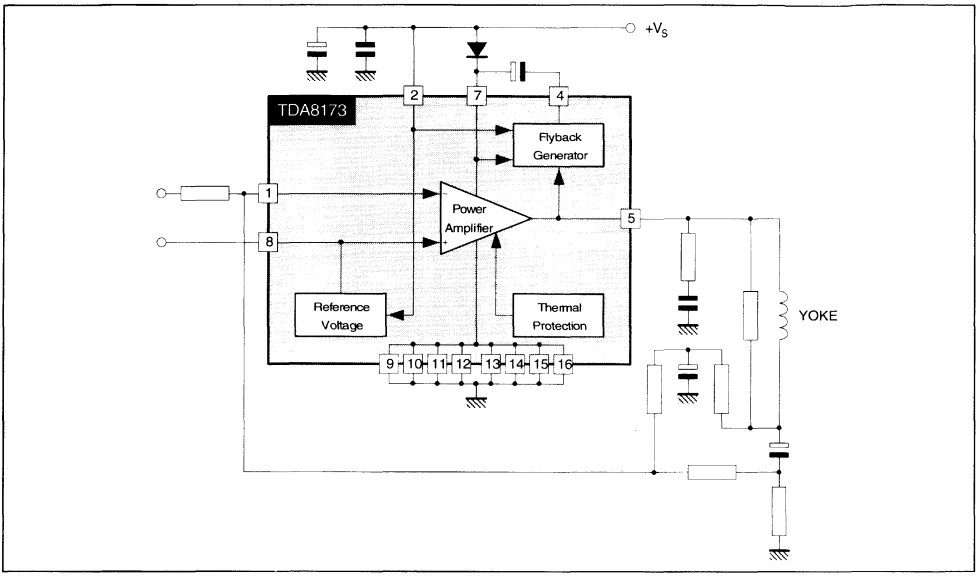
The TDA8173 is a monolithic integrated circuit in POWERDIP package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television sets as well as in monitors, and displays.

PIN CONNECTIONS (top view)



8173-01.EPS

BLOCK DIAGRAM



8173-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5	Flyback Peak Voltage	60	V
V_4	Voltage at Pin 4	+ V_s	
V_1, V_8	Amplifier Input Voltage	+ V_s − 0.5	V
I_o	Output Peak Current (non repetitive, t = 2 ms)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, t ≤ 10 µs	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µs	2	A
I_4	Pin 4 DC Current at $V_5 < V_2$	100	mA
I_4	Pin 4 Peak to Peak Flyback Current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$ ms	3	A
P_{tot}	Total Power Dissipation at T_{case} = 60 °C	6	W
T_{stg}, T_j	Storage and Junction Temperature	− 40 to 150	°C

8173-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-case	Max.	15	°C/W
$R_{th\ (j-a)}$	Thermal Resistance Junction-ambient	Max.	70	°C/W

8173-02.TBL

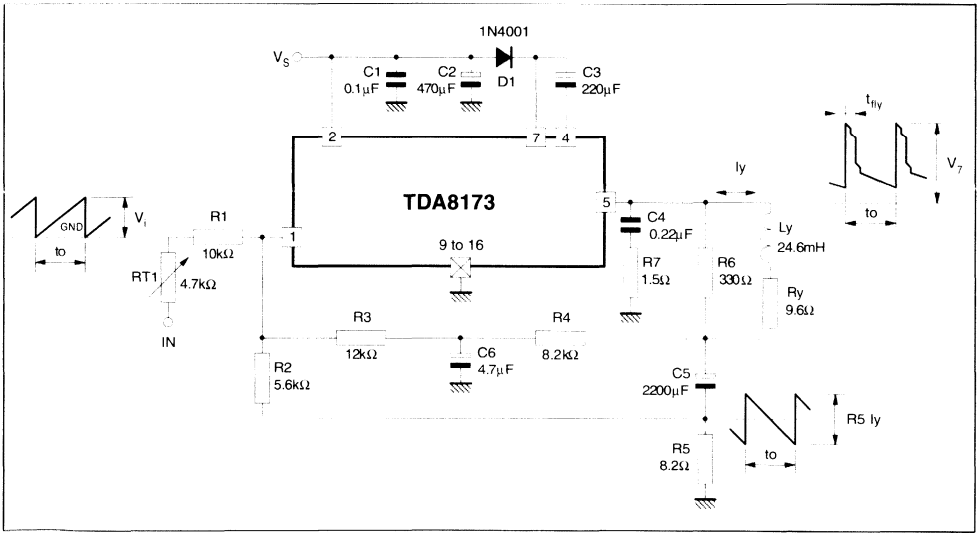
ELECTRICAL CHARACTERISTICS

(refer to the test circuits, V_S = 35V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I = 0, I_5 = 0		8	16	mA
I_7	Pin 7 Quiescent Current	I = 0, I_5 = 0		16	36	mA
I_1	Amplifier Input Bias Current	V_1 = 1 V		– 0.1	– 1	µA
V_{4L}	Pin 4 Saturation Voltage to GND	I_4 = 20 mA		1		V
V_5	Quiescent Output Voltage	V_s = 35 V, R_a = 39 kΩ		18		V
V_{5L}	Output Saturation Voltage to GND	I_5 = 1.2 A		1	1.4	V
		I_5 = 0.7 A		0.7	1	V
V_{5H}	Output Saturation Voltage to Supply	– I_5 = 1.2 A		1.6	2.2	V
		– I_5 = 0.7 A		1.3	1.8	V
T_j	Junction Temperature for Thermal Shut Down			140		°C
V_8	Reference Voltage			2.2		V
$\frac{\Delta V_8}{\Delta V_S}$	Reference Voltage Drift versus Supply Voltage	V_s = 15 to 30 V		1	2	mV

8173-03.TBL

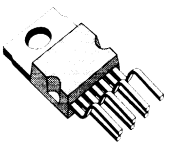
TEST CIRCUITS



8173-03.EPS

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- AUTOMATIC PUMPING COMPENSATION
- THERMAL PROTECTION
- REFERENCE VOLTAGE



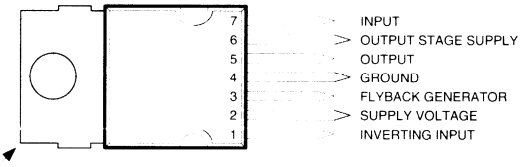
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8175

DESCRIPTION

The TDA8175 is a monolithic integrated circuit in HEPTAWATT package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television sets as well as in monitors and displays.

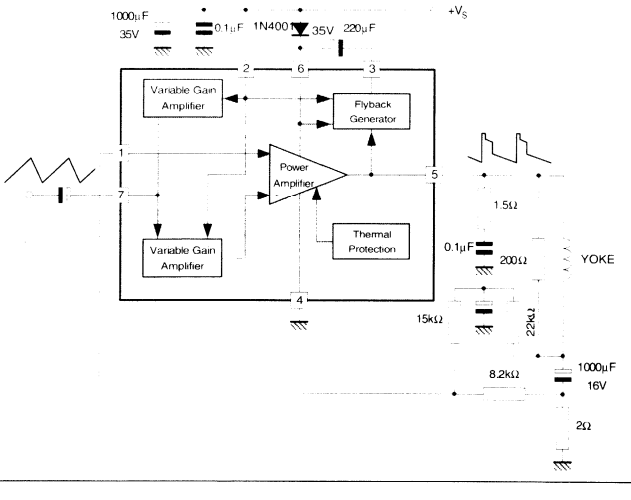
PIN CONNECTIONS



Tab connected to Pin 4

81-75-01.EPS

BLOCK DIAGRAM



81-75-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+V_S$	
V_1, V_7	Amplifier Input Voltage	$+V_S$	
I_O	Output Peak Current (non-repetitive, t = 2ms)	2.5	A
I_O	Output Peak Current at : f = 50 or 60Hz, $t \leq 10\mu s$ f = 50 or 60Hz, $t > 10\mu s$	 3 2	 A A
I_3	Pin 3 DC Current at V5 < V2	100	mA
I_3	Pin 3 Peak-to-peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq 1.5ms$	3	A
P_{tot}	Total Power Dissipation at $T_{case} = 70°C$	20	W
T_j, T_{stg}	Storage and Junction Temperature	-40, +150	°C

8175-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

8175-02.TBL

ELECTRICAL CHARACTERISTICS (V_S = 35V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current			18	36	mA
I_6	Pin 6 Quiescent Current			16	36	mA
I_1	Amplifier Input Bias Current	V_1 = 1V		-0.1	-1	µA
V_3	Pin 3 Saturation to GND	I_3 = 20mA		1	1.5	V
V_5	Quiescent Output Voltage	V_S = 35V, R_a = 39kΩ		19		V
V_5	Output Saturation Voltage to GND	I_5 = 1.2A I_5 = 0.7A		1 0.7	1.4 1	V V
V_5	Output Saturation Voltage to Supply	$-I_5$ = 1.2A $-I_5$ = 0.7A		1.6 1.3	2.2 1.8	V V
V_O	Ramp Amplitude versus Voltage Supply	22V < V_S < 30V		4		%/V
G	AC Gain	V_S = 26V	0.54	0.61	0.67	V
V_O	DC Output Voltage Accuracy			8		%
V_7	Internal Bias			2.7		V
R_7	Input Resistance			50		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

8175-03.TBL

THERMAL PROTECTION

The thermal protection circuit intervenes when the die temperatures reaches 150°C and turns-off the output power device.

PUMPING COMPENSATION

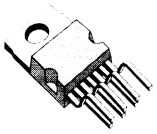
The device incorporates a special preampliflier, the gain of which varies with changes in supply voltage. This function allows perfect compensation of height variations caused by changes in brightness.

SGS-THOMSON MICROELECTRONICS

TDA8178FS

TV VERTICAL DEFLECTION BOOSTER

- POWER AMPLIFIER
- FLYBACK SUPPLY VOLTAGE SEPARATED
- THERMAL PROTECTION
- REFERENCE VOLTAGE



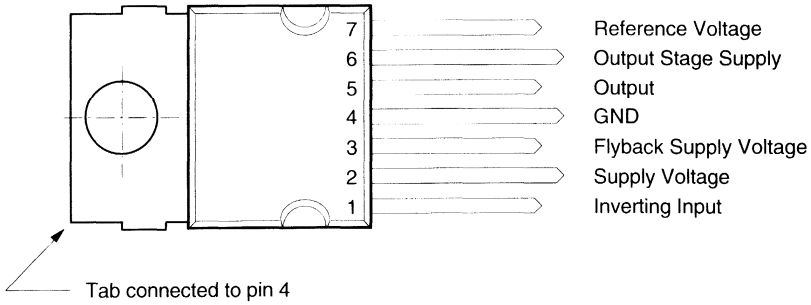
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8178FS

DESCRIPTION

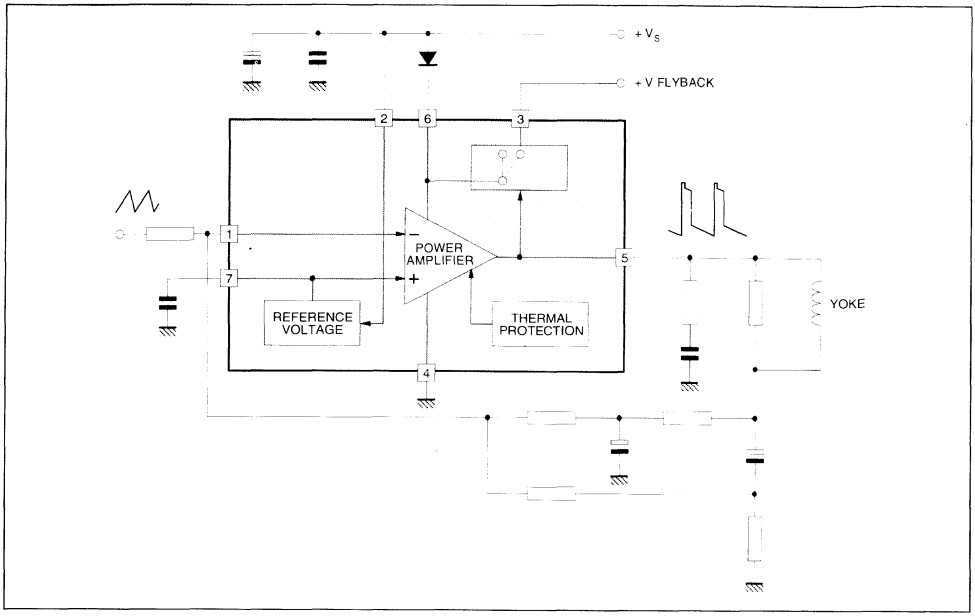
Designed for monitors and high performance TVs, the TDA8178FS vertical deflection booster is able to work with a flyback voltage more than the double of V_S.
The TDA8178FS operates with supplies up to 42V, flyback output up to 92V and provides up to 2App output current to drive to yoke.
The TDA8178FS is offered in HEPTAWATT package.

PIN CONNECTIONS

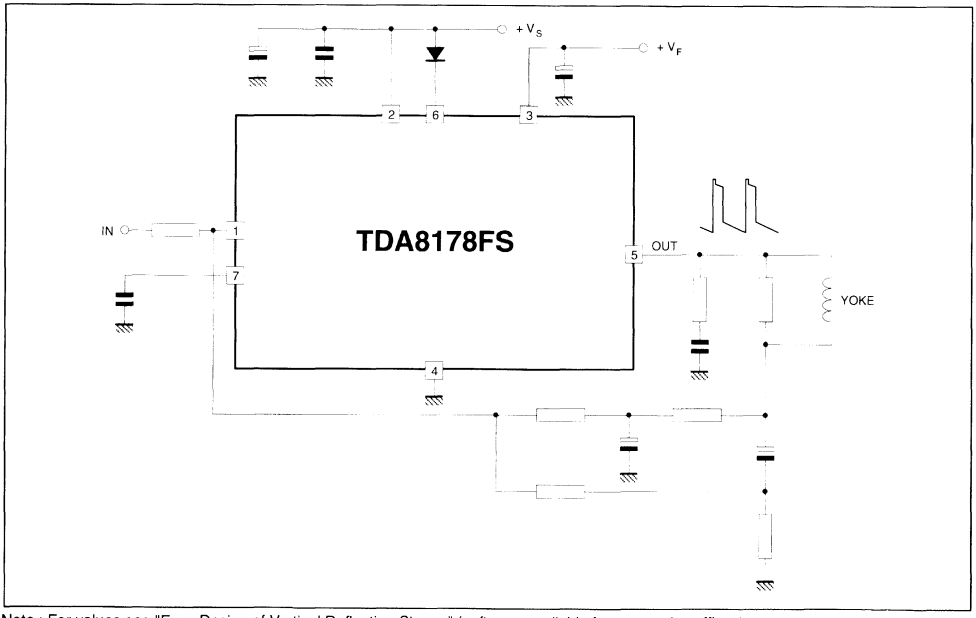


8178F-01.EPS

BLOCK DIAGRAM



APPLICATION CIRCUIT



Note : For values see "Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	50	V
V_F	Flyback Supply Voltage	100	V
$V_F - V_S$	Difference between Flyback Supply Voltage and Supply Voltage	50	V
V_1 , V_7	Amplifier Input Voltage	+ V_S	
I_O	Output Peak Current Non-repetitive, t = 2ms f = 50 or 60Hz, t ≤ 10µs f = 50 or 60Hz, t > 10µs	 2 2 1.8	A
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq 1.5$ms	1.8	A
P_{tot}	Total Power Dissipation at $T_C = 70°C$	20	W
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	0, +150	°C

8178F-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

8178F-02.TBL

ELECTRICAL CHARACTERISTICS

(V_S = 42V, T_A = 25°C, unless otherwise specified)(refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	$I_3 = 0$ $I_5 = 0$		10	20	mA
I_6	Pin 6 Quiescent Current	$I_3 = 0$ $I_5 = 0$		20	40	mA
I_1	Amplifier Bias Current	$V_1 = 1V$		- 0.2	- 1	µA
V_5	Quiescent Output Voltage	 $V_S = 42V$ $R_a = 3.9k\Omega$ $V_S = 35V$ $R_a = 5.6k\Omega$	 23.4 17	 24.2 17.8	 25 18.5	V
V_{5L}	Output Saturation Voltage to GND	$I_5 = 1A$		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	$- I_5 = 1A$		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	$I_D = 1A$		1.5	3	V
V_{D3-6}	Diode Forward Voltage between Pins 3-6	$I_D = 1A$		1.5	3	V
V_7	Internal Reference		2.1	2.2	2.3	V
$\Delta V_7/\Delta V_S$	Reference Voltage Drift versus V_S	V_S = 24 to 42V		2	4	mV/V
K_T	Reference Voltage Drift versus T_j	T_j = 0 to 125°C $K_T = \frac{\Delta V_7 \cdot 10^6}{\Delta T_j \cdot V_7}$		100	150	ppm/°C
R_1	Input Resistance			200		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

8178F-03.TBL

FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1,I_2,I_6,V_7, $\Delta V_7/\Delta V_S$

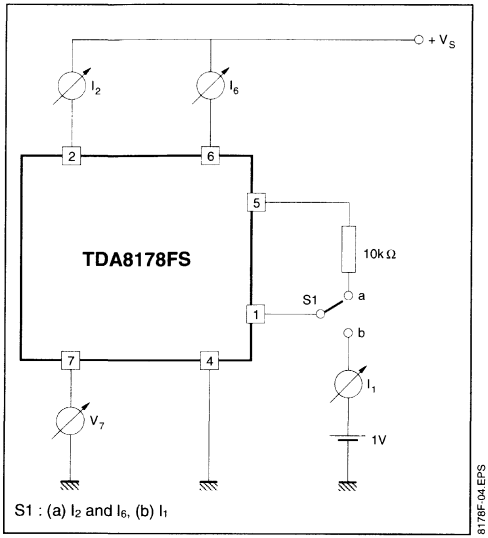


Figure 1b : Measurement of V_{5H}

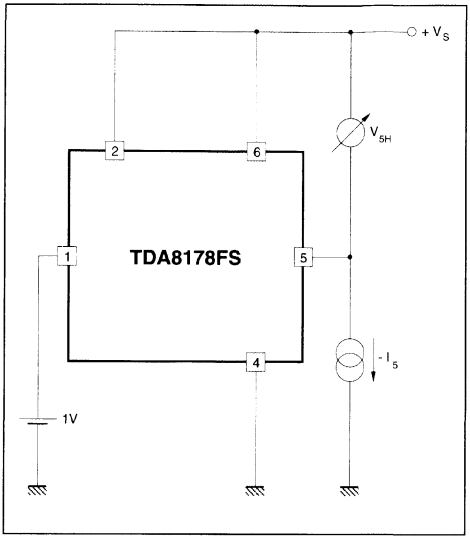


Figure 1c : Measurement of V_{5L}

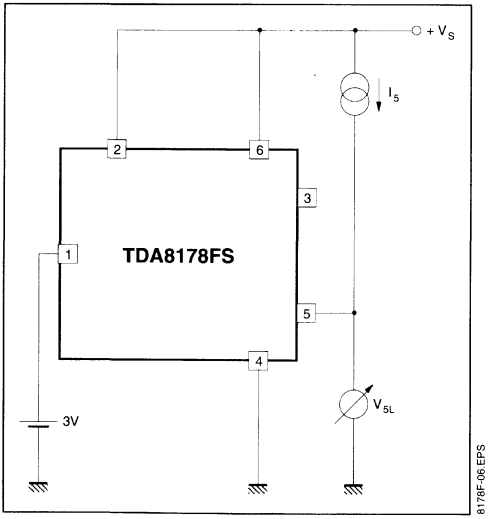


Figure 1d : Measurement of V_5

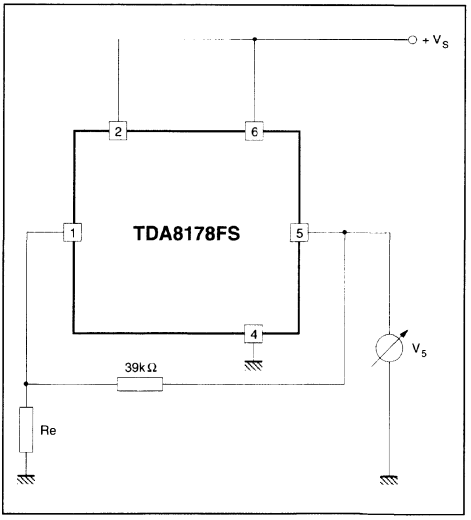
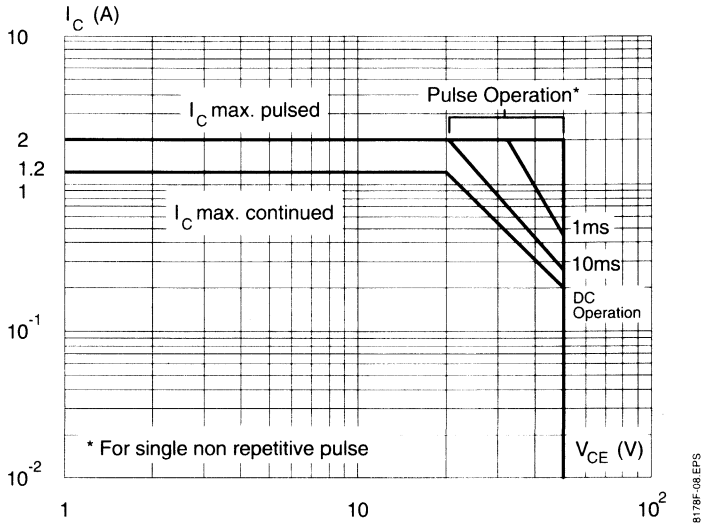


Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^oC$

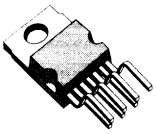


SGS-THOMSON MICROELECTRONICS

TDA8178S

TV VERTICAL DEFLECTION BOOSTER

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION
- REFERENCE VOLTAGE



HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8178S

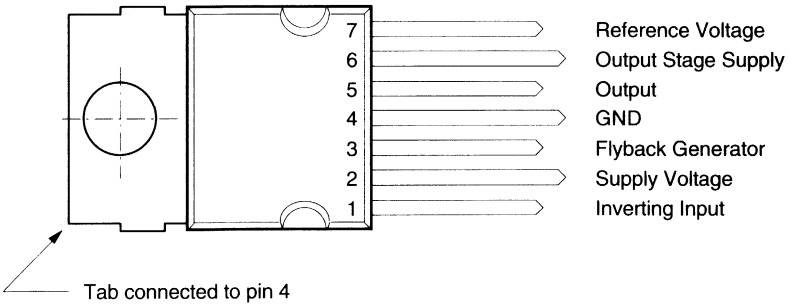
DESCRIPTION

Designed for monitors and high performance TVs, the TDA8178S vertical deflection booster delivers flyback voltages up to 90V.

The TDA8178S operates with supplies up to 42V and provides up to 2App output current to drive to yoke.

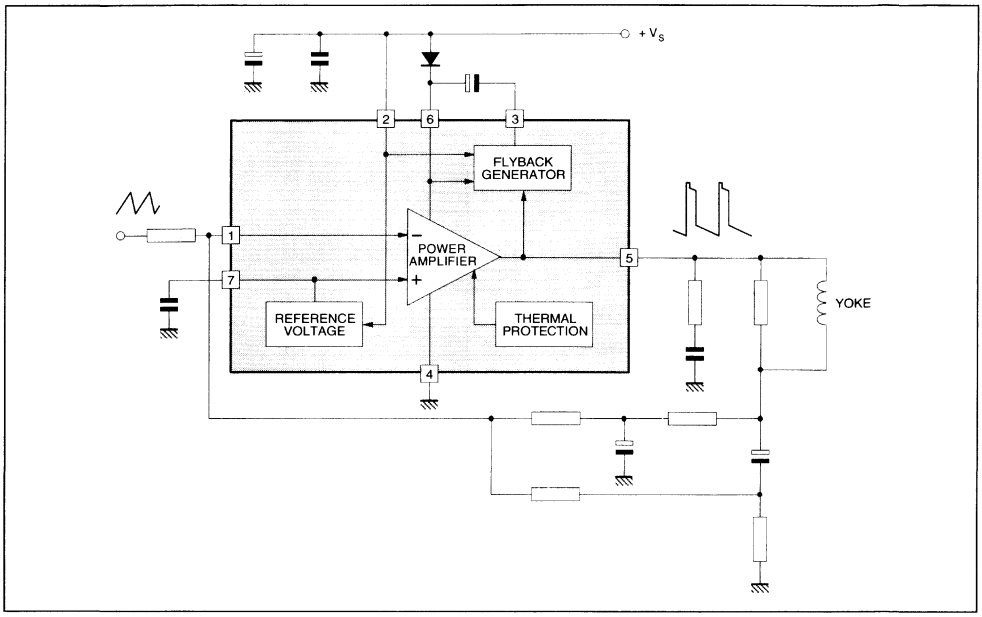
The TDA8178S is offered in HEPTAWATT package

PIN CONNECTIONS

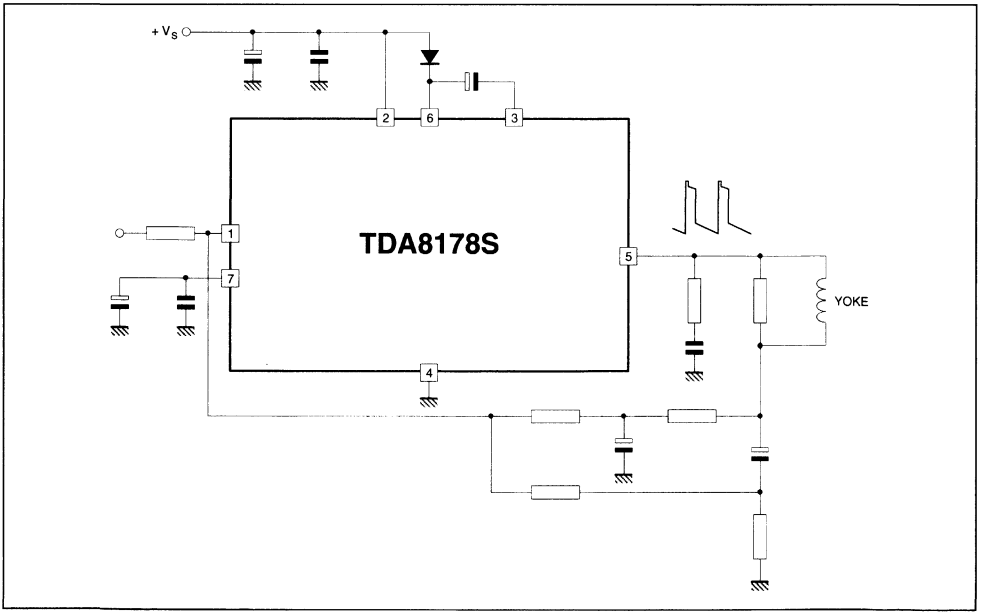


8178S-01.EPS

BLOCK DIAGRAM



APPLICATION CIRCUIT (V_S = 42V)



Note : For values see "Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	50	V
V_5 , V_6	Flyback Peak Voltage	100	V
V_1 , V_7	Amplifier Input Voltage	+ V_S	
I_O	Output Peak Current Non-repetitive, t = 2ms f = 50 or 60Hz, t ≤ 10µs f = 50 or 60Hz, t > 10µs	 2 2 1.8	A
I_3	Pin 3 DC at $V_5 < V_2$ Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq 1.5$ms	100 1.8	mA A
P_{tot}	Total Power Dissipation at $T_C = 70°C$	20	W
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	0, +150	°C

8178S-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

8178S-02 TBL

ELECTRICAL CHARACTERISTICS

(V_S = 42V, $T_A = 25°C$, unless otherwise specified) (refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	$I_3 = 0$ $I_5 = 0$		10	20	mA
I_6	Pin 6 Quiescent Current	$I_3 = 0$ $I_5 = 0$		20	40	mA
I_1	Amplifier Bias Current	$V_1 = 1V$		0.2	1	µA
V_{3L}	Pin 3 Saturation to GND	$I_3 = 20mA$		1.3	1.8	V
V_5	Quiescent Output Voltage	 $V_S = 42V$ $R_a = 3.9k\Omega$ $V_S = 35V$ $R_a = 5.6k\Omega$	 23.4 17	 24.2 17.8	 25 18.5	V
V_{5L}	Output Saturation Voltage to GND	$I_5 = 1A$		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	$-I_5 = 1A$		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	$I_D = 1A$		1.5	3	V
V_{D3-2}	Diode Forward Voltage between Pins 3-2	$I_D = 1A$		1.5	3	V
V_7	Internal Reference		2.1	2.2	2.3	V
$\Delta V_7/\Delta V_S$	Reference Voltage Drift versus V_S	V_S = 24 to 42V		2	4	mV/V
K_T	Reference Voltage Drift versus T_j	T_j = 0 to 125°C $K_T = \frac{\Delta V_7 \cdot 10^6}{\Delta T_j \cdot V_7}$		100	150	ppm/°C
R_1	Input Resistance			200		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

8178S-03 TBL

FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1, I_2, I_6, V_7, $\Delta V_7/\Delta V_S$

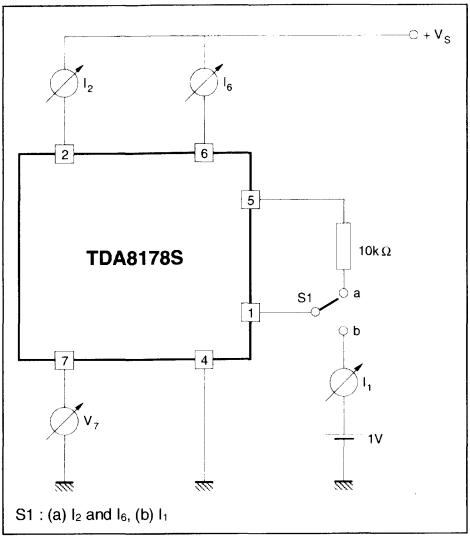


Figure 1b : Measurement of V_{5H}

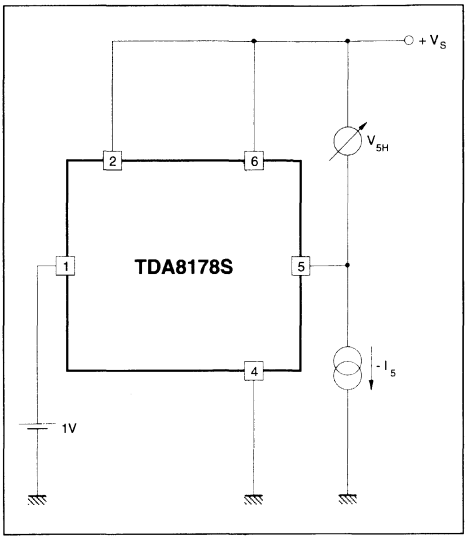


Figure 1c : Measurement of V_{3L}, V_{5L}

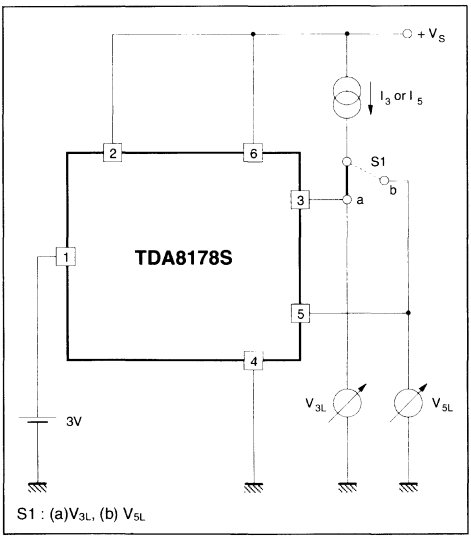


Figure 1d : Measurement of V_5

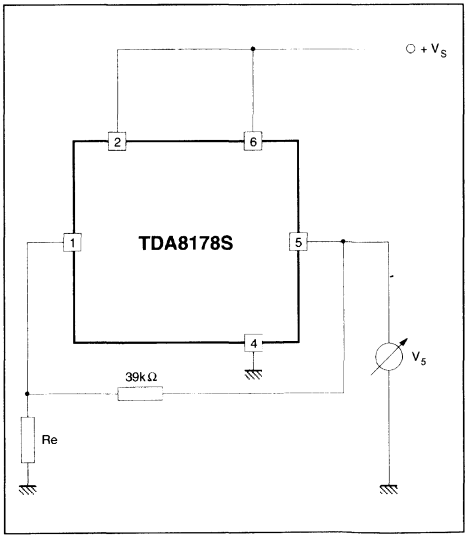
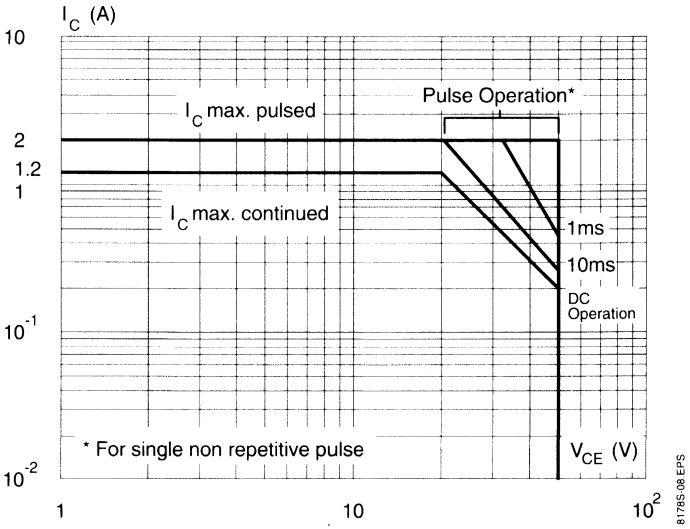


Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^oC$

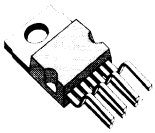


SGS-THOMSON MICROELECTRONICS

TDA8179FS

TV VERTICAL DEFLECTION BOOSTER

- POWER AMPLIFIER
- FLYBACK SUPPLY VOLTAGE SEPARATED
- THERMAL PROTECTION



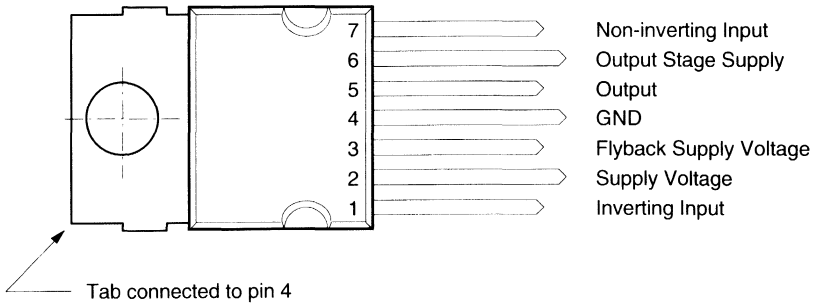
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8179FS

DESCRIPTION

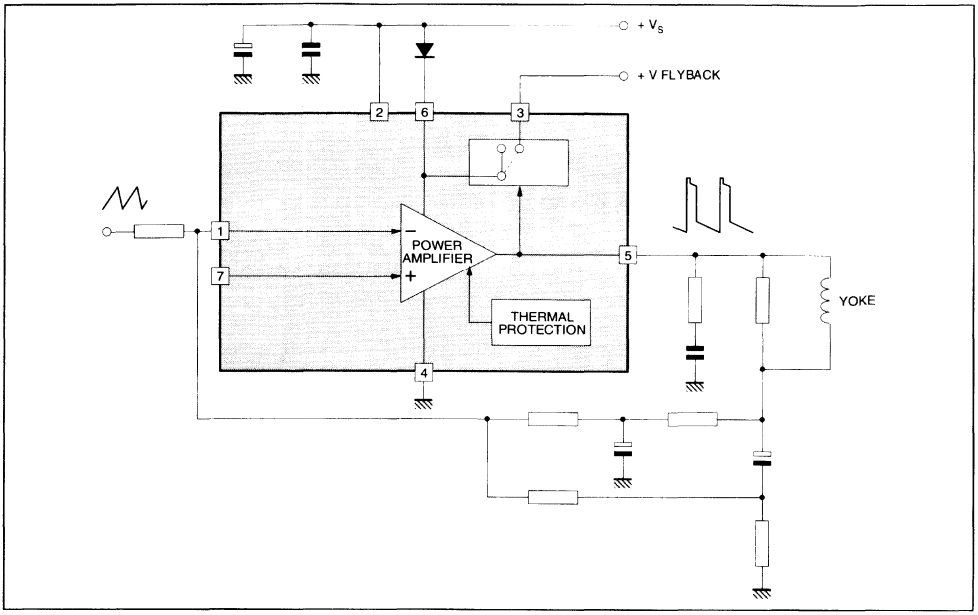
Designed for monitors and high performance TVs, the TDA8179FS vertical deflection booster is able to work with a flyback voltage more than the double of V_S.
The TDA8179FS operates with supplies up to 42V, flyback output up to 92V and provides up to 2App output current to drive to yoke.
The TDA8179FS is offered in HEPTAWATT package.

PIN CONNECTIONS

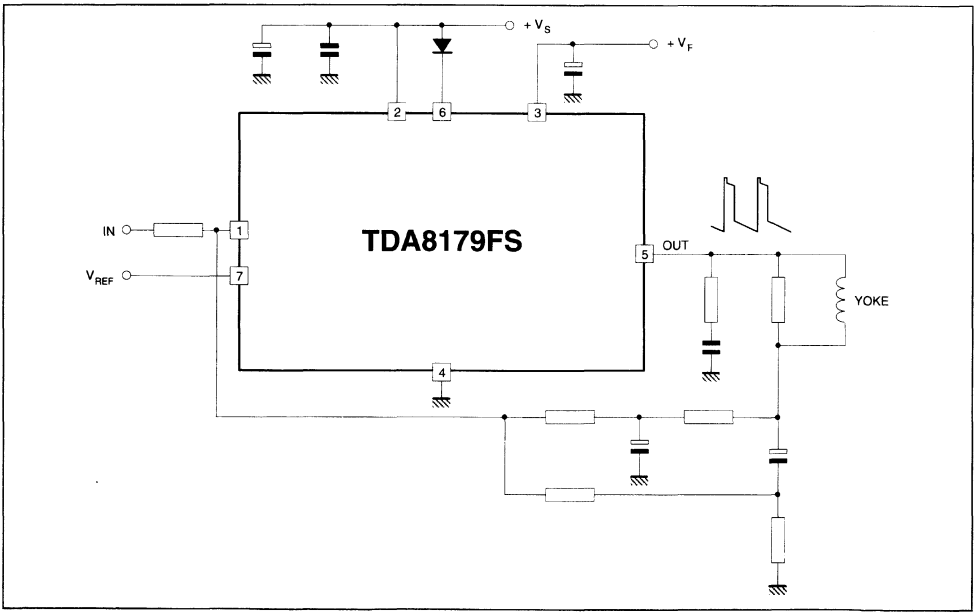


8179F-01.EPS

BLOCK DIAGRAM



APPLICATION CIRCUIT



Note : For values see " Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	50	V
V_F	Flyback Supply Voltage	100	V
$V_F - V_S$	Difference between Flyback Supply Voltage and Supply Voltage	50	V
V_1 , V_7	Amplifier Input Voltage	+ V_S	
I_O	Output Peak Current Non-repetitive, t = 2ms f = 50 or 60Hz, t ≤ 10µs f = 50 or 60Hz, t > 10µs	 2 2 1.8	A
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, t_{fly} ≤ 1.5ms	1.8	A
P_{tot}	Total Power Dissipation at T_C = 70°C	20	W
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	0, +150	°C

8179F-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

8179F-02.TBL

ELECTRICAL CHARACTERISTICS

(V_7 = 2.2V, V_S = 42V, T_A = 25°C, unless otherwise specified)
(refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	I_3 = 0 I_5 = 0		10	20	mA
I_6	Pin 6 Quiescent Current	I_3 = 0 I_5 = 0		20	40	mA
I_1	Amplifier Bias Current	V_1 = 1V		- 0.2	- 1	µA
V_5	Quiescent Output Voltage	 V_S = 42V R_a = 3.9kΩ V_S = 35V R_a = 5.6kΩ	 23.4 17	 24.2 17.8	 25 18.5	V
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	- I_5 = 1A		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_D = 1A		1.5	3	V
V_{D3-6}	Diode Forward Voltage between Pins 3-6	I_D = 1A		1.5	3	V
R_1	Input Resistance			200		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

8179F-03.TBL

FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1, I_2, I_6

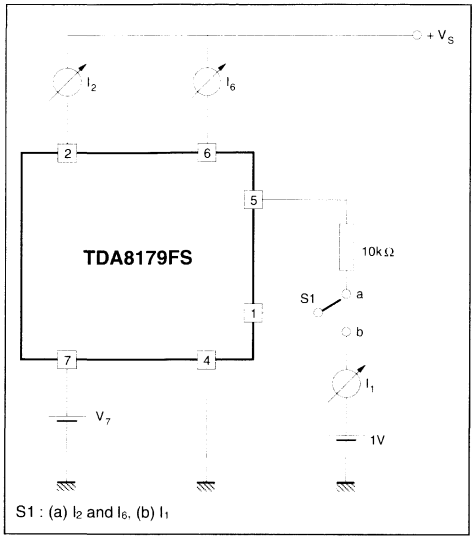


Figure 1b : Measurement of V_{5H}

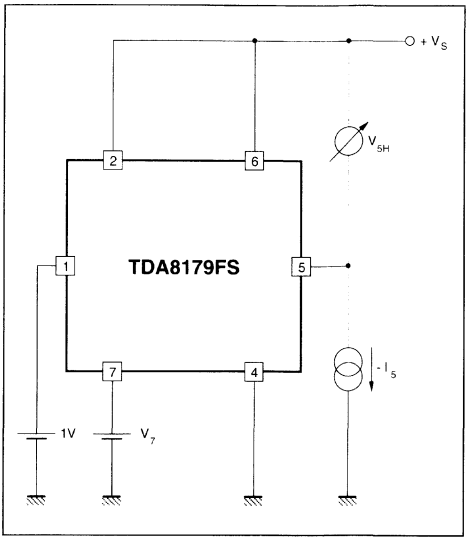


Figure 1c : Measurement of V_{5L}

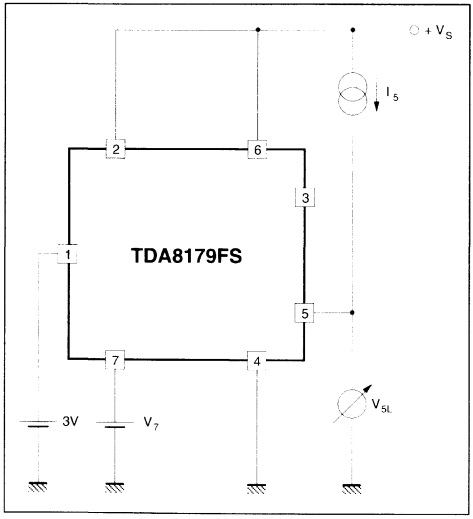


Figure 1d : Measurement of V_5

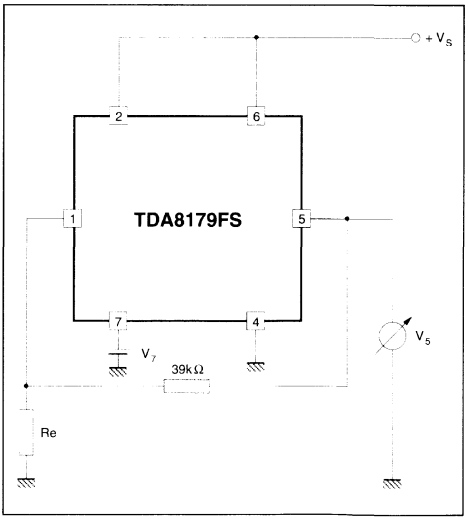
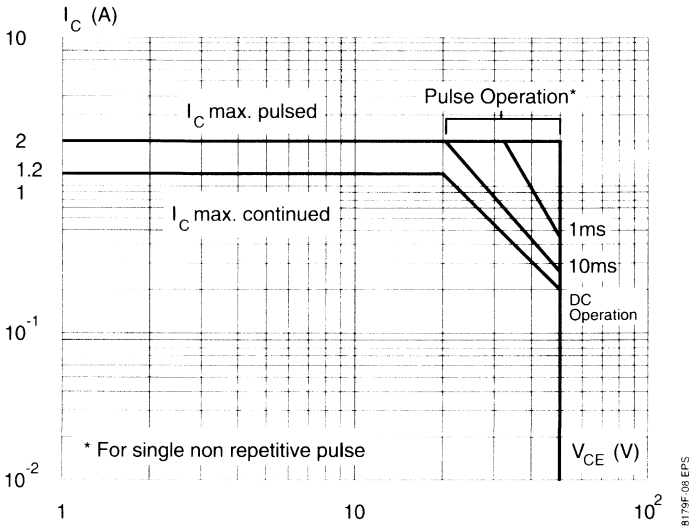


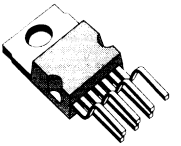
Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^oC$



TDA9302H

VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION



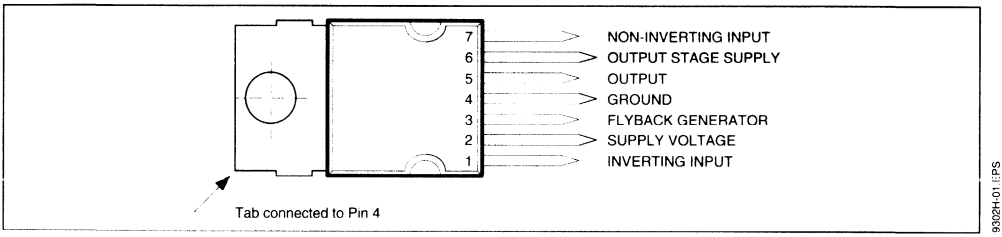
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA9302H

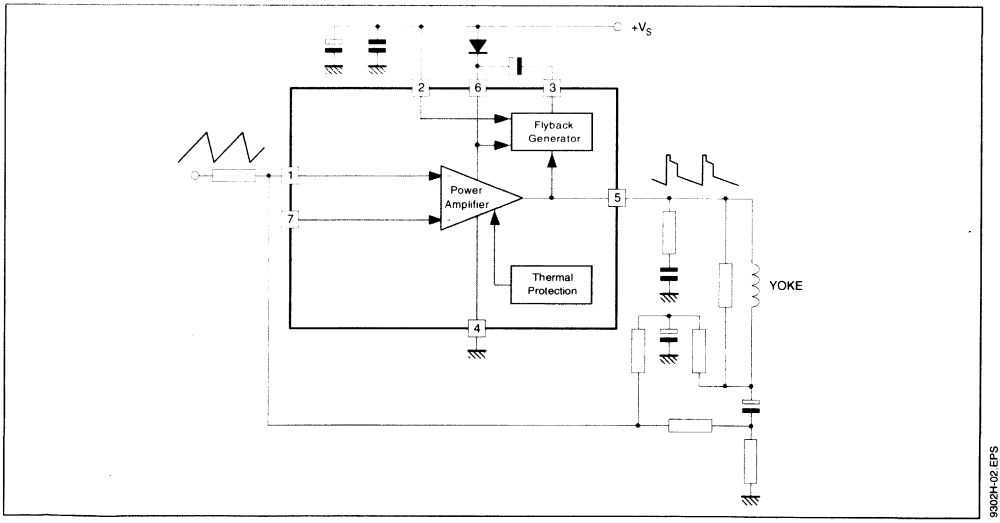
DESCRIPTION

The TDA9302H is a monolithic integrated circuit in HEPTAWATT™ package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television as well as in monitors and displays.

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS AT $T_A = 25^oC$

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+ V_s$	
V_1, V_7	Amplifier Input Voltage	$+ V_s$ $- 0.5$	V
I_o	Deflection Output Current	$\pm$ 1.8	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
P_{tot}	Total Power Dissipation at T_{case} = 90 °C	15	W
T_{stg}, T_j	Storage and Junction Temperature	– 40, +150	°C

9302H-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-case	Max.	4	°C/W

9302H-02.TBL

RECOMMENDED OPERATING CHARACTERISTICS AT $T_A = 25^oC$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{2M}	Recommended Supply Voltage			25		V
V_{2R}	Operating Supply Voltage Range		15		30	V
I_{5PP}	Deflection Output Current				2	App

9302H-03.TBL

ELECTRICAL CHARACTERISTICS

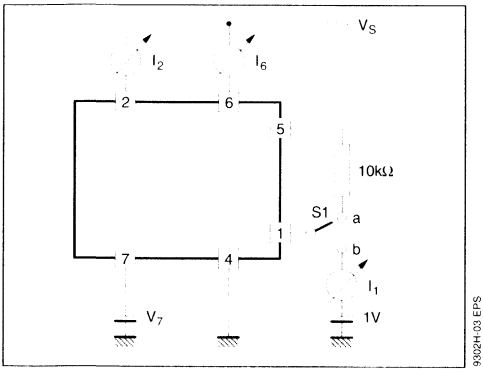
(refer to the test circuits, V_S = 35V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$, $I_5 = 0$			16	mA	1a
I_6	Pin 6 Quiescent Current	$I_3 = 0$, $I_5 = 0$			36	mA	1a
I_1	Amplifier Input Bias Current	V_1 = 1 V, V_7 = 2 V		– 0.1	– 1	µA	1a
		V_1 = 2 V, V_7 = 1 V		– 0.1	– 1	µA	1a
V_{3L}	Pin 3 Saturation Voltage to GND	I_3 = 20 mA		1	1.5	V	1c
V_5	Quiescent Output Voltage	V_s = 35V, R_a = 39 kΩ		18		V	1d
V_{5L}	Output Saturation Voltage to GND	I_5 = 1 A		0.9	1.3	V	1c
		I_5 = 0.7 A		0.7	1	V	1c
V_{5H}	Output Saturation Voltage to Supply	$- I_5$ = 1 A		1.5	2	V	1b
		$- I_5$ = 0.7 A		1.3	1.8	V	1b
T_j	Junction Temperature for Thermal Shut Down			140		°C	

9302H-04.TBL

Figure 1 : DC Test Circuits.

Figure 1 a : Measurement of I_1 ; I_2 ; I_6



S_1 : (a) I_2 and I_6 ; (b) I_1

Figure 1 b : Measurement of V_{5H}

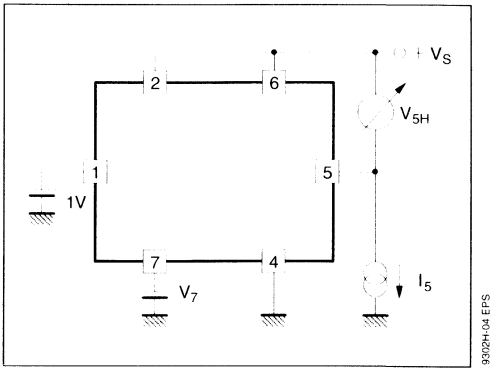
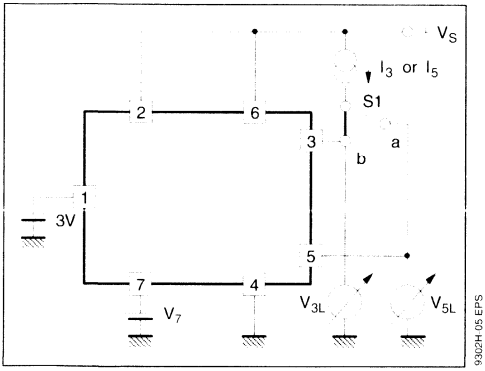


Figure 1 c : Measurement of V_{3L} ; V_{5L}



S_1 : (a) V_{3L} ; (b) V_{5L}

Figure 1 d : Measurement of V_5

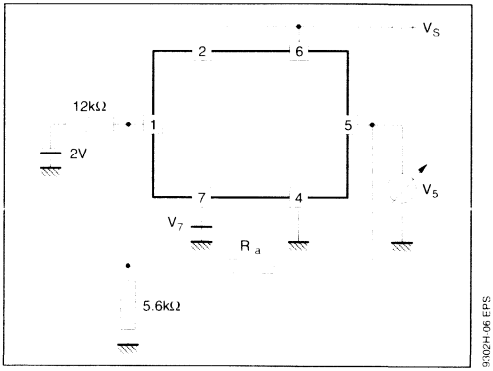
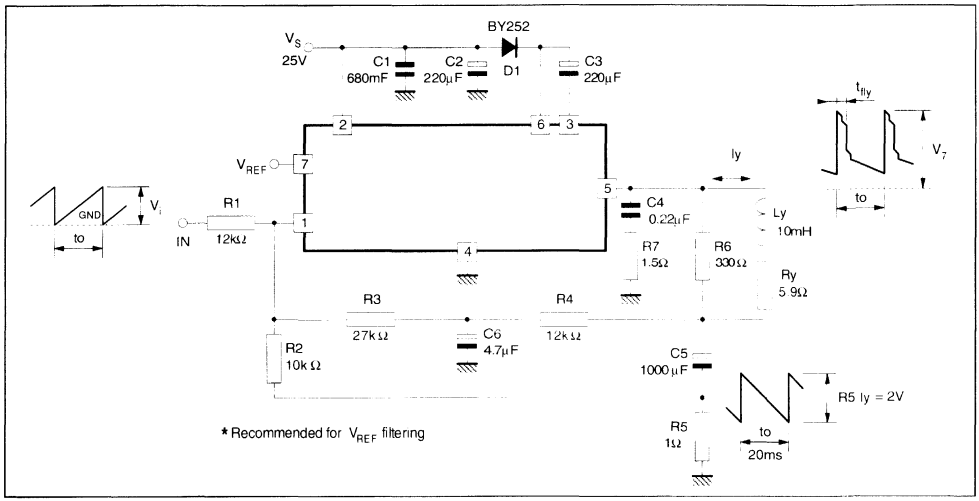


Figure 2 : AC Test Circuit

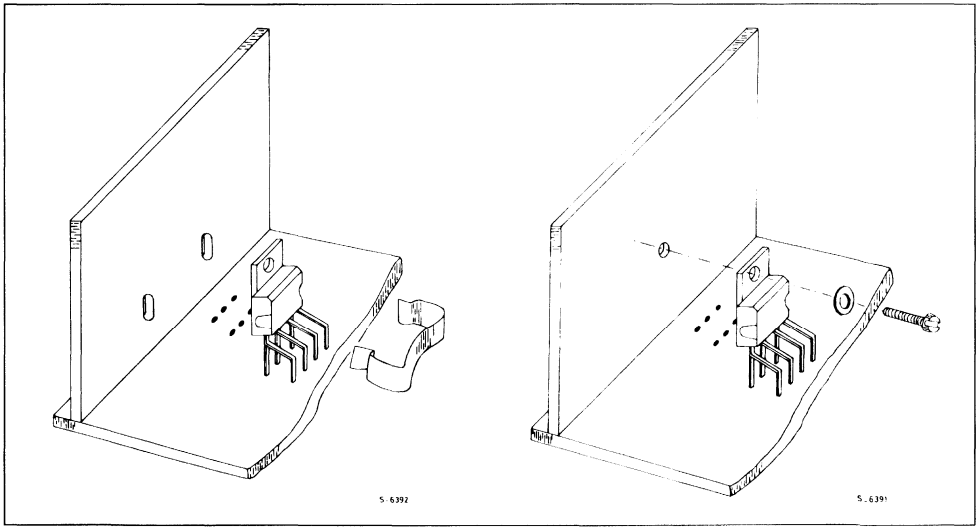


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the HEPTAWATT™ package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient.

Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces, since the tab is connected to Pin 4 which is ground.

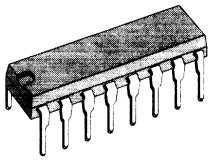
Figure 3 : Mounting Examples



HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH THE OUTPUT ON

The current source characteristic of this device is adapted to the on-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA8140 is internally protected against short circuit and thermal overload.



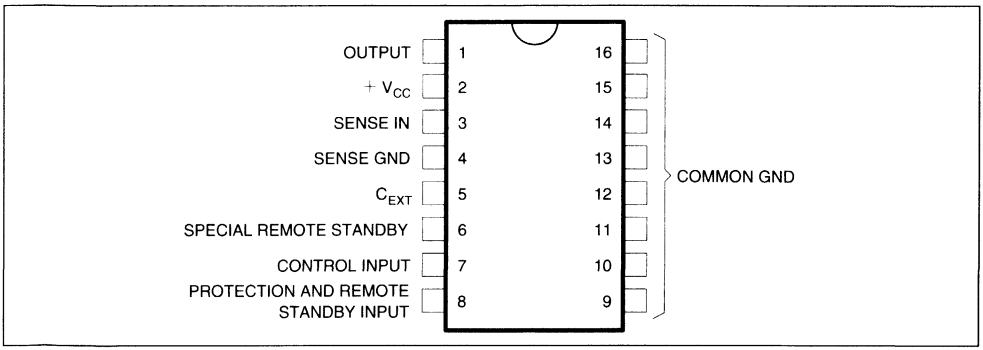
POWERDIP (8 + 8)
(Plastic Package)

ORDER CODE : TDA8140

DESCRIPTION

The TDA 8140 is a monolithic integrated circuit designed to drive the horizontal deflection power transistor.

PIN CONNECTIONS

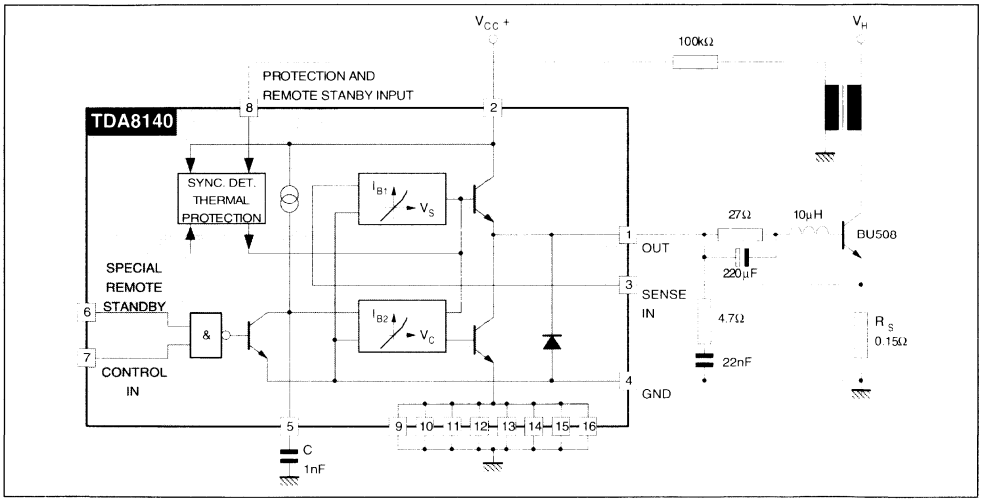


PIN FUNCTION

Pin	Name	Function
1	Output	Device Output
2	V_{CC}	Supply Voltage
3	Sense Input	Input voltage that determines output current.
4	Sense GND	Reference Ground for Input Voltage at Sense Input
5	C_{EXT}	Capacitor between this terminal and Sense Ground determines the current slope dI_o/d_t during off phase.
6	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from control input (2nd priority) (in standard applications pin 6 must be left unconnected).
7	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
8	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).
9-16	Power Ground	Common Ground

8140-01.TBL

BLOCK DIAGRAM



8140-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40, + 150	°C
T_{oper}	Operating Temperature	0, + 70	°C

8140-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	15	°C/W

8140-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{p0}	Positive Output Current (source)		1.5			A
I_{n0}	Negative Output Current (sink)		2			A
I_{o0}	Positive quiescent output current forcing the output to 6 V and the sense input to ground, output externally forced to 6V	Remote Input 1 Remote Input 0	120 50	150 80	200 100	mA mA
G_{ON}	Transconductance ON Phase (1)	See Figure 1	1.8	2.0	2.2	A/V
G_{OFF}	Transconductance OFF Phase (2)	See Figure 1	1.8	2.0	2.2	A/V
G_{REMOTE}	Transconductance Standby Mode	Remote Input 0	0.675	0.75	0.825	A/V
I_5	Current Source Pin 5	V_6 = 500mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	V_S = 0, Remote Input 1	– 200	– 300	– 400	µA
R_{SYN}	Synchronous Detection Input Resistance	$V_{SYN} < 7V$ $V_{SYN} > 7V$	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	Sync Detect Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA} + 0.5V$	– 50 - 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V
I_{INB}	Pull up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB} + 0.5V$	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time (3)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
V_{CC}–V_{OUT}	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_O \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage (4)		0.8	0.9	1	V

8140-04.TBL

Notes : 1. G_{ON} is measured with V_3 varying from 150mV to 350mV (Pin 5 is grounded)
2. G_{OFF} is measured with V_5 varying from 150mV to 350mV (Pin 3 is grounded)
3. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
4. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_O is going to the positive quiescent current I_{O0}.

TRUTH TABLE

Logic Inputs		Output I_o		Mode
Control Input	Remote/Standby			
0	Floating or 1	$I_o > 0$	BU508 ON	Normal Function
Floating or 1	Floating or 1	$I_o < 0$ (5)	BU508 OFF	
X	0	$I_o < 0$ (5) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_o > 0$ $t > td_r$	BU508 ON	

8140-05.TBL

Note : 5. $I_O < 0$ means that the sink current flows into the output to ground.

Figure 1 : $\frac{G_{ON}}{V_{Pin3}}$ and $\frac{|G_{OFF}|}{V_{Pin5}}$

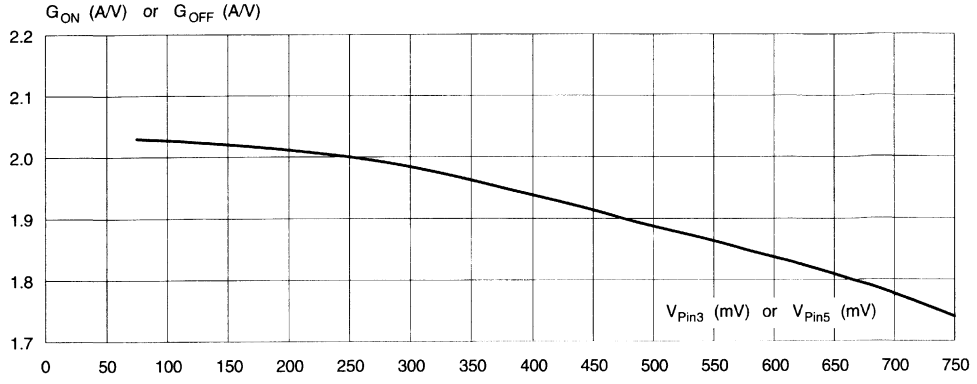


Figure 2 : Large Screen Application

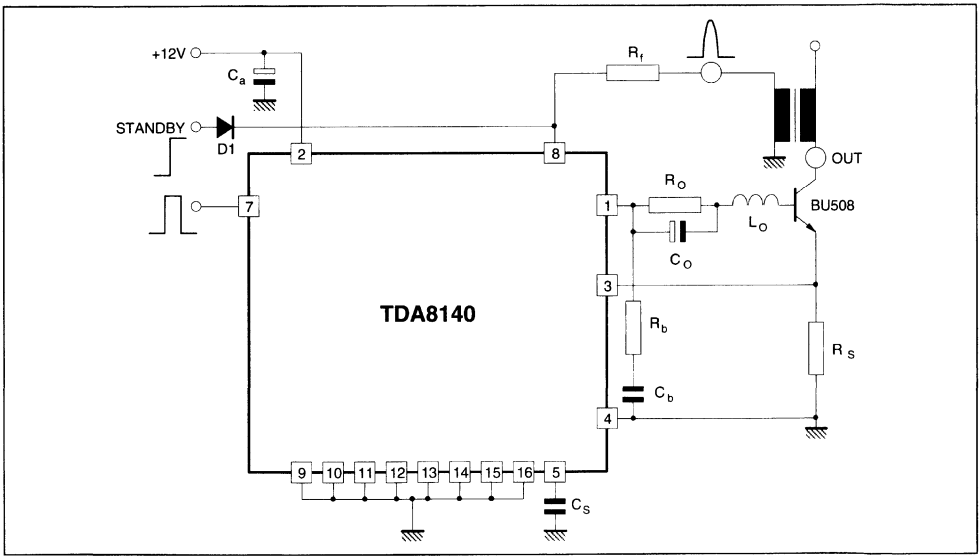
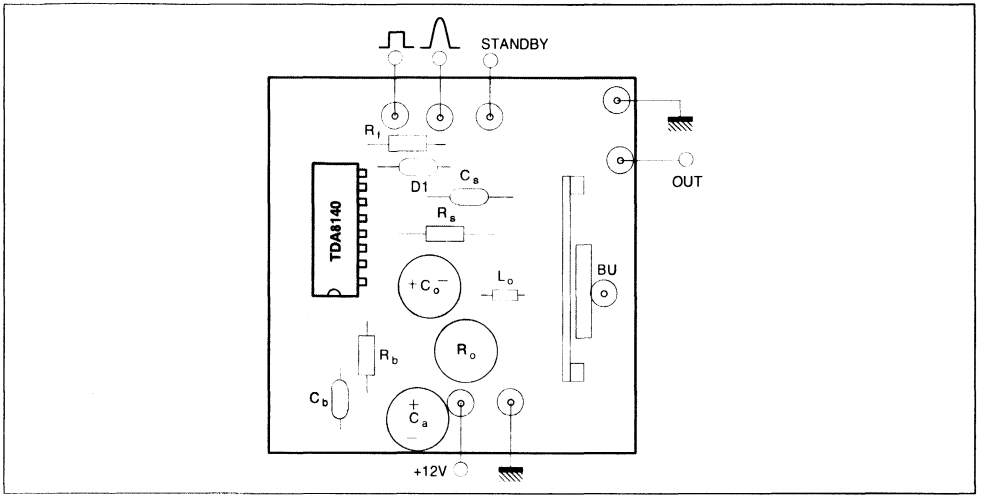


Figure 3 : P.C. Board and Components Layout of the Figure 2 (1 : 1 scale)



8140-05.EPS

COMPONENTS LIST FOR TYPICAL APPLICATION

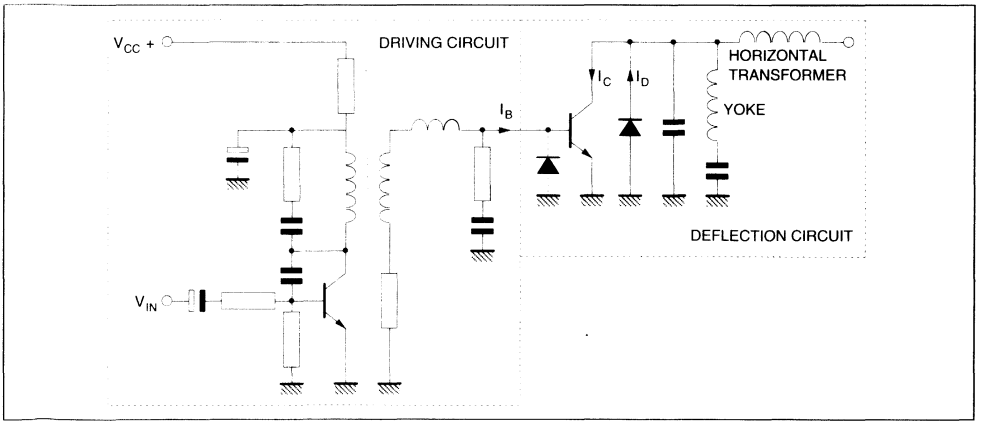
CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 µF	47 µF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 µF	220 µF	R_s	0.15 Ω	0.1 Ω
L_o	10 µH	10 µH	C_s	1 nF	1 nF

8140-06.TBL

APPLICATION INFORMATION

The conventional deflection system is shown in Figure 4. The driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

Figure 4 : Conventional Horizontal Deflection System for TVs



8140-06.EPS

During the active deflection phase the collector current of the power transistor is linearly rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.
According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in Figure 5 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.
The marked area represents a useless base current which gives an additional power dissipation on the power transistor.
Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the conventional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.
The new approach, using the TDA 8140, overcomes these restrictions by means of a feedback principle.
As shown in Figure 5, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_S at the emitter of the power transistor and delivers :

$$I_b = R_S \cdot g_m \cdot I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1+\beta min} \cdot \frac{1}{R_S} < gm < \frac{1}{R_S}$$

Where β_{min} is the minimum current gain of the transistor. This method always ensures the correct base current and acts time independent on principle.
For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in Figure 6.
Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.
This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.
As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 5 : Waveforms of Collector and Base Current

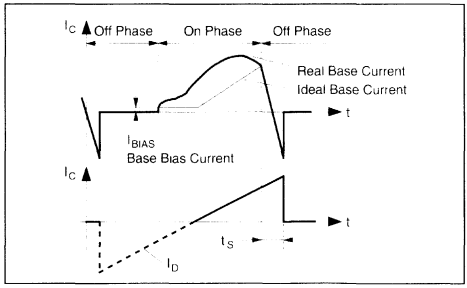
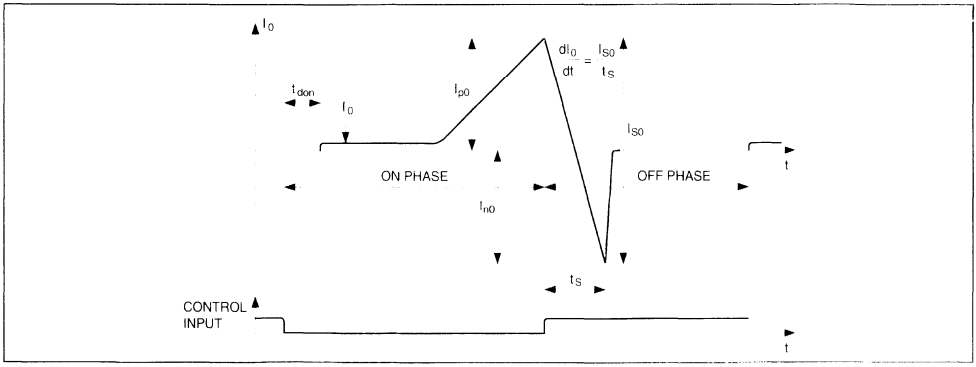


Figure 6



CIRCUIT DESCRIPTION

Figure 7 shows the block diagram of the TDA8140, the circuit consists of an input transconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2A sink current and 2A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \cdot \frac{1}{R5}$$

A current source I_1 generates a drop of 70mV across the resistor R4 which provides an output bias current of 140mA ; the control input determines the turn ON/OFF function.

In the ON phase, Q5 shorts the external capacitor C_t. Within the input voltage range $0 < V_{in} < 750mV$ the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750mV, Q7 limits the maximum output current at 1.5A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linearly and the system stability is reached.

During the flyback phase, the IC is disabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

In Figure 8 is shown the application diagram of the TDA 8140, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in Figure 4.

In Figure 9 is shown the currents and voltages waveforms of the driver circuit of Figure 8, as to be seen, the driving charge Ib · t_{on} has been reduced at minimum.

Figure 7 : Block Diagram of the Integrated Horizontal Driver

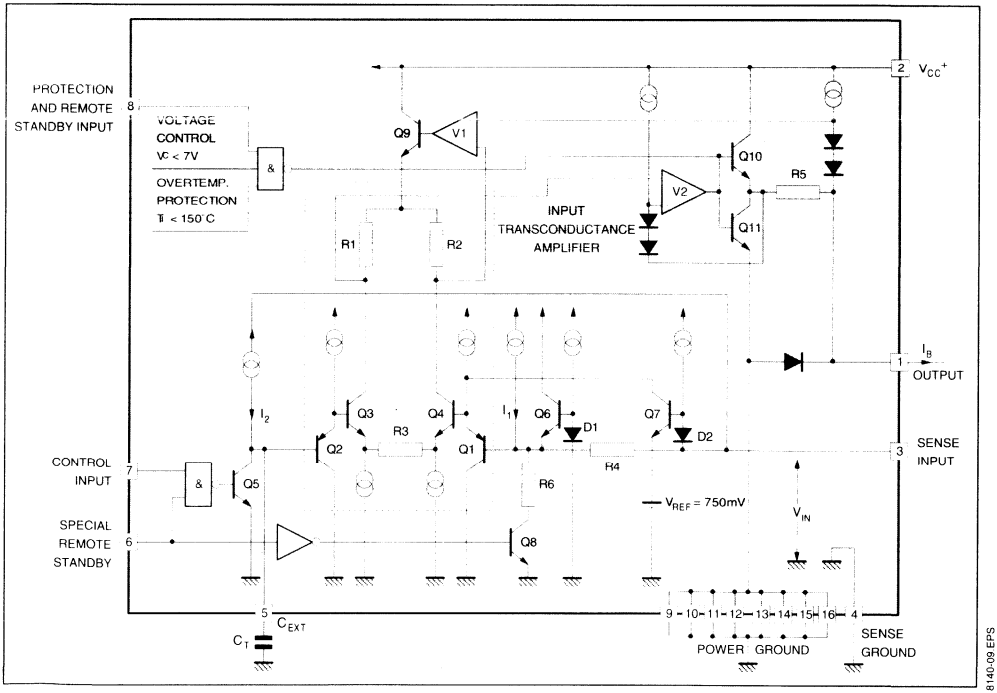


Figure 8 : Integrated Horizontal Driver

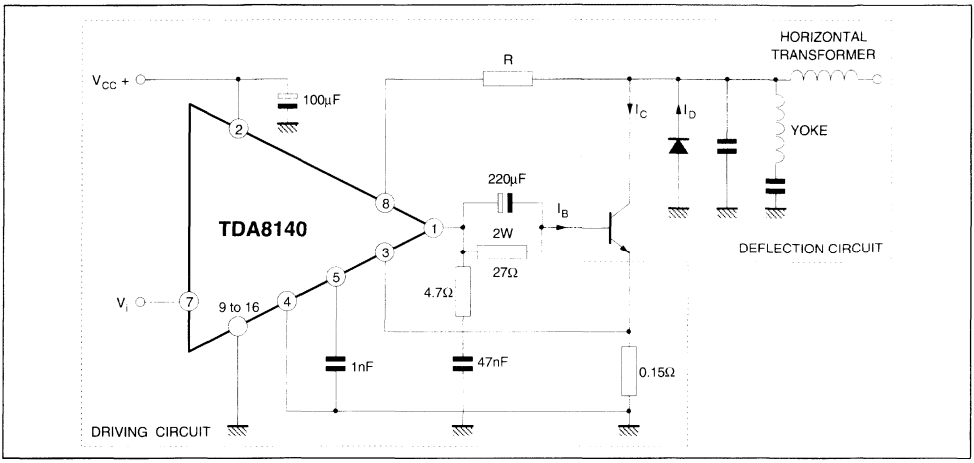
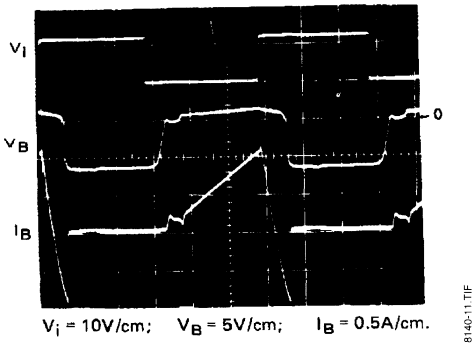
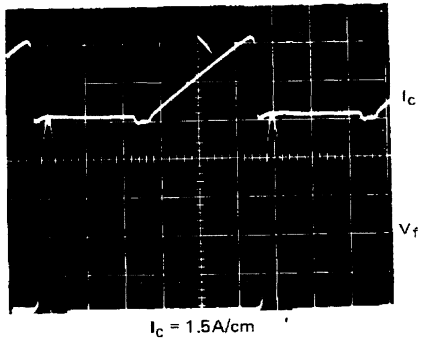


Figure 9 : Signal Diagrams of the Driver Circuits



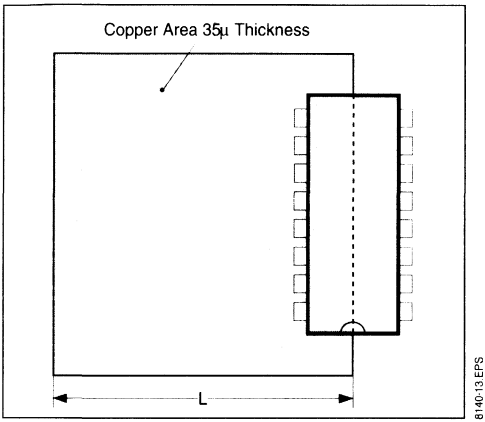
V_i = 10V/cm; V_B = 5V/cm; I_B = 0.5A/cm.



I_C = 1.5A/cm

The power dissipation on this application condition is about 1.3W and Figures 10 and 11 show two ways of heatsinking.
In the first case, a PCB copper area is used as a heatsink L= 65mm while in the second case, the device is soldered to an external heatsink ; in both examples, the thermal resistance junction ambient is 35°C/W.

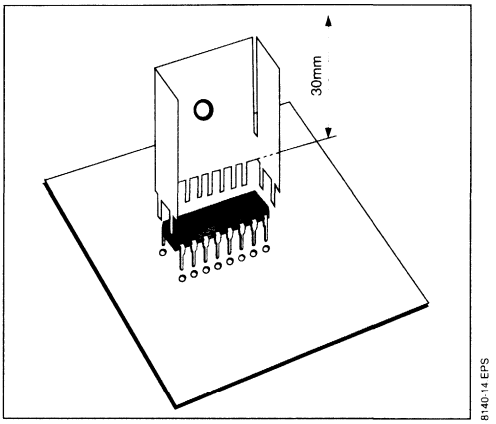
Figure 10 : Example of Heatsink using P.C. Board Copper (L = 65mm)



The presence of thermal shut-down circuit does mean that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply switches off the device.

Figure 11 : Example of an External Heatsink

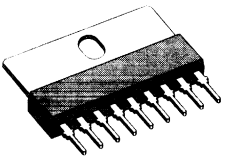


SGS-THOMSON MICROELECTRONICS

TDA8143

HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH THE OUTPUT ON



SIP9
(Plastic Package)

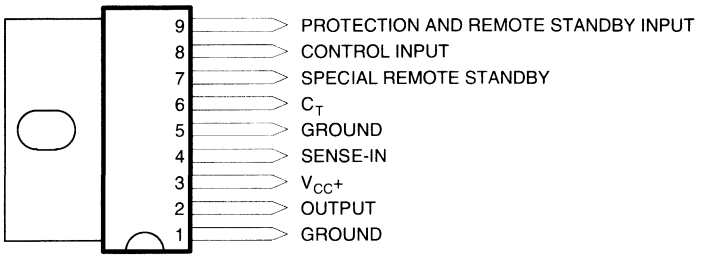
ORDER CODE : TDA8143

DESCRIPTION

The TDA8143 is a monolithic integrated circuit designed to drive the horizontal deflection power tran-sistor.

The current source characteristic of this device is adapted to the non-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA8143 is internally protected against short circuits and thermal overload.

PIN CONNECTIONS



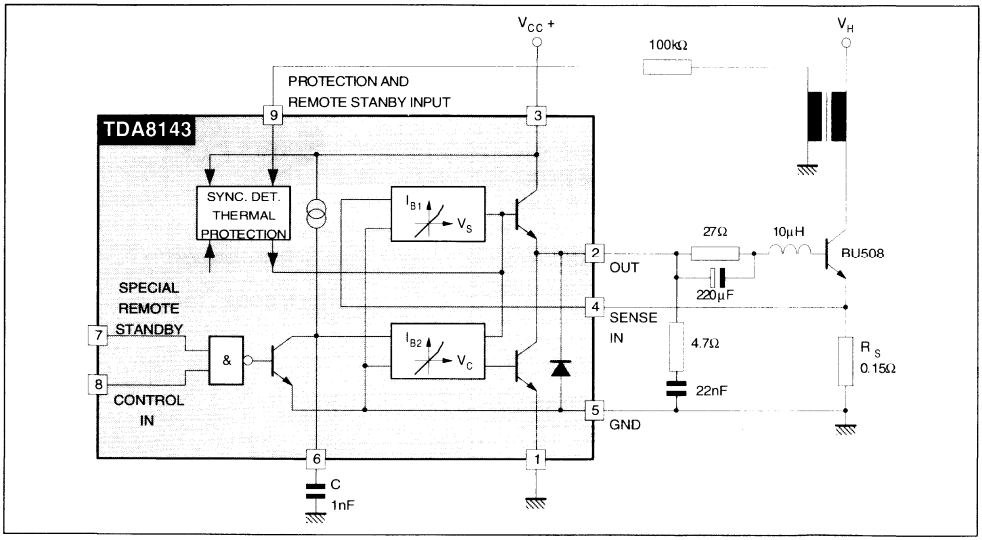
8143-01.EPS

PIN FUNCTIONS

Pin	Name	Function
1	Power Ground	Common Ground
2	Ouptut	Device Output
3	V_{CC}	Supply Voltage
4	Sense Input	Input voltage that determines output current.
5	Sense GND	Reference Ground for Input Voltage at SENSE INPUT.
6	C_{EXT}	Capacitor between this terminal and SENSE GROUND determines the current slope dI_O/dt during OFF phase.
7	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from CONTROL INPUT (2nd priority).
8	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
9	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).

8143-01.TBL

BLOCK DIAGRAM



8143-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40, + 150	°C
T_{oper}	Operating Temperature	0, + 70	°C

8143-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-ambient	Max.	70	°C/W
$R_{th\ (j-c)}$	Thermal Resistance Junction–case	Max.	10	°C/W

8143-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{p0}	Positive Output Current (source)		1.5			A
I_{n0}	Negative Output Current (sink)		2			A
I_{o0}	Positive quiescent output current forcing the output to 6 V and the sense input to ground output externally forced to 6 V.	Remote Input1 Remote Input0	120 50	150 80	200 100	mA mA
G_{ON}	Transconductance ON Phase (1)	See Figure 1	1.8	2.0	2.2	A/V
G_{OFF}	Transconductance OFF Phase (2)	See Figure 1	1.8	2.0	2.2	A/V
G_{REMOTE}	Transconductance Standby Mode	Remote Input0	0.675	0.75	0.825	A/V
I_5	Current Source Pin 6	V_7 = 500 mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	V_S = 0 Remote Input = 1	 – 200	 – 300	 – 400	 µA
R_{SYN}	Synchronous Detection Input Resistance	V_{SYN} < 7 V V_{SYN} > 7 V	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	SYNC DETECT Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA}$ + 0.5 V	– 50 – 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V
I_{INB}	Pull-up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB}$ + 0.5 V	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time (3)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
V_{CC}–V_{OUT}	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_0 \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage (4)		0.8	0.9	1	V

8143-04 TBL

Notes : 1. G_{ON} is measured with V_4 varying from 150mV to 350mV (Pin 6 is grounded)
2. G_{OFF} is measured with V_6 varying from 150mV to 350mV (Pin 4 is grounded)
3. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
4. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g. V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_0 is going to the positive quiescent current I_{o0}.

TRUTH TABLE

Logics Inputs		Output I_0		Mode
Control Input	Remote/Standby			
0 Floating or 1	Floating or 1 Floating or 1	$I_0 > 0$ $I_0 < 0$ (5)	BU508 ON BU508 OFF	Normal Function
X	0	$I_0 < 0$ (5) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_0 > 0$ $t > t_{dr}$	BU508 ON	

8143-05 TBL

Note : 5. $I_O < 0$ means that the sink current flows into the output to ground.

Figure 1 : $\frac{G_{ON}}{V_{Pin3}}$ and $\frac{|G_{OFF}|}{V_{Pin5}}$

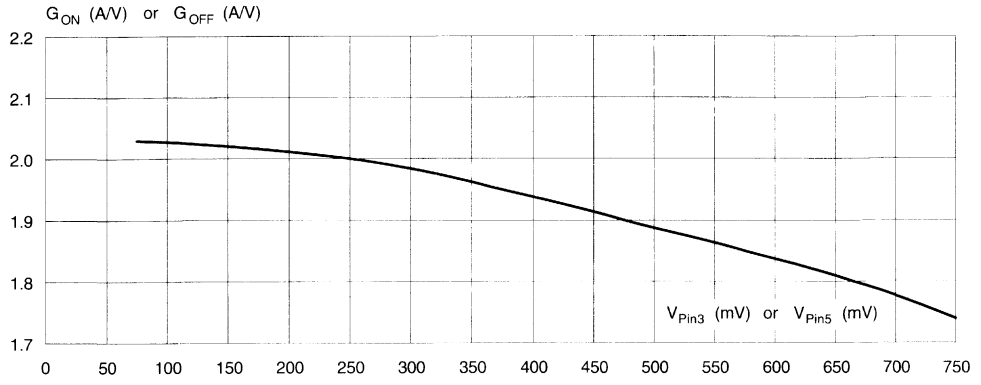
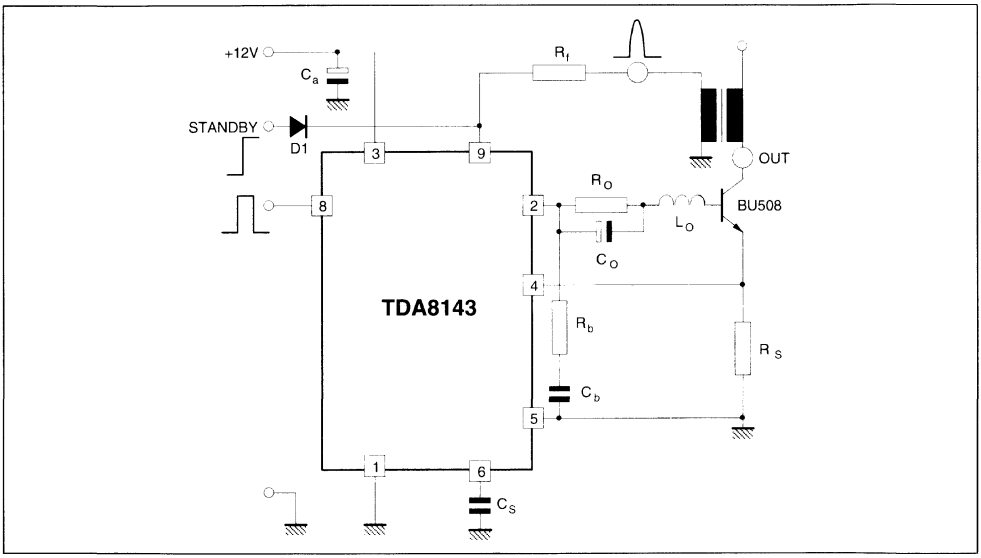


Figure 2 : Large Screen Application



COMPONENTS LIST FOR TYPICAL APPLICATION

CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 µF	47 µF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 µF	220 µF	R_s	0.15 Ω	0.1 Ω
L_o	10 µH	10 µH	C_s	1 nF	1 nF

8143-06.TBL

APPLICATION INFORMATION

The conventional deflection system is shown in Figure 3. The driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

During the active deflection phase the collector current of the power transistor is linearly rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.

According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in Figure 4 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.

The marked area represents a useless base current which gives an additional power dissipation on the power transistor.

Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the convenctional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.

The new approach, using the TDA8143, overcomes these restrictions by means of a feedback principle.

As shown in Figure 4, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_s at the emitter of the power transistor and delivers :

$$I_b = R_S \bullet g_m \bullet I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1+\beta min} \cdot \frac{1}{R_S} < gm < \frac{1}{R_S}$$

where β is the minimum current gain of the transitor. This method always ensures the correct base current and acts time independent on principle.

For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in Figure 5.

Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.

Figure 3 : Conventional Horizontal Deflection System for TVs

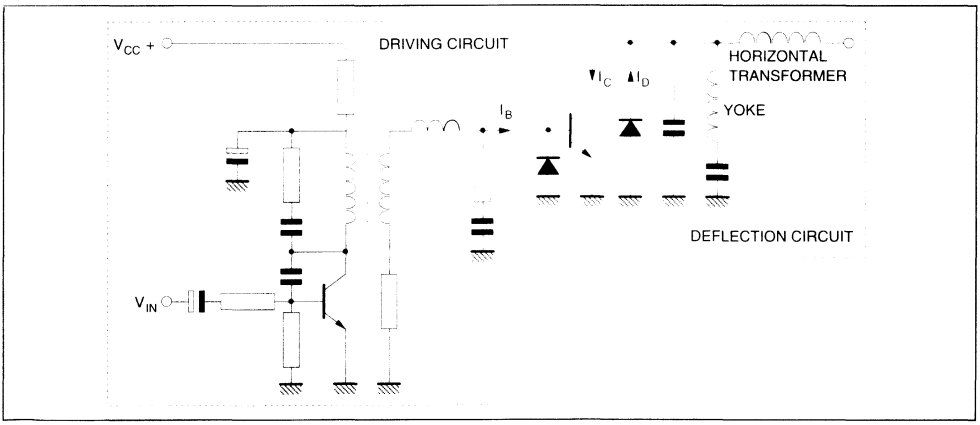
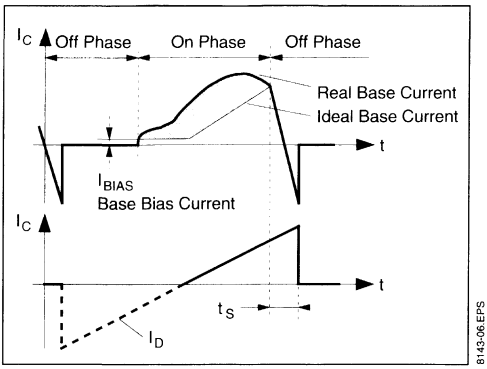


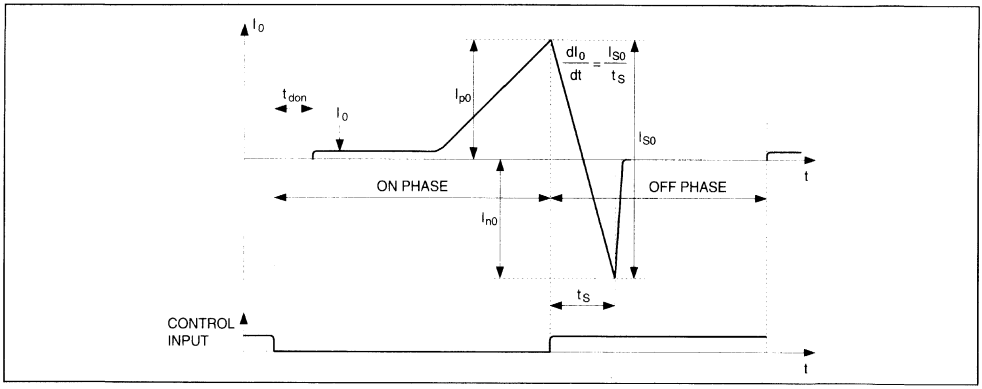
Figure 4 : Waveforms of Collector and Base Current



This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.

As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 5



CIRCUIT DESCRIPTION

Figure 6 shows the block diagram of the TDA8143, the circuit consists of an input transconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2A sink current and 2A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \cdot \frac{1}{R5}$$

A current source I_1 generates a drop of 70mV across the resistor R4 which provides an output bias current of 140mA ; the control input determines the turn ON/OFF function.

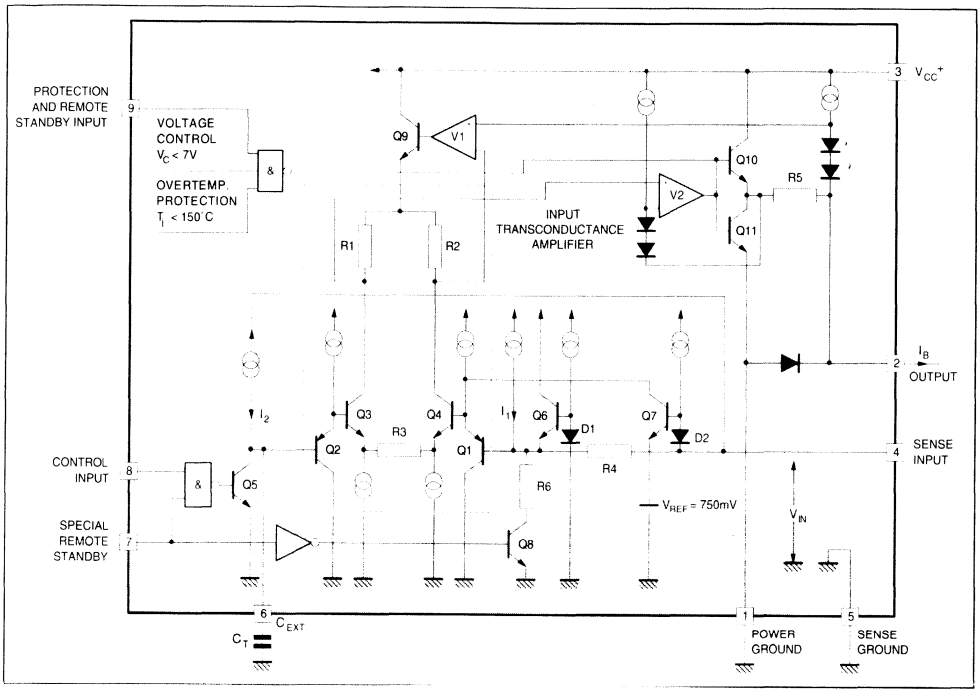
In the ON phase, Q5 shorts the external capacitor C_t. Within the input voltage range $0 < V_{in} < 750mV$ the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750mV, Q7 limits the maximum output current at 1.5A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linearly and the system stability is reached.

During the flyback phase, the IC is enabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

Figure 6 : Block Diagram of the Integrated Horizontal Driver



In Figure 7 is shown the application diagram of the TDA8143, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in Figure 3.

In Figure 8 is shown the currents and voltage waveforms of the driver circuit of Figure 7 as to be seen, the driving charge $I_b \cdot t_{on}$ has been reduced at minimum.

The power dissipation on this application condition is about 1.3W.

The presence of thermal shut-down circuit means that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply switches off the device.

Figure 7 : Integrated Horizontal Driver

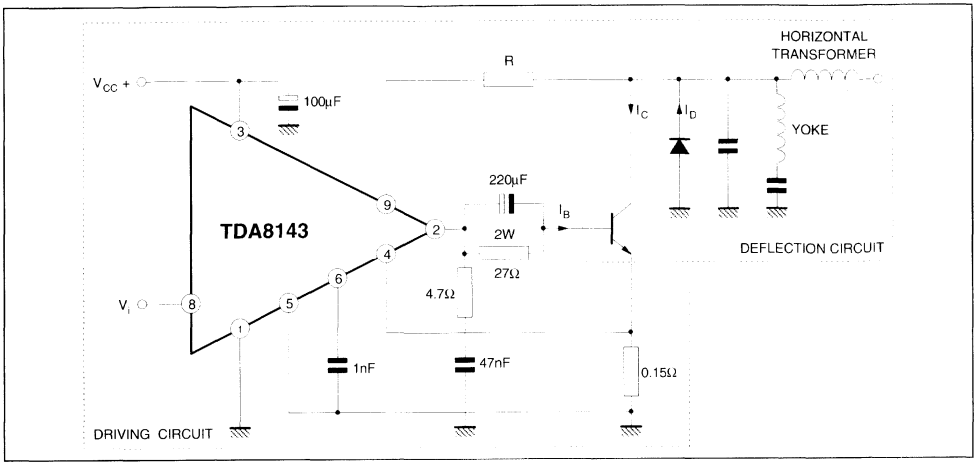
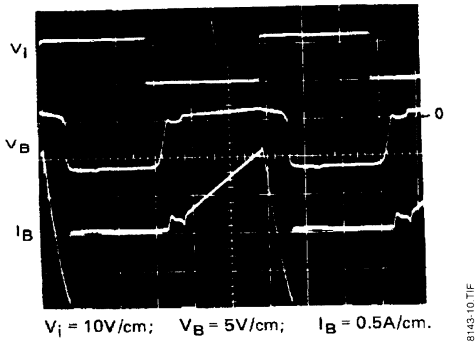
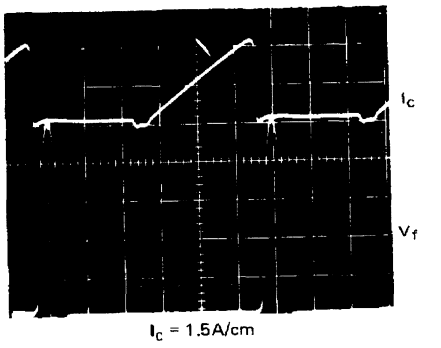


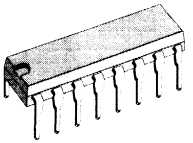
Figure 8 : Signal Diagrams of the Driver Circuits





TV HORIZONTAL PROCESSOR

- NOISE GATED HORIZONTAL SYNC SEPARATOR
- NOISE GATED VERTICAL SYNC SEPARATOR
- HORIZONTAL OSCILLATOR WITH FREQUENCY RANGE LIMITER
- PHASE COMPARATOR BETWEEN SYNC PULSES AND OSCILLATOR PULSES (PLL)
- PHASE COMPARATOR BETWEEN FLYBACK PULSES AND OSCILLATOR PULSES (PLL)
- LOOP GAIN AND TIME CONSTANT SWITCHING (VCR)
- COMPOSITE BLANKING AND KEY PULSE GENERATOR
- PROTECTION CIRCUITS
- OUTPUT STAGES WITH HIGH CURRENT CAPABILITY



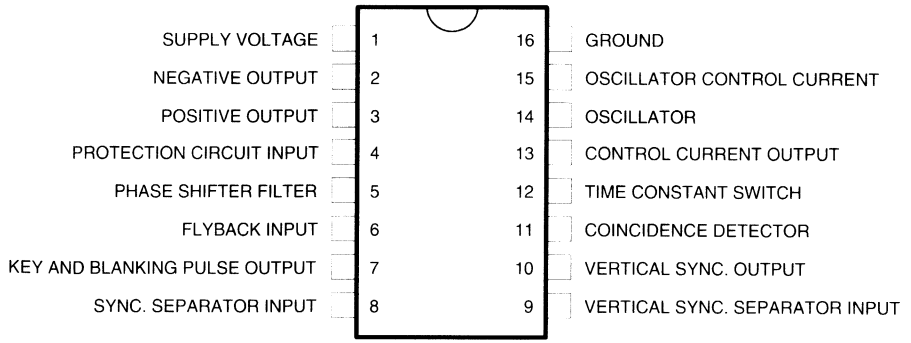
DIP16
(Plastic Package)

ORDER CODE : TDA1180P

DESCRIPTION

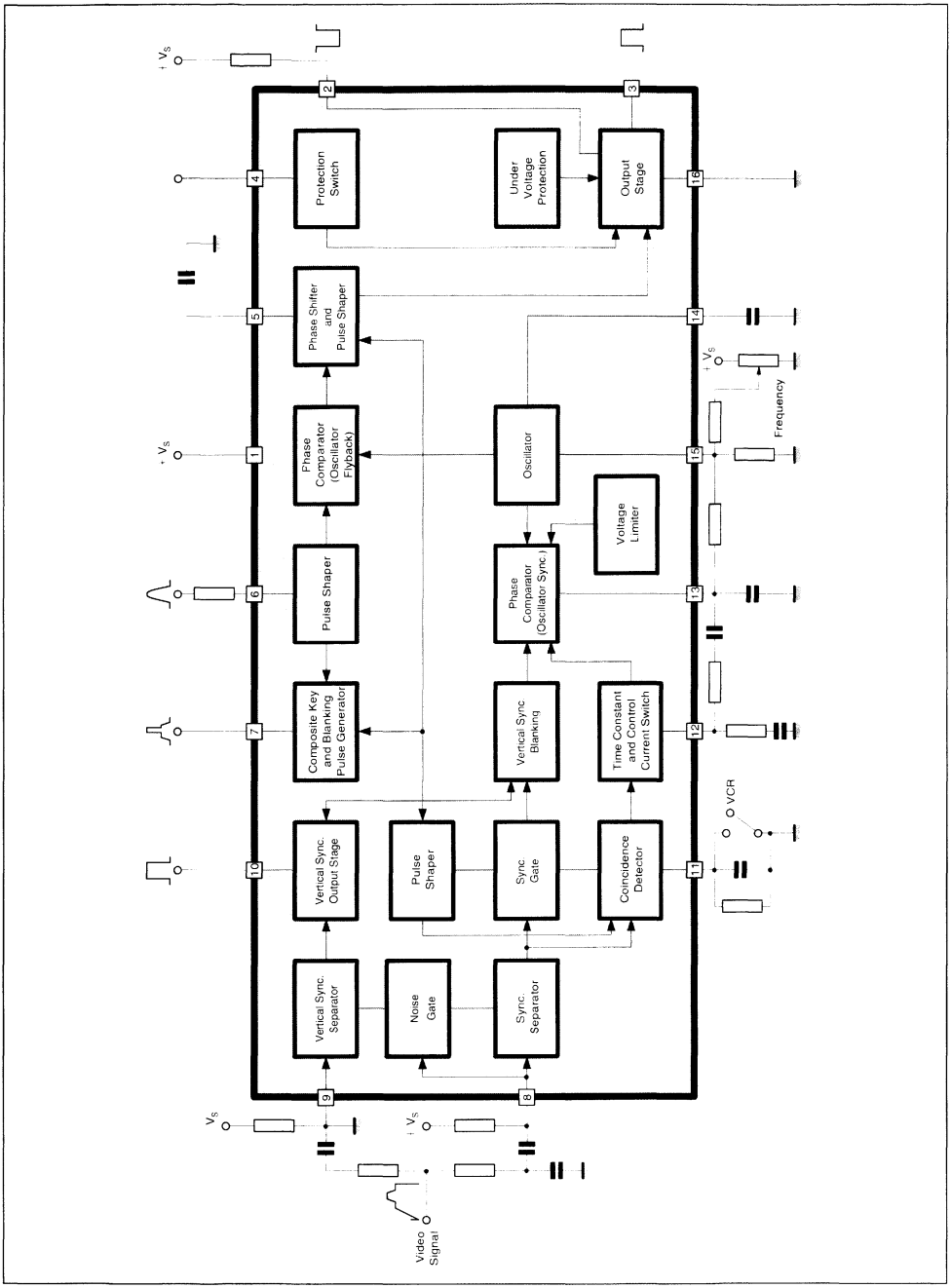
The TDA1180P is a horizontal processor circuit for b.w. and colour monitors. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package.

PIN CONNECTIONS



1180P-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply voltage (Pin 1)	15	V
V_2	Voltage at Pin 2	18	V
V_4	Voltage at Pin 4	V_S	
V_8	Voltage at Pin 8	- 6 , V_S	V
V_9	Voltage at Pin 9	± 6	V
V_{11}	Voltage at Pin 11	V_S	
I_2	Pin 2 peak current	1	A
I_3	Pin 3 peak current	0.5	A
I_6	Pin 6 current	30	mA
I_7	Pin 7 current	20	mA
I_{10}	Pin 10 current	30	mA
P_{tot}	Total power dissipation at Tamb ≤ 70°C	1	W
T_{stg} , T_j	Storage and junction temperature	- 40 , + 150	°C

1180P-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-Ambient	Max	80	°C/W

1180P-02 TBL

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		9.5	12	13.2	V
I_S	Supply current	I_3 = 0		42	52	mA
V_S	Supply voltage at which the output pulses (at pin 2 and 3) are switched off				4	V
HORIZONTAL SYNC. SEPARATOR						
V_I	Peak to peak input signal		1	3	6	V
V_8	Input switching voltage	I_8 = 80 µA		1.5		V
I_8	Input switching current	V_8 = 1.4V		10		µA
I_8	Leakage current	V_8 = -5V			1	µA
VERTICAL SYNC. SEPARATOR						
V_I	Peak to Peak Input Signal		1	3	6	V
V_9	Input Switching Voltage	I_9= 80µA		1.5		V
I_9	Input Switching Current	V_9 = 1.4V		5		µA
I_9	Leakage Current	V_9 = -5V			1	µA
V_{10}	Vertical Sync. Pulse Output Voltage	No Load Pin10	11			V
R_{10}	Output Resistance			10		kΩ
t_{LV}	Delay between Leading Edge of Input and Output Signals			17		µs
t_{LV}	Delay between Trailing Edge of Input and Output Signals			50		µs
t_V	Vertical Sync Pulse Duration			190		µs

1180P-03 TBL

ELECTRICAL CHARACTERISTICS (continued)
(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PROTECTION CIRCUIT						
V_4	Input Voltage for Switching off the Output Pulses	Output Pulses OFF Output Pulses ON	1		0.5	V
R_4	Input Resistance			200		kΩ
I_4	Input Current		5			µA
FLYBACK PULSE						
V_6	Input Threshold Voltage of Blanking Generator			1.8		V
V_6	Input Threshold Voltage of Phase Comparator			7.6		V
I_6	Input Switching Current	$V_6 \geq$ 1.7V		0.45		mA
OUTPUT PULSE						
V_3	Peak-to-Peak Output Voltage	I_3 = 150 mApp		10		V
I_3	Output Current	V_3 = 5V		500		mA
R_3	Output Resistance	At Leading Edge of output pulse At Training Edge of Output Pulse		3 20		Ω Ω
t_p	Output Pulse Duration		20	22	26	µs
COMPOSITE BLANKING AND KEY PULSE						
V_{7k}	Key Pulse Output Peak Voltage		9	11		V
V_{7B}	Blanking Pulse Output Voltage		4.2	4.5	4.8	V
R_7	Output Resistance			100		Ω
t_{sk}	Phase Relation Between Trailing Edge of Key Pulse and Middle of Sync. Input Pulse			2.7		µs
t_k	Key Pulse Duration		3.5	3.8		µs
t_{fb}	Delay between Flyback Pulse and Blanking Pulse	V_6 = 1.7V			0.2	µs
INTERNAL GATING PULSE						
t_g	Gating Pulse Duration			7.5		µs
t	Phase Relation between Middle of Sync. Pulse and Trailing and Leading Edge of Gating Pulse			3.75		µs
COINCIDENCE DETECTOR						
V_{11}	Output Voltage	With Coincidence Without Coincidence		6.8	4	V V
I_{11}	Peak Output Current			0.5		mA
VCR SWITCH						
V_{11}	Input Voltage		0 to 4 or 8.5 to 12			V
- I_{11}	Output Current		35			µA
I_{11}	Output Current		0.4			mA
TIME CONSTANT SWITCH						
V_{12}	Output Voltage			3		V
R_{12}	Output Resistance	4.5V < V_{11} < 8V V_{11} > 8.5V or V_{11} < 4V		100 40		Ω kΩ

1180P-04.TBL

ELECTRICAL CHARACTERISTICS (continued)
(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OSCILLATOR						
V_{14}	Low Level Threshold Voltage			5.4		V
V_{14}	High Level Threshold Voltage			8.2		V
I_{14}	Charge Current			0.6		mA
I_{14}	Discharge Current			0.3		mA
V_{15}	Current Source Supply Voltage			3		V
I_{15}	Current Source Supply Current			0.3		mA
f_O	Free Running Frequency			15625		Hz
$\frac{\Delta f_O}{f_O}$	Adjustment Range			± 10		%
$\frac{\Delta f_O}{\Delta I_{15}}$	Frequency Control Sensitivity			52		Hz µA
Δf_O	Frequency Change when V_S Drops to 4V				± 10	%
OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR						
V_5	Control Voltage Range			9.4 to 8.2		V
I_5	Peak Control Current		-0.6		+0.6	mA
I_5	Input Current (blocked Phase Detector)				5	µA
t_D	Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge			$t_p - t_f$		µs
$\frac{\Delta t}{\Delta t_D}$	Static Control Error				0.2	%
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
V_{13}	Control Voltage Range		4.6 to 1.4			V
I_{13}	Control Peak Current		+2	-2.2	-2	mA
$\frac{\Delta f}{\Delta t}$	Phase Lock Loop Gain			2		kHz µs
f	Catching and Holding Range			± 700		Hz
OVERALL PHASE RELATIONSHIP						
t_O	Phase Relation between Middle of Flyback Pulse and Middle of Sync. Pulse			2.2		µs
$\frac{\Delta V_5}{\Delta t_O}$	Adjustment Sensitivity			65		mV µs
$\frac{\Delta I_5}{\Delta t_O}$	Adjustment Sensitivity			16		µA µs

1180P-05.TBL

TEST CIRCUIT

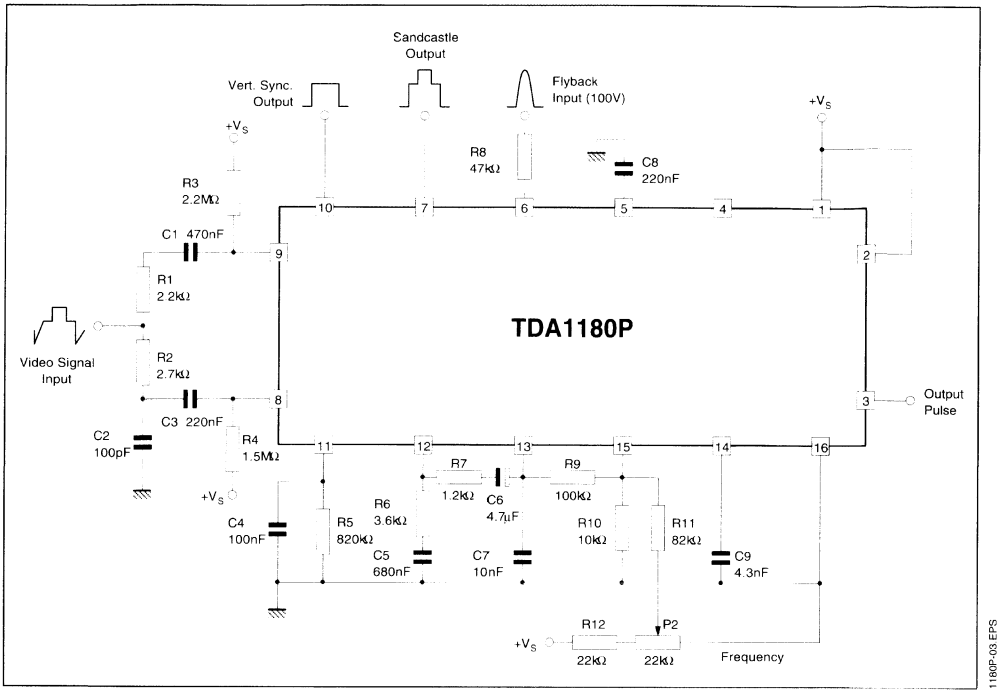


Figure 1 : Vertical Sync. Output Pulse

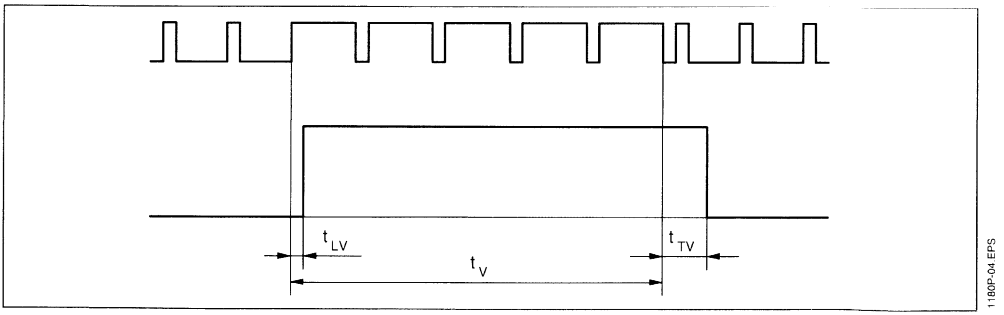


Figure 2 : Relation Ship of Main Waveform Phases

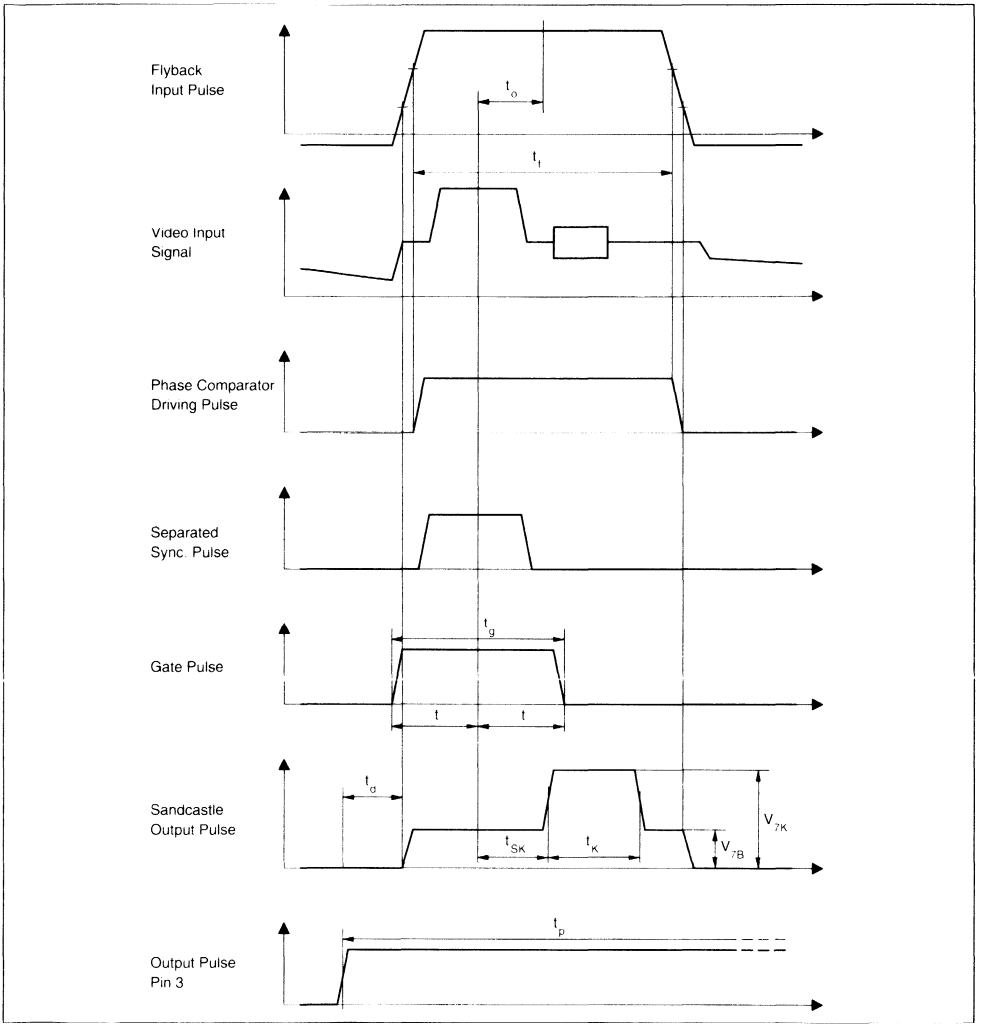


Figure 3 : Free Running Frequency versus Supply Voltage

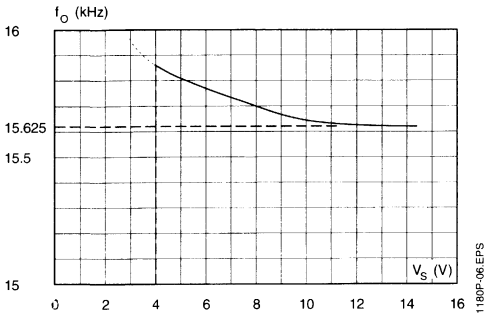
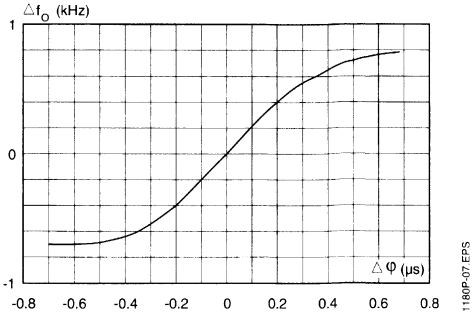


Figure 4 : Loop Gain



APPLICATION INFORMATION

Pin 1 - Positive supply

The operating supply voltage of the device ranges from 10V to 13.2V

Pin 2 and 3 - Output

The outputs of TDA1180P are suitable for driving transistor output stages, they deliver positive pulse at Pin 3 and negative pulse at Pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.
The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

Pin 4 - Protection circuit input

By connecting Pin 4 of the IC to earth the output pulses at Pin 2 and 3 are shut off ; this function has been introduced to produced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

Pin 5 - Phase shifter filter

To compensate for the delay introduced by the line final stages, the flyback pulses to Pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to Pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is: $t_d = t_p - t_f$ where t_f is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

Pin 6 - Flyback input

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

Pin 7 - Key and blanking pulse output

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at Pin 6.
The sum of the two signals (sandcastle pulse) is available on low impedance at output Pin 7.

Pin 8 and 9 - Sync separators inputs

The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.

Pin 10 - Vertical sync output
The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.
The output impedance is typically 10kΩ and the lowest amplitude without load is 11V.

Pin 11 - Coincidence detector
From the oscillator waveform a gate pulse 7 µs wide is taken whose phase position is centered on the horizontal synchronism.
The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.
When the two signals are not accurately aligned in time it means that the oscillator is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on Pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.
Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on Pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting Pin 11 to earth or to + V_S. The characteristics of the phase lock thus correspond to the lack of synchronization.

Pin 12 - Time constant switch, (see Pin 11)

Pin 13 - Control current output
The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I13 (proportional to the phase difference between the two signals) to Pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by Pin 12.
The voltage limiter at the output of the phase comparator limits the voltage excursion on Pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of Pin 13 is:
- low when V13 > 4.3 or V13 < 1.6V
- high when 1.6V < V13 < 4.3V

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync,a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage; inhibition remain even if the video signal is not present.
The free running frequenc of the oscillator is determined by the values of the capacitor and of the resistor connected to Pins 14 and 15 respectively.
To generate the line frequency output pulses, two theresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

Pin14 - Oscillator (see Pin 13)

Pin 15 - Oscillator control current input (see Pin 13)

Pin 16 - Ground

Figure 5 : Application Circuit for Large Screen Black & White and Colour TV

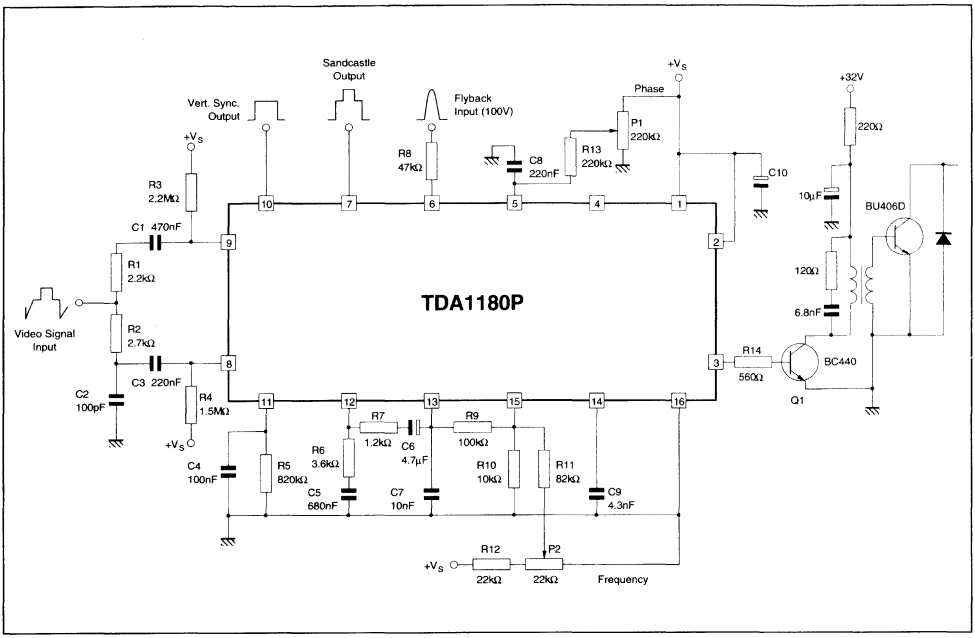


Figure 6 : P.C. Board and Component Layout for the Circuit in Figure 6 (1:1 scale)

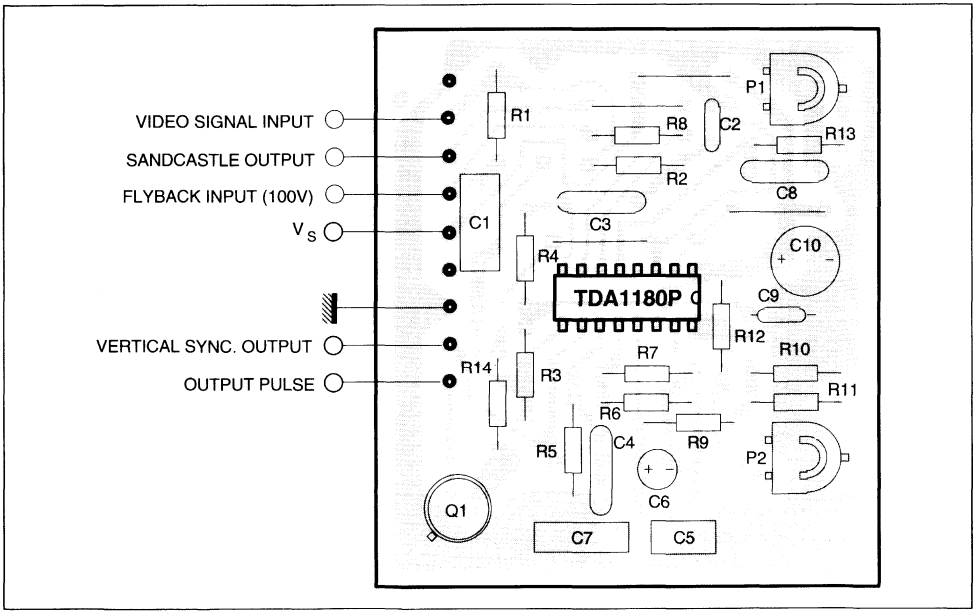


Figure 7 : Application Circuit for Small Screen b.w. TV

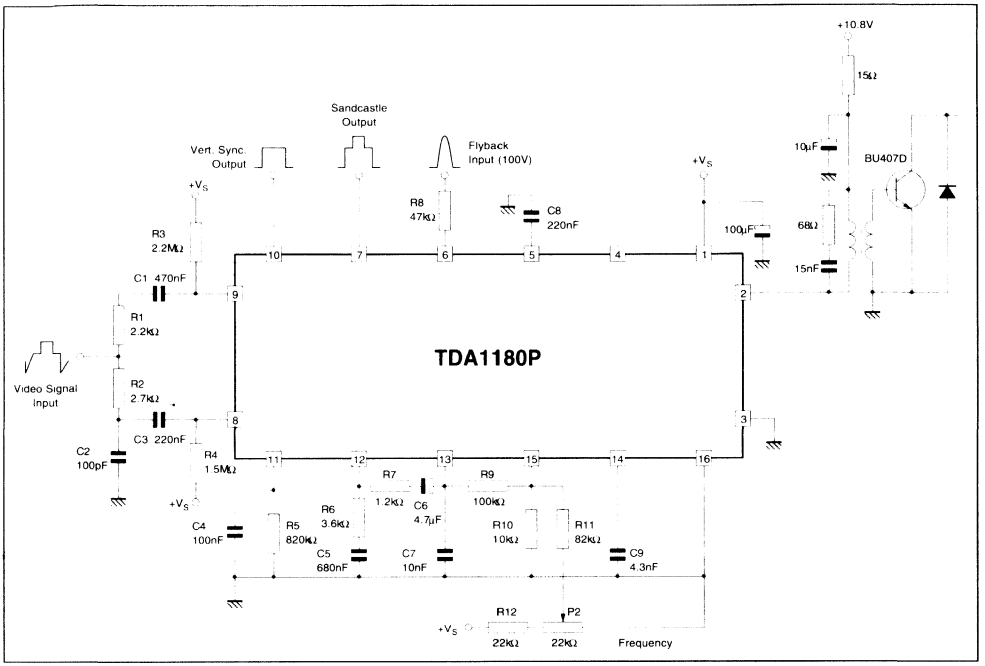
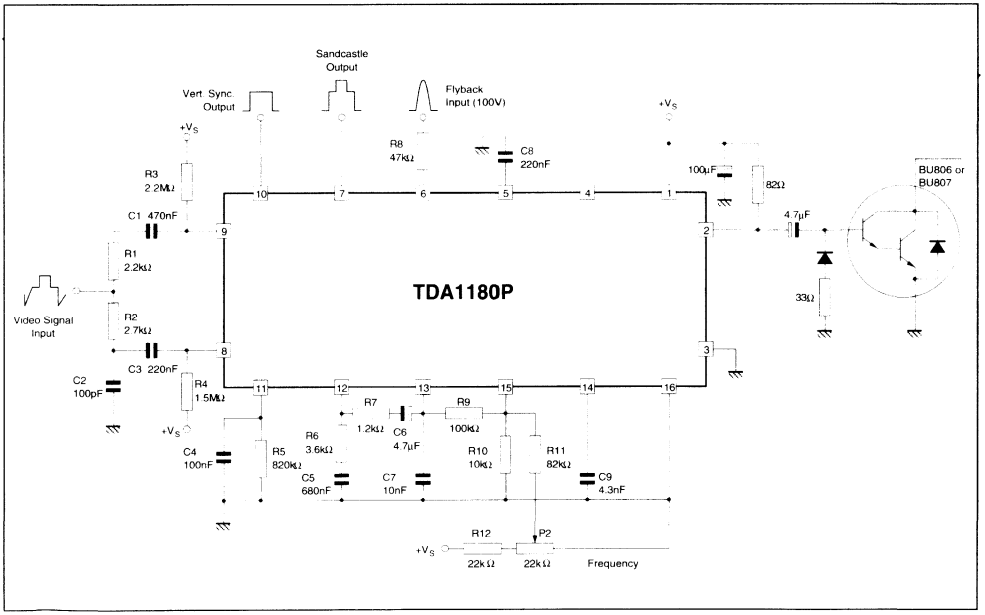


Figure 8 : Application Circuit for Darlington Output Stage



SGS-THOMSON MICROELECTRONICS

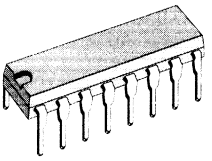
TDA2593

SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET

- LINE OSCILLATOR (two levels switching)
- PHASE COMPARISON BETWEEN SYNCHRO-PULSE AND OSCILLATOR VOLTAGE Ø 1, ENABLED BY AN INTERNAL PULSE, (better parasitic immunity)
- PHASE COMPARISON BETWEEN THE FLYBACK PULSES AND THE OSCILLATOR VOLTAGE Ø 2
- COINCIDENCE DETECTOR PROVIDING A LARGE HOLD-IN-RANGE
- FILTER CHARACTERISTICS AND GATE SWITCHING FOR VIDEO RECORDER APPLICATION
- NOISE GATED SYNCHRO SEPARATOR
- FRAME PULSE SEPARATOR
- BLANKING AND SAND CASTLE OUTPUT PULSES
- HORIZONTAL POWER STAGE PHASE LAGGING CIRCUIT
- SWITCHING OF CONTROL OUTPUT PULSE WIDTH
- SEPARATED SUPPLY VOLTAGE OUTPUT STAGE ALLOWING DIRECT DRIVE OF SCR'S CIRCUIT
- SECURITY CIRCUIT MAKES THE OUTPUT PULSE SUPPRESSED WHEN LOW SUPPLY VOLTAGE

DESCRIPTION

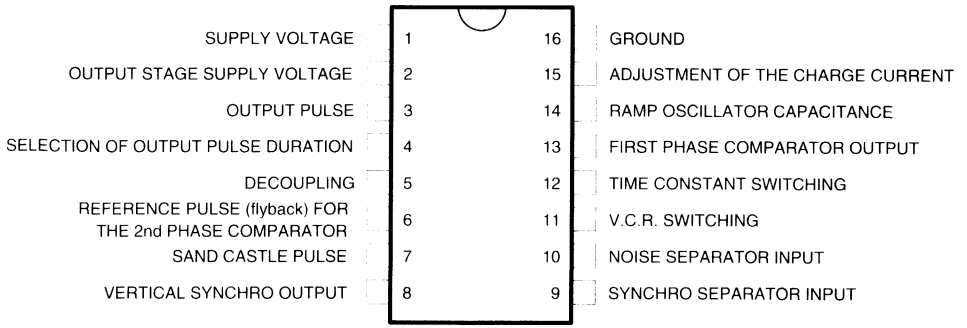
The TDA2593 is a circuit intended for the horizontal deflection of color TV sets, supplied with transistors or SCR'S.



DIP16
(Plastic Package)

ORDER CODE : TDA2593

PIN CONNECTIONS



2593-01 EPS

MAIN CHARACTERISTICS

Symbol	Parameter	Typ.	Unit
V(1–16)	Supply Voltage	12	V
I(1)	Supply Current	30	mA

INPUT SIGNALS

V(9–16) (pp)	Synchro Separator Input Voltage	3 to 4	V
V(10-16) (pp)	Noise Separators Input Voltage	3 to 4	V
	Control Voltage of the Output Pulse Switching Circuit		
V(4–16)	t = 7 µs (thyristor)	9.4 to V(1–16)	V
V(4–16)	t = 14 µs + t_d (transistor)	0 to 3.5	V
V(4–16)	t = 0 (V(3–16) = 0)	5.4 to 5.6	V

OUTPUT SIGNALS

V(8–16) (pp)	Frame Synchro Pulse	11	V
V(7–16) (pp)	Sandcastle Pulse	11	V
V(3–16) (pp)	Horizontal Driver Stage Control Pulse	10.5	V

2593-01.TBL

ABSOLUTE MAXIMUM RATINGS (Maximum Ratings according to CEI 134 Datasheet)

Symbol	Parameter	Value	Unit
V(1–16)	Supply Voltage to Pin 1	13.2	V
V(2–16)	Supply Voltage to Pin 2	18	V
V(4–16)	Voltage to Pin 4	13.2	V
V(9–16)	Voltage to Pin 9	±6	V
V(10–16)	Voltage to Pin 10	±6	V
V(11–16)	Voltage to Pin 11	13.2	V
$I_{2M} = -I_{3M}$	Current ai Pins 2 and 3 (with thyristor)	650	mA
$I_{2M} = I_{3M}$	Current ai Pins 2 and 3 (with transistor)	400	mA
I(4)	Current to Pin 4	1	mA
I(6)	Current to Pin 6	±10	mA
I(7)	Current to Pin 7	-10	mA
I(11)	Current to Pin 11	2	mA
P_{tot}	Power Dissipation	800	mW
T_{oper}	Operating Ambient Temperature	-20, +70	°C
T_{stg}	Storage Temperature	-25, +125	°C

2593-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

(T_{amb} = 25°C, V_1–V_{16} = 12V , unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input Signals				
	Synchro Separator (Pin 9)				
V_{9-16}	Input Threshold Voltage		0.8		V
I_9	Input Threshold Current			5	µA
I_9	On-state Input Current		5 to 100		µA
I_9	Disconnect Input Current	100	150		µA
I_9	Off-state Input Current (V_{9-16} = – 5V)			– 1	µA
V_9	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		V_{PP}
	Noise Separator (Pin 10)				
V_{10-16}	Input Threshold Voltage		1.4		V

2593-03.TBL

Note : 1. Allowed range 1 to 7V

ELECTRICAL OPERATING CHARACTERISTICS

(T_{amb} = 25°C, V_1–V_{16} = 12V , unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{10}	Input Threshold Current	100	150		µA
I_{10}	Input Current		5 to 100		µA
I_{10}	Off-state Input Current (V_{10-16} = – 5V)			– 1	µA
V_{10}	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		V_{PP}
V_{10}	Allowed superimposed parasitic signal			7	V
V_{6-16}	Fly-back Pulse (Pin 6) Input Threshold Voltage		1.4		V
V_6	Input Limitation Level		–0.7 and +1.4		V
I_6	Input Current	0.01	1	2	mA
V_{4-16}	Output Pulse Width Control Switch (Pin 4) Input Voltage t = 7 µs (thyristor) t = 14 µs + t_d (transistor) t = 0 (V_{3-16} = 0) (note 2)		 9.4 to V_{1-16} 0 to 3.5 5.4 to 6.6		 V V V
I(4)	Input Current t = 7 µs (thyristor) t = 14 µs + t_j (transistor) t = 0 (V_{3-16} = 0)	200 200	 0		µA µA µA
V_{11-16}	Video Recorder Switch (Pin 11) Input Voltage (Pin 11 low level) (Pin 11 to + V_{CC})		 0 to 2.5 9 to V_{1-16}		 V V
I_{11}	Input Current (Pin 11 low level) (Pin 11 to + V_{CC})			200 2	µA mA
V_{8-16}	Output Signals Frame Synchro Pulses (positive) (Pin 8) Output Voltage (peak value)	10	11		V
R_8	Output Impedance		2		kΩ
t_{on}	Delay Between Leading Edge of Input Signal and Leading Edge of Output Signal		15		µs
t_{off}	Delay Between Trailing Edge of Input Signal and Trailing Edge of Output Signal		15		µs

SANDCASTLE PULSE (POSITIVE) (PIN 7)

V_{7-16}	Output Voltage (peak valve)	10	11		V
R_7	Output Impedance		70		Ω
I_7	Output Current During Trailing Edge		2		mA
t_7	Sandcastle Pulse Width (V_7 = 7 V)	3.7		4.3	µs
Δt	Phase Between Middle Input Synchro Pulse and Leading Edge of Sandcastle Pulse (V_7 = 7 V)	2.15		3.15	µs

FLY-BACK BLANKING PULSE (PIN 7)

V_{7-16}	Output Voltage (peak value)	4		5	V
R_7	Output Impedance		70		Ω
I_7	Output Current During Trailing Edge		2		mA

CONTROL PULSE FOR HORIZONTAL DRIVER (POSITIVE) (PIN 3)

V_{3-16}	Output Voltage (peak value)		10.5		V
R_3	Output Impedance (leading edge) (trailing edge)		2.5 20		Ω Ω
t_3 t_3	Control Pulse Width V_4 = 9.4 to V_{1-16} V_4 = 0 to 4V (note 3)	5.5	 14 + t_c	8.5	µs µs
V_{1-16}	Control pulse is disabled for		4		V

2593-04.TBL

Notes : 1. Allowed range 1 to 7V
2. Or Pin 4 not connected.
3. With t_r = 12µs

ELECTRICAL OPERATING CHARACTERISTICS (contined)

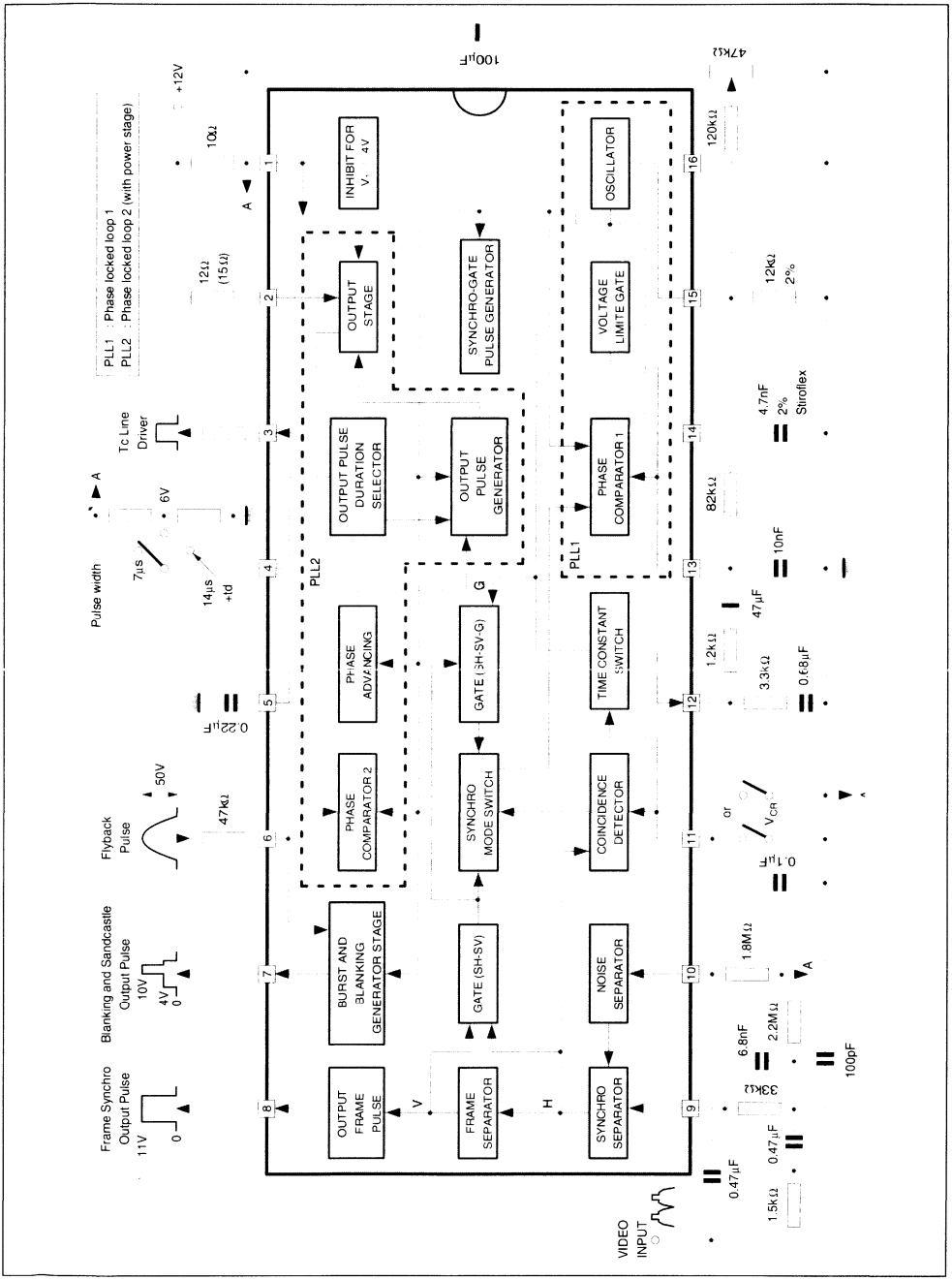
(T_{amb} = 25°C, V_1–V_{16} = 12V , unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
OVERALL PHASE RELATION SHIP					
t_z	Phrase Between Middle Synchro Pulse and Middle Fly-back Pulse (t_r = 12 µs, note 4	1.9		3.3	µs
$\Delta I/\Delta t$	Sensitivity to Current Adjust		30		µA/µs
OSCILLATOR (PINS 14 AND 15)					
V_{14-16}	Threshold Voltage (low level) (high level)		4.4 7.6		V V
I_{14}	Current Generator		± 0.47		mA
f	Free Running Frequency (C_{osc} = 4700pF, R_{osc} = 12kΩ)		15625		Hz
Δf	Tolerance on Frequency (note 5)			± 5	%
$\Delta f/15$	Frequence Control Sensitivity		31		Hz/µA
Δf	Spread of Frequency		± 10		%
$\frac{\Delta f/f}{\Delta V/V \text{ nom.}}$	nfluence of Supply Voltage on Frequency (note 5)			± 0.05	%
Δf	Frequency change when decreasing the supply down to 5 V (V_{1-16} = 5V, note 5)			± 10	%
T	Frequency Temperature Coefficient (note 5)			$\pm 10^{-4}$	Hz/°C
PHASE COMPARATOR ø 1 (PIN 13)					
V_{13-16}	Control Voltage Range		3.8 to 8.2		V
I_{13}	Control Current (peak value)		±1.9 to ±2.3		mA
I_{13}	Off-state Current (V_{13-16} = 4 to 8 V)			– 1	µA
R_{13}	Output Impedance (V_{13-16} = 4 to 8 V, note 6) (V_{13-16} < 3.8 V cr > 8.2 V, note 7)		High Low		
	Control Sensibility		2		kHz/µs
Δf	Catching and Holding Range		± 780		Hz
$\Delta f/f$	Catching and Holding Range Tolerance (note 5)		± 10		%
PHASE COMPARATOR ϕ 2 AND PHASE-SHIFT (PIN 5)					
V_{5-16}	Control Voltage Range		5.4 to 7.6		V
I_5	Control Current (peak value)		± 1		mA
I_5	Off-state Output Current (V_{5-16} = 5.4 to 7.6 V)			– 5	µA
R_5	Output Impedance (V_{5-16} = 5.4 to 7.6 V, note 6) (V_{5-16} < 5.4 V or > 7.6 V)		High 8		 kΩ
t_d	Max. delay Between Output Pulse Leading Edge and Fly-back Pulse Trailing Edge (t_r = 12 µs)			15	µs
$\Delta t_f/\Delta t_d$	Static Control Error			0.2	%
COÏNCIDENCE DETECTOR (PIN 11)					
V_{11-16}	Output Voltage		0.5 to 6		V
I_{11}	Output Current (without coïncidence) (with coincidence)		0.1 – 0.5		mA mA
TIME CONSTANT SWITCH (PIN 12)					
V_{12-16}	Output Voltage		6		V
I_{12}	Output Current		± 1		mA
R_{12}	Output Impedance (V_{11-16} = 2.5 to 7 V) (V_{11-16} < 1.5 or > 9 V)		100 60		Ω kΩ
PULSE GENERATOR (INTERNAL)					
t	Pulse Width		7.5		µs

2593-05.TBL

Notes : 4. The adjustement of overall phase relation (and output pulse leading edge position) is automatically performed by phase comparator Ø 2. If additional adjustement is needed, a current have to be imposed at pin 5.
5. Tolerance of peripheral components not included.
6. Current generator.
7. Emitter-follower

BLOCK DIAGRAM AND TYPICAL APPLICATION

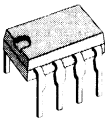


SGS-THOMSON MICROELECTRONICS

TDA8128

SYNC SEPARATOR AND VIDEO SIGNAL IDENTIFICATION

- AC COUPLED COMPOSITE VIDEO SIGNAL
- COMPOSITE SYNC OUTPUT
- EDGE TRIGGERED VERTICAL SYNC OUTPUT
- AUDIO MUTING OUTPUT



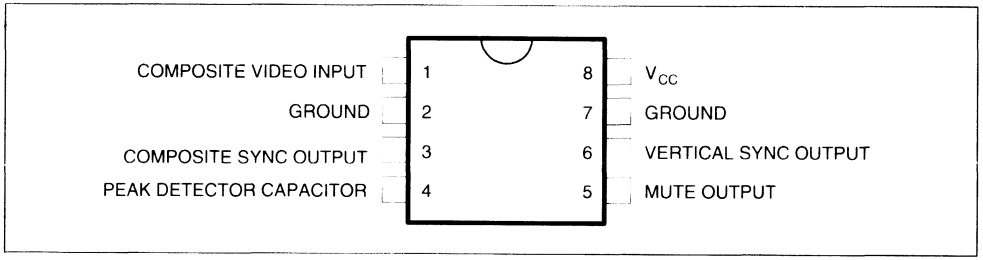
DIP8
(Plastic Package)

ORDER CODE : TDA8128

DESCRIPTION

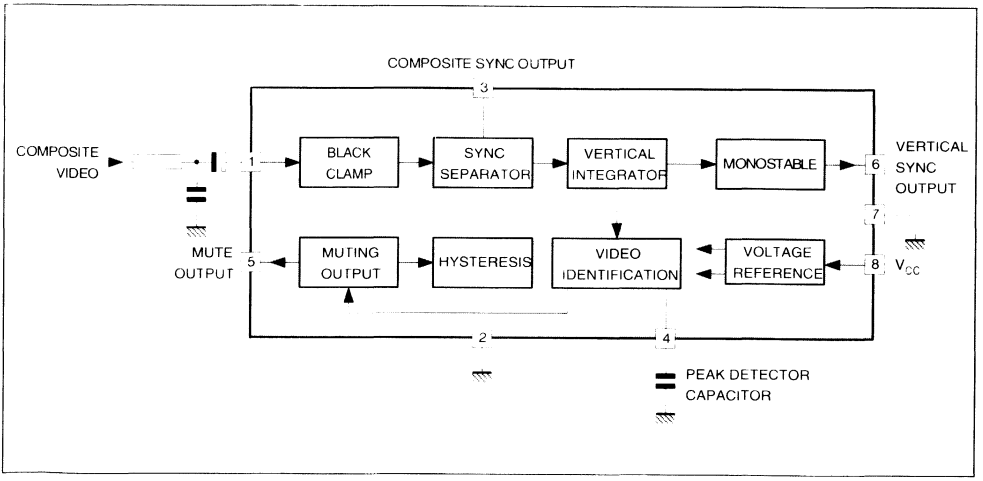
The TDA8128 is a monolithic integrated circuit in DIP8 package. It provides composite sync, edge triggered vertical sync and audio muting signals.

PIN CONNECTIONS



8128-01 EPS

BLOCK DIAGRAM



8128-02 EPS

GENERAL DESCRIPTION

The TDA8128 extracts the composite and vertical sync signals from a video input signal with a negative going horizontal sync pulse.
By means of an internal monostable, the beginning of the vertical sync is triggered by the rising edge of the first serration in the vertical sync period.

The device also provides information when the input signal is not a true video signal or if its amplitude is below a certain limit.
The output stages are supplied by an internal reference voltage so that no external pull-up resistors are needed.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
	Sink Current (Pins 3, 5, 6)	20	mA
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	-40, +150	°C

8128-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Typ.	90	°C/W

8128-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_{amb} = 25°C,
Video Signal : standard PAL color bar generator (V_I = 2V_{PP}) (unless otherwise specified)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_8	Supply Voltage	8		10.8	12	13.2	V
I_8	Supply Current	8			8	15	mA
V_{IN}	Input Signal Range	1			2	5	V_{PP}
COMPOSITE SYNC OUTPUT							
WH	Min. Horizontal Input Sync Width	3	For stable output signals	4	4.7	5.5	µs
$V_{1\ min}$	Min. Input Sync Pulse Amplitude	1	Stable output signal on Pin 3		330	400	mV_{PP}
V_3	Pulse Amplitude	3		4.2	4.6	5.2	V
$V_{3\ sat}$	Output Saturation Voltage	3	I_3 = 1mA		100	200	mV
R3	Input Pull-up Resistor	3		3.5	5	6.5	kΩ
T3/1	Composite Sync Extract Delay	3/1	At 50% of sync pulse amplitude		1	2	µs
IDENTIFICATION OUTPUT							
$V_{1\ ON}$	Min. Input Composite Sync Pulse Amplitude	1	Identification output going from no ident to ident		320	370	mV_{PP}
V_{1OFF}	Max. Input Composite Sync Pulse Amplitude	1	Identification output going from ident to no ident	150	210		mV_{PP}
HYS	Hysteresis	5	By attenuation of the input signal PIn 1		3.5		dB
V_{5H}	Identification Output Voltage	5	Video not identified	4.5	4.9	5.3	V
V_{5L}		5	Video identified, I_5 = 1mA		80	200	mV
R5	Internal Pull-up Resistor	5		3.5	4.8	6.5	kΩ
TI	Identification Delay	5/1	Delay between the first incoming inverted line pulse and ident output signal • C4 = 1µF • C4 = 470nF		 2 1	 3	 Frame Frame

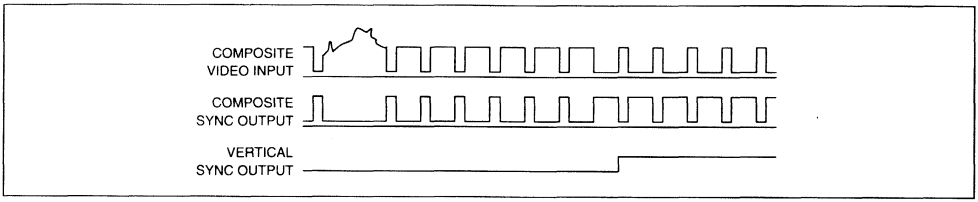
8128-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
V_{CC} = 12V, T_{amb} = 25°C,
Video Signal : standard PAL color bar generator (V_I = $2V_{PP}$) (unless otherwise specified)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
VERTICAL PULSE OUTPUT							
$V_{1\ min}$	Min. Input Composite Sync Pulse Amplitude	1	Stable output pulse (Pin 6) Input pulse increasing		300	350	mV_{PP}
TFR	Vertical Pulse Width	6	Standard PAL color bar pattern ($2V_{PP}$)	100	250	400	µs
V_{6H}	Vertical Pulse Amplitude	6		4.5	4.9	5.3	V
$V_{6\ sat}$	Output Saturation Voltage	6	I_6 = 1mA		100	200	mV
R6	Internal Pull-up Resistor	6		3.5	5	6.5	kΩ
TDFR	Vertical Pulse Delay	6/1	Delay between the first incoming inverted line pulse (Pin 1) and vertical pulse at 50% amplitude		1	2	µs

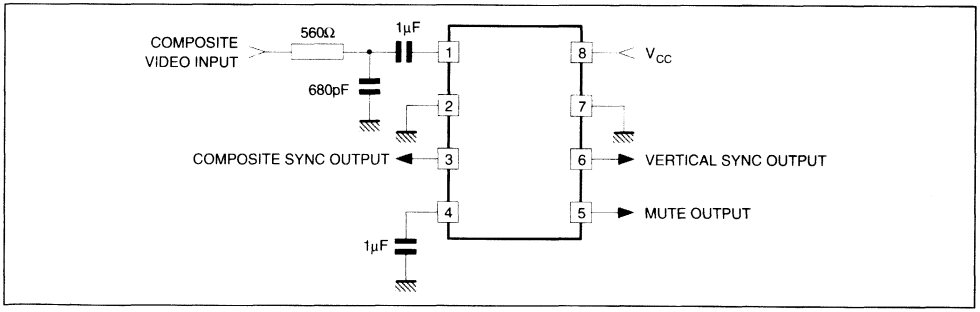
8128-04.TBL

WAVEFORMS (Pin 7 grounded)



8128-03.EPS

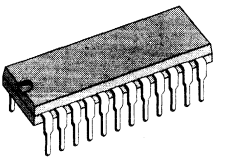
TYPICAL APPLICATION



8128-04.EPS

HORIZONTAL AND VERTICAL PROCESSOR

- 503kHz REFERENCE OSCILLATOR
- 5.5V SUPPLY VOLTAGE INTERNALLY REGULATED
- VERY SOPHISTICATED SYNC. SEPARATOR
- COUNT DOWN TIMING LOGIC
- ADAPTS AUTOMATICALLY TO 625 LINE/50Hz AND 525 LINE/60Hz STANDARDS
- 50/60 Hz IDENTIFICATION OUTPUT
- AUTOMATIC VERTICAL AMPLITUDE CORRECTION 50/60Hz
- CRT PROTECTION CIRCUIT
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY CYCLE



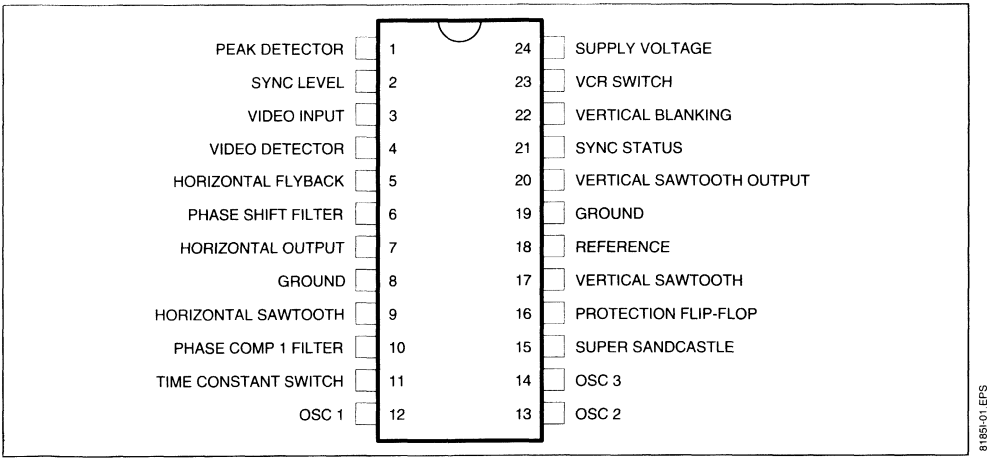
DIP24
(Plastic Package)

ORDER CODE : TDA8185I

DESCRIPTION

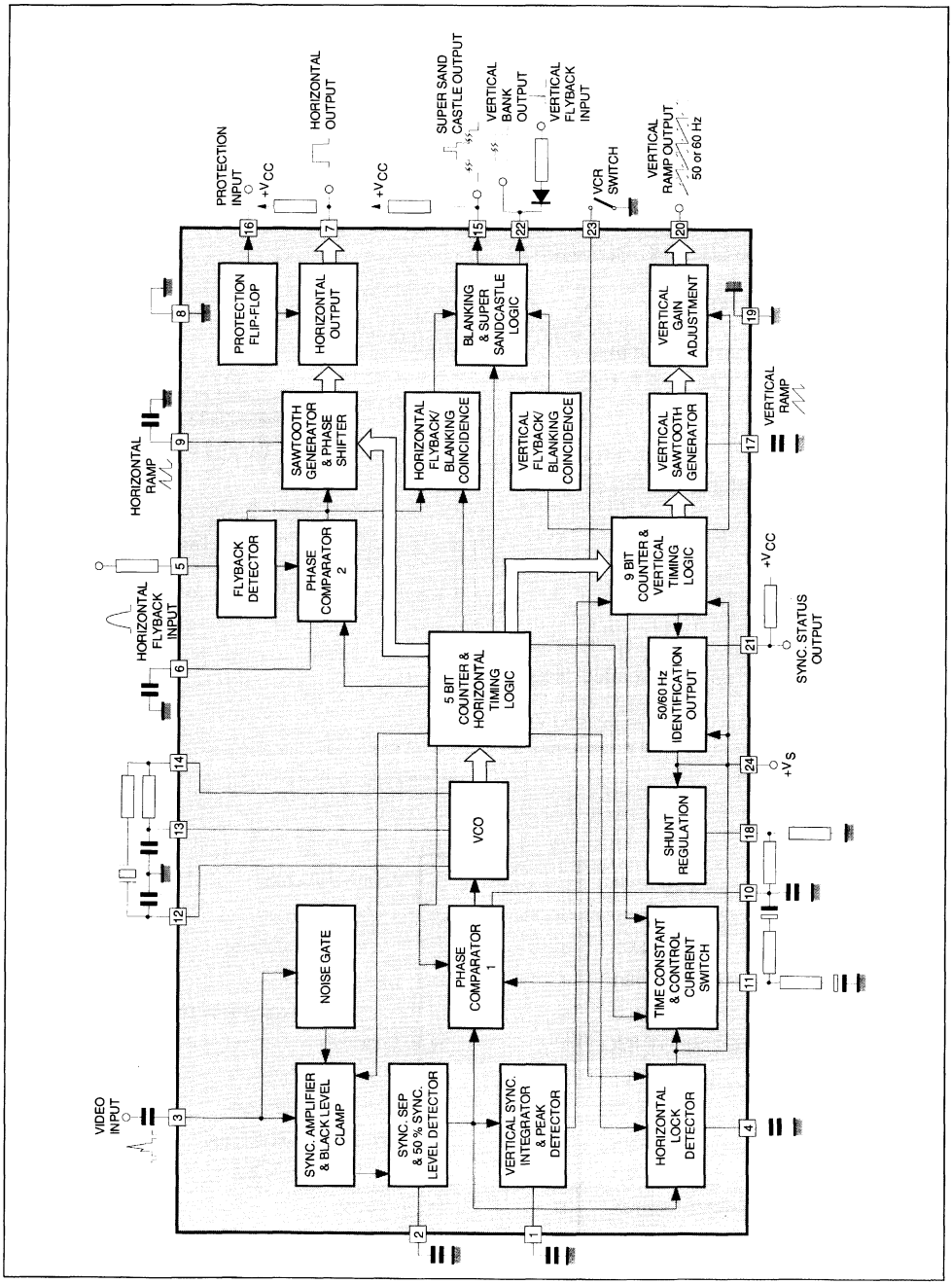
The TDA8185I is a monolithic integrated circuit in 24 pins dual in line plastic package intended for TV signal processing and driving Horizontal and Vertical output stages. It was specially designed for VCR working conditions.

PIN CONNECTIONS



8185I-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 24 (low impedance)	5.25	V
V_{CC}	Voltage at Pins, 7, 15, 21	20	V
V_I	Input Signals	5	V
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	1	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

8185I-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	80	°C

8185I-02.TBL

ELECTRICAL CHARACTERISTICS

(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 24)		4.75	5	5.25	V
I_s	Supply Current (pin 24)		30	60	85	mA
V_{24}	Stabilized Voltage at Pin 24			5.6		V
SYNC. SEPARATOR						
V_3	Peak to Peak Input Signal (negative video signal)		0.3	1	4	V
VIDEO IDENTIFICATION AND VCR SWITCH						
V_{23}	VCR Switch Voltage		1.6	2.1	2.4	V
V_4	Threshold Voltage for Time Constant Switching			2.3		V
I_4	Peak Output Current	Lock		1		mA
$-I_4$	Output Current			20		µA
OSCILLATOR						
F_O	Free Running Frequency			500		kHz
S_O	Frequency Control Sensitivity			1.0		kHz/V
V_{10}	Control Voltage Range			2.6 to 4		V
SYNC–OSCILLATOR PHASE COMPARATOR						
I_{10}	Control Peak Curent			± 0.3		mA
I_{10}	VCR Control Peak Current			± 0.6		mA
Δf	Catching and Holding Range			± 400		Hz
FLYBACK – OSCILLATOR PHASE COMPARATOR						
V_6	Control Voltage Range			2.8 to 3.7		V
I_5	Flyback Input Current		0.1			
	Flyback Input Threshold			5		mA
I_6	Peak Control Current			± 0.5		mA
	Static Control Error			1		%
t_d	Permissible Delay between Output Pulse and Flyback Pulse	$t_{flyback}$ = 12 µs		17		µs

8185I-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

(V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
COMPOSITE BLANKING AND KEY PULSE (supersandcastle)						
V_K	Key Pulse Output Peak Voltage			10		V
V_L	Line Blanking Voltage		4.25	4.5	4.75	V
V_F	Frame Blanking Voltage		2.38	2.5	2.63	V
t_{KS}	Phase Relationship between Leading Edge of Key Pulse and Middle of Sync. Pulse			2.5		µs
t_K	Key Pulse Duration			4		µs
t_F	Vertical Blanking Duration			1.4		ms
FRAME						
V_{20}	Output p.p. Sawtooth Voltage	50Hz and 60Hz		2.7		V
V_{20}	Pedestal Voltage			0.3		V
LINE						
I_7	Output Current			50		mA
V_7	Saturation Voltage	I_7 = 50mA		0.4		V
t_L	Output Pulse Duration			29		µs
SYNC. STATUS OUTPUT						
V_{21}	Output Voltage	50Hz 60Hz Unlock	6.25	12 7	7.45 0.3	V V V
OVERALL PHASE RELATION SHIP						
t_O	Phase Difference between Middle of Flyback and Middle of Sync. Pulses			2		µs
VERTICAL BLANKING OUT AND FLY. INPUT						
V_{22}	Blanking Output Voltage			4		V
V_{22}	Flyback Threshold Input			5.7		V
I_{22}	Flyback Current Input		0.1			mA

8185I-04.TBL

Notes : 1. With t_{fly} = 12 µs and t_l = 29 µs.
2. The TDA8185I may be operated on a 5V supply directly. A 5.5 V shunt regulator is available internally for operation on higher supply voltage ; in this case an external limiting resistor is required.
Without the external limiting resistor care must be taken to ensure that the supply voltage does not exceed 5.5V or the regulator will intervene and the device could be damaged.

Figure 1 : Horizontal and Vertical Deflections for 30AX C.R.T.

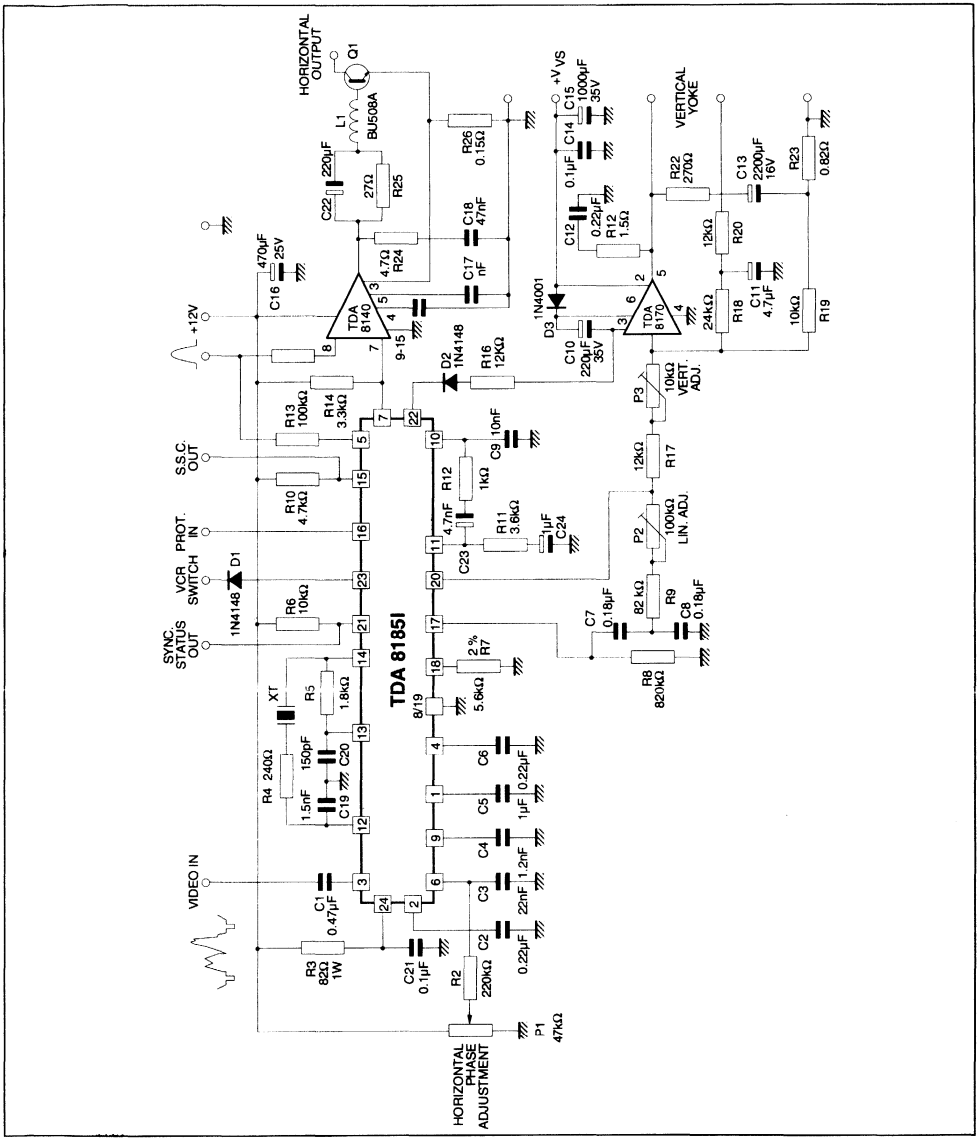


Figure 2 : Horizontal and Vertical Deflections for S4 C.R.T.

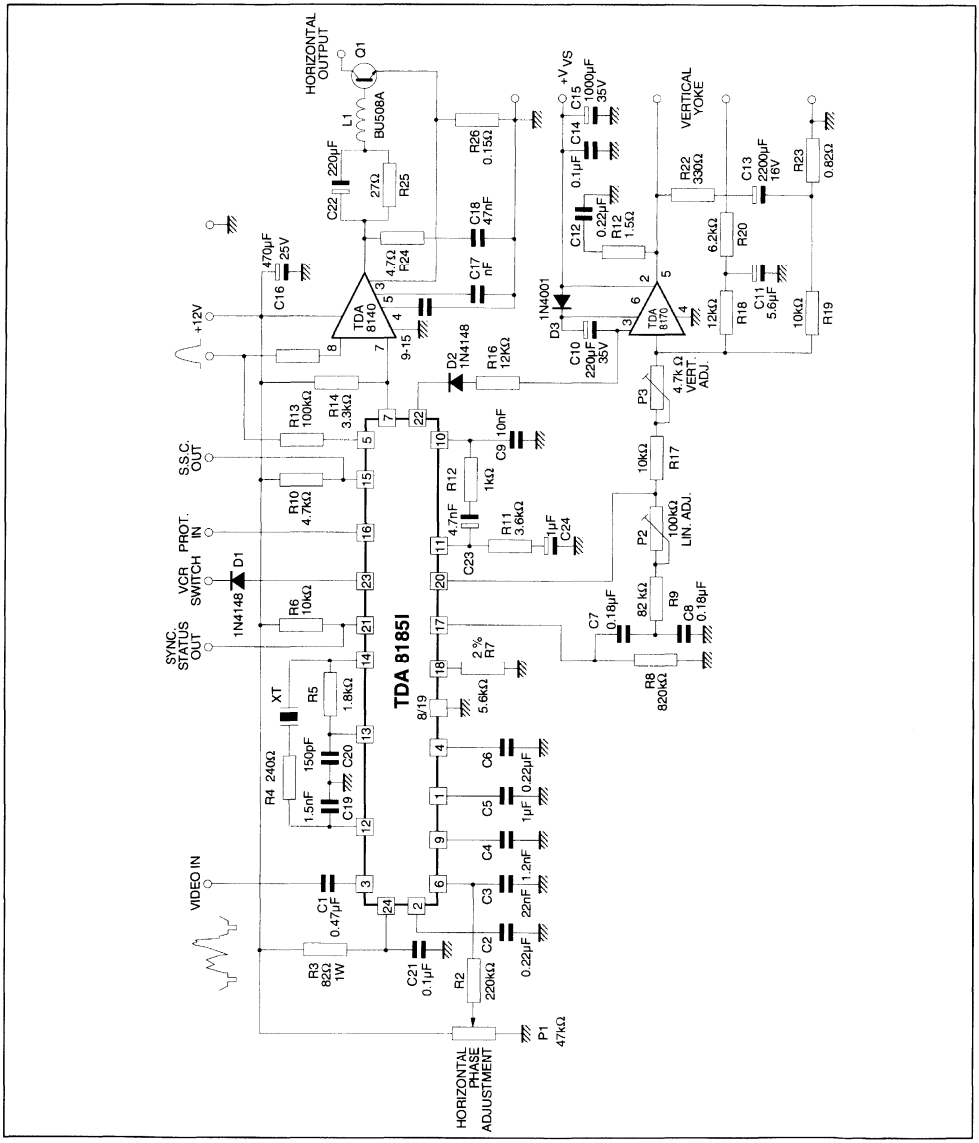
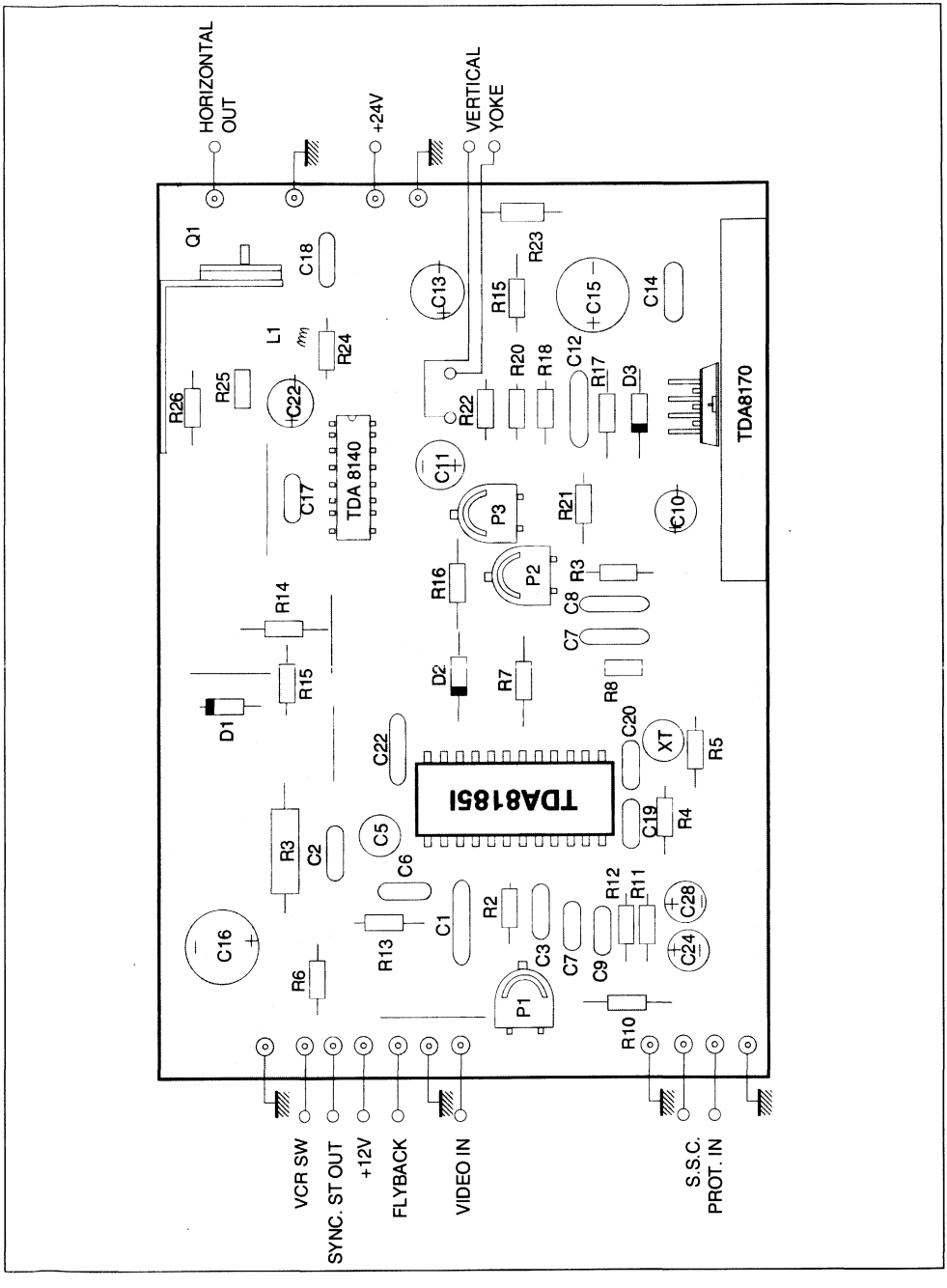


Figure 3 : P.C. Board and Components Layout of the Circuit of Figure 2 (1 : 1 scale)

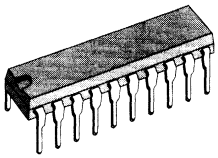


SGS-THOMSON MICROELECTRONICS

TDA8214B

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



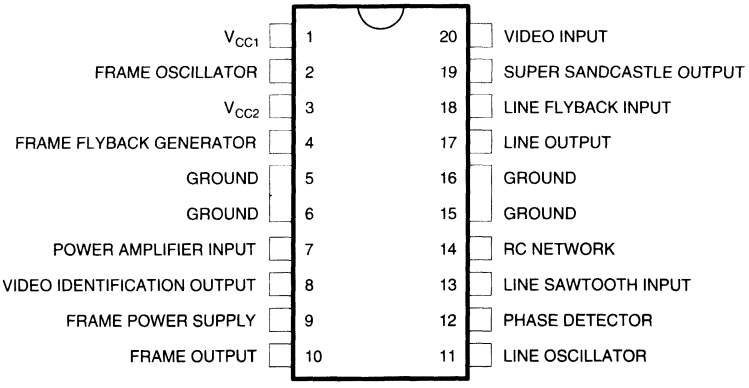
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8214B

DESCRIPTION

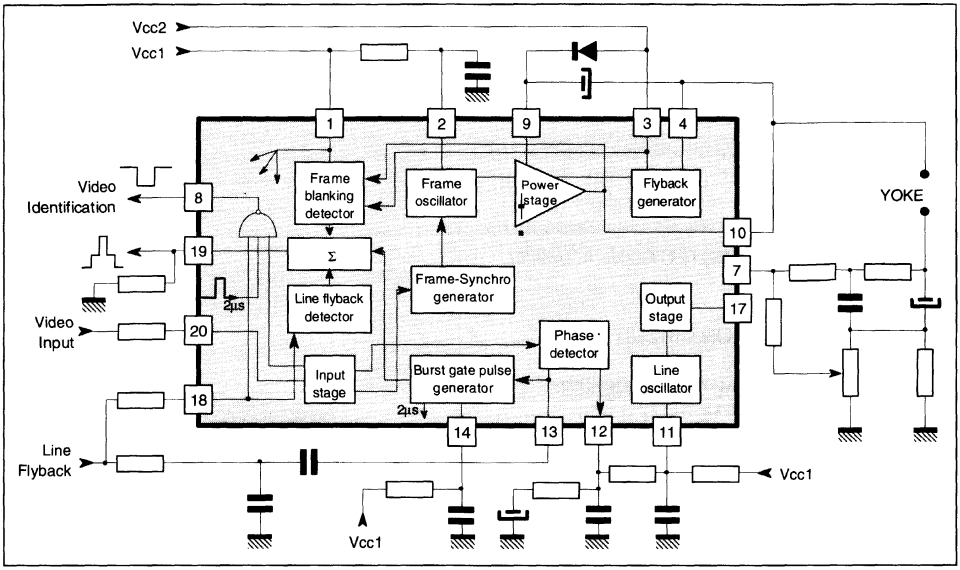
The TDA8214B is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



8214B-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

8214B-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

8214B-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output, Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 200mA)		1.1	1.6	V
OPW	Output Pulse width (line period = 64µs)	27	29	31	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control RangeVoltage	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line syn. tip is centered in the line retrace				
V_{H8}	Without video signal (I_8 = -500µA)	4.5	6.3		V
V_{L8}	With video signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

82148-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
V_{CC2}	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Voltage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V V4/3 with				
F2DA	$I_{4 \rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V V3/4 with				
FSVA	$I_{3 \rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

8214B-04.TBL

Notes : 1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is V_{CC2} - $2V_{BE}$ and the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
2. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

GENERAL DESCRIPTION

The TDA8214B performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:

- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line driver
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

The slice level of sync-separation is fixed by value of the external resistors R1 and R2. V_R is an internally fixed voltage.

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 1 : Synchronization Separator Circuit

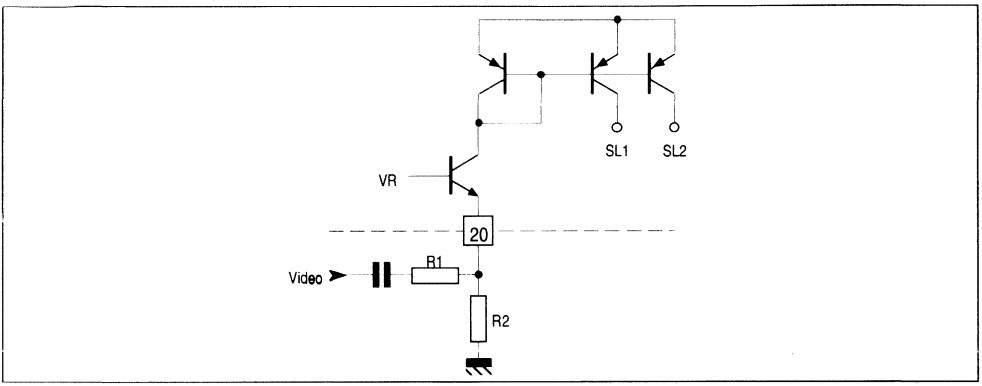


Figure 2 : Frame Separator

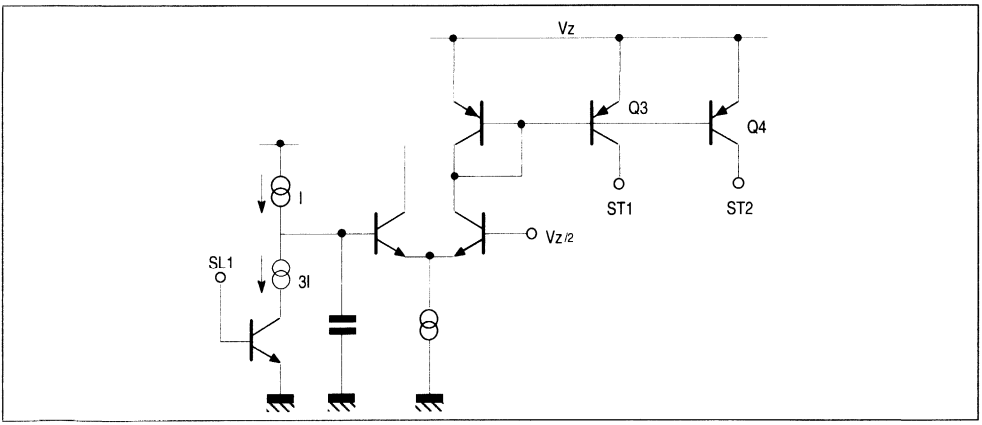
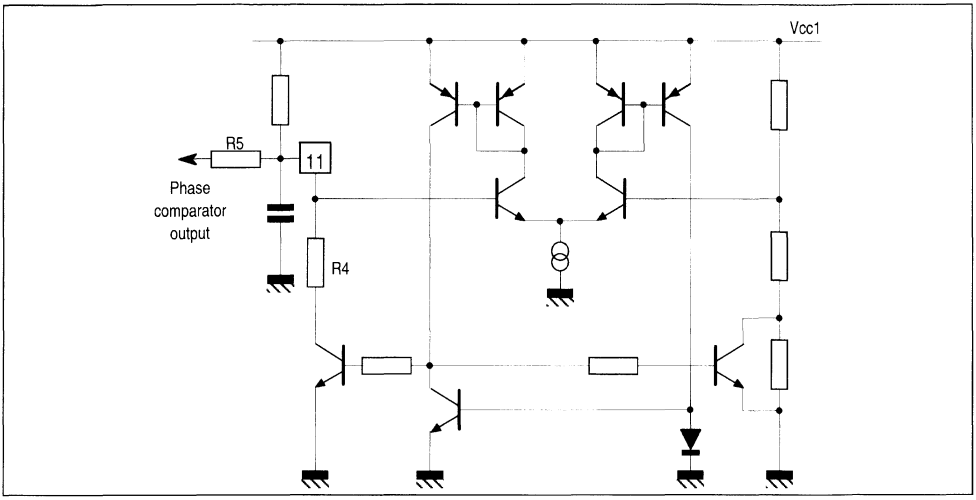
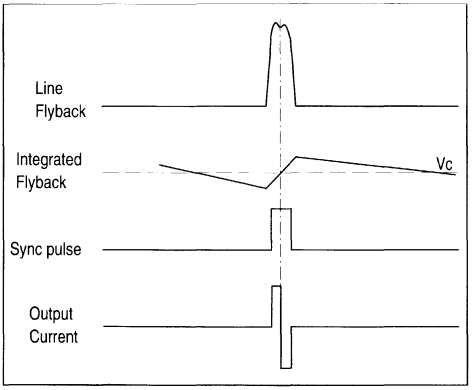


Figure 3 : Line Oscillator



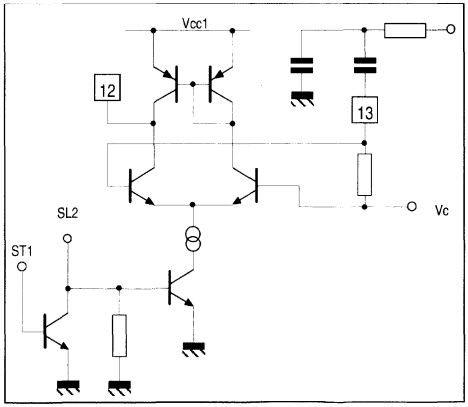
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4 : Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

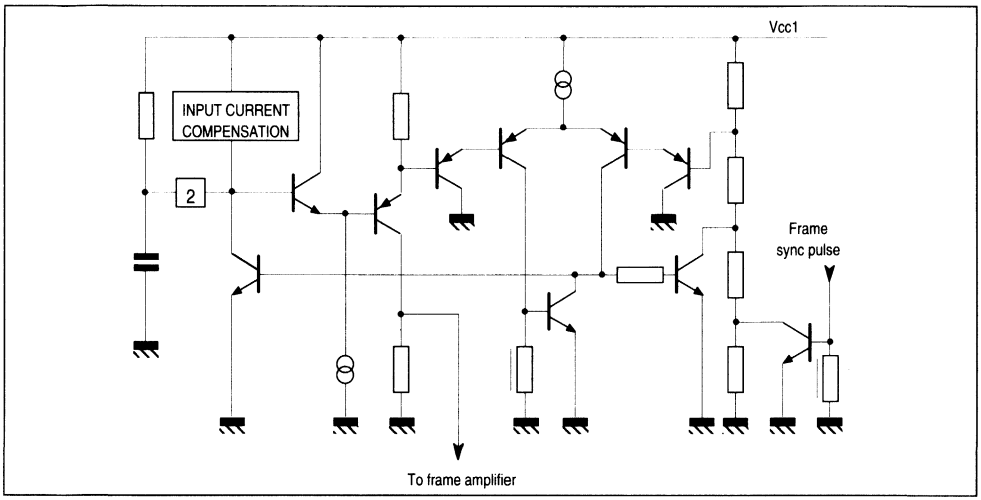
Figure 5



Line output (Pin 17)

It is an open-collector output. The output positive pulse time is 29µs for a 64µs period.
The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Figure 6 : Frame Oscillator



Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2\text{-}2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (Pin 14). It is referenced to the middle of the line flyback.

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be $2V_{PP}$ (typ. : $2.5V_{PP}$).

Figure 7 : Super Sandcastle Generator

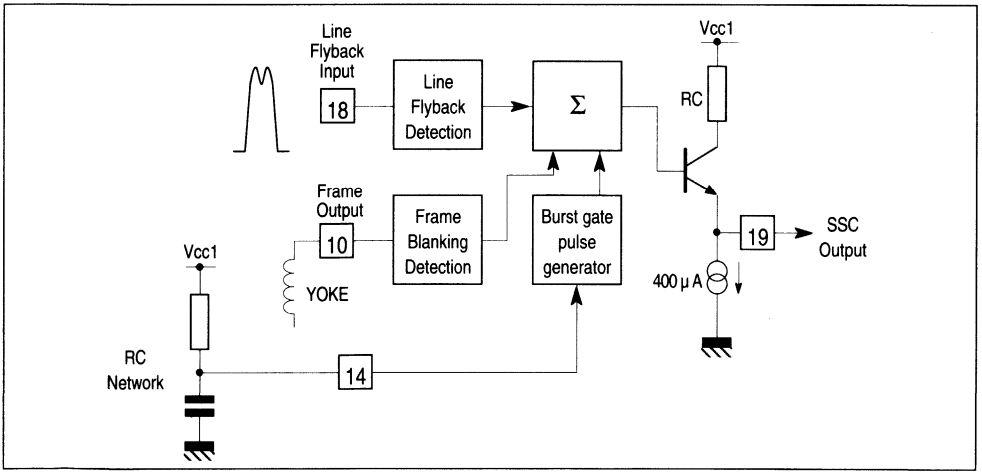
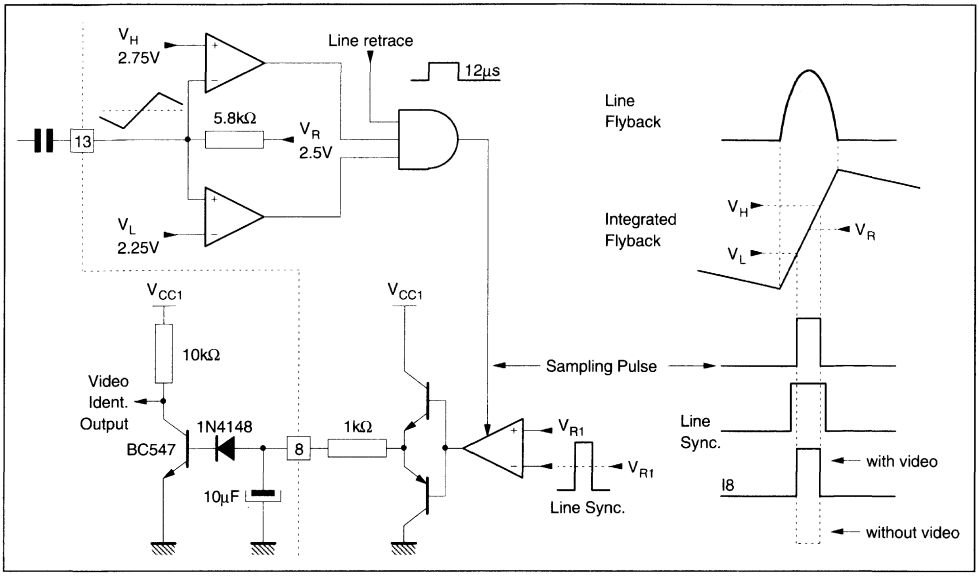
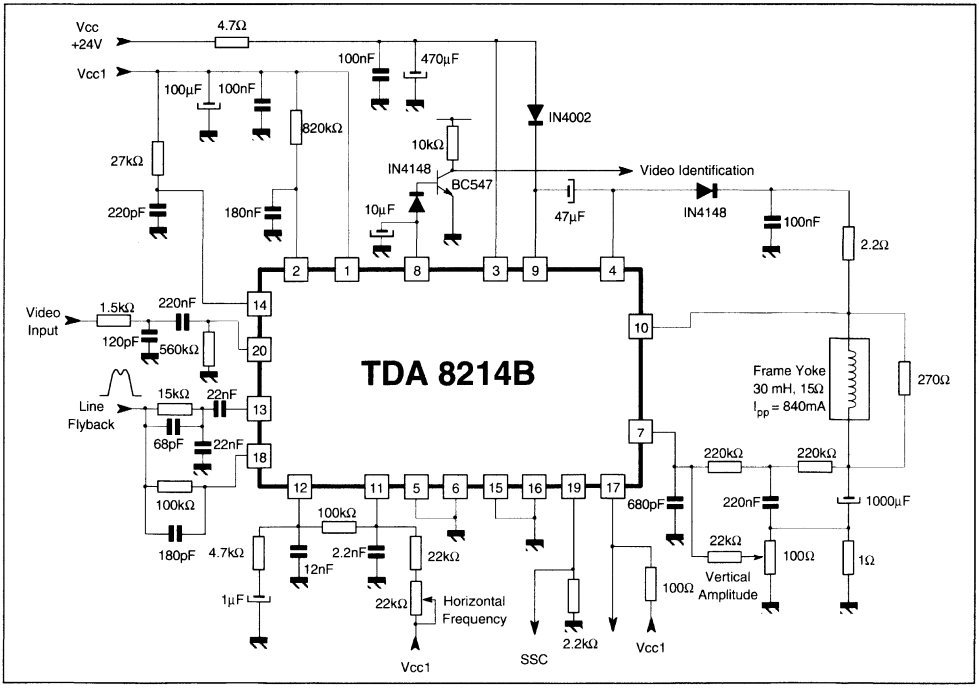


Figure 8 : Video Identification Circuit (Pin 8)



TYPICAL APPLICATION

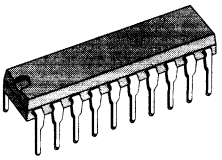


SGS-THOMSON MICROELECTRONICS

TDA8215B

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



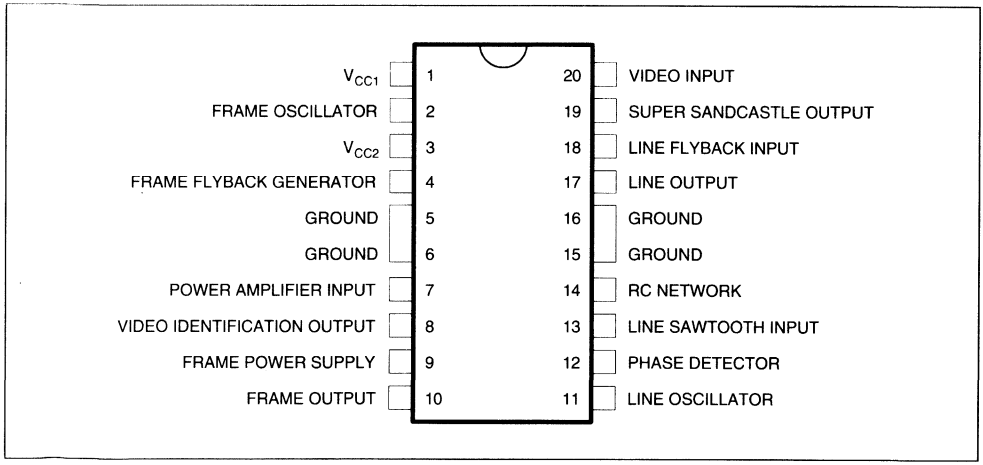
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8215B

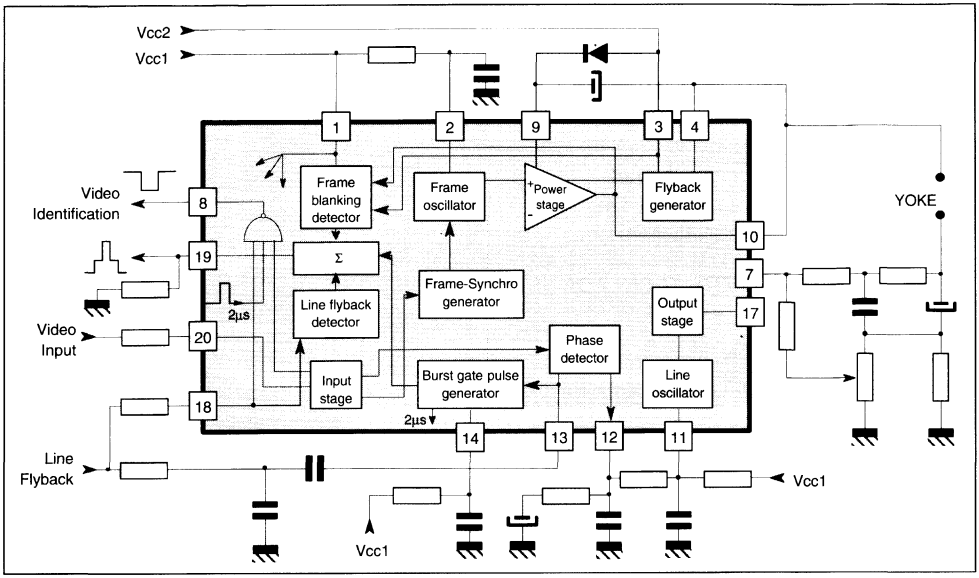
DESCRIPTION

The TDA8215B is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications. The TDA8215B has been specially designed for direct drive of line DARLINGTON transistors.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

8215B-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

8215B-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I_{20} = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 800mA during 2µs)		2.2		V
OPW	Output Pulse width (line period = 64µs , negative pulse)	19	21	23	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control Voltage Range	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line synchro tip is centered in the line retrace				
V_{H8}	without Video Signal (I_8 = -500µA)	4.5	6.3	0.9	V
V_{L8}	with Video Signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I_{20} = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

8215B-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
V_{CC2}	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Votage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4\rightarrow3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4\rightarrow3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3\rightarrow4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3\rightarrow4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

8215B-04.TBL

Notes : 1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is V_{CC2} - $2V_{BE}$ and the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
2. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

GENERAL DESCRIPTION

The TDA8215B performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

The slice level of sync-separation is fixed by value of the external resistors R1 and R2. VR is an internally fixed voltage.

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 1 : Synchronization Separator Circuit

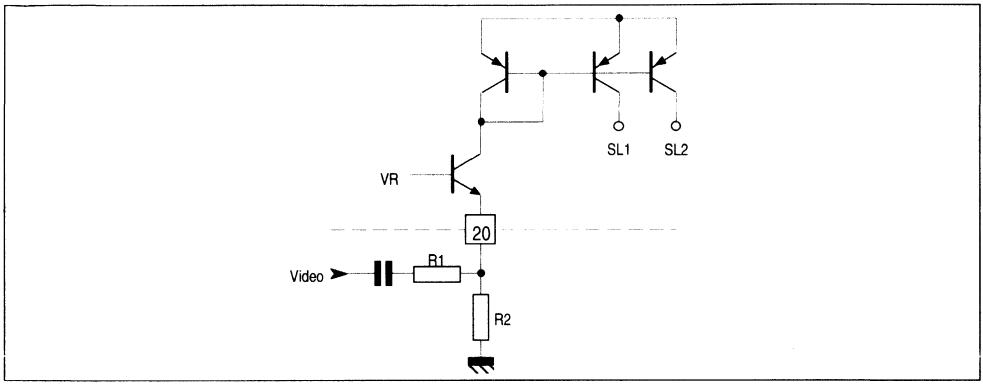


Figure 2 : Frame Separator

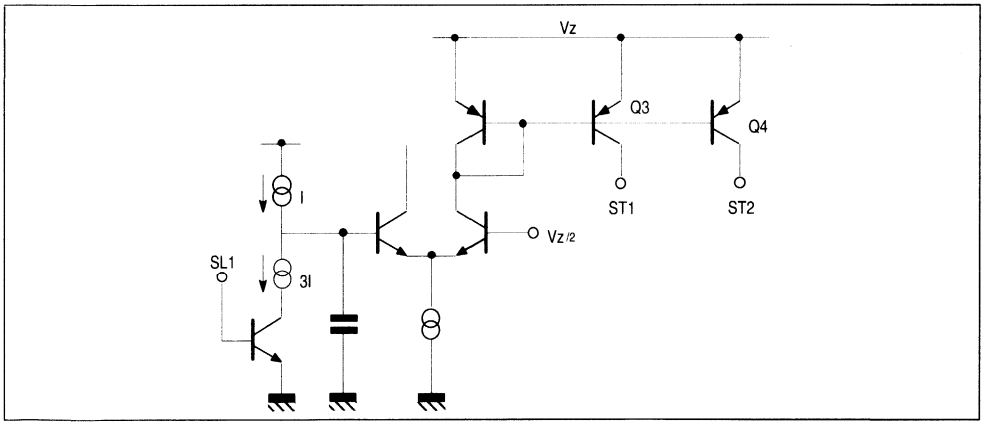
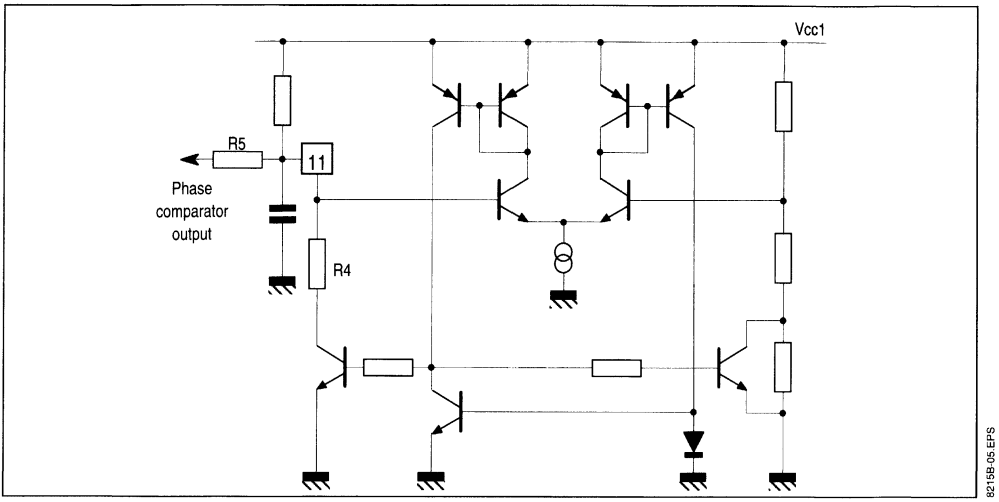
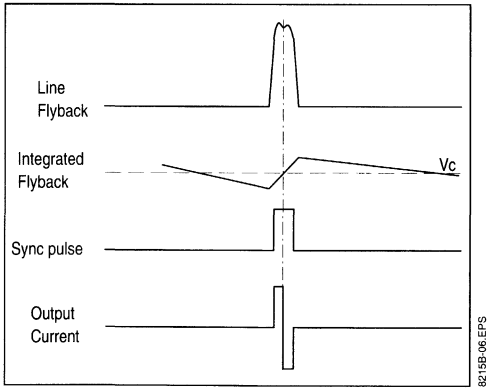


Figure 3 : Line Oscillator



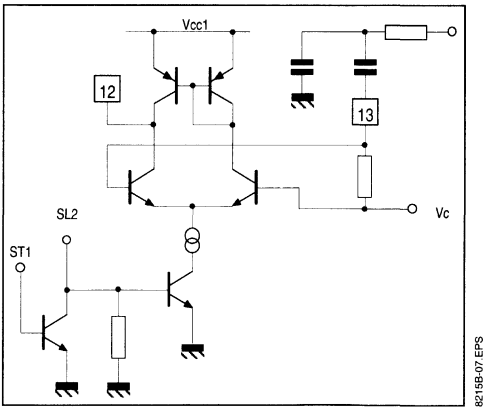
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4 : Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

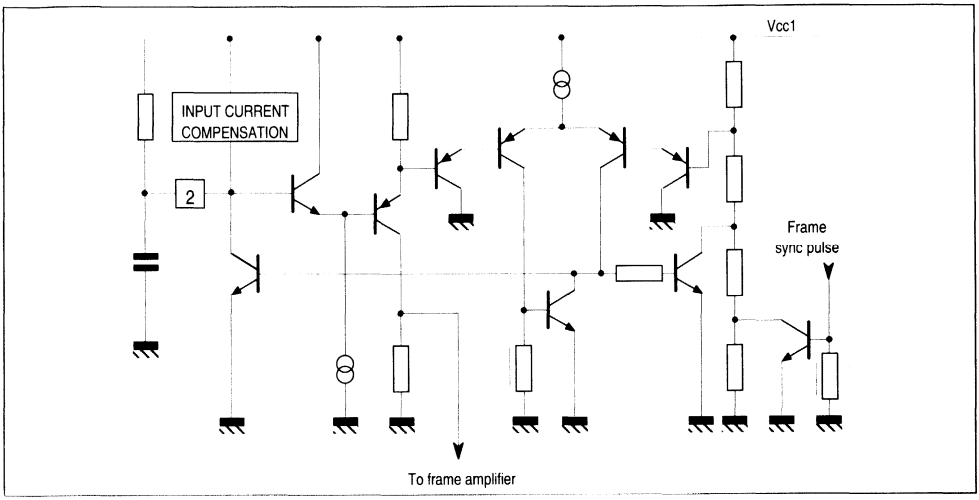
Figure 5



Line output (Pin 17)

It is an open-collector output. The output negative pulse time is 22µs for a 64µs period.
The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Figure 6 : Frame Oscillator



Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2\text{-}2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (Pin 14). It is referenced to the middle of the line flyback.

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be $2V_{PP}$ (typ. : $2.5V_{PP}$).

Figure 7 : Super Sandcastle Generator

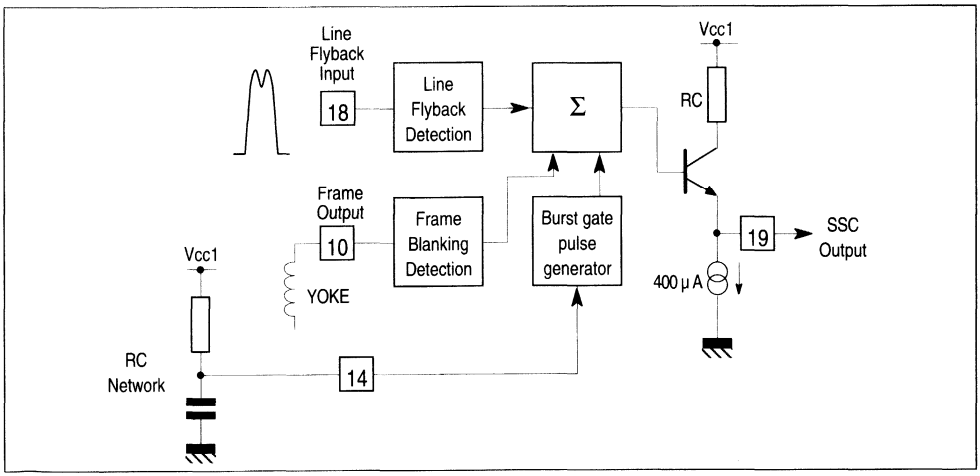
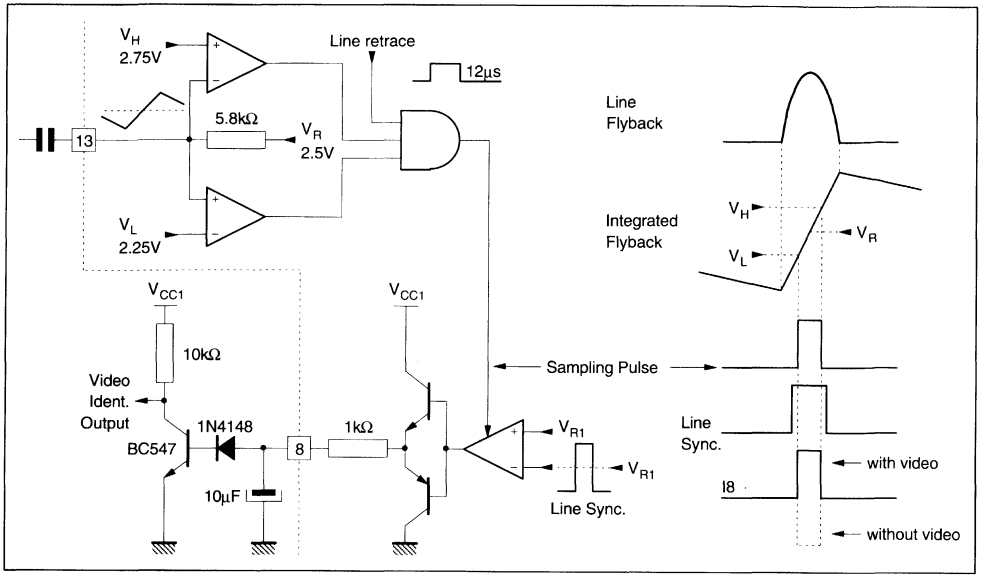
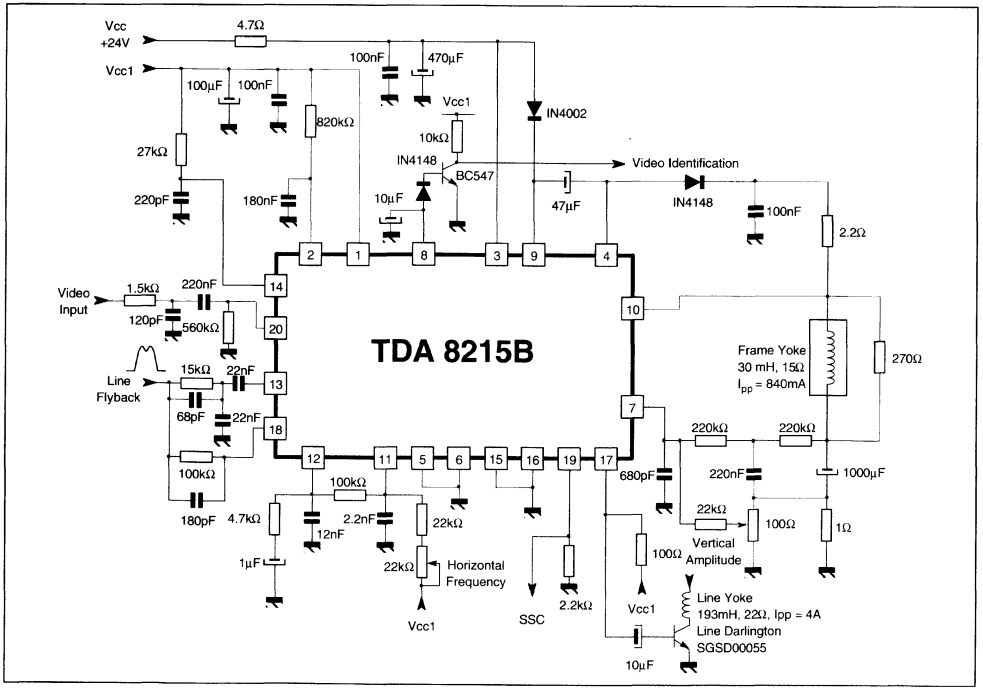


Figure 8 : Video Identification Circuit (Pin 8)

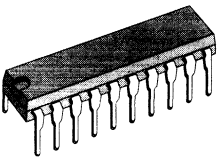


TYPICAL APPLICATION



HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE
- STABLE FRAME BLANKING PULSE, GENERATED BY EXTERNAL RC, FOR COMPATIBILITY WITH TEA 5640



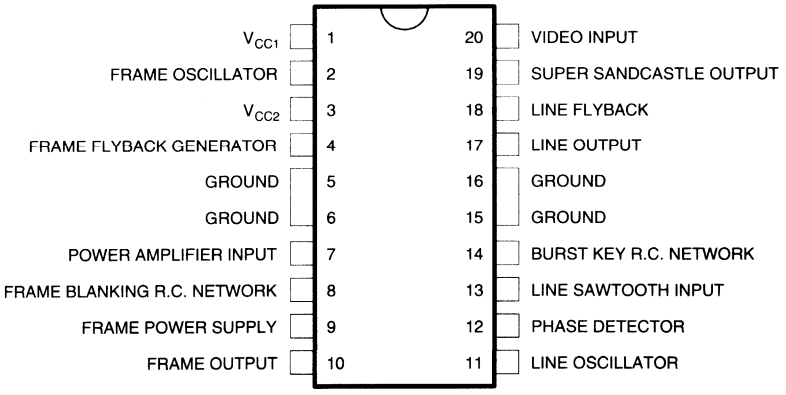
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8218

DESCRIPTION

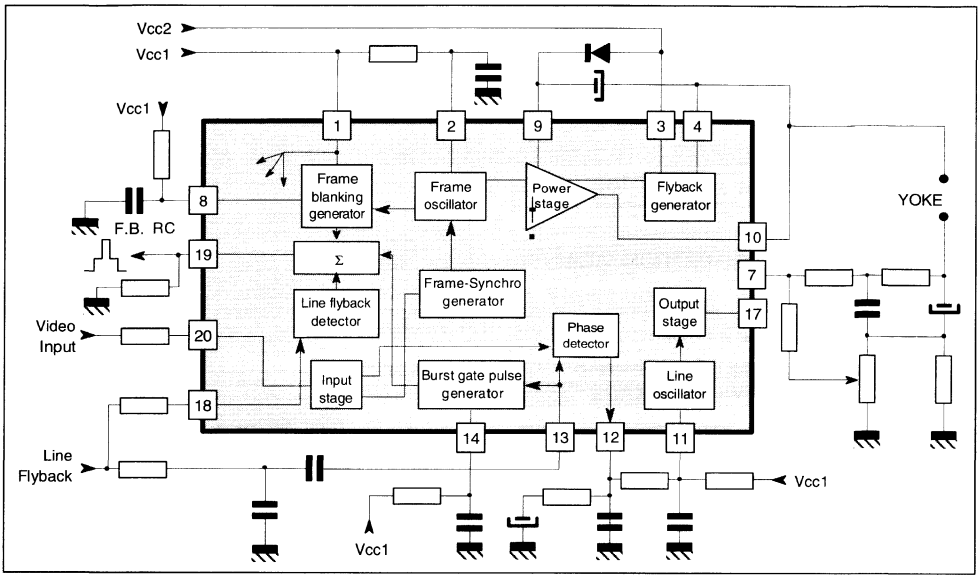
The TDA8218 is an horizontal and vertical deflection circuit with super sandcastle generator. Used with automatic PAL/SECAM decoder TEA5640, this IC permits a complete low-cost solution for PAL/SECAM applications.

PIN CONNECTIONS



8218-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

8218-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

8218-02.TBL

ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15	22	mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I20 = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (when synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 200mA)		1.1	1.6	V
OPW	Output Pulse width (line period = 64µs)	26	28	30	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control RangeVoltage	2.60		7.10	V
FRAME BLANKING GENERATOR (Pin 8)					
	External R.C. Network (Typical values : R = 100kΩ, C = 22nF)				
T_{fb}	Blanking Time (PIn 19, T_{fb} = K8 .R.C.)		1.35		ms
K8	Time Blanking Coefficient	0.588	0.613	0.644	
I_{O8}	Output Current during the Frame Blanking : V_8 = 2V		- 0.2	1	µA
I_{I8}	Input Current after the Frame Blanking : V_8 = 7V	300	450	600	µA
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 866kΩ Tied to V_{CC1}, C = 220nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I20 = -100µA) with the Same RC		12.8		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	

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ELECTRICAL CHARACTERISTICS

V_{CC1} = 10 V, T_{AMB} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME OSCILLATOR (Pin 2) (continued)					
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		9	15	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
$V_{CC}2$	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Voltage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4\rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4\rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3\rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3\rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width : Defined by external R.C. Pin 8	3.7	4	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 1) for the burst key pulse		6		µS

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Note : 1. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

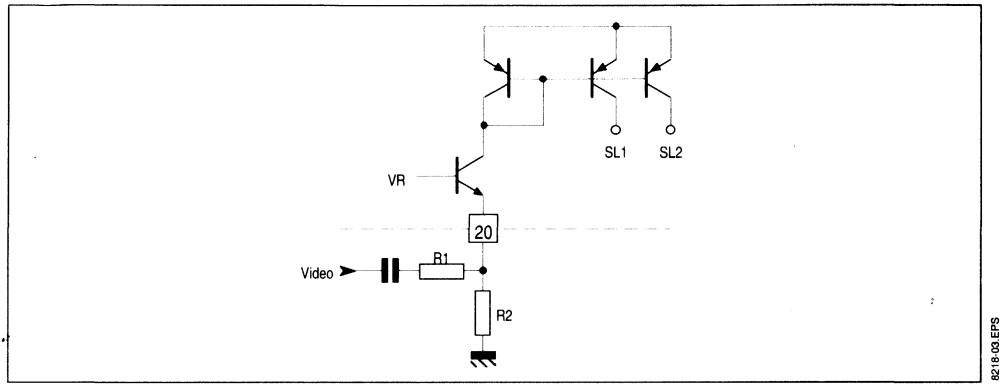
GENERAL DESCRIPTION

The TDA8218 performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:

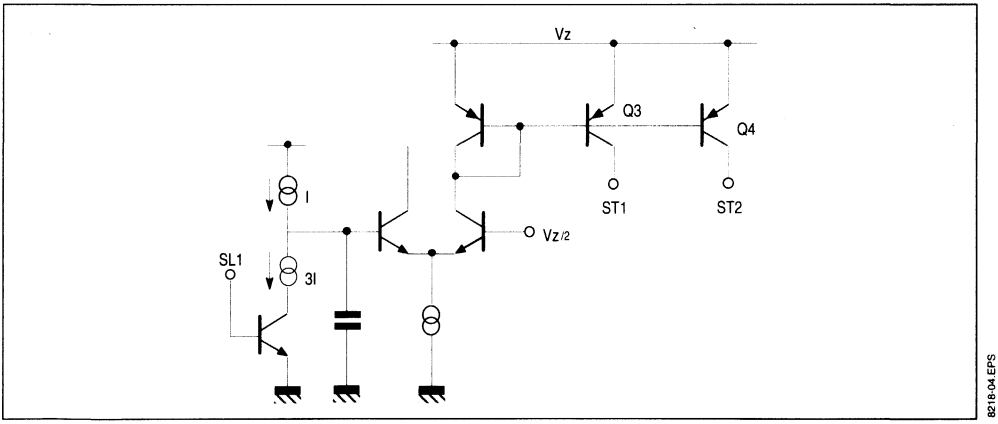
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line driver
- A line phase detector and a voltage control oscillator
- A super sandcastle generator.

Figure 1 : Synchronization Separator Circuit



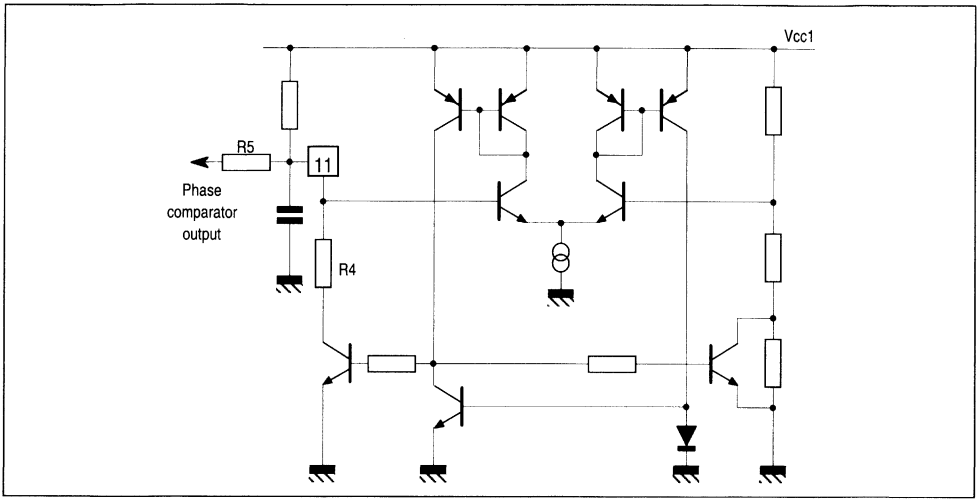
The slice level of sync-separation is fixed by value of the external resistors R1 and R2. V_R is an internally fixed voltage.

Figure 2 : Frame Separator



The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 3 : Line Oscillator



The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.
The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

Figure 4 : Phase Comparator

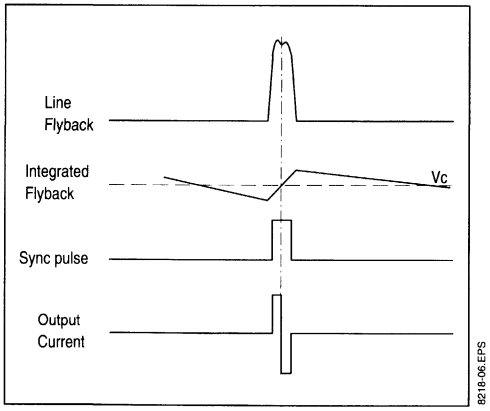
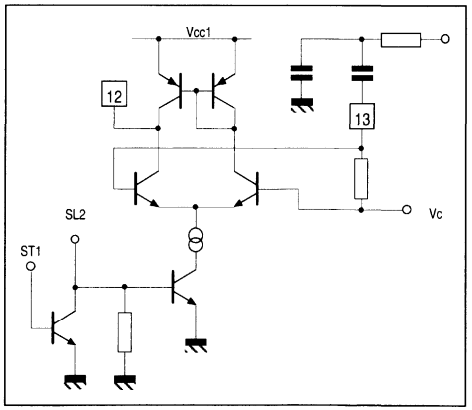


Figure 5



Line output (Pin 17)

It is an open-collector output. The output positive pulse time is 28µs for a 64µs period. The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (pin 14). It is referenced to the middle of the line flyback.

The frame blanking generator is a monostable with external R.C. The start blanking pulse is triggered by the falling edge of the frame saw-tooth (Pin 2). The reset is provided by a comparator which compares the capacitor voltage during its charge to an internal threshold fixed by resistors.

The frame blanking time is defined by :

$$T_{fb} = 0.613 \cdot R.C.$$

This pulse is available on Super Sand Castle output (Pin 19).

Remark : For compatability with TEA5640, frame blanking time must be larger than 1.15ms with centered value @ 1.35ms (R = 100kΩ ± 1%, C = 22nF ± 5%)

Figure 6 : Frame Oscillator

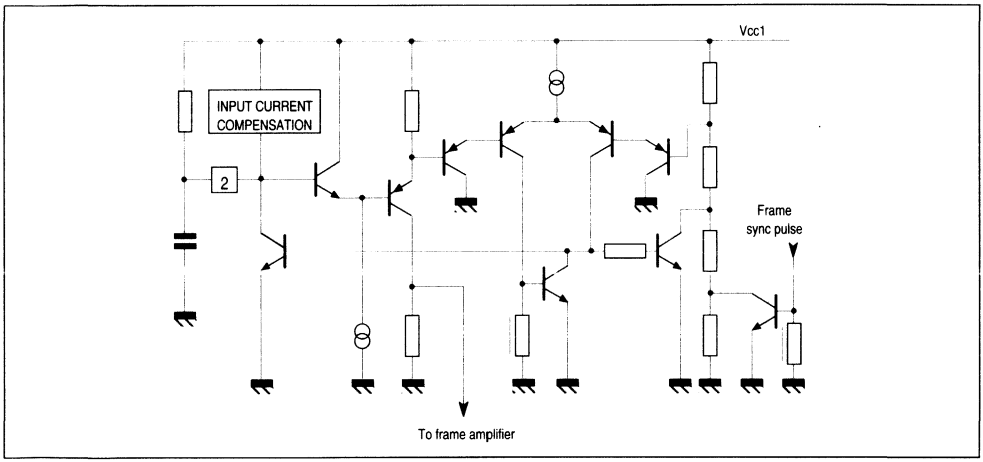
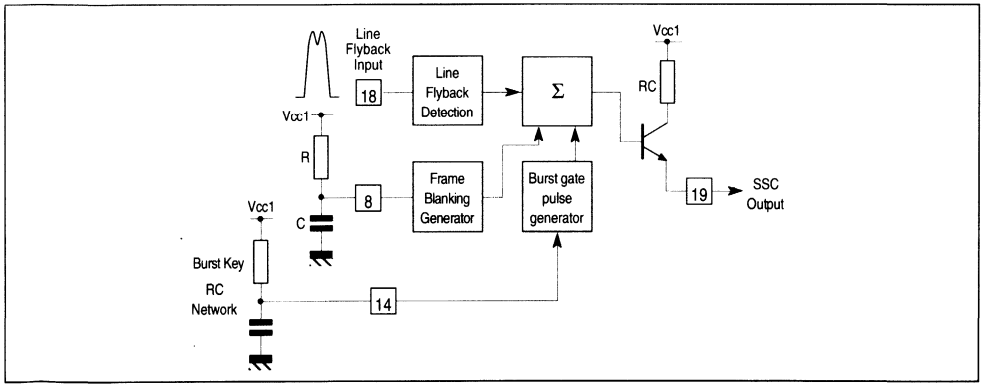
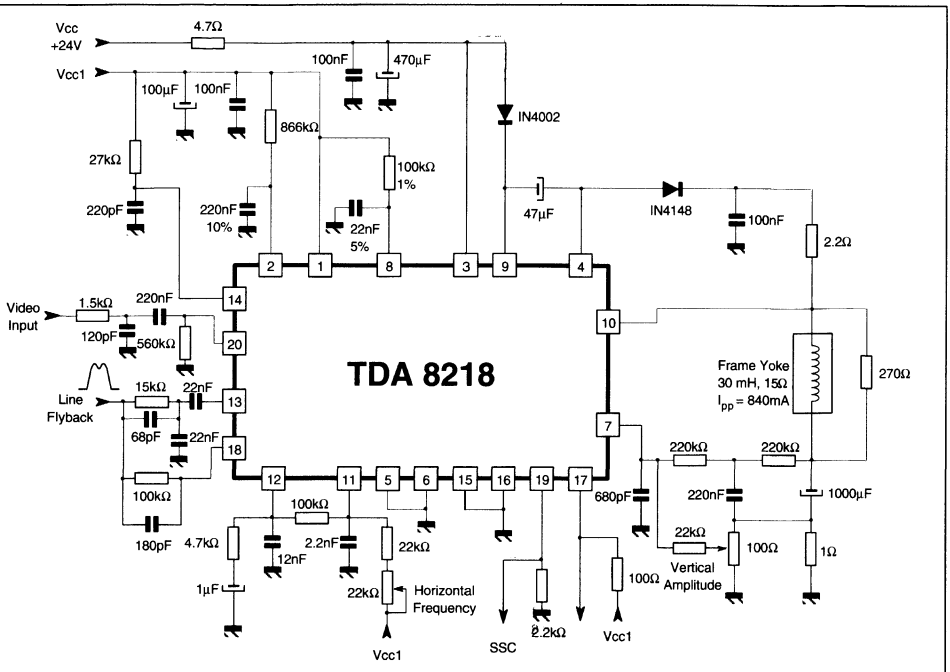


Figure 7 : Super sandcastle generator



TYPICAL APPLICATION



Note : Pins 5 - 6 : Frame oscillator ground
Pins 15 - 16 : Frame and line power ground

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TDA9102C

H/V PROCESSOR FOR TTL V.D.U

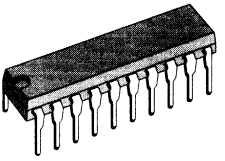
PRELIMINARY DATA

HORIZONTAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 15kHz to 100kHz
- HORIZONTAL OUTPUT PULSE SHAPER AND SHIFTER
- PHASE COMPARATOR BETWEEN SYNCHRO AND OSCILLATOR (PLL1)
- PHASE COMPARATOR BETWEEN FLYBACK AND OSCILLATOR (PLL2)
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR PHASE AND FREQUENCY
- HORIZONTAL OUTPUT DUTY CYCLE : 41%

VERTICAL SECTION

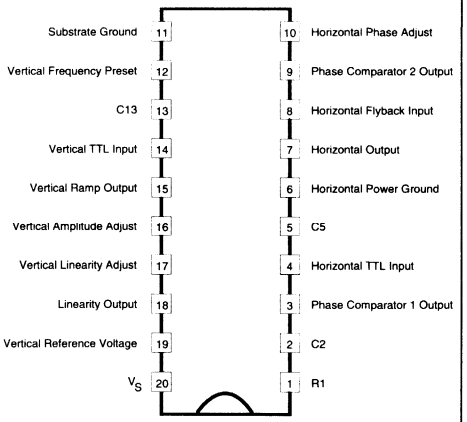
- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 30Hz to 120Hz
- RAMP GENERATOR WITH VARIABLE GAIN STAGE
- VERTICAL RAMP VOLTAGE REFERENCE
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR FREQUENCY, AMPLITUDE AND LINEARITY



DIP20
(Plastic package)

ORDER CODES : TDA9102C

PIN CONNECTIONS



9102001.EPS

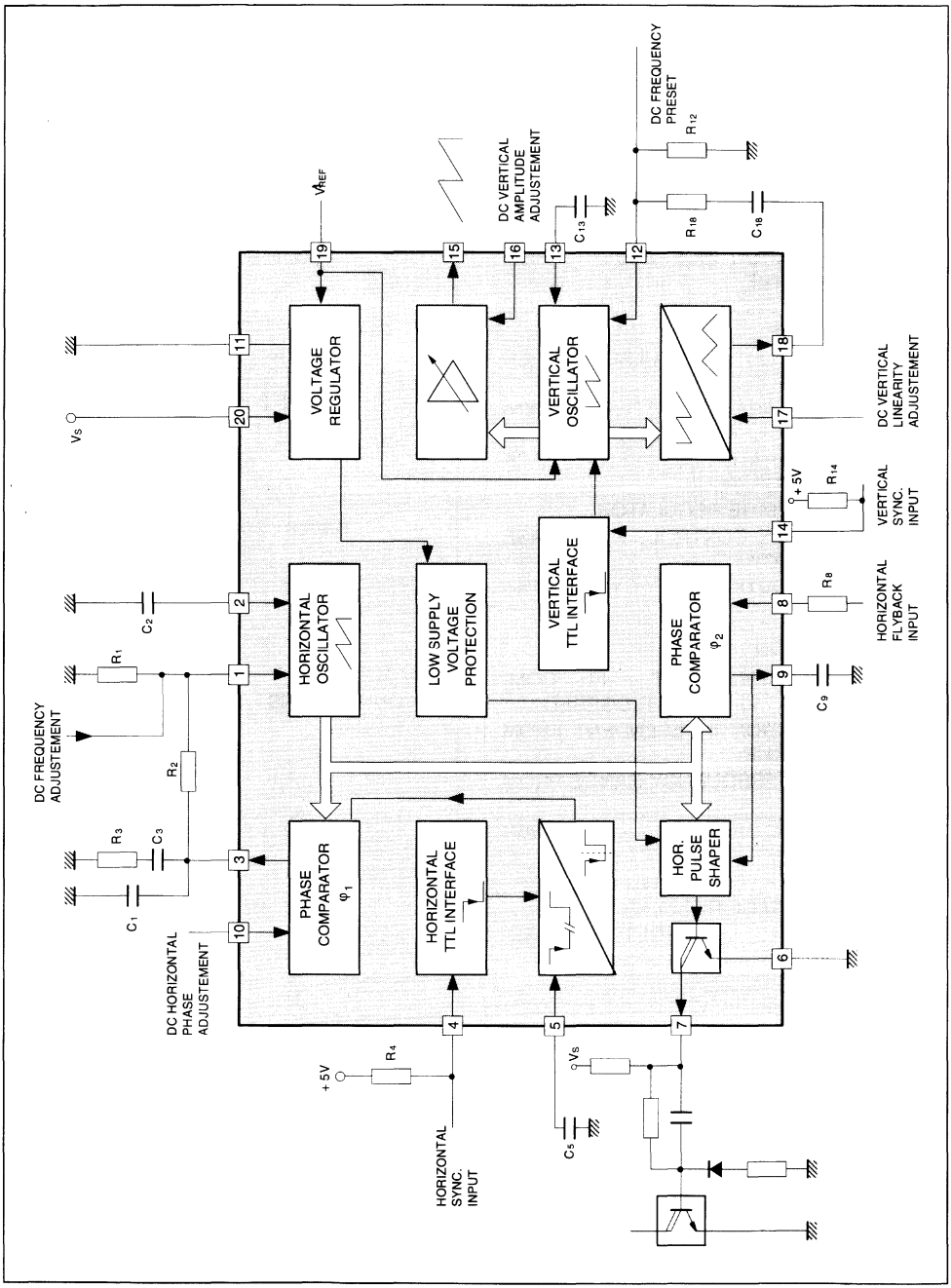
DESCRIPTION

The TDA9102C is a monolithic integrated circuit for horizontal and vertical sync processing in monochrome and color video displays driven by input TTL compatible signals.

The TDA9102C is supplied in a 20 pin dual in line package with pin 11 connected to ground and used for heatsinking.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	18	V
V_{SYNC}	Sync Input Peak Voltage	+ V_S	V
I_{OH}	Output Sinking Peak Current (Pin 7 ; t < 3µs)	2	A
I_{15}	Output Current (Pin 15)	- 10	mA
I_{19}	Output Current (Pin 19)	- 10	mA
P_{TOT}	Total power dissipation • T_{amb} < 70°C • T_{pin} < 90°C	 1.4 1.5	 W W
T_{STG} , T_J	Storage and Junction Temperature	- 40 to 150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(J-C)}$	Junction-case Thermal Resistance	40	°C/W
$R_{TH(J-A)}$	Junction-ambient Thermal Resistance	55	°C/W

9102002.TBL

ELECTRICAL CHARACTERISTICS

(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SECTION						
V_S	Supply Voltage Range		10.5	12	15.5	V
I_S	Supply Current			40	70	mA
V_1	Voltage Reference at Pin 1	I_1 = 0.5mA	3.2	3.5	3.8	V
I_1	Current at Pin 1		- 1			mA
V_2	Voltage Swing at Pin 2		3.7	4	4.3	V_{PP}
K_0	Free Running Frequency Constant	$f_o = 1/(K_0 \times R1 \times C2)$	2.8	3.04	3.2	
$\lvert V_3 - V_1 \rvert$	Control Voltage Range	(See technical note 1)	1.6	2.5		V
$\lvert I_3 \rvert$	Peak Control Current			3		mA
K_3	Gain Phase Comparator ϕ1 $K_3 = 2 \times I_3 / 360$			17		µA / degree
V_4	Sync Threshold Input (neg. edge)	• Sync high • Sync low	2		8 0.8	V V
I_4	Current at Pin 4	• Input high • Input low	 - 10		10	µA µA
T_4	Input Pulse Duration T = $1/f_H$	@ f_H = 27.64kHz	1		0.9T	µs
V_5	Monostable Threshold		5.6	6	6.4	V
t_5	Internal Pulse Width (t_5 = C5 x V_5 /I_5)	C5 = 220 pF (see technical note 2)		3.6		µs
t_7	Output Pulse Duration (low) - T = $1/f_H$	f_H = 27kHz f_H = 70kHz	0.38T 0.35T	0.41T 0.39T	0.44T 0.43T	µs µs
V_7 sat	Output Saturation Voltage	I_7 = 600 mA		1.2	2.5	V
t_D	Permissible delay between output pulse leading edge and flyback pulse leading edge (for keeping a constant duty cycle) ; T = $\frac{1}{f_H}$	See technical note 4 @ f_H = 27kHz	0.41 T - t_{FLY}			s
I_{FLY}	Flyback Input Current at Pin 8	• Flyback On • Flyback Off	0.7 -1		2	mA mA
V_8	Clamp voltage at Pin 8	• I_8 = 1mA • I_8 = - 1mA	0.6		 - 0.6	V V
I_8	Current for switching low the output pulse		0.7		2	mA
$\lvert I_9 \rvert$	Peak control current			0.9		mA

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ELECTRICAL CHARACTERISTICS (continued)

(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SECTION						
K_9	Phase sensitivity at Pin 9	(See technical note 3)		67.5		$\frac{\text{degree}}{\text{V}}$
V_{10}	Control voltage range		0.5		4.5	V
K_{10}	Phase control sensitivity at Pin 10		20	22.5	25	$\frac{\text{degree}}{\text{V}}$
HADJ	Horizontal phase adjustment for V_{10} varying from 0.5 to 4.5V (27.64kHz)	Zero degree phase: flyback centered on the middle of the pulse at Pin 5	- 45		+ 45	degree
K_1	Phase jitter constant (jitter = $\frac{K_1}{10^6 \cdot f_H}$)			100	150	ppm
K_2	Frequency drift versus supply voltage $K_2 = \frac{dF \cdot 10^6}{dV \cdot f_H}$	V_S = 10.5V to 15.5V			400	$\frac{\text{ppm}}{\text{V}}$
VERTICAL SECTION						
V_{12}	Voltage reference at Pin 12		3.2	3.5	3.8	V
$\frac{I_{13}}{I_{12}}$	Current gain at Pin 13	I_{12} = 100µA (I_{12} max. = 200µA)	0.94	1	1.06	
V_{13}	Typical Vertical Sawtooth Amplitude (Pin 13) for Center Frequency	To be adjusted by I_{12}		4		V_{PP}
t_{FALL}	Discharge time at Pin 13	C_{18} = 0.22 µF, V_{13} = 4V_{PP}		10	22	µs
f_{VL}	Maximum Vertical Frequency	Vertical Sync Low $C_{Pin\ 13}$ = 220nF, $R_{Pin\ 12}$ = 58kΩ		84		Hz
f_{VH}	Minimum Vertical Frequency	Vertical Sync High $C_{Pin\ 13}$ = 220nF, $R_{Pin\ 12}$ = 58kΩ		56		Hz
K_{14}	Synchro window constant $t_s = \frac{K_{14}}{f_V}$	(See technical note 6)		0.333		
V_{14}	Sync input threshold (negative edge)	• Sync high • Sync Low	2		8 0.8	V V
I_{14}	Current at Pin 14	• Input high • Input Low V_{14} = 0.8V	- 10		10	µA µA
t_{14}	Input pulse duration $T = \frac{1}{f_V}$	@ f_V = 64.75Hz	10		0.5T	µs
V_{15}	Average value of voltage on Pin 15	V_{13} = 4V_{PP}, V_{16} = 2.5V		4		V
$\|I_{15}\|$	Output current at Pin 15				1	mA
K_{15}	Buffer gain constant at Pin 15 $V_{15PP} = K_{15} \cdot V_{13PP}$	V_{16} = 2.5V		0.95		
K_{16}	Buffer variable gain constant at Pin 15 : $K_{16} = \frac{\Delta V_{15PP}}{\Delta V_{16} \cdot V_{13PP}}$	2.5V < V_{16} < 4.5V 0.5V < V_{16} < 2.5V		0.1 0.1		V^{-1} V^{-1}
I_{16}	Input bias current at Pin 16	V_{16} = 0.5V	- 50			µA
I_{17}	Input bias current at Pin 17	V_{17} = 4.5V			50	µA
V_{18}	Average voltage at Pin 18 : $V_{18} = 2 + \frac{V_{18PP}}{2}$	V_{17} = 3.5V, R_{18} not connected		3		V
K_{18}	Linearity correction constant : $K_{18} = \frac{\Delta V_{18PP}}{\Delta V_{17}}$	V_{13PP} = 4V, 1.5V < V_{17} < 4.5V		1		
V_{19}	Voltage reference at Pin 19	(See technical note 5)	7.6	8	8.4	V
$\|I_{19}\|$	Current at Pin 19				2	mA

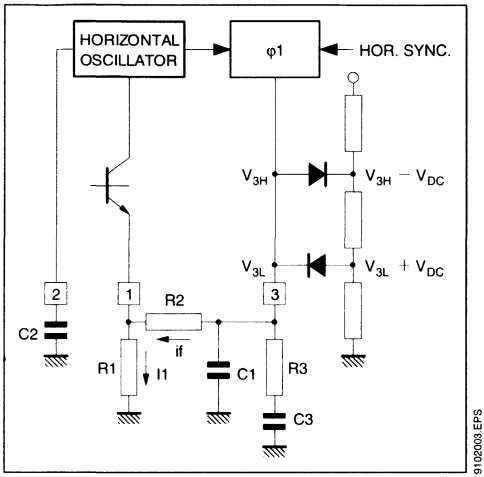
9102004.TBL

ELECTRICAL CHARACTERISTICS (continued)
(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VERTICAL SECTION						
K_{17}	Frequency drift versus supply voltage $K_{17} = \frac{dF \cdot 10^6}{dV \cdot f_V}$	V_S = 10.5V to 15.5V			300	ppm/V

9102005.TBL

Technical note 1



9102003 EPS

$f_{H\,(nom)}$ = 26.8 kHz
R1 = 6.8k Ω
R2 = 56 kΩ
C2 = 1.8 nF

$$f_{pull\text{-}in} = f_{H\,(nom)} \frac{|V_3 - V_1| / R2}{V_1 / R1} = f_{H\,(nom)} \frac{I_f}{I_o} \qquad (A)$$

where: V_1 = 3.5V and $|V_3 - V_1|$ is the control voltage range.

The voltage at Pin 3 is limited by two clamping diodes at the voltage V_{3H} and V_{3L}
When the PLL1 is synchronized and perfectly tuned, $V_3 = V_1$.

Remark: The value of C2 influences the horizontal oscillator free running frequency; it doesn't effect the relative pull-in range. If the horizontal frequency is changed by using R1, the pull-in range changes accordingly with the formula (A).

Technical note 2

The internal pulse "t_5", is generated by the current generator "I_5" charging the external capacitor "C5", according with the formula (B):

$$t_5 = \frac{C5 \cdot V_5}{I_5} \quad (B), \quad t_5 = \frac{T_H}{12} \quad \text{is recommended.}$$

Technical note 3

K_9 = 67.5 degrees/volt represents the slope of the oscillator charging period of the waveform at Pin 2:

$$K_9 = \frac{360 \times 0.75}{4} \quad \frac{\text{degree}}{V}$$

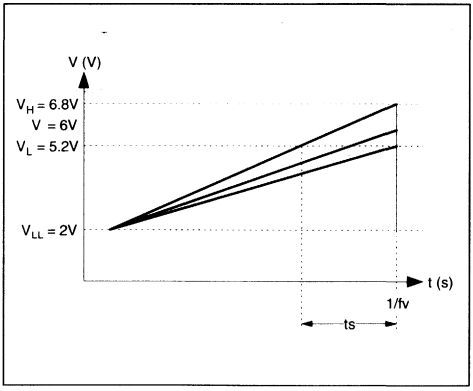
Technical note 4

The second PLL can recover the storage of horizontal output stage maintaining a constant duty cycle till the trailing edge of the output pulse gets the trailing edge of the flyback pulse. From this point on, only the leading edge of the output pulse will be shifted covering a total phase shift of: 0,30T; overcoming this value, it will produce a notch in the output pulse (@ f_H = 27kHz).

Technical note 5

The voltage reference at Pin 19 can be used to polarize the DC operating point of the vertical booster. This voltage corresponds to the double of the mean value voltage of the vertical sawtooth at Pin 13.

Technical note 6



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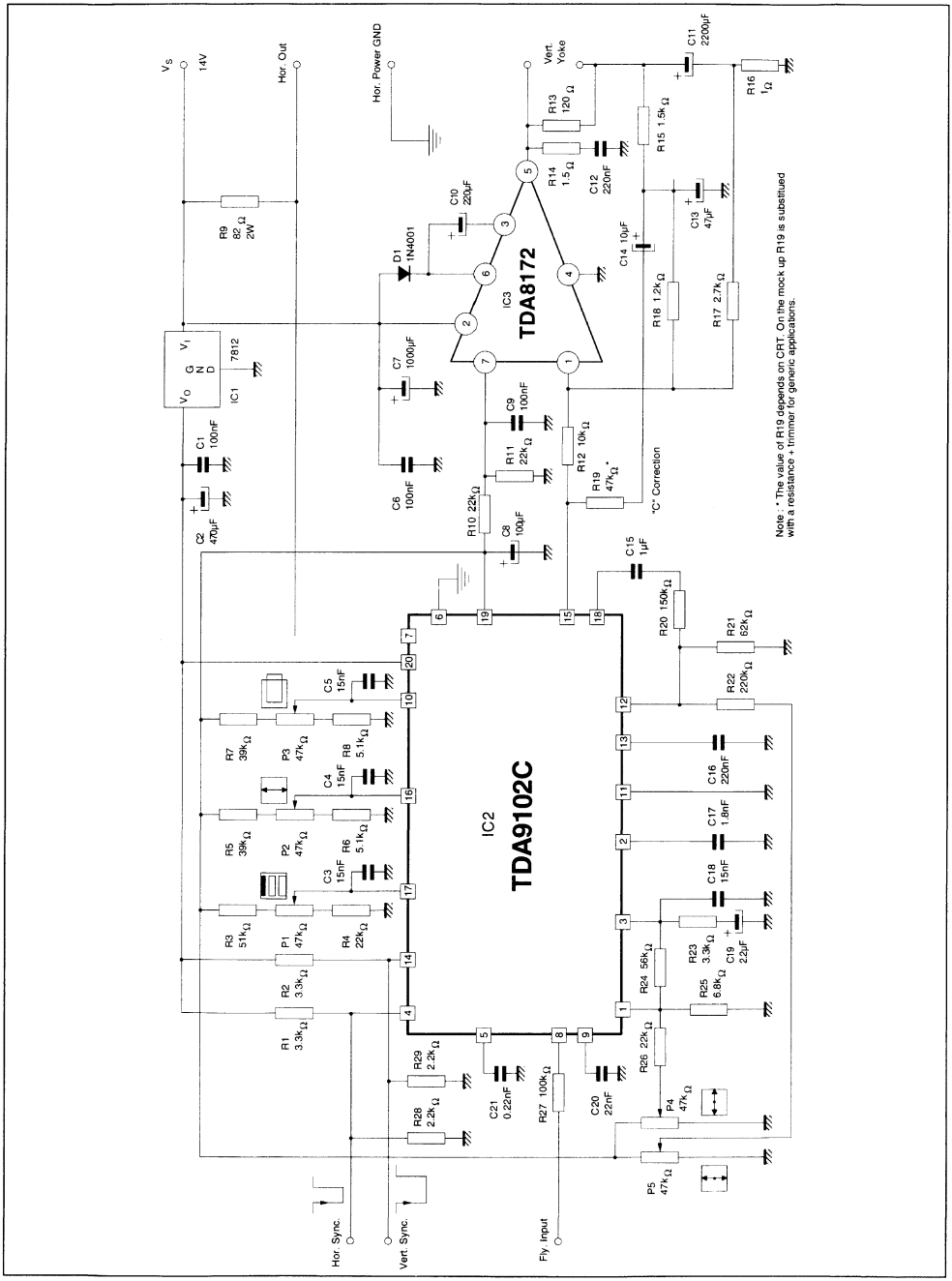
$$\frac{V_H - V_L}{t_s} = \frac{V_H - V_{LL}}{1/f_V}$$

$$t_s = \frac{(V_H - V_L)}{(V_H - V_{LL})} \frac{1}{f_V} = \frac{K_{14}}{f_V}$$

APPLICATION DIAGRAM (with TDA8172)

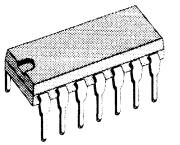


SGS-THOMSON MICROELECTRONICS

TDA9108

MONITOR HORIZONTAL PROCESSOR

- POS/NEG SYNC INPUT
- SYNC POLARITY DETECTION
- 2 PLLs CONCEPT
- 2 COMPLEMENTARY OUTPUTS
- DC ADJUSTABLE FREQUENCY
- DC ADJUSTABLE DUTY CYCLE
- X-RAY PROT INPUT
- BACK PORCH CLAMPING PULSE GENERATOR
- H-DRIVE INHIBITION WHEN $V_S < V_{S\ START}$



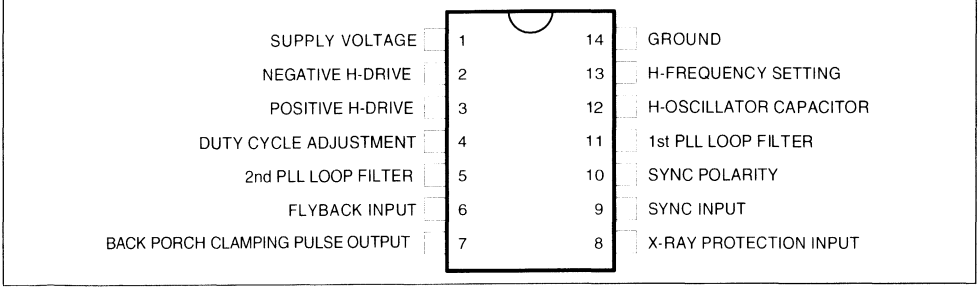
DIP14
(Plastic Package)

ORDER CODE : TDA9108

DESCRIPTION

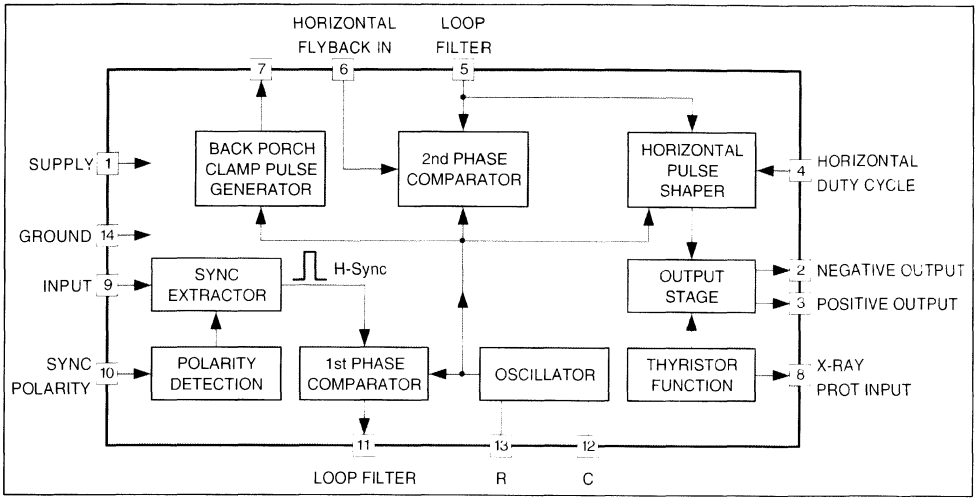
The TDA9108 is a horizontal deflection processor specially designed for monitor applications. The H-drive output duty cycle, the horizontal frequency and the horizontal position are DC adjustable ; it accepts both POS/NEG polarity on sync input and delivers polarity information on a dedicated pin. All these features make the device a good choice for multifrequency application. In addition to this, X-ray protection, 2 complementary H-drive output , and a back porch clamping pulse generator are also included. It is a monolithic integrated circuit encapsulated in a 14 lead dual line plastic package.

PIN CONNECTIONS



9108-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pin 1)	15	V
V_2	Voltage at Pin 2	18	V
V_4	Voltage at Pin 4	0, V_S	V
V_8	Voltage at Pin 8	0, V_S	V
V_9	Voltage at Pin 9	0, V_S	V
V_{10}	Voltage at Pin 10	0, V_S	V
I_2	Pin 2 Peak Current	1	A
I_3	Pin 3 Peak Current	0.5	A
I_6	Pin 6 Input Current	30	mA
I_7	Pin 7 Input Current	10	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70^{\circ}C$	0.9	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	°C

9108-11.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-ambient	Max.	90	°C/W

9108-12.TBL

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		10	12	13.2	V
I_S	Supply Current (Pin 1)	$I_3 = 0$		38	55	mA
V_S	Supply voltage at which the output pulses (at Pin 2 and 3) are switched off				4	V

9108-13.TBL

ELECTRICAL CHARACTERISTICS (continued)

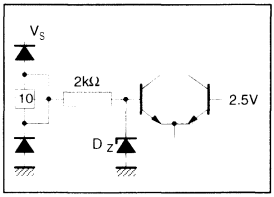
(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SYNC. INPUT						
V_{9SW}	Sync Input Threshold	• Sync high • Sync Low	2		V_S 0.8	V V
I_{9SW}	Sync Input Current	• Sync high • Sync Low	 -20	 -7	1 	µA µA
SYNC POLARITY SELECTION						
V_{10th}	Polarity Selection Threshold Positive sync on Pin 9 for $V_{10} < V_{10th}$ Negative sync on Pin 9 for $V_{10} > V_{10th}$		2.3	2.5	2.7	V
I_{10}	Input Current	V_{10} = 2V V_{10} = 3V			1 12	µA µA
V_{10ZL}	Low Impedance (2kΩ) Threshold	(see note 1)		6.3		V
X-RAY PROTECTION CIRCUIT						
V_{8th}	X-ray Prot Input Threshold Voltage (when $V_8 > V_{8th}$ Pin 2 and 3 are inhibited until V_S is switched off/on)		2.6	2.9	3.2	V
I_8	Input Current	$V_8 \leq 2.5$ $V_8 \geq 3.3$	-0.5		 0.5	µA µA
FLYBACK INPUT						
V_6	Phase Comparator Input Threshold				10	V
I_6	Input Switching Current		0.1			mA
OUTPUT PULSE						
V_2	Saturation Voltage (Pin 3 grounded)	I_2 = 150mA		2.2	3.2	V
I_2	Output Current (Pin 3 grounded)	V_2 = 5V			150	mA
V_3	Output Voltage (Pin 2 connected to supply)	• High level (I_3 = 150mA) • Low level (I_3 = 100mA)	8.8	9.8 1.5	10.8 2.7	V V
I_3	Output Current Capability	• Source • Sink			150 100	mA mA
R_3	Output Resistance	• At leading edge of output pulse • At falling edge of output pulse		3 20		Ω Ω
DUTY CYCLE ADJUSTMENT						
t_p	Horizontal Output Pulse Duty Cycle on Pin 3 (high level, line transistor off time)	f = 31.5kHz Pin 4 not connected	26	30	34	%
V_4	Voltage on Pin 4 (see note 2)	Pin 4 not connected	0.178 V_S	0.19 V_S	0.202 V_S	V
R_4	Serial Equivalent Resistor on Pin 4 (see note 2)	Pin 4 not connected	1.7	2.3	2.9	kΩ

9108-04 TBL

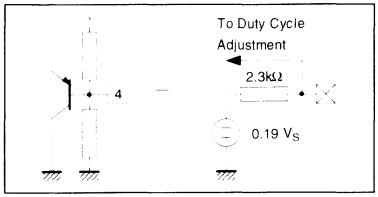
Note 1 : The voltage on the polarity detection comparator is clamped by an internal Zener diode (V_Z).

When voltage on Pin 10 reaches V_Z, then $I_{Pin\ 10} = \frac{V_{Pin\ 10} - V_Z}{2k\Omega}$.



9108-03 EPS

Note 2 : Pin 4 internal schematic



9108-04 EPS

ELECTRICAL CHARACTERISTICS (continued)

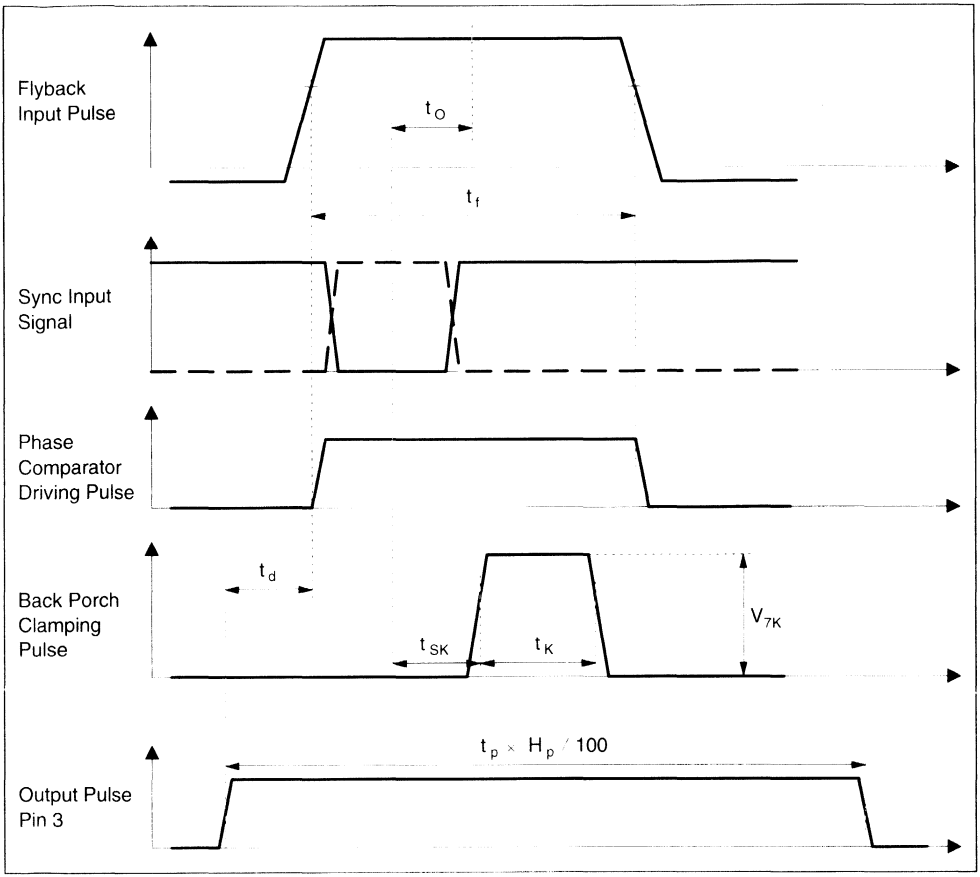
(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DUTY CYCLE ADJUSTMENT (continued)						
t_{pADJ}	Max. Horizontal Output Duty Cycle Range (function of V_4) $t_p = K4 \cdot \frac{V_4}{V_S}$ (see note 3)	f = 31.5kHz		50		%
K4	Duty Cycle Adjustment Coefficient		1.6	1.8	2	
KEY PULSE OUTPUT						
V_{7k}	Key Pulse Output Peak Voltage (emitter follower)	I_7 = 5mA	4	5		V
V_{7L}	Low Level (outside the key pulse)			0.2	0.5	V
t_{SK}	Phase Relation between Trailing Edge of Key Pulse and Middle of Sync. Input Pulse	f = 31.5kHz Sync width = 2µs	1.1	1.5	1.9	µs
t_K	Key Pulse Duration		1.25	1.7	2.15	µs
OSCILLATOR						
V_{12}	Low Level Threshold Voltage			5.4		V
V_{12}	High Level Threshold Voltage			8.2		V
I_{12}	Charge Current	R_{13} = 10kΩ		0.6		mA
I_{12}	Discharge Current	R_{13} = 10kΩ		0.3		mA
V_{13}	Reference Voltage on Pin 13		2.6	2.9	3.2	V
f_O	Free Running Frequency	R_{13} = 10kΩ C_{12} = 2.2nF	27	30	33	kHz
$f_{Max.}$	Maximum Oscillator Frequency	R_{13} = 47kΩ C_{12} = 2.2nF	66			kHz
Jitt.	Horizontal Jitter	f = 31.5kHz		5		ns
$\frac{\Delta f_O}{\Delta I_{13}}$	Frequency Control Sensitivity	R_{13} = 10kΩ C_{12} = 2.2nF		100		Hz/µA
Δf_O	Frequency Change when V_S Drops to 7.5V				-6	%
PHASE COMPARATOR						
V_5	Control Voltage Range			9.4 to 8.2		V
I_5	Peak Control Current	During flyback pulse		± 0.85		mA
I_5	Input Current (blocked Phase Detector)	Outside flyback pulse			5	µA
t_D	Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge			$t_p - t_f$		µs
$\frac{\Delta t}{\Delta t_D}$	Static Control Error				0.2	%
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
V_{11}	Control Voltage Range			4.6 to 1.4		V
I_{11}	Control Peak Current	During Sync Pulse		± 2.3		mA
$\frac{\Delta f}{\Delta t}$	Phase Lock Loop Gain	$R_{11\text{-}13}$ = 100kΩ		4		kHz/µs
f	Catching and Holding Range	See Typical Application		± 700		Hz
OVERALL PHASE RELATIONSHIP						
t_O	Phase Relation between Middle of Flyback Pulse and Middle of Sync. Pulse	R_{13} = 10kΩ C_{12} = 2.2nF		1.1		µs
$\frac{\Delta V_5}{\Delta t_O}$	Adjustment Sensitivity			130		mV/µs
$\frac{\Delta I_5}{\Delta t_O}$	Adjustment Sensitivity			50		µA/µs

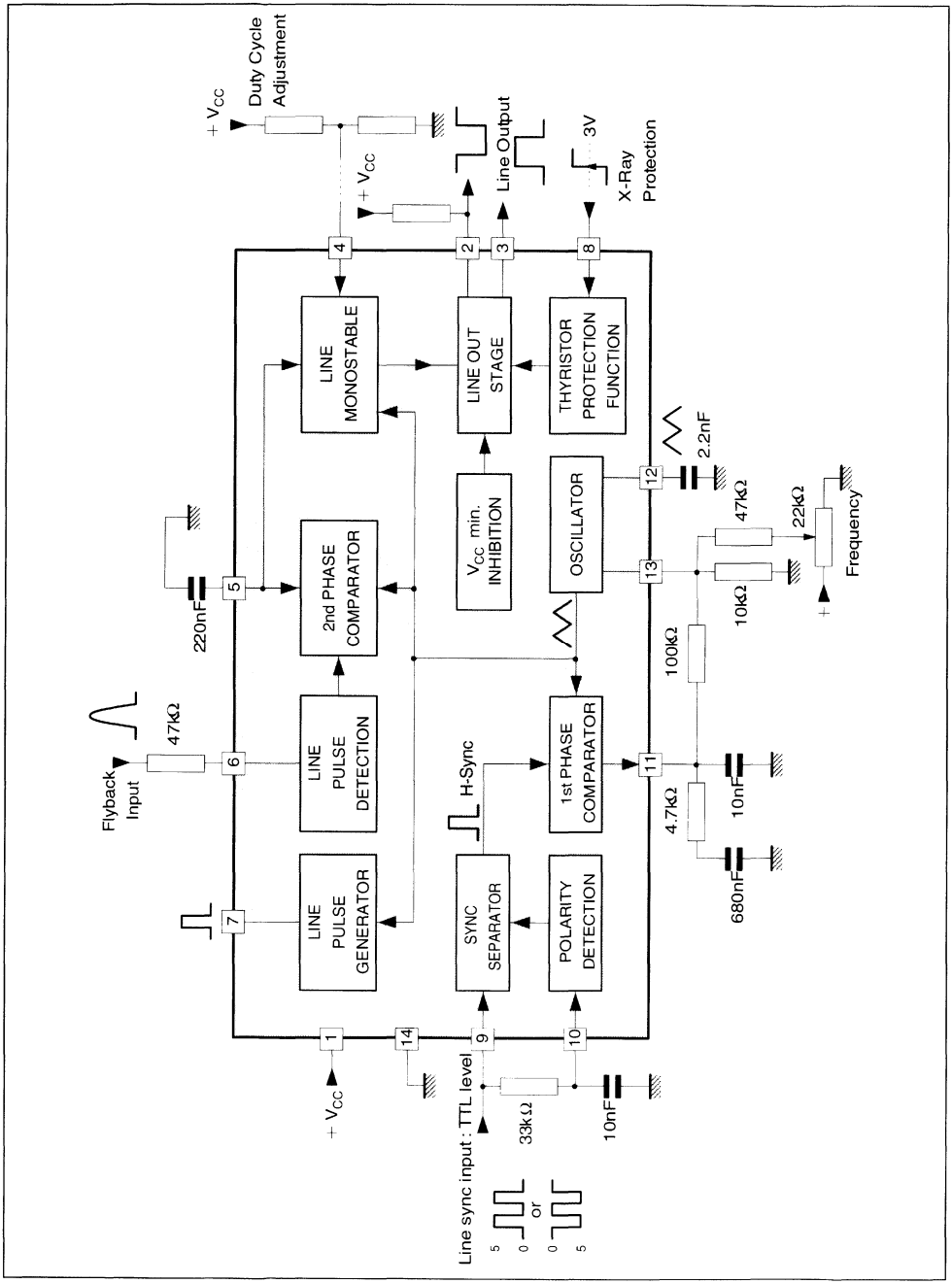
3108-05.TBL

Note 3 : t_d must be ≥ $(H_{period}\left[\frac{t_p}{100} - 0.25\right] - \frac{t_{fly}}{2})$ in order to have ± 5% horizontal phase adjustment range.

Figure 1 : Relation Ship of Main Waveform Phases



TYPICAL APPLICATION



APPLICATION INFORMATION

Sync Extractor and Polarity Detection

This circuit is able to handle both positive or negative TTL input signal on Pin 9. The voltage on Pin 10 drives an internal inverter providing a constant sync polarity to the 1st phase comparator.

When using a RC network between Pin 9 and 10 (see Typical Application), the IC will adapt itself automatically to positive or negative sync. On an other hand, and in order to simplified the application, the Pin 10 can be connected to ground or supply (through a resistor), in this case the IC will work only with one sync polarity.

1st PLL

It is composed by a phase comparator, the oscillator and an external loop filter (see Figure 2)

- The phase comparator receives the H-sync signal (with positive polarity) and a signal coming from the internal current controlled oscillator. The loop is closed through an external resistor between Pin 11 and 13.
- The oscillator generates a sawtooth waveform on Pin 12 by charging and discharging the external capacitor. The capacitor is discharging by the current flowing Pin 13 and charged by two times this latter (see Figure 3).

The sawtooth is used internally to generate all the required timings.

It is possible to DC control the frequency by adding or substracting a DC current on Pin 13 (see Figure 2).

Figure 2

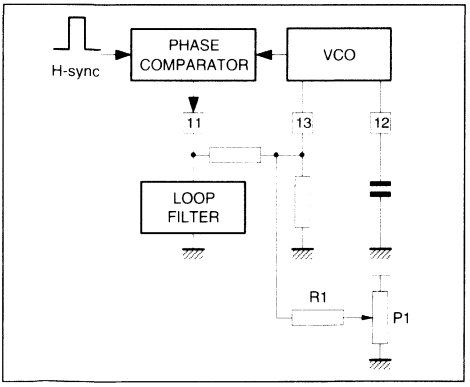
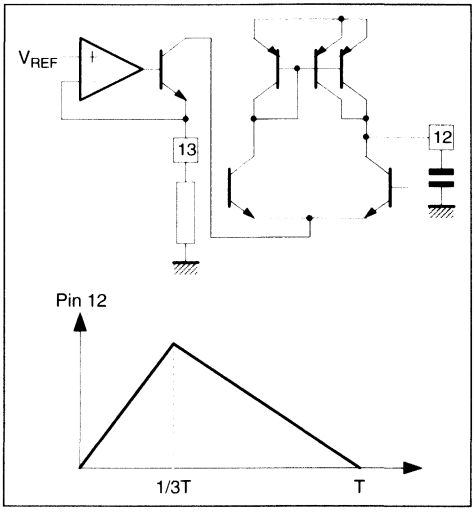


Figure 3



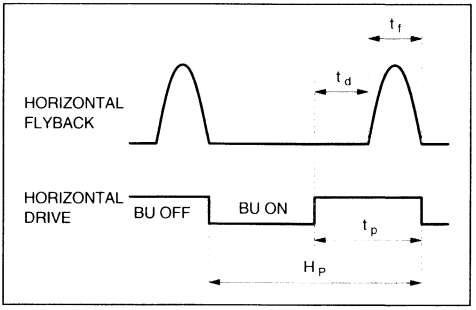
2nd Phase Locked Loop

To compensate the delay introduced by the horizontal final stage, the flyback pulse (Pin 6) and the oscillator waveform (Pin 12) are compared in the 2nd phase comparator. The result of the comparison is a control current which, after it has been filtered by the external capacitor on Pin 5, is sent to a phase shifter which adequately regulates the horizontal output pulses phase.

The maximum phase shift allowed is $t_d = t_p - t_f$ where t_f is the flyback duration (see Figure 4).

If $t_d > t_p - t_f$, then the horizontal output transistor will be tunned on during flyback distroying it.

Figure 4



X-Ray Protection Input (Pin 8)

When the voltage on this pin becomes higher then 2.9V (typ.), the horizontal outputs are inhibited (Pins 2 and 3) and will remains in this condition until a reset is made on supply voltage (power-off/power-on).

H-Duty Cycle (see Figure 5)

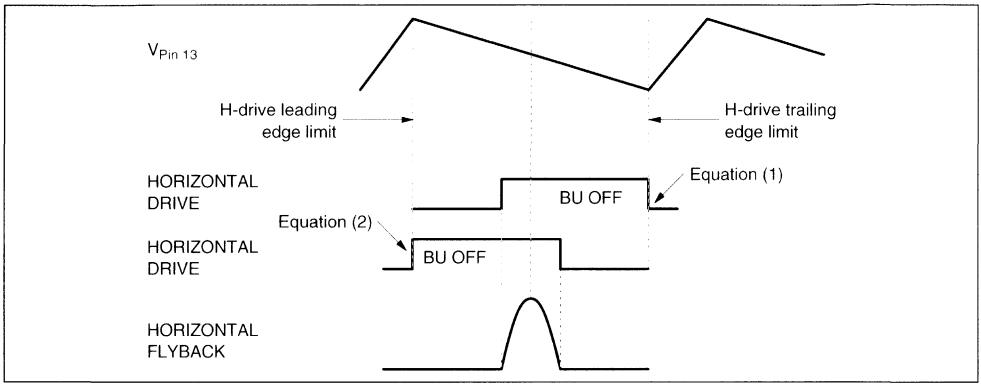
The output duty cycle is variable between 0 and 50% by varying the voltage on Pin 4.

In order to maintain ± 5% horizontal phase adjustment possibilities the following equation must be respected.

(1) $H_{period}\left[\frac{t_p}{100} - 0.25\right] - \frac{t_{fly}}{2} \leq t_d$ ⇒ If not, t_p will decrease because of H-drive trailing edge wrong position (phase shifter saturation)

(2) $t_d \leq 0.36\ H_p - \frac{t_{fly}}{2} - 2\mu s$ ⇒ If not, t_p will decrease because of H-drive leading edge wrong position (phase shifter saturation)

Figure 5



SGS-THOMSON MICROELECTRONICS

TEA2029C

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION

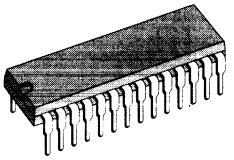
- CERAMIC 500kHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR
- FRAME PHASE MODULATOR FOR THYRISTOR

SMPS CONTROL

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START UP PROCESSOR
- OUTPUT PULSES ARE SENT TO THE PRIMARY SMPS IC (TEA2261) THROUGH A LOW COST TRANSFORMER

DESCRIPTION

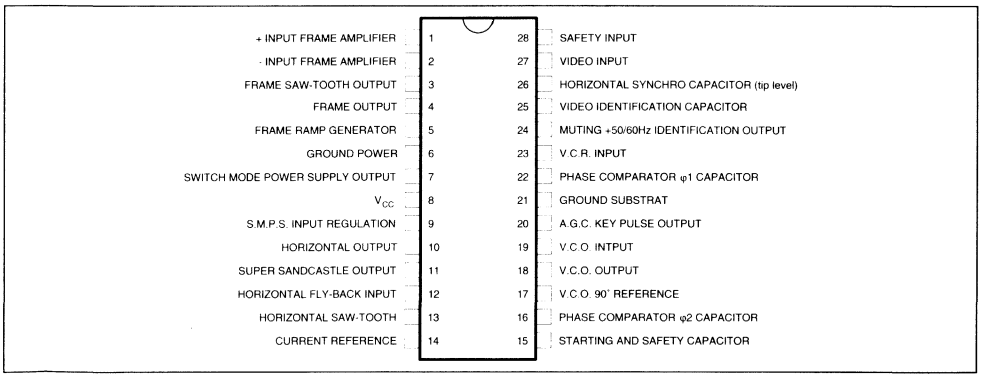
The TEA2029C is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.



DIP28
(Plastic Package)

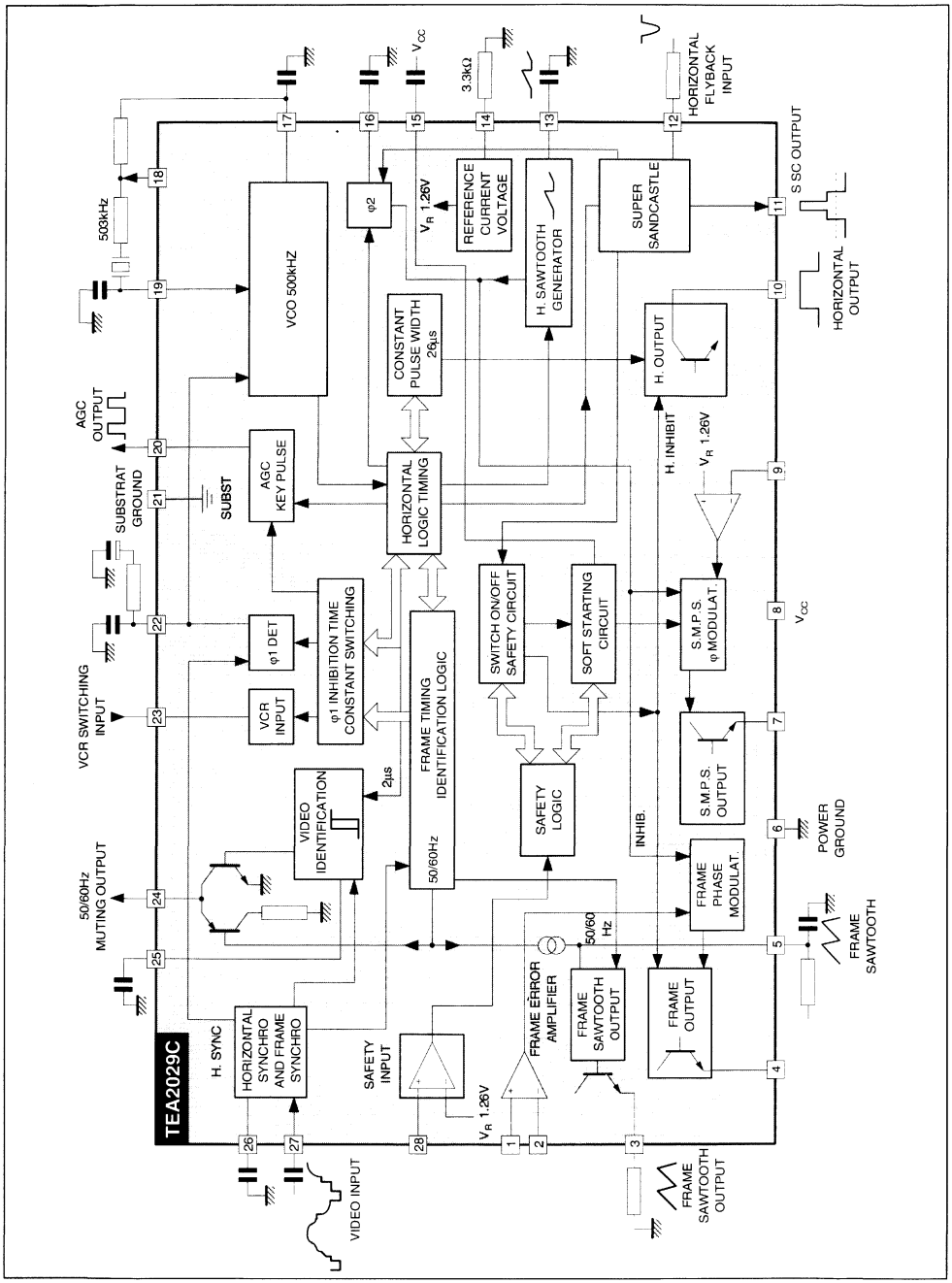
ORDER CODE : TEA2029C

PIN CONNECTIONS



2029C-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.
Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500KHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.
A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :
- Horizontal scanning processor.
- Frame scanning processor. Two applications are possible :
  - D Class : Power stage using an external thyristor.
  - B Class : Power stage using an external power amplifier with fly-back generator such as the TDA8170.
- Secondary switch mode power regulation. The SMPS output synchronize a primary I.C. (TEA2260/61) at the mains part. This concept allows ACTIVE STANDBY facilities.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- AGC key pulse output.
- Automatic 50-60Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500kHz VCO

The circuit is supplied in a 28 pin DIP case.
V_{CC} = 12V.

Synchronization Separator

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.
The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

Frame Synchronization

Frame synchronization is fully integrated (no external capacitor required).
The frame timing identification logic permits automatic adaptation to 50 - 60Hz standards or non-interlaced video.

An automatic synchronization window width system provides :
- fast frame capture (6.7ms wide window),
- good noise immunity (0.4ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly back effects.
Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.
A 32µs timing is automatically applied on standardized transmissions, for perfect interlacing.
In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

Horizontal Scanning

The horizontal scanning frequency is obtained from the 500kHz VCO.
The circuit uses two phase-locked loops (PLL) : the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :
- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26µs, independent of V_{CC} and any delay in switching off the scanning transistor.

Video Identification

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :
- 0V : no video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers, and for audio muting.

Super Sandcastle with 3 levels : burst, line fly-back, frame blanking
In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.
Frame blanking time (start with reset of Frame divider) is 24 lines.

VCR Input

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).
In VCR mode, the frame synchronization window

widens out to a search window and there is no delay of frame fly-back (direct synchronization).

Frame Scanning

FRAME SAW-TOOTH GENERATOR. The current to charge the capacitor is automatically switched to 60Hz operation to maintain constant amplitude.

FRAME PHASE MODULATOR (WITH TWO DIFFERENTIAL INPUTS). The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.
This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance, however, and can therefore be used in class B operation with a power amplifier circuit.

Switch Mode Power Supply (SMPS) Secondary to Primary Regulation

This power supply uses a differential error amplifier with an internal reference voltage of 1.26V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.
The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.
The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.
The output pulse is sent to the primary S.M.P.S. I.C. (TEA2261) via a low cost synchro transformer.

Security Circuit and Start Up Processor

When the security input (pin 28) is at a voltage exceeding 1.26V the three outputs are simultaneously cut off until this voltage drops below the 1.26V threshold again. In this case the switch mode power supply is restarted by the "soft start" system. If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be zero volt.
This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.
On starting up, the horizontal and vertical scanning functions come into operation at V_{CC} = 6V. The power supply then comes into operation progressively.
On shutting down, the three functions are interrupted simultaneously after the first line fly-back.

ABSOLUTE MAXIMUM RATINGS (limiting values) T_{amb} = 25 °C (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage (pin 8)		14	V
VCC	Operating Supply Voltage (pin 8)	Starting threshold	13.2	V
I_{20}	AGC Current (pin 20)		5	mA
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Negative Line Retrace Voltage (pin 12)	– 20		V
I_{12}	Line Retrace Current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	– 10	40	mA
I_3	Frame Saw-tooth Generator (pin 3)		20	mA
I_4	Frame Output Current (pin 4)		100	mA
I_7	SMPS Output Current (pin 7)	– 40	40	mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	
V_1/V_2	Common Mode Range (pins 1-2)		10	V

2029C-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	55	°C/W

2029C-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8, frame, line and SMPS output without load)		50	80	mA
SYNCH SEPARATOR (Pins 26-27)					
	Positive Video Input AC Coupled (output impedance of signal source < 200Ω)	0.2	1.8	3	V_{pp}
$-I_{27}$	Negative Clamping Current (during synch, pulse)	- 25	- 40	- 55	µA
I_{27}	Clamping Current - Pin for slicing level 0.2V < V_{27pp} < 2V (50% of sync amplitude)	3	6	9	µA

2029C-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SYNCH SEPARATOR (Pins 26-27) (continued)					
$-I_{26}$	Positive Current	0	- 0.75	- 1	nA
I_{26}	Negative Current	17	25	36	µA
PULSE FOR KEYED AGC (Pin 20) - Positive (function : without video signal : low level, with video signal : key pulses)					
I_{20}	Output Current			5	mA
V_{20}	Output Saturation Voltage (I_{20} = 5 mA)		0.25	0.4	V
t_k	Pulse width (synchro pulse is always inside the key pulse)	6.5	8	8.5	µs
VCO (Pins 17-18 and 19)					
	Frequency control range after line divider (ceramic resonator : 503 kHz)	15.30 to 16.10			kHz
PHASE COMPARATOR φ 1 (Pin 22)					
	Output Current Low Loop Gain	± 0.35	± 0.50	± 0.65	mA
	Output Current High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
VCR SWITCHING (Pin 23)					
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0 V_{CC} = 12V)	- 0.030	- 0.25	- 1	mA
VIDEO IDENTIFICATION (Pin 24)					
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3 mA)		0.2	0.6	V
	Output Voltage (with 60 Hz video signal, I_{24} = 2.5 mA)	5	6.5	0.6	V
	Output Voltage (with 50 Hz video signal, I_{24} = 10 µA)	11	11.5	7.5	V
VIDEO IDENTIFICATION (Pin 25)					
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4.5	5	V
L_{HYS}	Hysteresis	150	240	400	mV
H-RAMP GENERATOR (Pin 13)					
I_{ch13}	Charge Current	185	200	215	µA
V_{I13}	Base Voltage of Saw-tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7		mA
SUPER SANDCASTLE (Pin 11)					
V_{B11}	Burst Key Pulse Level Output Voltage (I_{11} = - 5mA)	9			V
V_{L11}	Line Blanking Pulse Level Output Voltage (I_{11} = - 5mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level Output Voltage (and frame out of function) (I_{11} = - 5mA)	2	2.5	3	V
T_{B11}	Delay between Middle of Synch Pulse (pin 27) and Leading Edge of Burst Key Pulse	2.3		3	µs
	Duration of Burst Key Pulse	3.7	4	5	µs
T_{O11}	Delay between SSC Cutting at Pin 12 and Line Blanking Pulse			0.35	µs
NEGATIVE LINE FLY-BACK INPUT (Pin 12)					
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking	11	11.5	12	V
$V_{\varphi 12}$	Threshold for PLL2	- 1			V
I_{12}	Input Current 11V < V_{12}			- 200	µA
I_{12}	Input Current 1.3V < V_{12} < 11V	-3		3	µA
I_{12}	Input Current 0V < V_{12}< 1.3V	0		- 80	µA
I_{12}	Input Current - 1V < V_{12} < 0V	0	- 1	- 2	mA
	Line Blanking Trigger			80	µA

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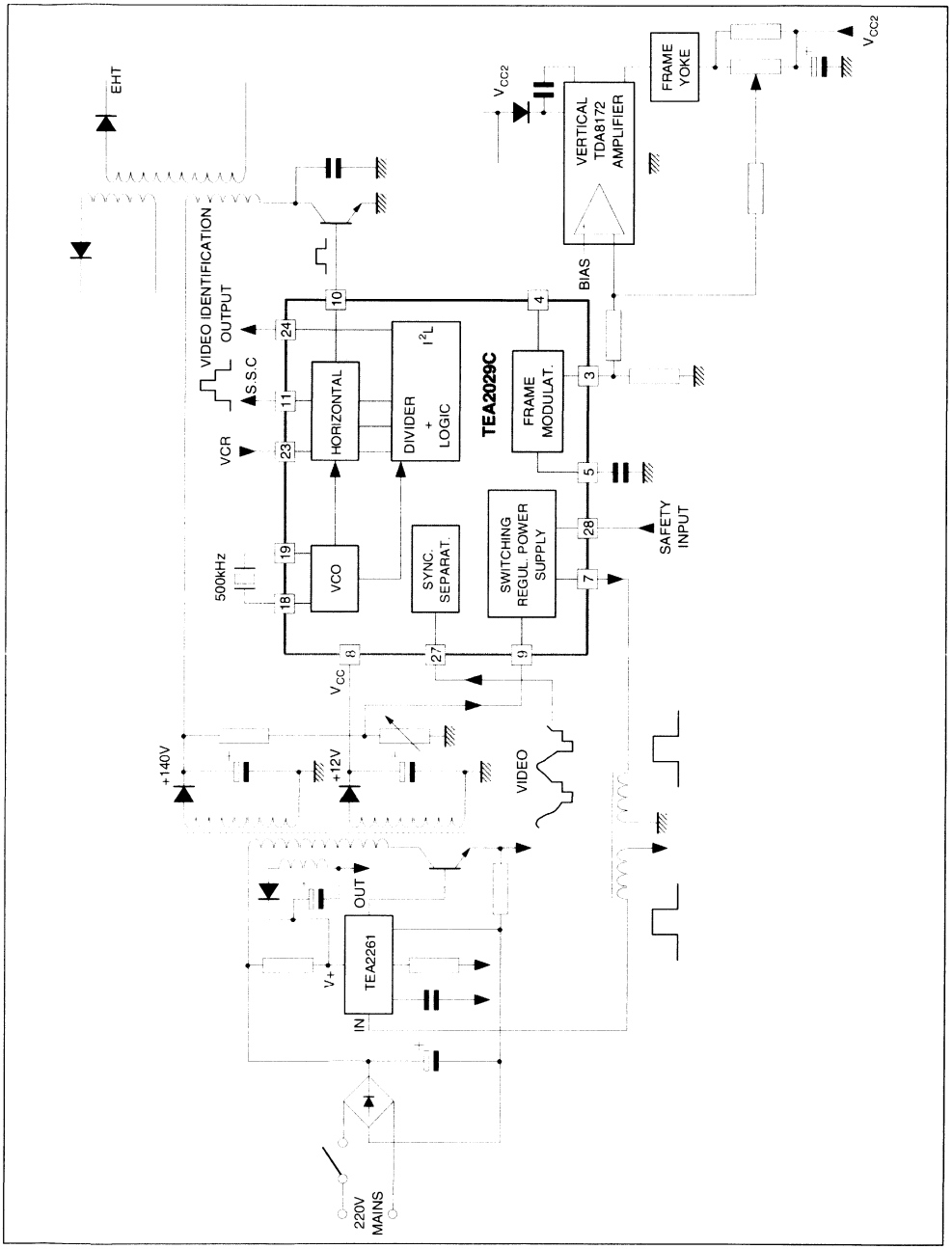
ELECTRICAL OPERATING CHARACTERISTICS (continued)

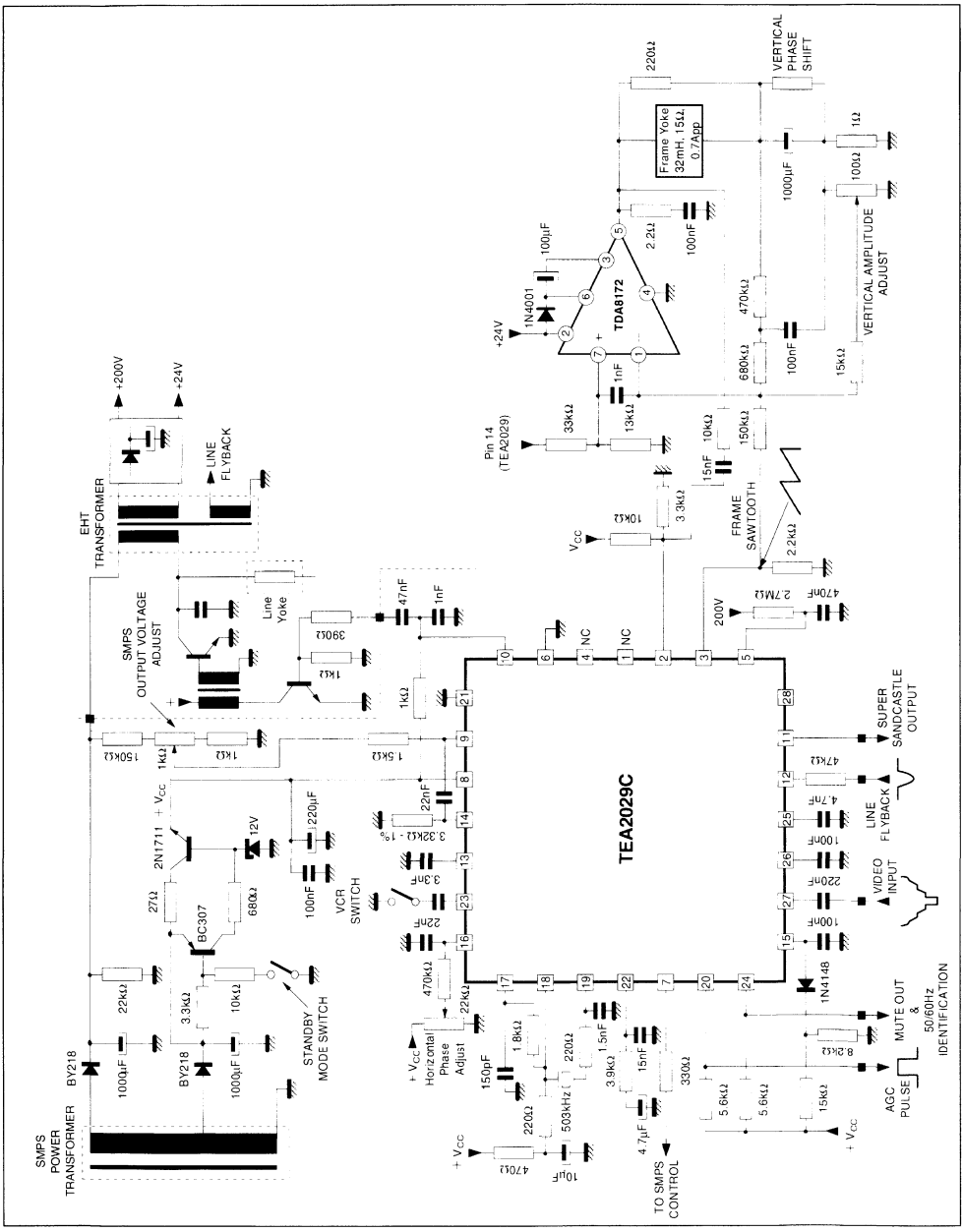
Symbol	Parameter	Min.	Typ.	Max.	Unit
PHASE COMPARATOR φ2 (Pin 16)					
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay between the Edges of φ1 and φ2 (f_{VCO} = 500kHz)	1.5	2	2.8	µs
LINE OUTPUT (OPEN COLLECTOR) (Pin 10)					
	Output Voltage (I_{10max} = 20mA)		1	1.5	V
T_{10}	Output Pulse Duration (when fly-back pulse is with in time T_{10}) (f_{VCO} = 500kHz)	24	26	30	µs
Δt	φ2 Phase Range	15	16	19	µs
FRAME LOGIC					
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50Hz Window	309		315	Line
	60Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
FRAME SAW-TOOTH GENERATOR (Pins 3-5)					
	Saw-tooth Amplitude	2	3	4	V_{PP}
$I_5(60)$	SInternal Current Generator (60Hz on)	12	14	16	µA
	Discharging Time (with C = 0.47µF, ΔV < 4V)	50		70	µs
V_S	Starting Level (0mA < I_S < 0mA)	1	1.26	1.4	V
	Saw-tooth Amplitude (I_S = 10mA)	2	3	4	V_{PP}
FRAME FEEDBACK INPUTS (Pins 1-2)					
$I_{1,2}$	Positive and Negative Input Current (V_1 - V_2) > 25mA for frame blanking safety			10	µA
FRAME OUPUT (Pin 4)					
	Output Voltage (0mA < $\|I_4\|$ < 80mA)	10			V
	T_{ON} max (f_{VCO} = 500kHz)	36	40	41	µs
	Output Phase Range	0		$t_{ON\ max}$	
SMPS CONTROL INPUT (Pin 9)					
I_9	Input Current (V_9 = $V_{ref\ 14}$)			2	µA
SMPS OUTPUT (Pin 7) - No Relation between End of SMPS Pulse (pin 7) and Leading Edge of Line Flyback (pin 12)					
V_7	Output Voltage (0 < I_7 < 20mA)	10			V
T_7	$t_{ON\ max}$ (f_{VCO} = 500kHz)	30	32	34	µs
	Nominal Time (V_9 = $V_{ref\ 14}$)	26		31	µs
	Output Phase Range	0		$t_{ON\ max}$	µs
SAFETY INPUT (Pin 28)					
V_{28}	Threshold Voltage (V_{28} = $V_{ref\ 14}$)	1.15	1.26	1.37	V
	Input Current (if V_{28} > $V_{ref\ 14}$ then SMPS, line and frame are switched off during the next line retrace)			3	µA
SWITCH-ON, SWITCH-OFF PROCESSING (Pin 15)					
$I_{ch\ 15}$	Charging Current (t_C = 4µs, T = 64µs)	70		130	µA
$\frac{I_{ch\ 15}}{I_{dis\ 15}}$	Ratio Charging/discharging	0.8	1	1.2	µA
STARTING SUPPLY VOLTAGE (Pin 8)					
V_{CC}	SMPS*, Frame and Line Starting (pins 7, 10 and 4)	5.25		6.5	V
V_{CC}	SMPS Stopping during Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
CURRENT REFERENCE (PIn 14)					
$V_{ref\ 14}$	Voltage Reference	1.2	1.26	1.35	V

2029C-05.TBL

APPLICATION WITH TDA8172 FOR B CLASS FRAME POWER AND TEA2261 FOR SECONDARY SMPS REGULATION



COMPLETE APPLICATION WITH B CLASS FRAME POWER

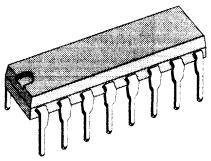


SGS-THOMSON MICROELECTRONICS

TEA2037A

HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- HORIZONTAL OSCILLATOR FREQUENCY RANGE FROM 15kHz TO 100kHz
- VERTICAL OSCILLATOR FREQUENCY RANGE FROM 30Hz TO 120Hz
- VERY FEW EXTERNAL COMPONENT
- VERY LOW COST POWER PACKAGE



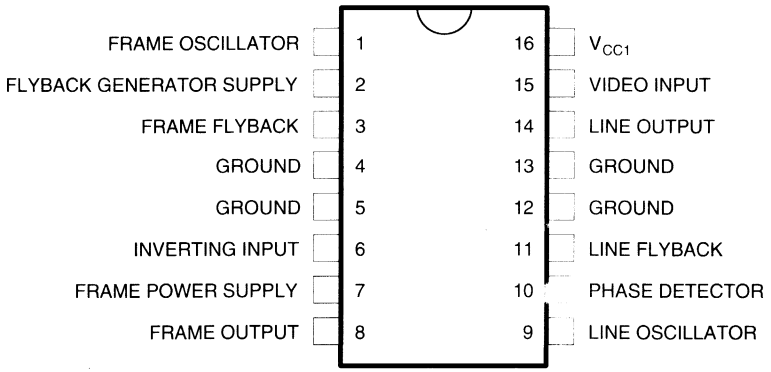
POWERDIP (8+8)
(Plastic Package)

ORDER CODE : TEA2037A

DESCRIPTION

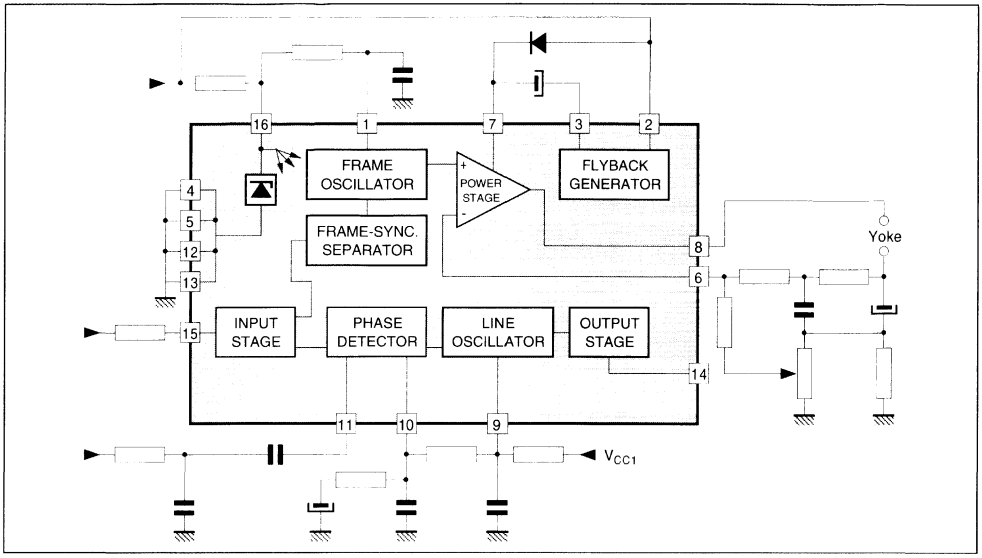
The TEA2037A is an horizontal and vertical deflection circuit. It uses the same concept as TEA2117 but optimised for small screens, for a very low cost solution.

PIN CONNECTIONS



2037A-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC1}	Supply Voltage	30	V
V_2	Flybcak Generator Supply Voltage	35	V
V_7	Frame Power Supply Voltage	60	V
I_{8nr}	Frame Output Current (non repetitive)	± 1.5	A
I_8	Frame Output Current (continuous)	± 1	A
V_{14}	Line Output Voltage (external)	60	V
I_{p14}	Line Output Peak Current	0.8	A
I_{C14}	Line Output Continuous Current	0.4	A
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Max. Operating Junction Temperature	+150	°C

2037A-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}c)}$	Junction-case Thermal Resistance	Max.	15	°C/W
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance (soldered on a 35µm thick 45cm^2 PC board copper area)	Typ.	45	°C/W
T_j	Recommended Junction Temperature	Max.	120	°C

2037A-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (shunt regulator) (Pin 16)					
I_{CC1}	Supply Current	10		20	mA
V_{CC1}	Supply Voltage (I_{CC1} = 15mA)	9	9.8	10.5	V
ΔV_{CC1}	Voltage Variation (I_{CC1} : 10mA to 20mA)	-280	50	+280	mV
LPS	Starting Threshold for Line Output Pulses			5	V

2037A-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIDEO INPUT (Pin 15)					
V_{15}	Reference Voltage (I_{15} = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (when synchronized with TTL Signal)	50			µs
V_{IN}	Sync Bottom to Black Level ($R_{SYNC\ 15}$ = 560kΩ)	0.2	0.3		V_{PP}
LINE OSCILLATOR (Pin 9)					
LT9	Low Threshold Voltage	2.8	3.2	3.6	V
HT9	High Threshold Voltage	5.4	6.6	7.8	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7kΩ, C = 2.2nF)		27		µs
OT9	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application Fig. 8)		2		Hz/°C
LINE OUTPUT (Pin 14)					
LV14	Saturation Voltage (I_{14} = 200mA)		1.1	1.6	V
OPW	Output Pulse Width (line period = 64µs)	20	22	24	µs
LINE FLYBACK INPUT (Pin 11)					
V_{11}	Bias Voltage	1.8	2.4	3.2	V
Z11	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR					
I_{10}	Output CUrrent during Synchro Pulse	250	450	800	µA
RI10	Current Ratio (positive/negative)	0.95	1	1.05	
LI10	Leakage Current	-2		+2	µA
CV10	Control Range Voltage	2.60		7.10	V
FRAME OSCILLATOR (PIn 1)					
LT1	Low Threshold Voltage	1.6	2.0	2.3	V
HT1	High Threshold Voltage	2.6	3.1	3.6	V
BI1	Bias Current		30		nA
DR1	Discharge Impedance	300	470	700	kΩ
FFP1	Free Running Line Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I_{15} = -100µA) (with the same RC)		12.8		ms
FFP2	Free Running Line Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio =	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain between Pin 1 and non-inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application Fig. 8)		$4 \cdot 10^{-3}$		Hz/°C
FRAME POWER SUPPLY (Pin 7)					
V_7	Operating Voltage (with flyback generator)	10		58	V
I_7	Supply Current (V_7 = 30V)			22	mA
FLYBACK GENERATOR SUPPLY (PIn 2)					
V_2	Operating Voltage	10		30	V

2037A-04.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C) (continued)

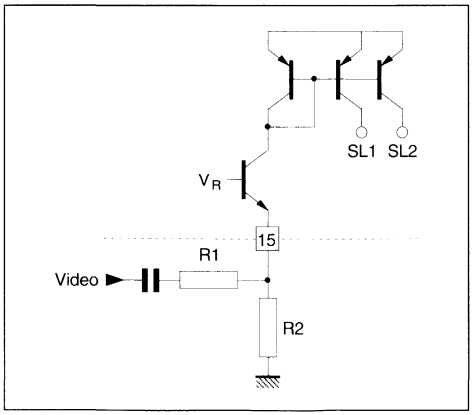
Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME OUTPUT (Pin 8)					
	Saturation Voltage to Ground (V_7 = 30V)				
LV8A	I_8 = 0.1		0.0.6	0.6	V
LV8B	I_8 = 1A		0.37	1	V
	Saturation Voltage to V_7 (V_7 = 30V)				
HV8A	I_8 = -0.1		1.3	1.6	V
HV8B	I_8 = -1A		1.7	2.4	V
	Saturation Voltage to V7 in Flyback Mode ($V_8 > V_7$)				
FV8A	I_8 = 0.1		1.6	2.1	V
FV8B	I_8 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pins 2 and 3)					
	Flyback Transistor on (output = high state) (V_2 = 30V)				
F2DA	V3/2 with $I_{3\rightarrow2}$ = 0.1A		1.5	2.1	V
F2DB	$I_{3\rightarrow2}$ = 1A		3.0	4.5	V
FSVA	V2/3 with $I_{3\rightarrow2}$ = 0.1		0.8	1.1	V
FSVB	$I_{3\rightarrow2}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V_7 - 8V) (V_7 = V_2 = 30V)				
FCI	Leakage Current Pin 2			170	µA

2037A-05.TBL

The TEA2037A performs all the video and power functions required to provide signals for the direct drive of the line darlington and frame yoke.

It contains :
- A shunt regulator
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator

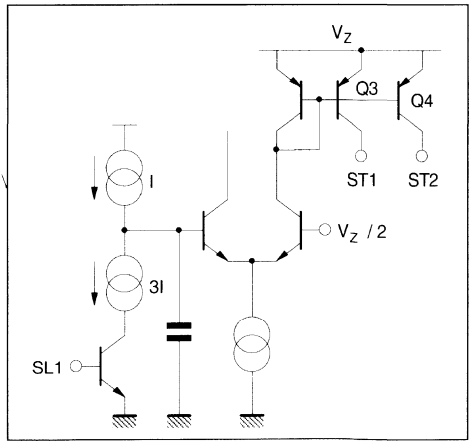
Figure 1 : Synchronization Separator Circuit



The slice level of sync-separation is fixed by value of the external resistors R_1 and R_2. V_R is an internally fixed voltage.

The sync-pulse allows the discharge of the capacitor by a 2 x 1 current. A line sync-pulse is not able to discharge the capacitor under V_Z/2. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

Figure 2 : Frame Separator



The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 3 : Line Oscillator

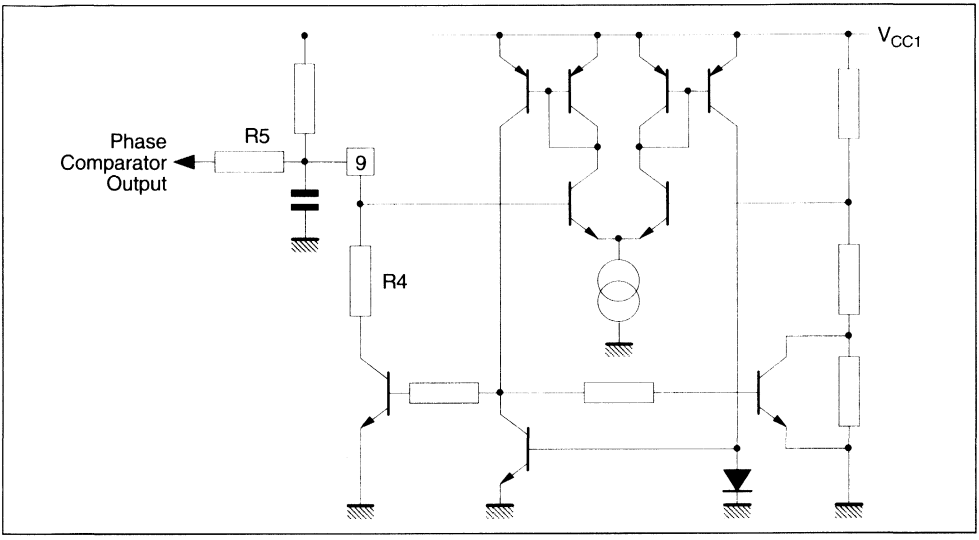
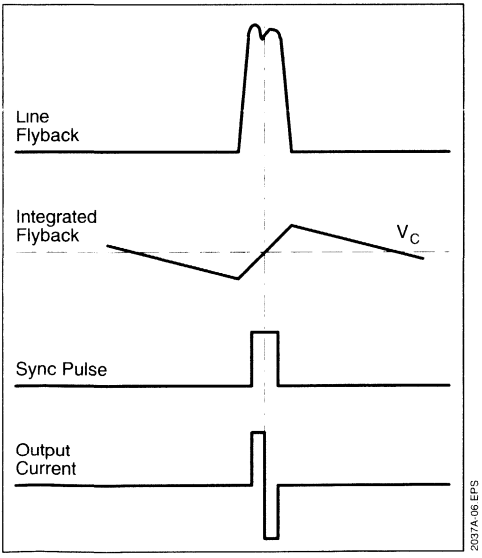
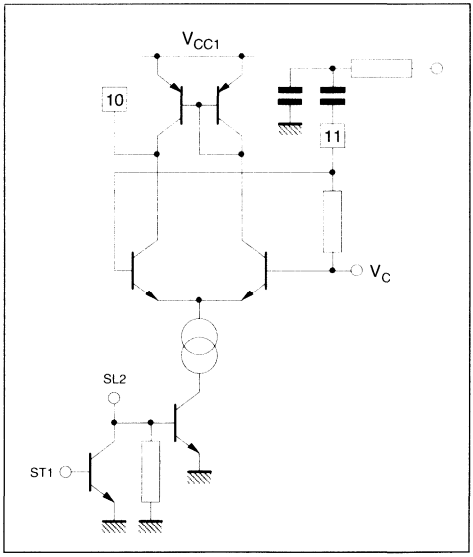


Figure 4 : Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 11 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 11 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

Figure 5



Line Output (pin 14)

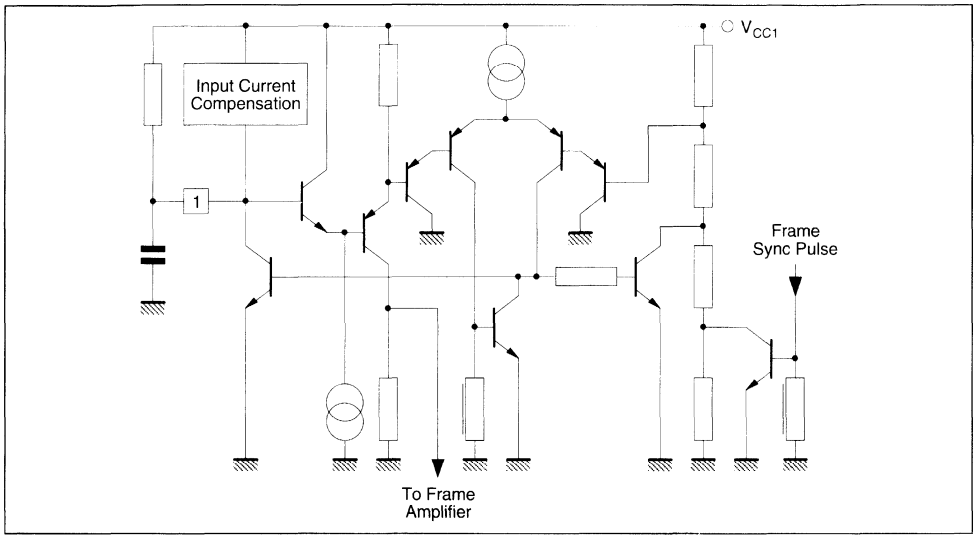
It is an open collector output which is able to drive pulse current of 800mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Frame Output Amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

Figure 6 : Frame Oscillator



TYPICAL APPLICATION FOR DISPLAY UNITS

Figure 7 : Application without flyback generator and with sync-pulse drive ; yoke : 72mH, 40W

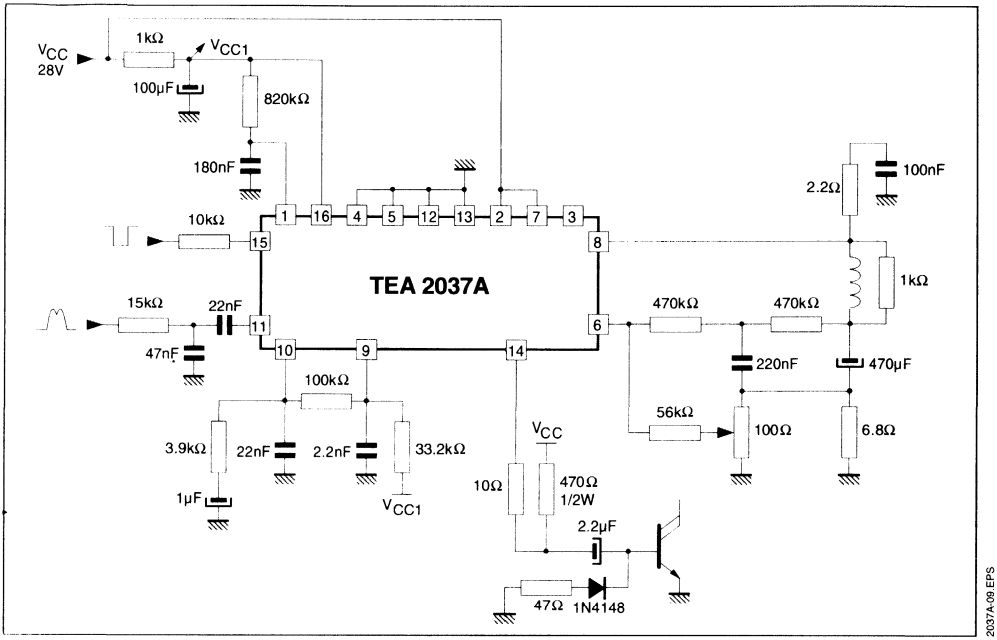
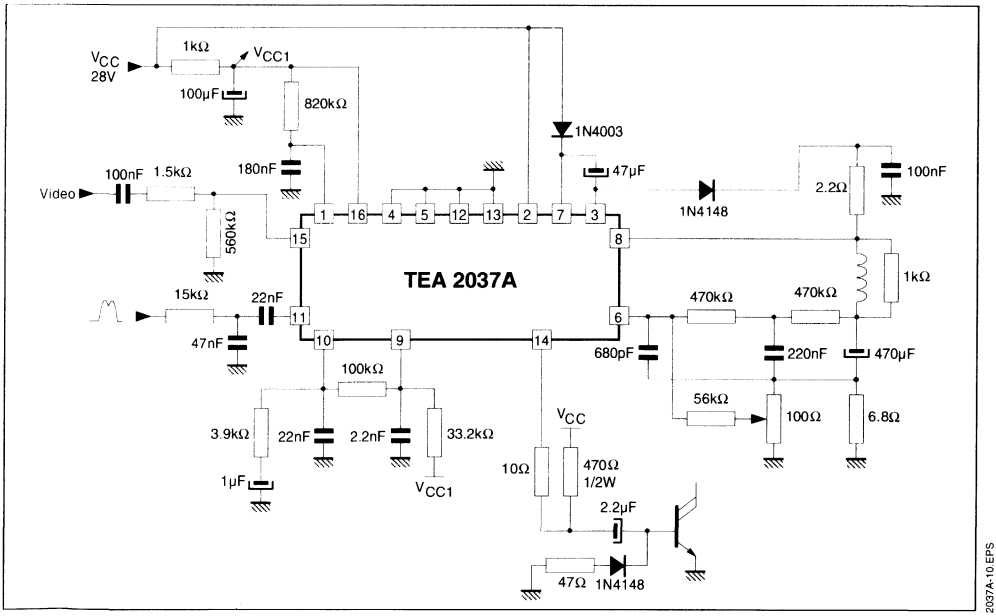


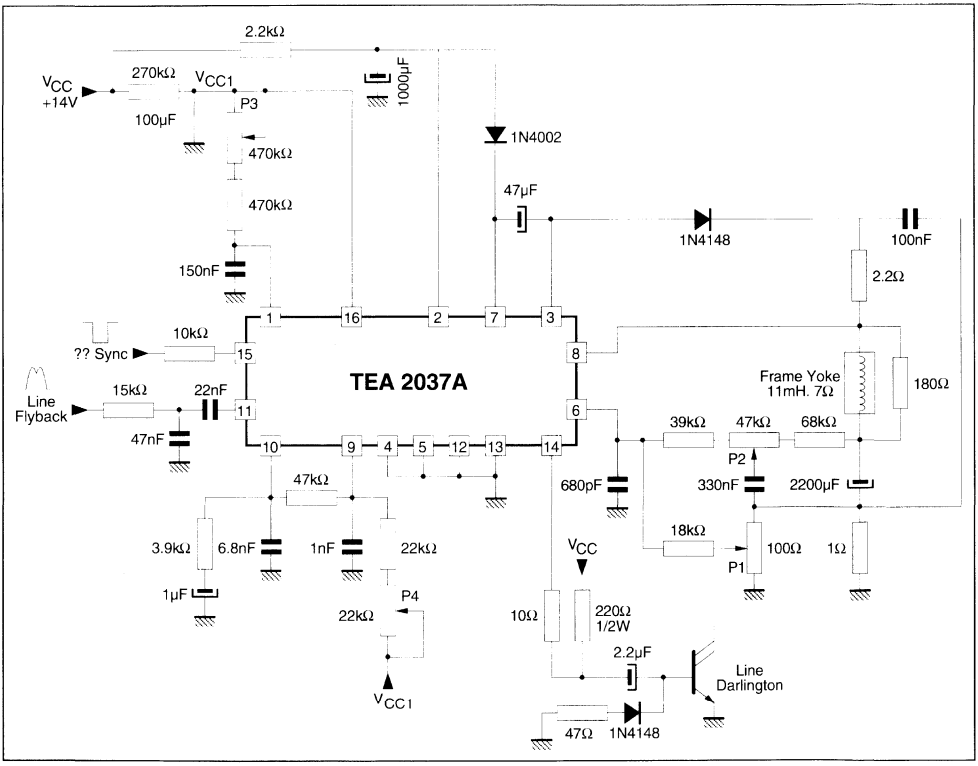
Figure 8 : Application with flyback generator and video ; yoke : 72mH, 40W



TYPICAL APPLICATION FOR HIGH FREQUENCY MONITOR

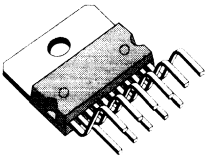
CHARACTERISTICS

- Screen : 14" Colour
- Frame deflection yoke : 11mH, 7Ω, 750mA peak–to–peak
- V_{CC} = + 14V with flyback generator
- Frame flyback time : 0.6ms
- Vertical frequency : 72Hz
- Vertical free–running period : 16ms (adjustable)
- Horizontal frequency : 35kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : ± 5µs (@ sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical Linearity
  - Vertical frequency
  - Horizontal frequency



HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT FRAME YOKE DRIVE ± 1.5A DRIVING CURRENT
- LINE DARLINGTON DRIVING CAPABILITY
- BUILT-IN FRAME SEPARATOR WITHOUT EXTERNAL COMPONENTS
- INTEGRATED FLYBACK GENERATOR
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- VERY FEW EXTERNAL COMPONENTS
- HIGH DISSIPATION POWER PACKAGE
- SEPARATE POWER GROUND
- HORIZONTAL OSCILLATOR FREQUENCY RANGE FROM 15kHz TO 100kHz
- VERTICAL OSCILLATOR FREQUENCY RANGE FROM 30Hz TO 120Hz



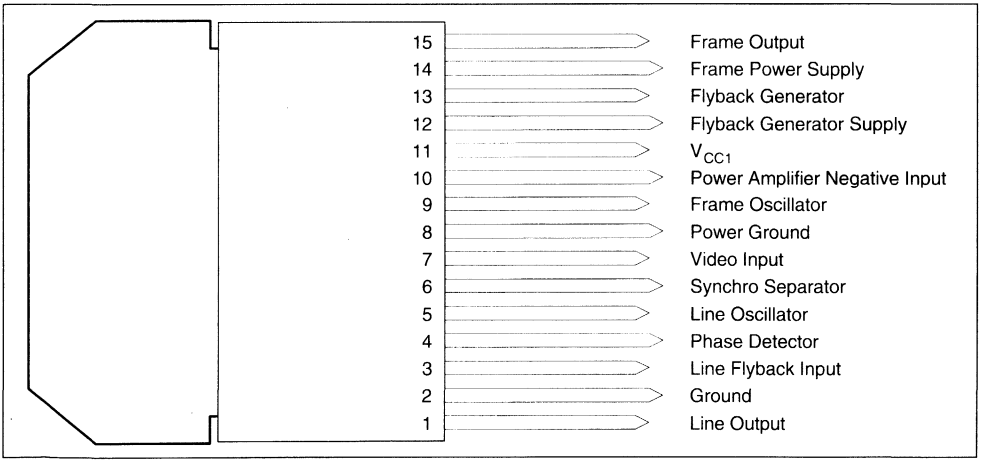
MULTIWATT 15
(Plastic Package)

ORDER CODE : TDA2117

DESCRIPTION

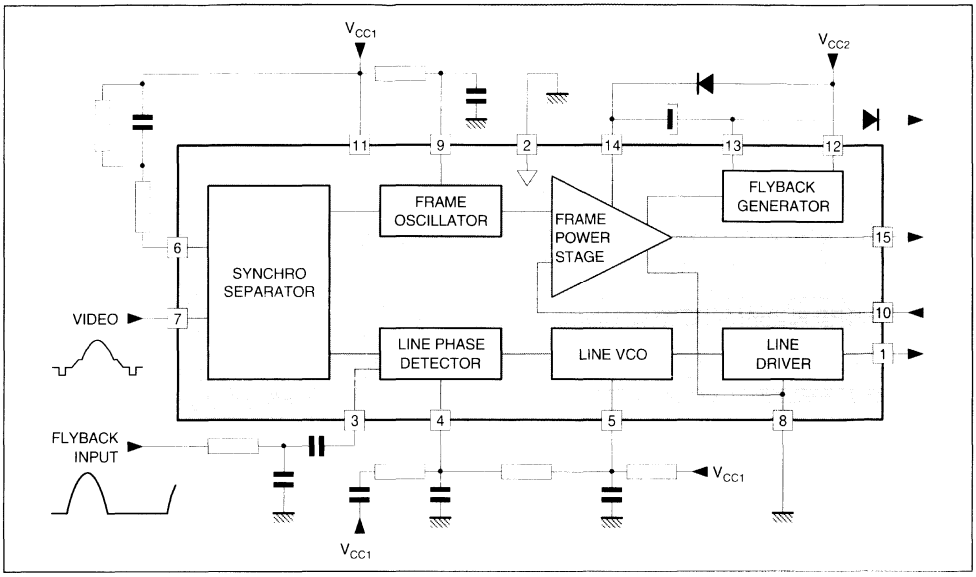
The TEA2117 is an horizontal and vertical deflection circuit. It is particularly intended for display video units. The TEA2117, with separate power ground, is particularly well-suited for high current applications.

PIN CONNECTIONS



2117-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATNGS

Symbol	Parameter	Value	Unit
V_{CC1}	Supply Voltage	20	V
V_{12}	Flyback Generator Supply Voltage	30	V
V_{14}	Frame Power Supply Voltage	60	V
I_{15}	Frame Output Current	± 1.5	A
V_1	Line Output Voltage (external)	60	V
I_{P1}	Line Output Peak Current	0.8	A
I_{C1}	Line Output Continuous Current	0.4	A
T_{stg}	Storage Temperature	– 40, + 150	°C
T_j	Max Operating Junction Temperature	150	°C

2117-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}c)}$	Max Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j\text{-}a)}$	Typical Junction-ambient Thermal Resis.	40	°C/W
T_j	Max Recommended Junction Temperature	120	°C

2117-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC1} = 10V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 11)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	8		20	V
VIDEO INPUT (Pin 7)					
V_7	Input Threshold Voltage (I_7 = – 1µA)		4		V
	Video Input Signal (see application diagram)	0.4		4	Vpp

2117-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25°C, V_{CC1} = 10V

Symbol	Parameter	Min.	Typ.	Max.	Unit
LINE FLYBACK INPUT (Pin 3)					
V_3	Bias Voltage		2.7		V
Z_3	Input Impedance	4.5	6	8	kΩ
PHASE COMPARATOR (Pin 4)					
I_4	Output Current During Synchro Pulse		± 600		µA
I_{4R}	Current Ratio (positive/negative)	0.9	1.0	1.1	
LI4	Leakage Current	− 1		+ 1	µA
	Control Range Voltage	2.5		7	V
	Control Sensibility (see application diagram)		750		Hz/µs
	Pull in Range (see application diagram)		± 800		Hz
LINE OSCILLATOR (Pin 5)					
LT5	Low Threshold Voltage		3.2		V
HT5	High Threshold Voltage		6.6		V
BI5	Bias Current		50		nA
DR5	Discharge Impedance		800		Ω
FLP1	Free Running Line Period (R = 12kΩ tied to V_{CC1}, C = 6.8nF tied to Ground)	61.5	64	66.5	µs
FLP2	Free Running Line Period (R = 12.3kΩ, C = 2.2nF)		27		µs
0T5	Oscillator Threshold for Line Output Pulse Triggering		5		V
$\frac{\Delta T}{\Delta V}$	Supply Voltage Influence on Free-running Period		0.051		µs/V

T_{amb} = 25°C, V_{CC1} = 10V, V_{14} = 30V

Symbol	Parameter	Min.	Typ.	Max.	Unit
LINE OUTPUT (Pin 1)					
LV1	Saturation Voltage to Ground (I_1 = 200mA)		1.1	1.5	V
CPW	Output Pulse Width (line period = 64µs)	20	22	24	µs
FRAME OSCILLATOR (Pin 9)					
LT9	Low Threshold Voltage	1.8	2	2.3	V
HT9	High Threshold Voltage	2.6	3.1	3.6	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance		500		Ω
FFP1	Free Running Frame Period (R = 845kΩ tied to V_{CC1}, C = 180nF tied to Ground)	21.4	22.5	25	ms
FFP2	Free Running Frame Period (R = 425kΩ, C = 220nF)		14.3		ms
MFP	Minimum Frame Period (I_7 = − 100µA) with the Same RC	14.6	17	19	ms
FG	Frame Sawtooth Gain between Pin 9 and Non-inverting Input of the Frame Amplifier (internal)		− 0.4		
FRAME POWER SUPPLY (Pin 14)					
V_{14}	Operating Voltage (with flyback generator)	10		58	V
I_{14}	Supply Current (V_{14} = 30V)		16	25	mA
FLYBACK GENERATOR SUPPLY (Pin 12)					
V_{12}	Operating Voltage	10		30	V
FRAME OUTPUT					
LV15A	Saturation Voltage to Ground I_{15} = 0.1A		60		mV
LV15B	I_{15} = 1A		0.4	0.8	V

2117-04.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC1} = 10V, V_{14} = 30V) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME OUTPUT (continued)					
	Saturation Voltage to V_{CC2}				
HV15A	I_{15} = – 0.1A		1.3		V
HV15B	I_{15} = – 1A		1.7	2.4	V
	Saturation Voltage to V_{CC2} in Flyback Mode ($V_{15} > V_{14}$)				
FV15A	I_{15} = 0.1A		1.7		V
FV15B	I_{15} = 1A		2.6	4	V
FLYBACK GENERATOR (Pins 12 and 13)					
	Flyback Transistor on (output = high state) V13/12 with				
F2DA	$I_{13} > I_{12}$ = 0.1A		1.6		V
F2DB	$I_{13} \rightarrow I_{12}$ = 1A		3	4	V
	Flyback Transistor on (output = high state) V12/13 with				
FSVA	$I_{12} \rightarrow I_{13}$ = 0.1A		0.9		V
FSVB	$I_{12} \rightarrow I_{13}$ = 1A		2	4	V
	Flyback Transistor off (output = V_{14} – 8V) $V_{12} = V_{14}$ = 30V				
FCI	Leakage Current Pin 12			100	µA

2117-05.TBL

GENERAL DESCRIPTION

The TEA2117 performs all of the video and power functions required to provide signals for the direct drive of a line darlington and the frame yoke.

It contains :

- A synchronizing separator with the slice level of synchro separation determined by the external components.
- An integrated frame synchronizing separator without external components.
- A saw tooth generator for the frame with synchronization allowed during the last fourth of the free run period.
- A power amplifier for direct drive of the frame yoke with overload, short circuit and thermal protections.
- A line phase detector and a voltage control oscillator.
- An open collector output for the direct drive of a line darlington.
- Separate power ground (Pin 8)

SYNCHRONIZATION SEPARATOR CIRCUIT (Figure 1)

The sync-tip DC level on pin 7 is clamped to 3.8V. The slice level of sync-separation present on capacitor C1 depends on the value of resistor R1 and R2. When the video signal on pin 7 decreases under the capacitor voltage the transistors Q1 and Q2 provide current for the other parts of the circuit.

FRAME SEPARATOR (Figure 2)

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR (Figure 3)

The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The voltage control is applied on resistor R5.

PHASE COMPARATOR (Figure 4)

The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 3 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 3 superior to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternately negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning. (see Figure 5)

LINE OUTPUT (Pin1)

It is an open collector output which is able to drive pulse current of 500mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

FRAME OSCILLATOR (Figure 6)

The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last fourth of the free run period. The input current during the charge of the capacitor is less than 100nA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.
Its positive input is directly connected to the invert of the frame saw tooth.

Figure 1

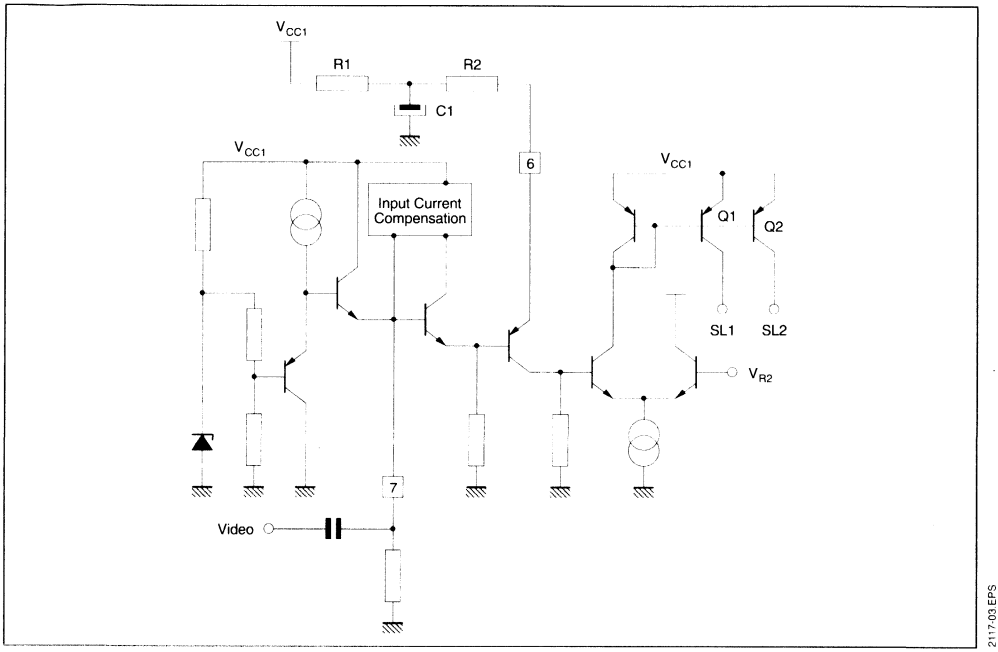


Figure 2

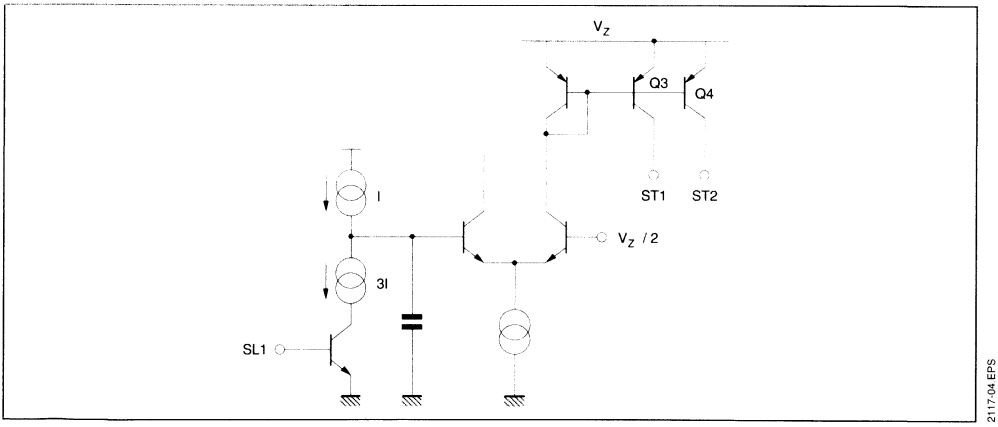


Figure 3

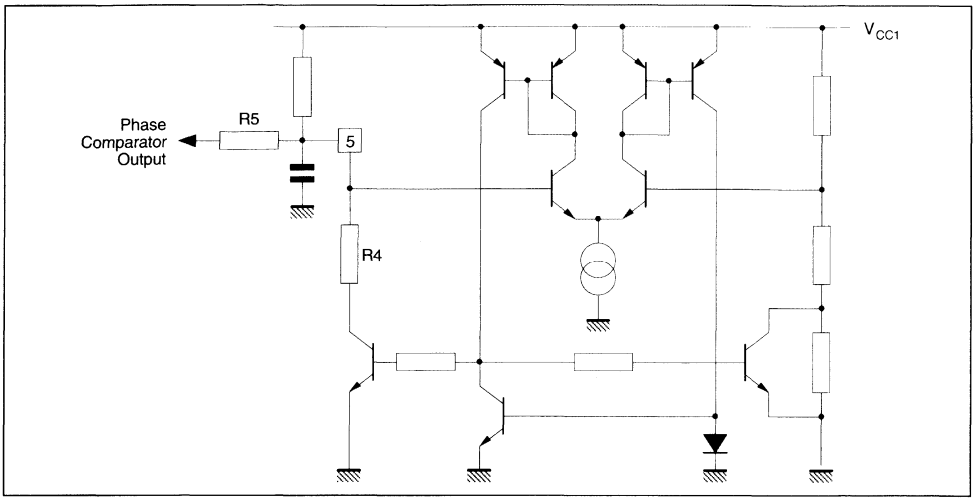


Figure 4

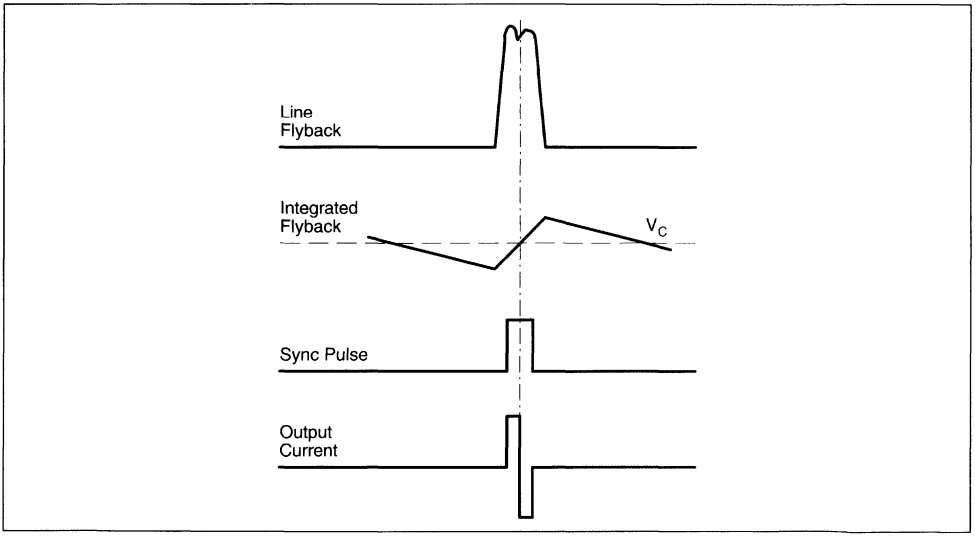
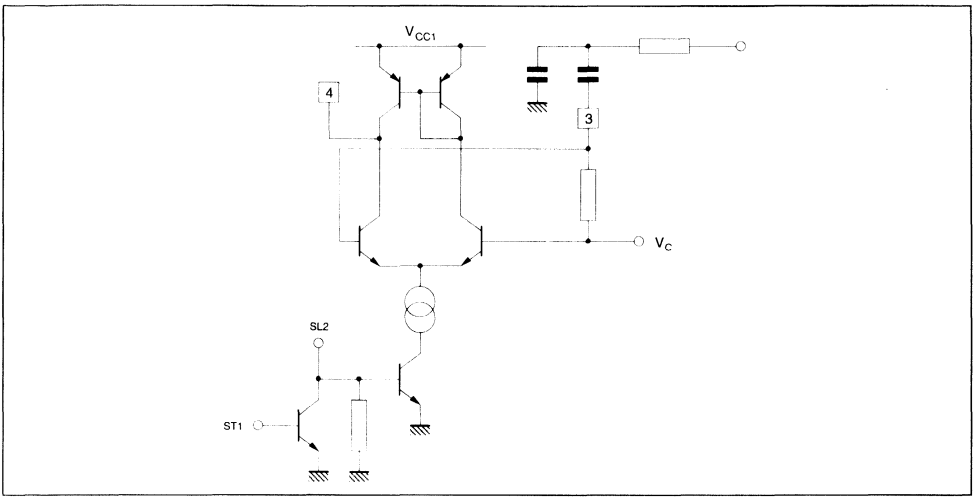
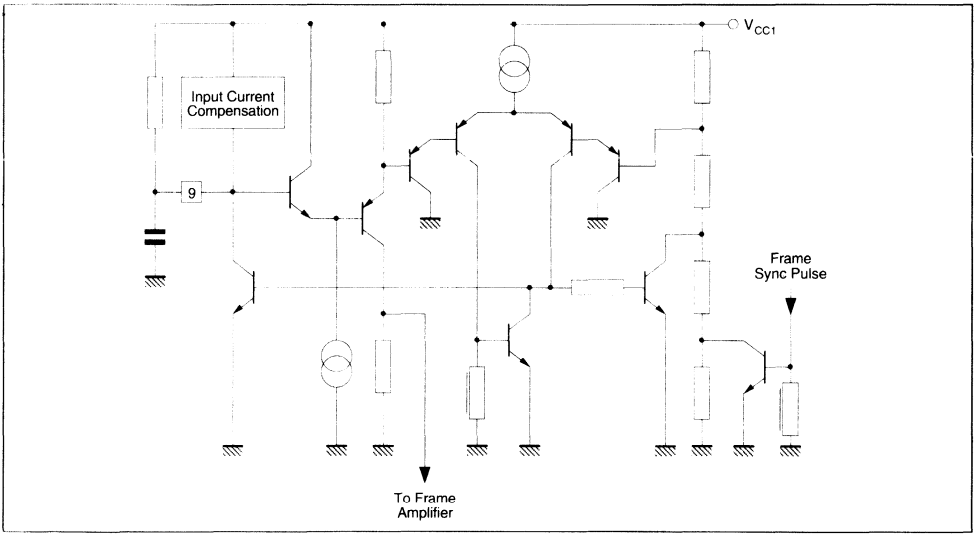


Figure 5



2117-07 EPS

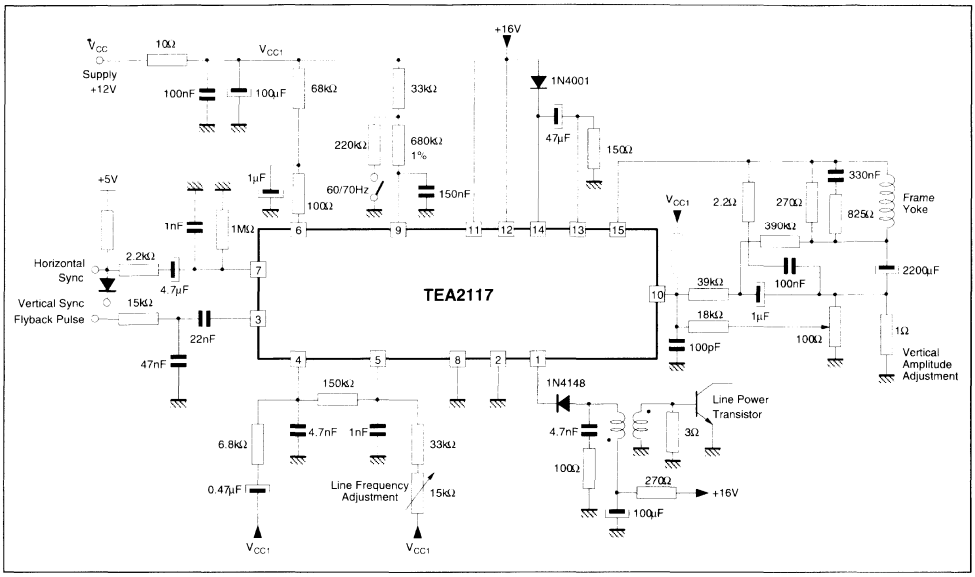
Figure 6



2117-08 EPS

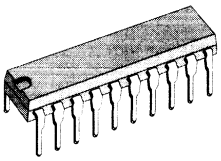
APPLICATION DIAGRAM (without internal flyback generator)

TYPICAL BLACK-WHITE MONITOR APPLICATION FOR 14" - 90° SCREEN
(with yoke L = 5.8mH, R = 2.7Ω, I_{PP} = 2A), f_H = 31.kHz, f_V = 60/70Hz



TV AND SATELLITE DECODER SCANNING PROCESSOR

- AUTOMATIC TIME CONSTANT SWITCHING FOR VCR
- DIGITAL VIDEO IDENTIFICATION CIRCUIT
- 500kHz RESONATOR OSCILLATOR
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- SUPER SANDCASTLE OUTPUT
- AUTOMATIC 50Hz/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- FRAME SAFETY INPUT
- FRAME SAWTOOTH GENERATOR
- FULLY ESD AND LATCH-UP PROTECTED



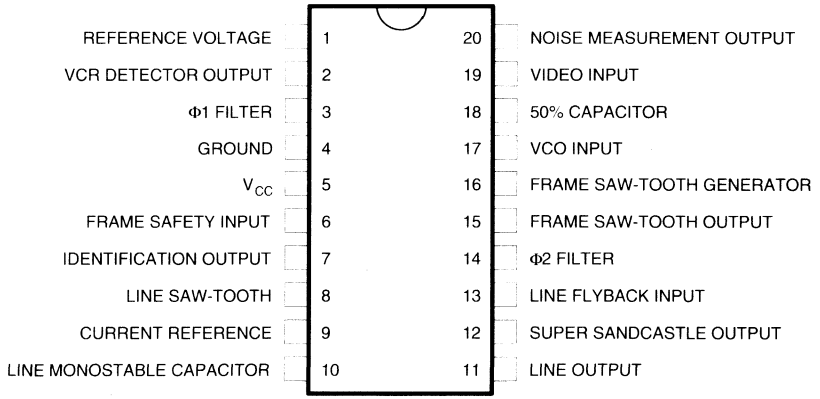
DIP20
(Plastic Package)

ORDER CODE : TEA2130

DESCRIPTION

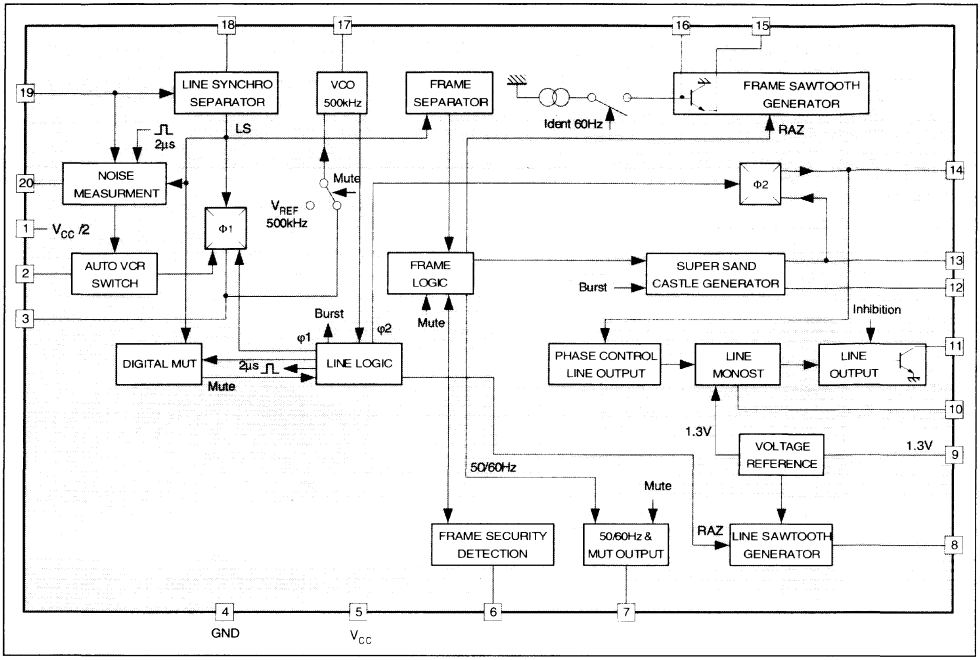
The TEA2130 is a complete (horizontal and vertical) deflection processor, for TV applications and all applications which require a flexible, high performance scanning processor (Satellite Decoder, Video Multimedia).

PIN CONNECTIONS



2130-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

Introduction

This integrated circuit uses high density I2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoid the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produces very accurate defined sampling pulses and the necessary timing signals.

Internal Functions

- Horizontal scanning processor
- Frame scanning processor
- B class frame output stage using an external power amplifier with flyback generator
- Line and frame synchronization separation
- Dual phase-locked loop horizontal scanning
- High performance frame and line synchronization with interlacing control.
- Supersandcastle generator with reduced burst gate pulse for 60Hz
- Automatic 50Hz / 60Hz standard identification
- Frame saw-tooth generator
- Digital video identification circuit
- Very steady free running mode of the line and frame oscillator when no video is detected. This allows on screen display without phase Jitter in research mode of the tuner
- Automatic VCR mode recognition for time constant switching
- Frame safety input

WORKING DESCRIPTION

Synchronization Separator

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signal in noise conditions.

Frame Synchronization

Frame synchronization is fully integrated (no external capacitor required).
The frame timing identification logic permits automatic adaptation to 50-60Hz standards or non-interlaced video.

An automatic synchronization window width system provides:
- Fast frame capture (7.3ms wide window)
- Good noise immunity (0.4ms narrow window)

The internal generator starts the discharge of the sawtooth generator capacitor, so that it is not disturbed by line flyback effects.
Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line flyback. A 32µs timing is automatically applied on standardized transmissions for perfect interlacing.
In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

Horizontal Scanning

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two PLL:
- The first one controls the frequency
- The second one controls the relative phase of the output line pulse and the line flyback signals.

The output pulse has a constant duration of 29µs, independent of V_{CC} and of any delay in switching-off the scanning transistor.

Supersandcastle Generator

This output delivers a 3 level synchronization signal:
- Burst level
- Line blanking level
- Frame blanking level

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame Scanning

The current to charge the frame sawtooth generator is automatically switched to 60Hz operation to maintain constant amplitude.

Automatic VCR Mode Recognition for Time Constant Switching

- A third phase comparator is used to detect VCR signals and to switch the $\phi 1$ short time constant.
- A noise level measurement is realized on the video synchronization pulse to inhibit the short time constant if the noise level is superior to an adjustable threshold.
- VCR signals are detected if peak to peak signal on pin 2 is superior to an internal threshold.

This threshold is depending on the noise level. So with a no noisy video signal, the auto VCR switch sensitivity is maximum, and it decreases when the noise increases.
- The sensitivity of the noise gate and the auto VCR switch is adjustable by external resistance.
- Long and short time constants can be selected manually by Pin 20.

Digital Video Identification

A digital circuit controls the identification signal. When identification signal is low, the line oscillator is set on a reference frequency. When identification signal is high, $\phi 1$ is locked and the catching phase can start. So that, the TEA2130 allowed on screen displays in a steady way even without video signal (during tuner research for example).

Identification Output

The identification function provides three different levels :
- 0V : No video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	13.5	V
V_{16}	Pulse/Frame Sawtooth Generator Voltage	V_{CC} - 3	V
I_{11}	Output Current	40	mA
I_{13}	Input Current	± 5	mA
T_{AMB}	Operating Ambient Temperature	0 , + 70	°C

2130-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

2130-02.TBL

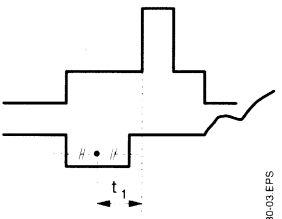
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Supply Voltage			12		V
	Supply Current	Without load in pins 7-12-15	20	29	40	mA
	V_{CC} Starting Voltage for Line Output	V_{CC} rising		7	7.5	V
	Switch-off Voltage for Line Output	V_{CC} decreasing		6.5		V
VIDEO INPUT (Pin 19)						
	Video Signal Amplitude	Z source < 220Ω	0.2	1	3	V_{PP}
	Push out Current	During the synch. pulse	- 40	- 32	- 24	µA
	Pull in Current	During the line	3	5	7	µA
50% SYNCH. PULSE CLAMP (Pin 18)						
	Push out Current	During the synch. pulse	- 960	- 350	- 40	µA
	Pull in Current	During the line	15	23	32	µA
ϕ 1 AND ϕ 3 COMPARATOR (Pin 2- Pin 3)						
	Short Time Output Current	Identification high	± 1.1	± 1.5	± 2	mA
	Long Time Output Current	Identification high	± 0.30	± 0.48	± 0.65	mA
VCO (Pin 17)						
	Catching Range	Ceramic CSB 503B R_{SERIAL} = 470Ω	15.40		15.92	kHz
	Transfer Characteristic	ΔF pin 11/ΔV pin 3		2		kHz/V
	Free Running Frequency	Without video signal	15.6	15.9	16.2	kHz
VIDEO IDENTIFICATION AND STANDARD OUTPUT (Pin 7)						
	No video on Pin 19	R_{LOAD}/GND = 5kΩ		0	500	mV
	60Hz video		5.5	6	6.5	V
	50Hz video		10.5	11.3		V
REFERENCE VOLTAGE (Pin 1)						
	Output voltage	I_1 = 0	5.5	6	6.5	V
	Output impedance	ΔI_1 = ± 50µA	400	600	800	Ω
	Max output current				200	µA
AUTO VCR SWITCH (Pin 2)						
	V Switching threshold /V_1 Short time ct2 on φ1 PM Active above Threshold	• With no noise on the video (V_{20} < 6V)	± 0.2	± 0.3	± 0.4	V
		• With noise on video (6V < V_{20} < 7.3V	0.69 x V20 - 3.85			V
NOISE GATE (Pin 20)						
	Measure sampling time	On the synch. pulse bottom	1	2	3	µs
	Max. push out current	Vnoise = 0.4V_{PP}, F = 1MHz on 2V_{PP} Video Signal		350		µA
	VCR mode inhibition threshold (long time cte)	Active above threshold Voltage hysteresis	6.9	7.3 100	7.5	V mV
	Measure bandwidth (-3dB)	High cut frequency Low cut frequency		2 0.7		MHz MHz
	Short time constant manual switching threshold	Active under threshold	4.5	5	5.5	V

2130-03 TBL

ELECTRICAL CHARACTERISTICS (continued)

(T_{amb} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
φ 2 COMPARATOR (Pin 14)						
	Output current	During line flyback	± 300	± 500	± 700	µA
	Delay between φ 2 falling edge and the middle video sync. pulse	F_{VCO} = 500 kHz	2.2	2.7	3.2	µs
LINE MONOSTABLE (Pin 10)						
	Charge current	Line output high		- 67		µA
	Discharge current	Line output low		170		µA
	Flip-Flop threshold	Falling edge on the line output		1.3		V
LINE OUTPUT (Pin 11)						
	Low level	I_{11}= 20 mA			1	V
	Pulse duration	R_9 = 3.32kΩ , C_{10} = 1.5nF	27	29.5	32	µs
	φ 2 adjustment range	Controlled by V_{14} compared with video signal	15	18		µs
LINE SAW-TOOTH (Pin 8)						
	Charge Current	R_9 = 3.32 kΩ	- 200	- 180	- 150	µA
	Discharge Current		3.5	7		mA
	Discharge Duration	Controlled by logic VCO 500kHz		6.5		µs
LINE FLYBACK INPUT (Pin 13)						
	Blanking Line Threshold	Active above threshold	0.35	0.4	0.6	V
	φ 2 Loop Threshold and Line Output Inhibition (Pin 11)	Active above threshold	2.7	3	3.3	V
	Input Current	- 0.4V < V_{13} < 0.4V 0.4V < V_{13} < 3V 3V < V_{13}	- 20 - 10	-10 - 5	- 4 - 4 - 1	µA µA µA
SUPER SANDCASTLE GENERATOR (Pin 12)						
	Burst Level	R_L = 2.2 kΩ to ground	9			V
	Line Blanking Level		4	4.5	5	V
	Frame Blanking Level		2	2.5	3	V
	Delay between the midde of the video sync. pulse and the rising edge of the burst (t_1)		2.45	2.8	3.15	µs
	Burst Pulse Duration	• 50Hz • 60Hz	4.1 3.6	4.4 3.9	4.7 4.2	µs µs
	Line Blanking Duration	Fixed by flyback Signal pin 13				
	Frame Blanking Duration	Fixed by the logic		21		Line

2130-04.TBL

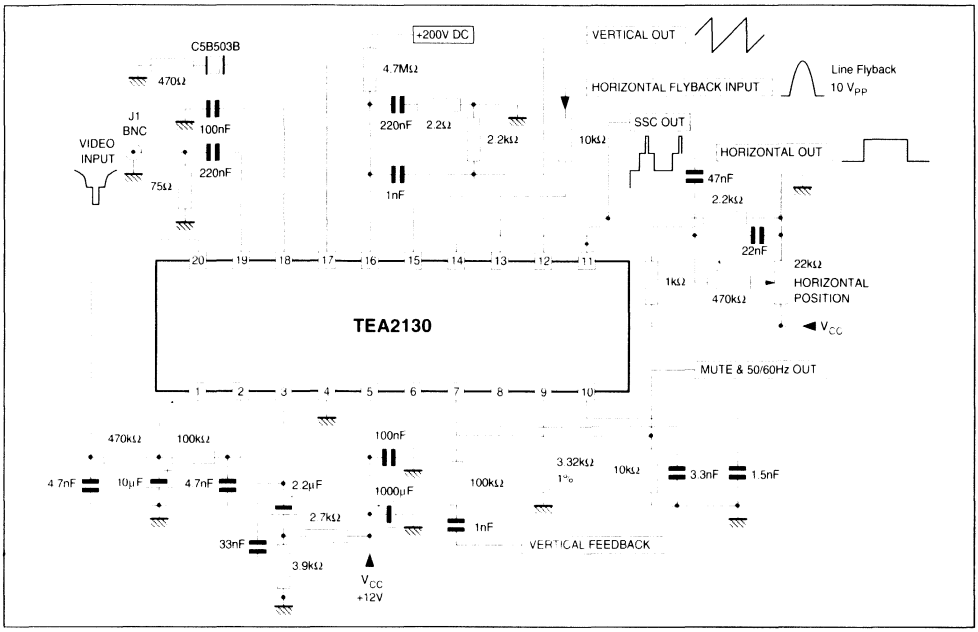
ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25°C; V_{CC} = 12V; Pulse duration 50% of the amplitude

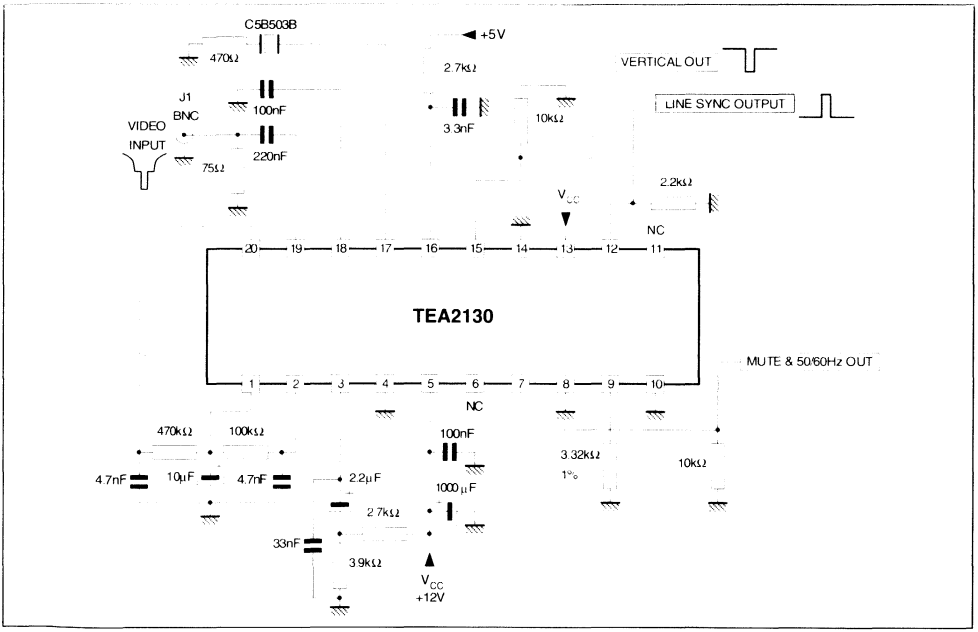
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FRAME SAW-TOOTH GENERATOR						
	Low DC Voltage		1.1	1.3	1.45	V
	Discharge Current		15		60	mA
	60Hz Internal Current		- 10	- 8	- 6	µA
FRAME LOGIC SYNCH.						
	Free Running Period	Without video signal		315		Line
	Synchronization Windows	Identification low Identification 60Hz high VCR mode	247 247 247		361 277 361	Line Line Line
CURRENT REFERENCE (Pin 9)						
	V_9 Voltage	R_9 = 3.32 kΩ (1%)	1.2	1.3	1.4	V
	Max. Temperature Shift	ΔT = 80°C		± 1		%
FRAME SAFETY INPUT (Pin 6)						
	Switching Threshold	Actived without negative pulse during frame blanking time for permanent frame blanking on SSC output Pin 12		1.3		V
	Output current		- 35	- 50	- 67	µA

2130-05.TBL

TYPICAL TV APPLICATION



TYPICAL SYNC SEPARATOR APPLICATION



SGS-THOMSON MICROELECTRONICS

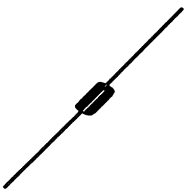
MTV32-400A

(CRT HORIZONTAL DEFLECTION) MODULATION DIODE

For complete specifications refer to "SCHOTTKY RECTIFIER DIODES"

MAIN PRODUCT CHARACTERISTICS

$I_{F\ peak}$	3A
V_{RRM}	400V
trr	22ns
V_F	1.35V



DO27A
(Plastic)

MTV32-400A

FEATURES

- PRODUCT SPECIFIC TO HORIZONTAL DEFLECTION
- HIGH REVERSE VOLTAGE
- LOW SWITCHING LOSSES DUE TO SMALL RECOVERY CHARGES

DESCRIPTION

High voltage diode especially designed for horizontal deflection stage in standard and high resolution displays for TV's and monitors.
This device is packaged in DO27A and is intented for use as a MODULATION diode in deflection circuitry with east-west correction.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		400	V
V_{RWM}	Reverse working voltage		400	V
$I_{F\ peak}$	Peak forward current (1)	T_{amb}=130°C (2)	3	A
I_{FRM}	Repetitive peak forward current	tp ≤ 10µs	60	A
I_{FSM}	Surge non repetitive forward current	tp=10ms sinusoidal	60	A
Tstg Tj	Storage and junction temperature range		- 40 to + 150 - 40 to + 150	°C °C

(1) δ = 0.5 and triangular waveform
(2) on infinite heatsink with 10mm lead length

SGS-THOMSON MICROELECTRONICS

DTV32-1000A
MTV32-600A

(CRT HORIZONTAL DEFLECTION) HIGH VOLTAGE DAMPER & MODULATION DIODES

For complete specifications refer to "SCHOTTKY RECTIFIER DIODES"

MAIN PRODUCTS CHARACTERISTICS

	MTV32	DTV32
$I_{F\ peak}$	3A	3A
V_{RRM}	600V	1000V
trr	50ns	70ns
V_F	1.6V	1.6V

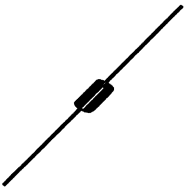
FEATURES

- PRODUCTS SPECIFIC TO HORIZONTAL DEFLECTION
- HIGH REVERSE VOLTAGE
- LOW SWITCHING LOSSES DUE TO SMALL RECOVERY CHARGES
- FULL KIT IN AXIAL PACKAGE

DESCRIPTION

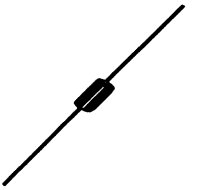
High voltage diodes especially designed for horizontal deflection stage in standard and high resolution displays for TV's and monitors.
The kit includes both the DAMPER diode and the MODULATION diode. These devices are packaged in DO27A and are intented for use as a low cost kit solution in deflection circuitry with east-west correction.

KIT



DO27A
(Plastic)

MTV32-600A



DO27A
(Plastic)

DTV32-1000A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value		Unit
			MTV32	DTV32	
V_{RRM}	Repetitive peak reverse voltage		600	1000	V
V_{RWM}	Reverse working voltage		600	1000	V
$I_{F\ peak}$	Peak forward current (1)	T_{amb}=120°C (2)	3	3	A
I_{FRM}	Repetitive peak forward current	tp ≤ 10µs	100	50	A
I_{FSM}	Surge non repetitive forward current	tp=10ms sinusoidal	150	150	A
Tstg Tj	Storage and junction temperature range		- 40 to + 150 - 40 to + 150		°C °C

(1) δ = 0.5 and triangular waveform
(2) on infinite heatsink with 10mm lead length

SGS-THOMSON MICROELECTRONICS

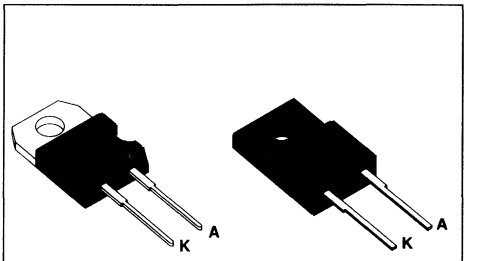
DTV32(F)-1200A
DTV32(F)-1500A

(CRT HORIZONTAL DEFLECTION) HIGH VOLTAGE DAMPER DIODE

For complete specifications refer to "SCHOTTKY RECTIFIER DIODES"

FEATURES

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- LOW AND MEDIUM FREQUENCY OPERATION
- SPECIFIED TURN ON SWITCHING CHARACTERISTICS
- TYPICAL TOTAL LOSSES : 2 W (I_{Fpeak} = 6 A, F = 32 kHz)
- SUITABLE WITH **BUH** TRANSISTORS SERIES
- INSULATED VERSION (ISOWATT220AC) : Insulating voltage = 2000 V DC Capacitance = 12 pF



TO220AC (Plastic)	ISOWATT220AC (Plastic)
DTV32-1200A DTV32-1500A	DTV32F-1200A DTV32F-1500A

DESCRIPTION

High voltage diode especially designed for horizontal deflection stage in standard and high resolution displays for TV's and monitors.
This device is packaged in TO220AC or ISOWATT220AC.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
$I_{F(RMS)}$	RMS forward current			15	A
$I_{F(AV)}$	Average forward current δ = 0.5	TO220AC	Tc=130°C	6	A
		ISOWATT220AC	Tc=115°C	6	
I_{FSM}	Surge non repetitive forward current		tp=10ms sinusoidal	100	A
Tstg Tj	Storage and junction temperature range			- 40 to + 150 - 40 to + 150	°C °C

Symbol	Parameter	DTV32(F)-		Unit
		1200A	1500A	
V_{RRM}	Repetitive peak reverse voltage	1200	1500	V
V_{RWM}	Reverse working voltage	1000	1350	V

SGS-THOMSON MICROELECTRONICS

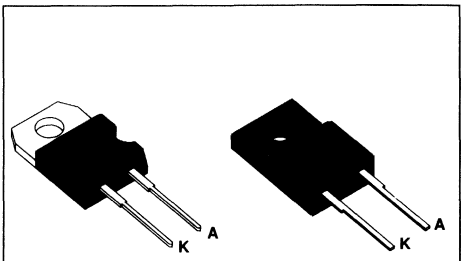
DTV32(F)-1200B
DTV32(F)-1500B

(CRT HORIZONTAL DEFLECTION) HIGH VOLTAGE DAMPER DIODE

For complete specifications refer to "SCHOTTKY RECTIFIER DIODES"

FEATURES

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- HIGH FREQUENCY OPERATION
- SPECIFIED TURN ON SWITCHING CHARACTERISTICS
- TYPICAL TOTAL LOSSES : 3.5W (I_{Fpeak} = 6 A, F = 64 kHz)
- SUITABLE WITH **BUH** TRANSISTORS SERIES
- INSULATED VERSION (ISOWATT220AC) : Insulating voltage = 2000 V DC Capacitance = 12 pF



TO220AC (Plastic)

DTV32-1200B
DTV32-1500B

ISOWATT220AC (Plastic)

DTV32F-1200B
DTV32F-1500B

DESCRIPTION

High voltage diode especially designed for horizontal deflection stage in standard and high resolution displays for TV's and monitors.
This device is packaged in TO220AC or ISOWATT220AC.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
$I_{F(RMS)}$	RMS forward current			15	A
$I_{F(AV)}$	Average forward current δ = 0.5	TO220AC	Tc=130°C	6	A
		ISOWATT220AC	Tc=110°C	6	
I_{FSM}	Surge non repetitive forward current		tp=10ms sinusoidal	100	A
Tstg Tj	Storage and junction temperature range			- 40 to + 150 - 40 to + 150	°C °C

Symbol	Parameter	DTV32(F)-		Unit
		1200B	1500B	
V_{RRM}	Repetitive peak reverse voltage	1200	1500	V
V_{RWM}	Reverse working voltage	1000	1350	V

SGS-THOMSON MICROELECTRONICS

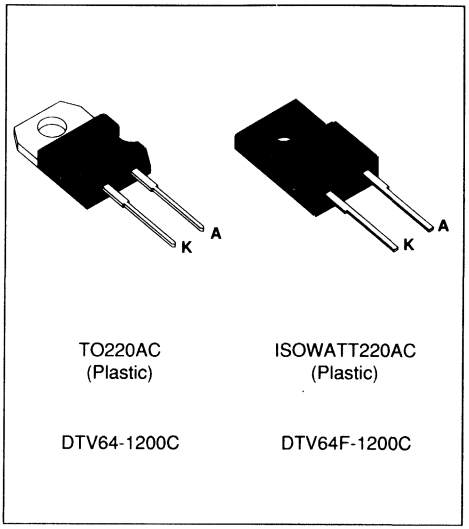
DTV64(F)-1200C

(CRT HORIZONTAL DEFLECTION) HIGH VOLTAGE DAMPER DIODE

For complete specifications refer to "SCHOTTKY RECTIFIER DIODES"

FEATURES

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- MEDIUM & HIGH FREQUENCY OPERATION
- SPECIFIED TURN ON SWITCHING CHARACTERISTICS
- TYPICAL TOTAL LOSSES : 3 W (I_{Fpeak} = 6 A, F = 64 kHz)
- SUITABLE WITH **BUH** TRANSISTORS SERIES
- INSULATED VERSION (ISOWATT220AC) : Insulating voltage = 2000 V DC Capacitance = 12 pF



TO220AC (Plastic) — DTV64-1200C

ISOWATT220AC (Plastic) — DTV64F-1200C

DESCRIPTION

High voltage diode especially designed for horizontal deflection stage in standard and high resolution displays for TV's and monitors.
This device is packaged in TO220AC or ISOWATT220AC.

ABSOLUTE MAXIMUM RATINGS

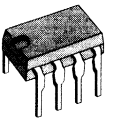
Symbol	Parameter			Value	Unit
V_{RRM}	Repetitive peak reverse voltage			1200	V
V_{RWM}	Repetitive working voltage			1200	V
$I_{F(RMS)}$	RMS forward current			20	A
$I_{F(AV)}$	Average forward current δ = 0.5	TO220AC	Tc=120°C	6	A
		ISOWATT220AC	Tc=90°C	6	
I_{FSM}	Surge non repetitive forward current		tp=10ms sinusoidal	100	A
Tstg Tj	Storage and junction temperature range			- 40 to + 150 - 40 to + 150	°C °C

SGS-THOMSON MICROELECTRONICS

TDA4950

TV EAST/WEST CORRECTION CIRCUIT

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT
- EXTERNAL KEYSTONE ADJUSTMENT (symmetry of the parabola)
- INPUT FOR DYNAMIC FIELD CORRECTION (beam current change)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY REDELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAWTOOTH



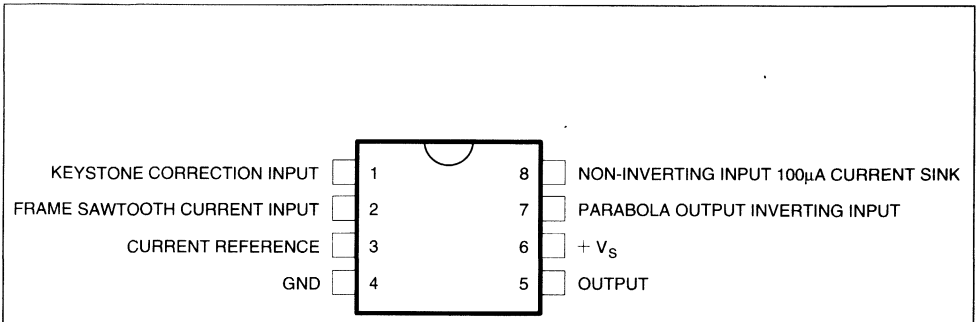
DIP8
(Plastic Package)

ORDER CODE : TDA4950

DESCRIPTION

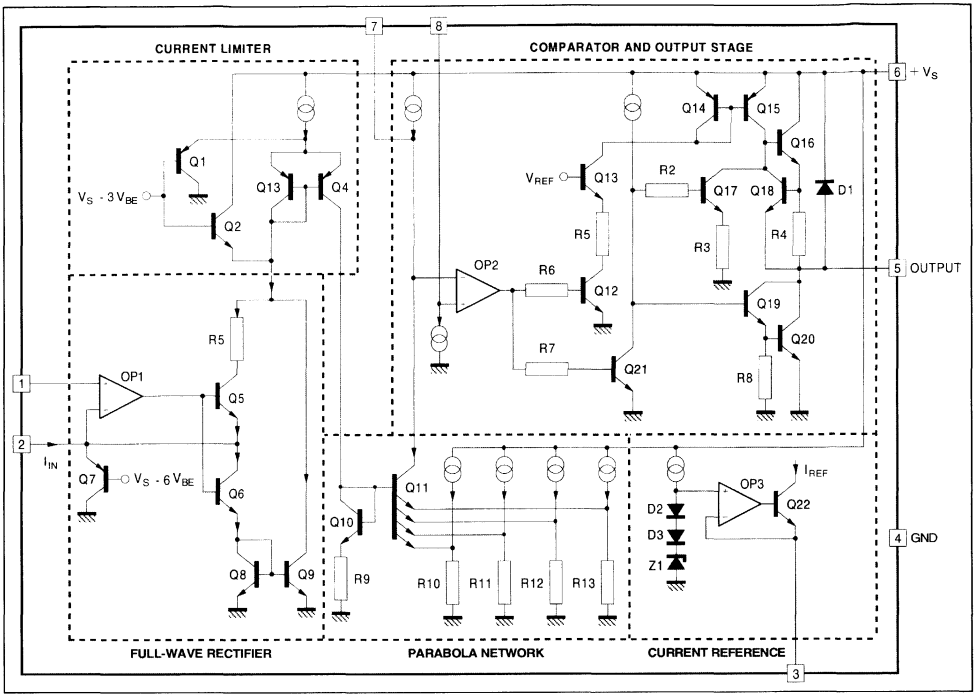
The TDA4950 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

PIN CONNECTIONS



4950-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
I_S	Supply Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 70 °C	800	mW
T_{stg}, T_j	Storage and Junction Temperature	– 25, +150	°C

4950-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}a)}$	Thermal Resistance Junction-ambient	Max.	100	°C/W
$R_{th\ (j\text{-}c)}$	Thermal Resistance Junction-pin (4)	Max.	70	°C/W

4950-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 26 V, V_{fr} = 0, S1 and S2 in "a" position, refer to test circuit unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		17	24	30	V
I_S	Supply Current			4.5	7	mA
V_{ref}	Internal Reference Voltage		7.6	8.0	8.8	V
$-I_{ref}$	Internal Reference Current	$V_{ref}/R3$		0.73		mA
$V_{7(A)}$	Pin 7 Output Voltage	I_{fr} = 0 µA, see Figure 2	15.3	16.0	16.7	V
$V_{7(B)}$	Pin 7 Output Voltage	I_{fr} = 30 µA, see Figure 2		15		V

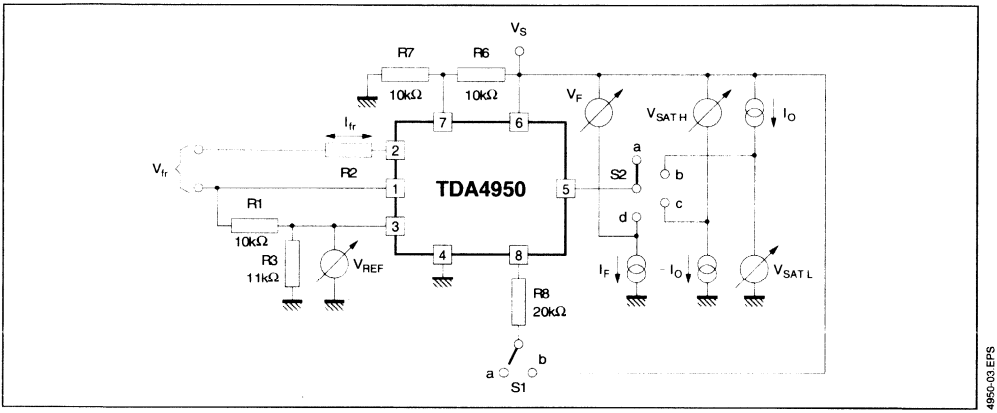
4950-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 26 V, V_{fr} = 0, S1 and S2 in "a" position, refer to test circuit unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K1	Parabola Coefficient	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$, see Figure 2		0.28		
K_2	Parabola Coefficient	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$, see Figure 2		0.71		
ΔV_7 (*)		$\Delta V_7 = V_{7E} - V_{7F}$, see Figure 2	- 40		40	mV
I_8	Current Source	S1 → b		100		µA
V_{SATL}	Saturation Voltage	Io = 400 mA Sink S2 → b		1	2	V
V_{SATH}	Saturation Voltage	Io = 100 mA Source S2 → c S1 → b		0.8	1.5	V
V_F	Forward Voltage	I_o = 400 mA S2 → d S1 → b		1.2	1.7	V
I_{fr}	Frame Sawtooth Current	V_{fr} = 6.6 V_{PP}		66		µA

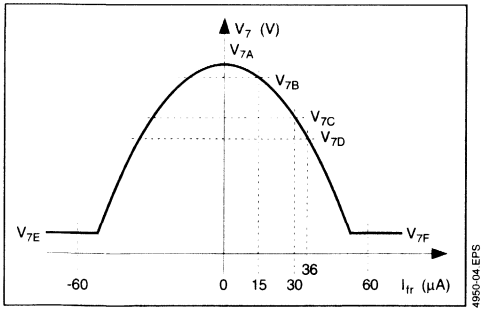
4950-04.TBL

Figure 1 : Test CIrcuit



4950-03.EPS

Figure 2 : Parabola Characteristics



4950-04.EPS

CIRCUIT OPERATION

(see the shematic diagram)

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of ± 33µA which is produced via an external resistor from the sawtooth voltage. The non-inverting input of this amplifier is connected with a reference voltage corresponding to the DC level of the sawtooth voltage. This DC voltage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current. This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

If the input is overmodulated (> 40µA) the internal current is limited to 40µA. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

The horizontal frequency pulse-width modulated output signal drives the final stage. It consists of a class D push-pull output amplifier that drives, via an external inductor, the diode modulator.

Figure 3 : Application Circuit with Keystone Correction

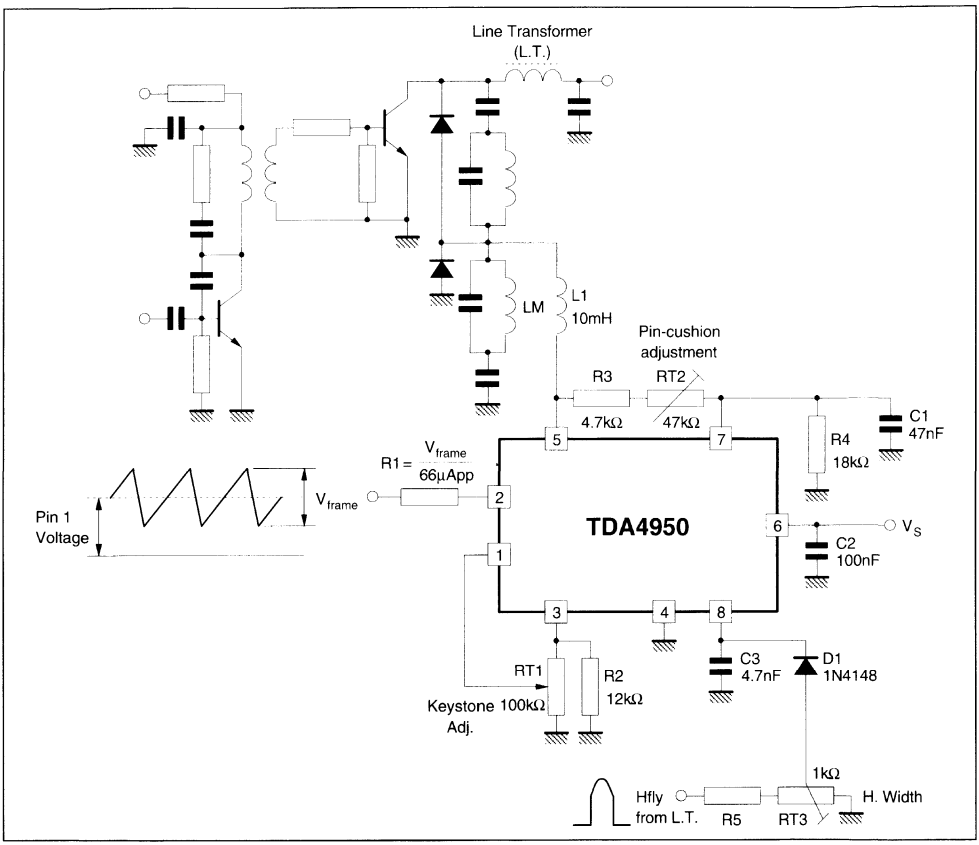
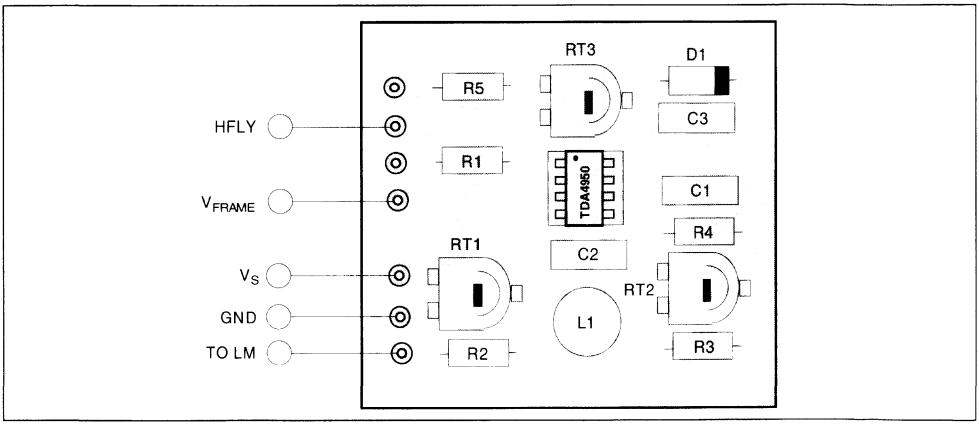


Figure 4 : P.C. Board and Component Layout of the Circuit of Figure 3 (1:1 scale)

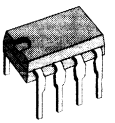


SGS-THOMSON MICROELECTRONICS

TDA8145

TV EAST/WEST CORRECTION CIRCUIT FOR SQUARE TUBES

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT SPECIALLY DESIGNED FOR SQUARE C.R.T. CORRECTION
- EXTERNAL KEYSTONE ADJUSTMENT (symmetry of the parabola)
- INPUT FOR DYNAMIC FIELD CORRECTION (beam current change)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY REDELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAWTOOTH



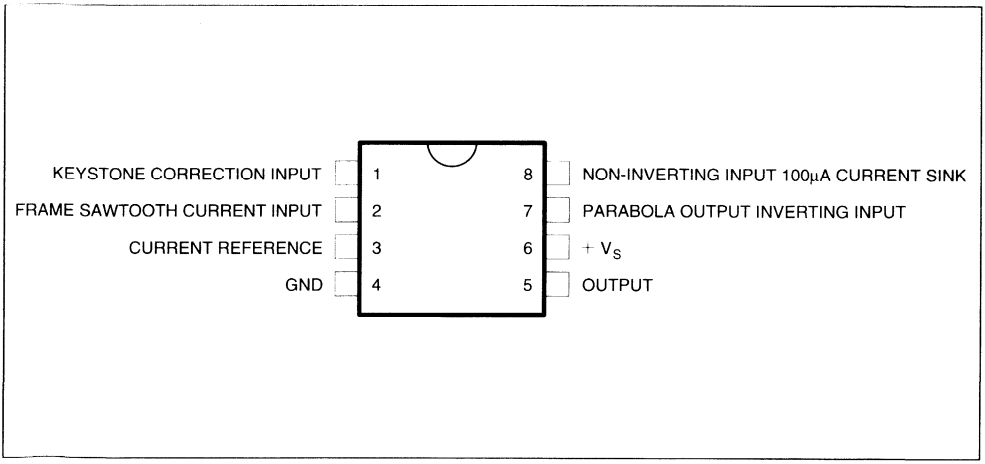
DIP8
(Plastic Package)

ORDER CODE : TDA8145

DESCRIPTION

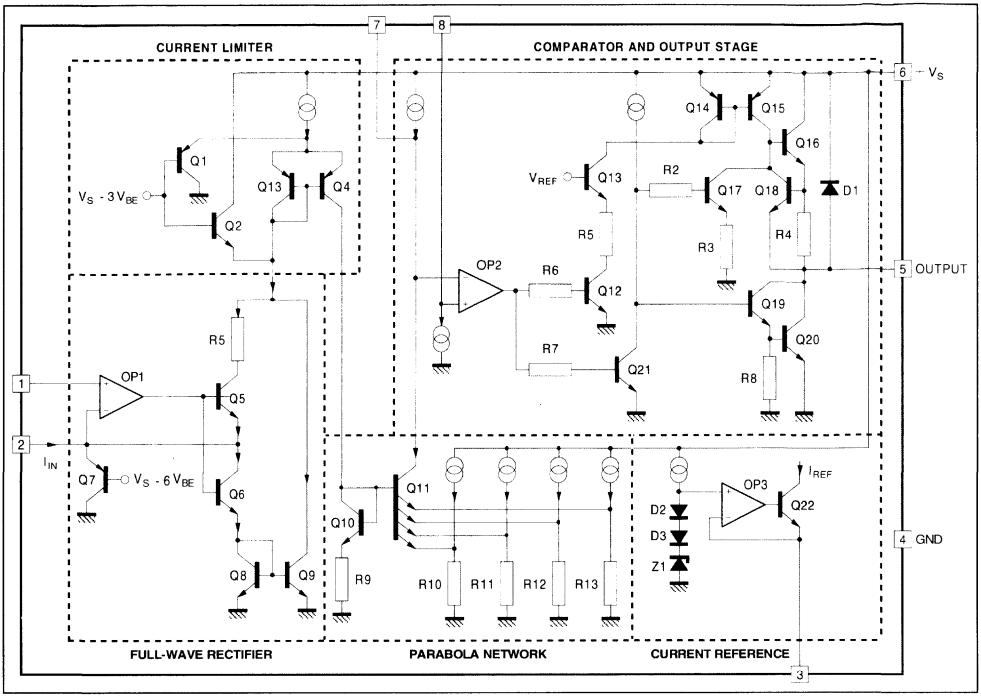
The TDA8145 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the square C.R.T. east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

PIN CONNECTIONS (top view)



8145-01.EPS

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
I_S	Supply Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 50 °C	500	mW
T_{stg}, T_j	Storage and Junction Temperature	– 25 to 150	°C

8145-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-ambient	Max.	100	°C/W
$R_{th\ (j-a)}$	Thermal Resistance Junction-pin 4	Max.	70	°C/W

8145-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 26V, V_{fr} = 0, S1 and S2 in "a" position, refer to the test circuit unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		17	24	30	V
I_S	Supply Current			4.5	7	mA
V_{ref}	Internal Reference Voltage		7.6	8.0	8.8	V
$-I_{ref}$	Internal Reference Current	$V_{ref}/R3$		0.73		mA
$V_{7(A)}$ (*)	Pin 7 Output Voltage	I_{fr} = 0 µA	15.3	16.0	16.7	V
$V_{7(B)}$ (*)	Pin 7 Output Voltage	I_{fr} = 30 µA		15		V

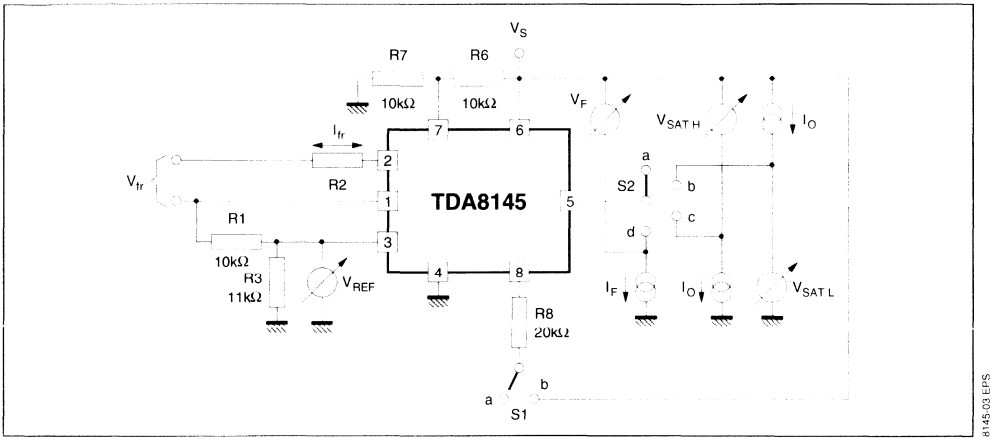
8145-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 26V, V_{fr} = 0, S1 and S2 in "a" position, refer to the test circuit unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_1	Parabola Coefficient (see Figure 2)	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$		0.26		
K2	Parabola Coefficient (see Figure 2)	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$		0.70		
ΔV_7 (*)		$\Delta V_7 = V_{7E} - V_{7F}$	– 40		40	mV
I_8	Current Source	S1 → b		100		µA
V_{SATL}	Saturation Voltage	I_o = 400 mA Sink S2 → b		1	2	V
V_{SATH}	Saturation Voltage	I_o = 100 mA Source S2 → c S1 → b		0.8	1.5	V
V_F	Forward Voltage	I_o = 400 mA S2 → d S1 → b		1.2	1.7	V
I_{fr}	Frame Sawtooth Current	V_{fr} = 6.6 V_{pp}		66		µA

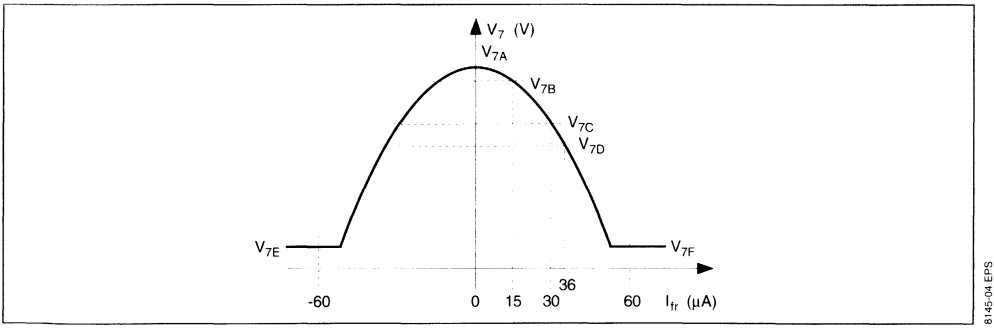
8145-04.TBL

Figure 1 : Test Circuit



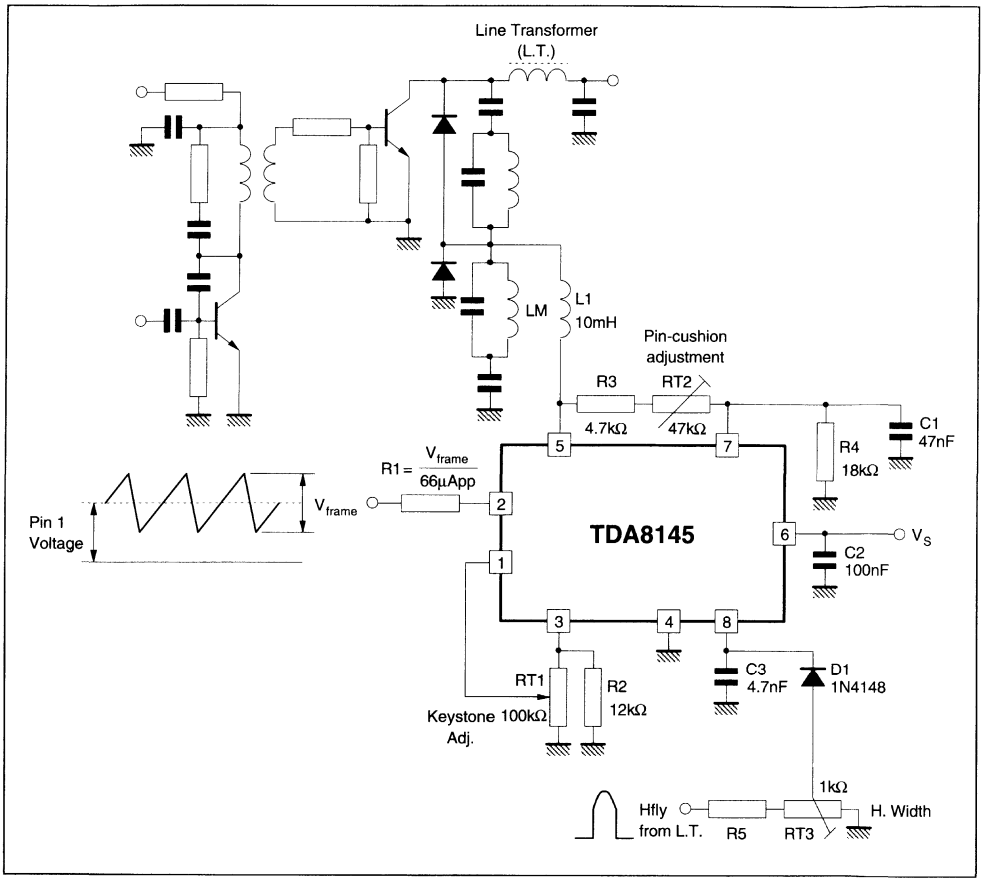
8145-03.EPS

Figure 2 : Parabola Characteristics



8145-04.EPS

APPLICATION CIRCUIT WITH KEYSTONE CORRECTION



CIRCUIT OPERATION (see the schematic diagram)

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of ± 33μA which is produced via an external resistor from the sawtooth voltage. The non–inverting input of this amplifier is connected with a reference voltage corresponding to the DC level of the sawtooth voltage. This DC vol tage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current.

This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

If the input is overmodulated (> 40μA) the internal current is limited to 40μA. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

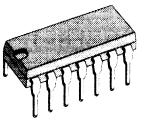
The horizontal frequency pulse–width modulated output signal drives the final stage. It consists of a class D push–pull output amplifier that drives, via an external inductor, the diode modulator.

SGS-THOMSON MICROELECTRONICS

TDA8146

EAST/WEST CORRECTION FOR RECTANGULAR TV-TUBES

- LOW POWER DISSIPATION
- PULSE WIDTH MODULATOR FOR SWITCH MODE OPERATION
- OUTPUT SINK CURRENT UP TO 800mA
- OUTPUT SOURCE CURRENT UP TO 100mA
- PARASITIC PARABOLA SUPPRESSION DURING VERTICAL FLYBACK
- VERTICAL CURRENT SENSE INPUTS GROUND COMPATIBLE
- PROGRAMMABLE PARABOLA CURRENT GENERATOR FOR DIFFERENT TV-TUBES
- EXTERNAL KEYSTONE ADJUSTMENT



DIP14
(Plastic Package)

ORDER CODE : TDA8146

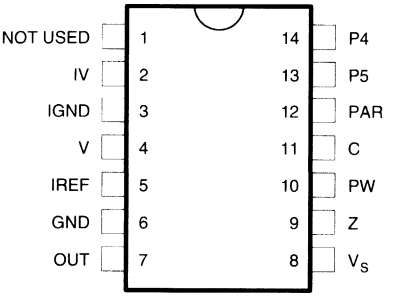
DESCRIPTION

The TDA8146 is a monolithic integrated circuit in a 14 pin dual-in-line plastic package.

The TDA8146 is designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

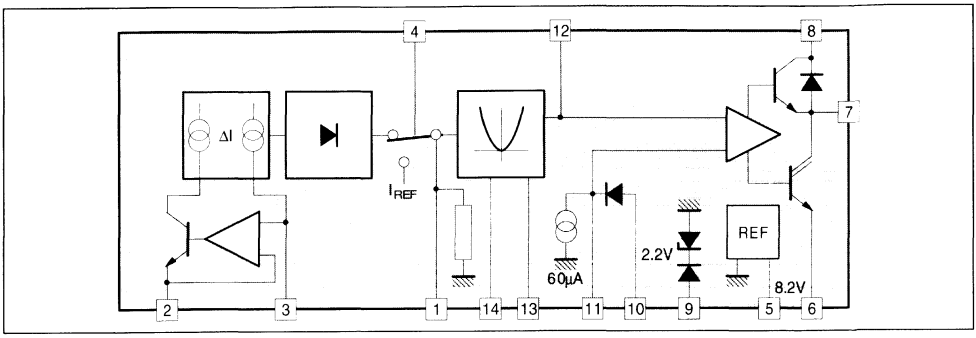
Since the parabola current generator is programmable the device can operate with different CRTs.

PIN CONNECTIONS



8146-01.EPS

BLOCK DIAGRAM



8146-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_7	Output Sink Current	800	mA
I_7	Output Source Current	100	mA
V_S	Supply Voltage	33	V
V_4	Vertical Flyback Input Voltage	– 0.3 to 60	V
V_{10}	Input Voltage at Pin 10	– 10 to V_S	V
V_9	Input Voltage at Pin 9	– 10 to 20	V
V_{in}	Input Voltage at all other Pins	– 0.3 to V_S	V
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

8146-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	80	°C/W

8146-02.TBL

ELECTRICAL CHARACTERISTICS

(refer to test circuit V_S = 24V, T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		15	24	29	V
I_S	Supply Current	V_{out} = LOW		4	7	mA
V_5	Reference Voltage			8.2		V
V_{7L}	Saturation Voltage	I_O = 800mA Sink		1.2	2	V
V_{SAT}	Diode Forward Voltage	I_O = – 800mA		1.1	1.7	V
V_{7H}	Saturation Voltage	I_O = 100mA Source		0.8	1.25	V
I_{11}	Current Sink Pin 11		40	60	80	µA
V_9	Zener Voltage	I_9 = 5mA	20	22	24	V
V_{4T}	Vertical Blanking Threshold Voltage		V_S – 0.5	V_S	V_S + 0.5	V
I_4	Vertical Blanking Input Current	V_4 = 50V	25	50	100	µA
V_2	Reference Voltage at Pin 2	R1 = R2 = 10K		1.3		V
V_3	Reference Voltage at Pin 3			1.3		V
V_{PARO}	Parabola Voltage at Pin 12	ΔV_{SE} = 0		9.7		V
V_C	Parabola Voltage at Pin 12	ΔV_{SE} = + 0.8V		7.05		V

8146-03.TBL

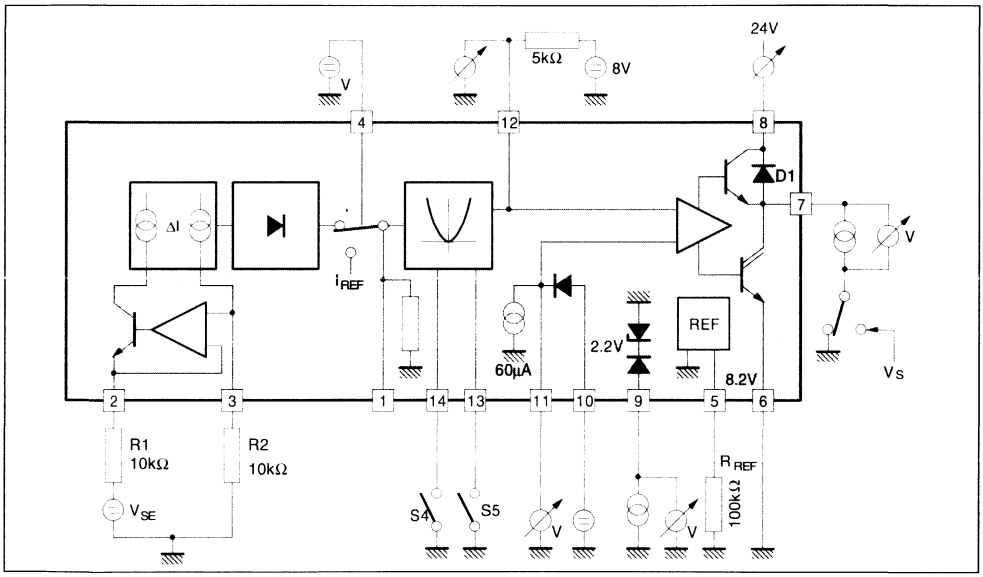
ELECTRICAL CHARACTERISTICS (continued)

(refer to test circuit V_S = 24V, T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_A	Parabola Coefficient	$K_A = \frac{VA}{VB}$		0.25		
K_C	Parabola Coefficient	$K_C = \frac{VC}{VB}$, S4 + S5 open		1.75		
K_5	Parabola Coefficient	$K_5 = \frac{VC5}{VC}$, S4 or S5 Closed		1.07		
K_4	Parabola Coefficient	$K_4 = \frac{VC4}{VC}$, S4 + S5 Closed		1.17		
K_S	Parabola Symmetry	$K_S = \frac{VC}{VD}$	0.94	1.0	1.06	
K_F	Flyback Coefficient	$K_F = \frac{VC}{VD}$, V4 = 15V		1.0		

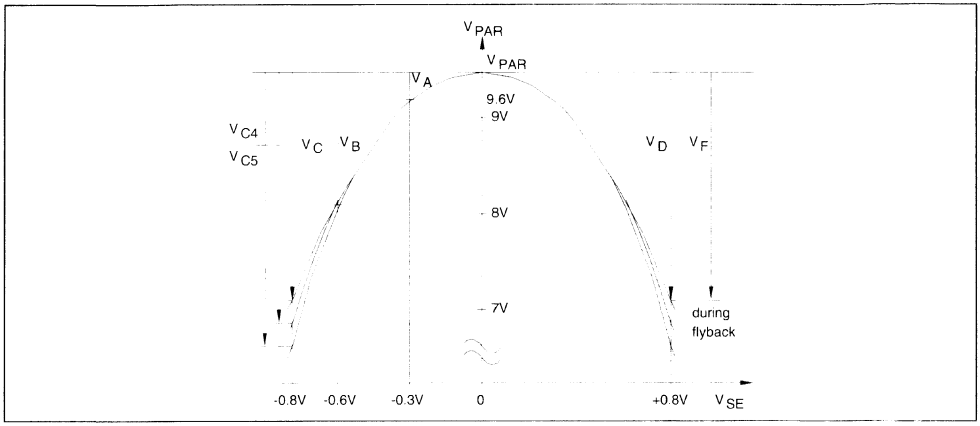
8146-04.TBL

TEST CIRCUIT

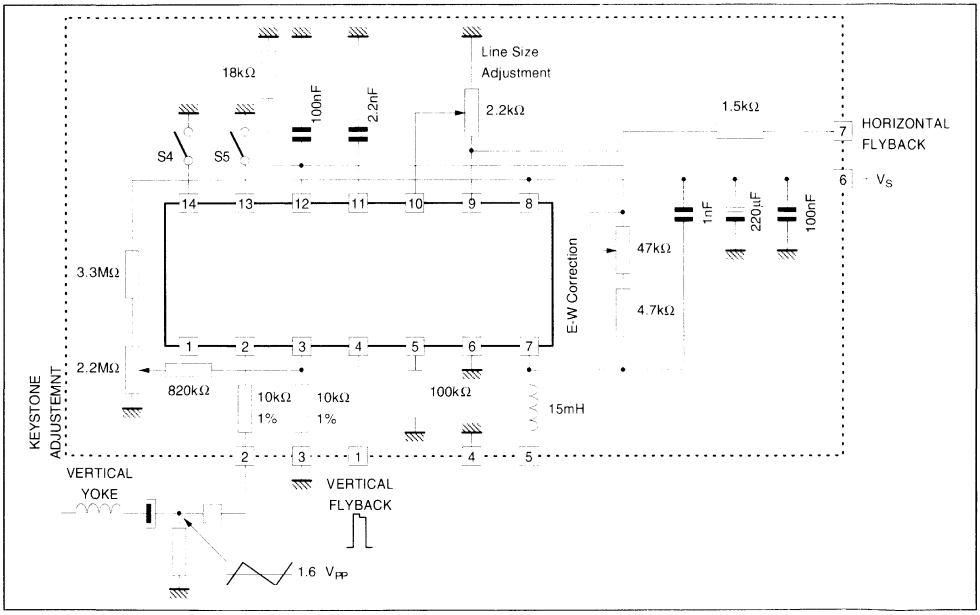


8146-03.EPS

PARABOLA CHARACTERISTICS



APPLICATION DIAGRAM

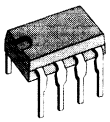


SGS-THOMSON MICROELECTRONICS

TEA2031A

COLOR TV EAST-WEST CORRECTION

- BUILD IN FRAME PARABOLA FROM EXTERNAL SAW-TOOTH
- PARABOLA CORRECTION ADJUSTMENT
- KEYSTONE CORRECTION ADJUSTMENT
- LINE SIZE ADJUSTMENT
- LINE DYNAMIC CORRECTION POSSIBILITY (beam current)
- D CLASS OUTPUT MODULATOR WITH BUILD IN RECOVERY DIODE
- 50 OR 60Hz OPERATION
- LOW DISSIPATION
- FEW EXTERNAL COMPONENTS



DIP8
(Plastic Package)

ORDER CODE : TEA2031A

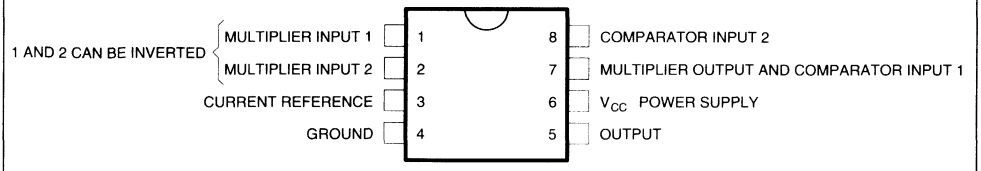
DESCRIPTION

The TEA2031A is intended to ensure frame rate modulated parabolic and keystone corrections to the horizontal deflection circuitry of 110° color TV sets.

The linear frame saw-tooth is applied to appropriate circuitry from which a corresponding parabolic waveforms is obtained. This waveform is then fed to a comparator together with the linear line saw-tooth for comparison. Comparator's output drives the output power stage which is capable of sinking the external coil currents of up to 0.5A.

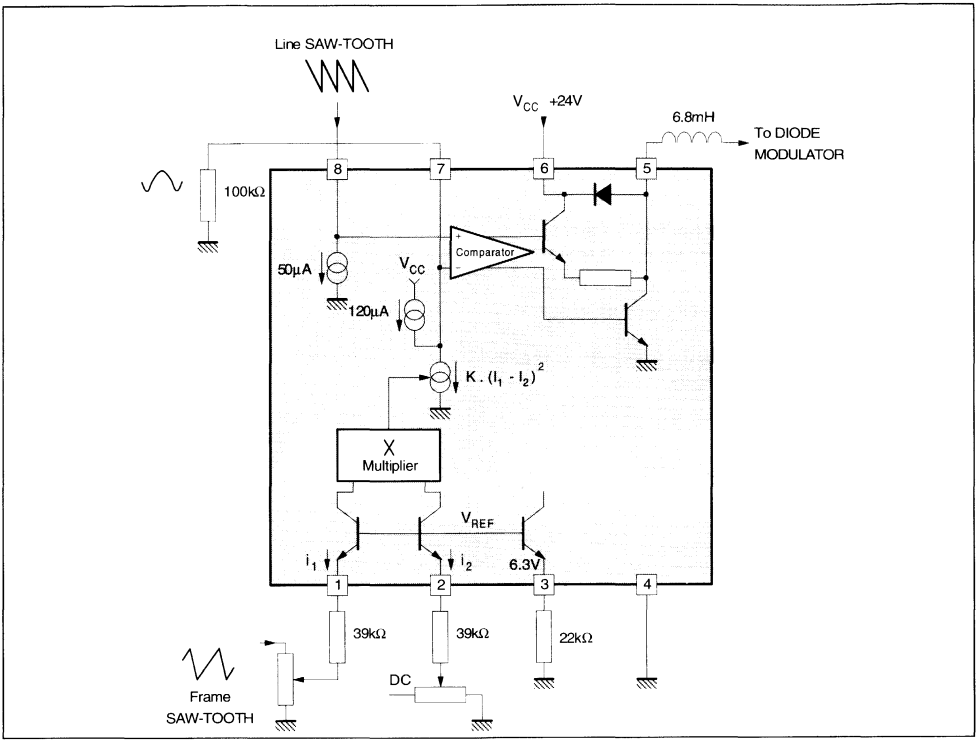
An internal recovery diode feeds back to the power supply the coil fly-back current pulses of as high as 0.5A.

PIN CONNECTIONS



2031A-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

The TEA2031A is intended to provide to 110° color TV sets a parabolic and keystone frame rate modulated correction in addition to the main horizontal scanning.

A stable 6.3V internal reference provides current and voltage references to the whole IC.

Pins 1 and 2 are two symmetrical inputs of an on-chip multiplier circuit and are internally held at 6.3V reference potential level. Current inputs to these pins are drawn from external sources via appropriate resistors. The frame saw-tooth waveform which has a peak-to-peak value of around 3 volts and a mean value of about 2.5 volts, supplies the required current via a series resistor to pin 1. Likewise, the current to pin 2 is drawn through a series resistor from an external dc voltage source. These series resistors can have values of around 40kΩ resulting in input currents of approximately 0.1mA ± modulation current.

Pin 7 should be loaded to ground through a 100kΩ resistor which as a result will produce a parabola of 5 volts peak-to-peak at pin 7. This parabola is symmetrical if the DC current flowing into pin 2 is equal to the mean input current of pin 1. Otherwise, the parabola becomes dissymmetrical and produces a keystone effect correction.

The line saw-tooth at pin 8 is obtained by feeding the line fly-back voltage through an integrator network formed by a diode and a grounded capacitor (see typical application diagram). The DC component of the line saw-tooth is compensated by an internal current sinking source ; so that the mean DC values of line saw-tooth and frame parabola voltages are equal.

Line saw-tooth and frame parabola signals are applied to a comparator whose output is in the form of width modulated pulses. During every pulse duration, the output (pin 5) can sink external coil currents of up to 0.5A associated with diode modulator of the main horizontal scanning circuit.

An internal recovery diode feeds back the fly-back energy of the coil to the power supply. This diode can carry currents of up to 0.5A.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{6-4}	Supply Voltage	35	V
I_{5-4}	Output Sink Current	0.5	A
I_{5-6}	Diode Output Current	0.5	A
I_1 and I_2	Input Current	– 0.5	mA
P_{tot}	Power Dissipation	0.8	W
T_{stg}	Storage Temperature Range	– 20 to 150	°C
I_{5-4}	Non Repetitive Peak Current on Output Transistor	1.5	A
I_{5-6}	Non Repetitive Peak Current on Output Diode	1.5	A

2031A-01.TBL

THERMAL DATA (T_{amb} = + 50°C)

Symbol	Parameter	Value	Unit
$R_{TH\ (j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

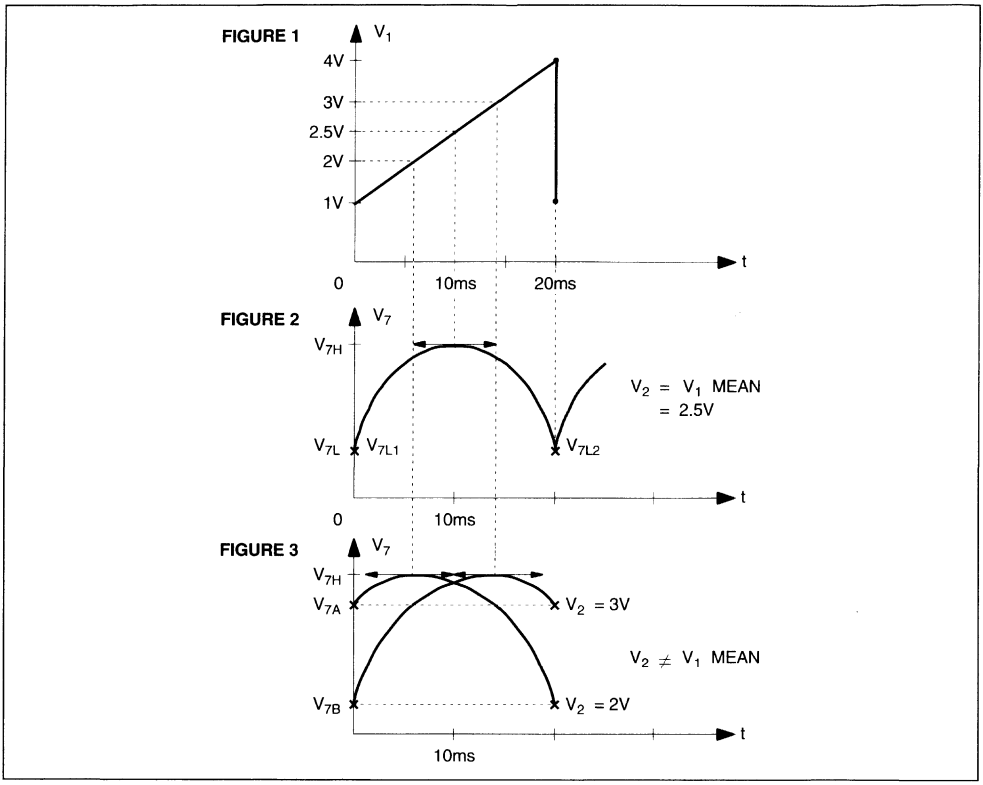
2031A-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{6-4}	Supply Voltage	16	24	35	V
I_6	Supply Current ($R_{(3-4)}$ = 22kΩ ; I_{OUT} = 0)		4	6	mA
	No Load Consumption ($R_{(3-4)}$ = 22kΩ ; I_{OUT} = 0 ; $V_{(6-4)}$ = 24V)		100	150	mW
V_{3-4}	Voltage Reference ($R_{(3-4)}$ = 22kΩ)	5.9	6.3	6.7	V
I_1 mean	Frame Saw-tooth Input DC Mean Current R_1 = 39kΩ at 2.5V Mean - saw-tooth Voltage		0.1		mA
I_{1pp}	Frame Saw-tooth Input Peak-to-peak Current R_1 = 39kΩ at 2.5V Mean - saw-tooth Voltage		70		µA
I_2	Keystone Correction Input DC Current If I_1 Mean = I_2 : No Keystone Effect. R_2 = 39kΩ at 2.5V DC ref.		0.1		mA
ΔI_2	Keystone Correction Input DC Current for Maximum Keystone Effect		± 12.5		µA
V_{7H}	Top Parabola Voltage (2V < V_1 = V_2 < 3V)	10		15	V
ΔV_{7H}	Top parabola temperature drift			0.5	mV/°C
SYMMETRICAL PARABOLA FOR NO KEYSTONE EFFECT (see Figure 2)					
$V_{7H} - V_{7L}$	Parabola Amplitude (V_2 = 2.5V ; V_1 mean = 2.5V, V_{1pp} = 3V)	3.5	5.2	6	V
$\Delta(V_{7H} - V_{7L})$	Parabola amplitude drift versus temperature			1	mV/°C
$\frac{V_{7H} - V_{7L1}}{V_{7H} - V_{7L2}}$	Symmetry	0.8	1	1.2	
MAXIMUM DISSYMMETRICAL PARABOLA FOR MAXIMUM KEYSTONE EFFECT (see Figure 3)					
$V_{7H} - V_{7B}$	Parabola Amplitude (V_2 = 2V or V_2 = 3V ; V_1 mean = 2.5V ; V_{1pp} = 3V)	5.3	8.5	9.2	V
$\frac{V_{7H} - V_{7B}}{V_{7H} - V_{7A}}$	Parabola Amplitude Ratio	2.6		4.1	
DIFFERENTIAL AMPLIFIER					
	Input 8 Sink Current Source	0.04		0.06	mA
$\Delta I_8 = F(\theta)$	Input 8 Current Drift Versus Temperature			0.1	%/°C
	Transfer Characteristics (pins 7-8) (F = 1MHz)	5		500	mA/mV
	Input Noise (pins 7-8)			50	µV
	Rise and Fall Time (Iouput = 250mA)	1			A/µs
V_{5-4}	Output Saturation Voltage to Ground (I_5 = 0.5 A)			1.2	V
V_{6-5}	Output Saturation Voltage to V_{CC} (I_5 = 0.1A)			2	V
V_{5-6}	Output Diode Direct Voltage (I_5 = + 0.5A)			1.2	V

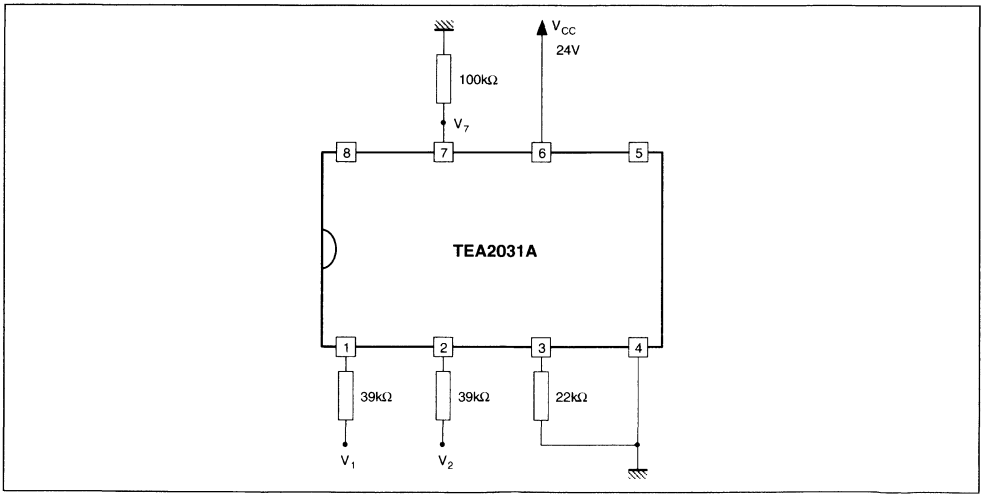
2031A-03.TBL

PARABOLA OUTPUT



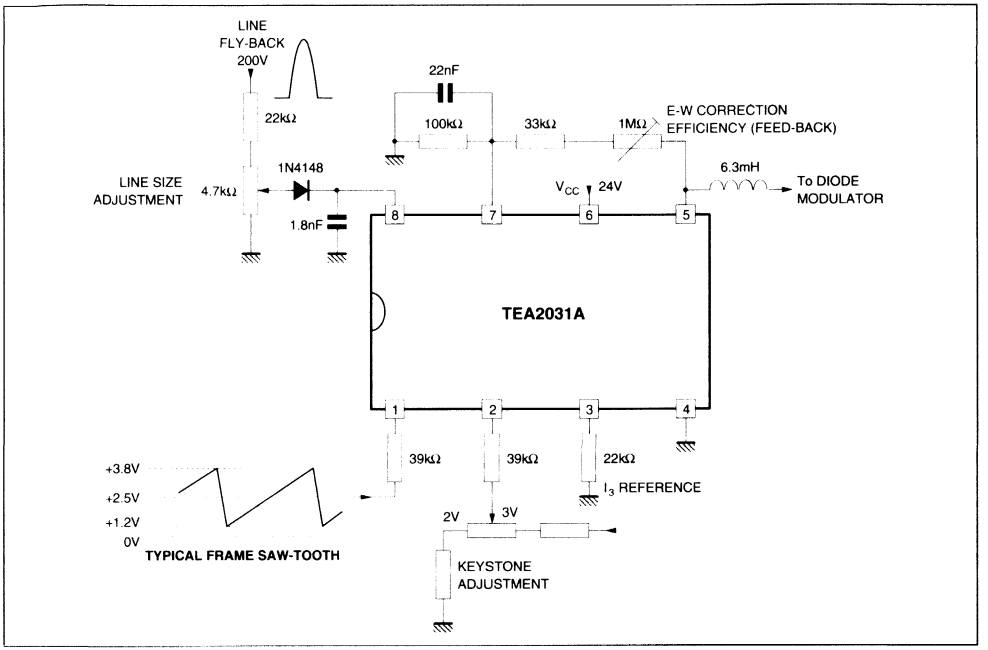
2031A.03.EPS

PARABOLA TEST DIAGRAM



2031A.04.EPS

TYPICAL APPLICATION



2031A-05.EPS

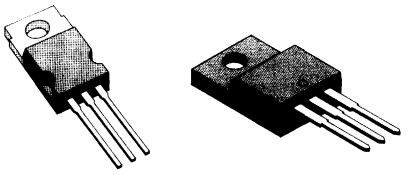
SGS-THOMSON MICROELECTRONICS

BU806/FI
BU807/FI

FAST SWITCHING DARLINGTON TRANSISTORS

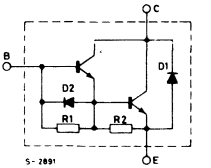
DESCRIPTION

The BU806/807 and BU806FI/807FI are silicon epitaxial planar NPN power transistors in Darlington configuration with integrated base-emitter speed-up diode, mounted respectively in TO-220 plastic package and ISOWATT220 fully isolated package. They are high voltage, high current devices for fast switching applications. In particular they can be used in horizontal output stages of 110°CRT video displays. The BU806/FI are primarily intended for large screen, while the BU807/FI are for medium and small screens.



TO-220 ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	BU806/FI	BU807/FI	Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	400	330	V
V_{CEV}	Collector-emitter Voltage (V_{BE} = – 6V)	400	330	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	200	150	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	6		V
I_C	Collector Current	8		A
I_{CM}	Collector Peak Current	15		A
I_{DM}	Damper Diode Peak Forward Current	10		A
I_B	Base Current	2		A
		TO-220	ISOWATT220	
P_{tot}	Total Power Dissipation at T_c < 25°C	60	30	W
T_{stg}	Storage Temperature	– 65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

THERMAL DATA

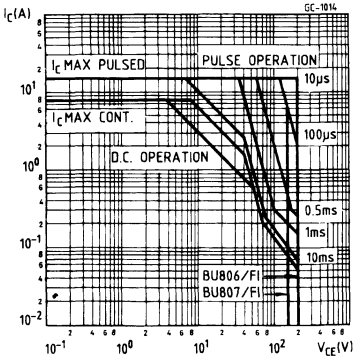
			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.08	4.16	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70		°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

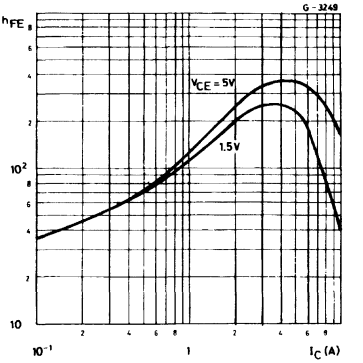
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	for **BU807/FI** V_{CE} = 330V for **BU806/FI** V_{CE} = 400V			100 100	μA μA
I_{CEV}	Collector Cutoff Current (V_{BE} = − 6V)	for **BU807/FI** V_{CE} = 330V for **BU806/FI** V_{CE} = 400V			100 100	μA μA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 6V			3.5	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage (I_B = 0)	I_C = 100mA for **BU807/FI** for **BU806/FI**	150 200			V V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5A I_B = 50mA			1.5	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5A I_B = 50mA			2.4	V
V_F*	Damper Diode Forward Voltage	I_F = 4A			2	V
t_{off}**	Turn-off Time	I_C = 5A I_{B1} = 50mA		0.4	1	μs
t_{on}	Turn-on Time	**RESISTIVE LOAD**		0.35		μs
t_s	Storage Time	I_C = 5A I_{B1} = 50mA I_{B2} = − 500mA V_{CC} = 100V		0.55		μs
t_f	Fall Time			0.2		μs

* Pulsed : pulse duration = 300 μs, duty cycle = 1.5 %.
* * See Test Circuit.

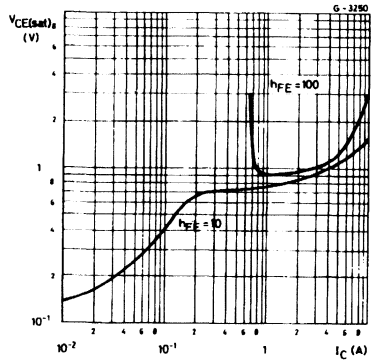
Safe Operating Areas.



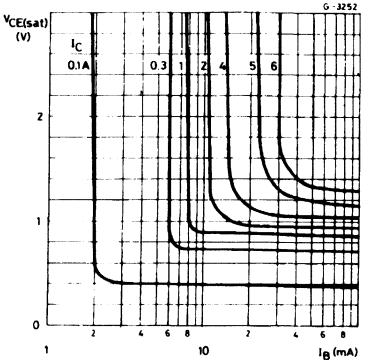
DC Current Gain.



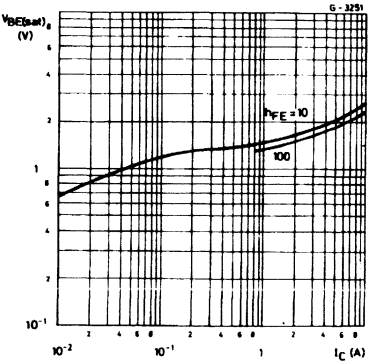
Collector–emitter Saturation Voltage.



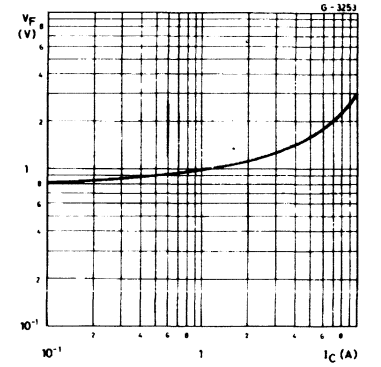
Collector–emitter Saturation Voltage.



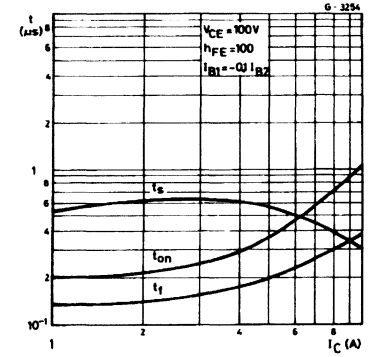
Base–emitter Saturation Voltage.



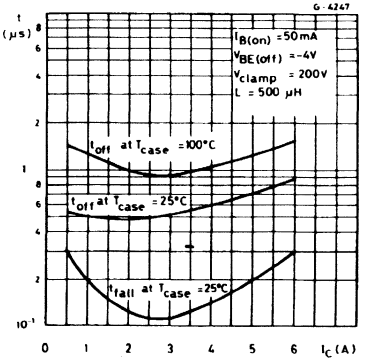
Damper Diode.



Saturated Switching Characteristics (resistive load).

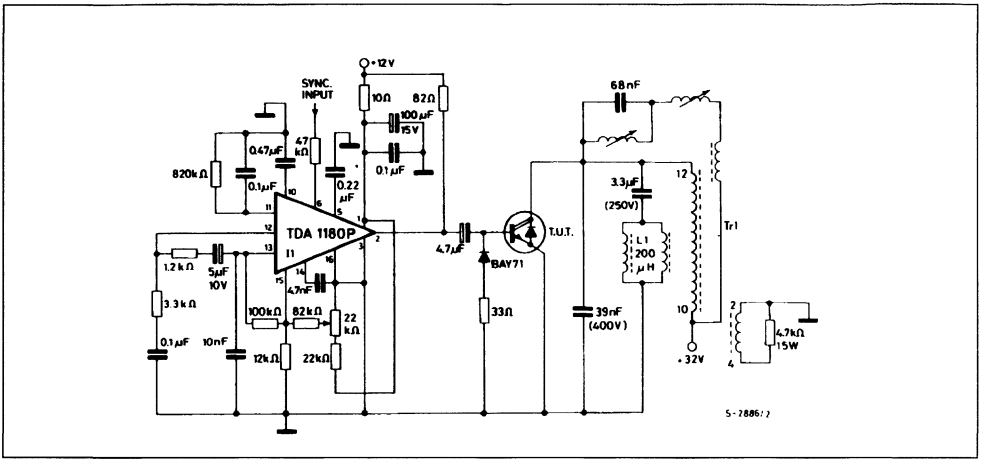


Saturated Switching Characteristics (inductive load).



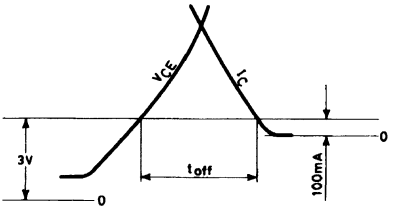
HORIZONTAL DEFLECTION TURN–OFF TIME

TEST CIRCUIT



L1 = Horizontal yoke = 200 µH.
Tr1 = EHT Transformer SAREAtype 900914 or equivalent.
I1 = Horizontal oscillator linear I. C. TDA 1180P.

TURN–OFF TIME WAVEFORM

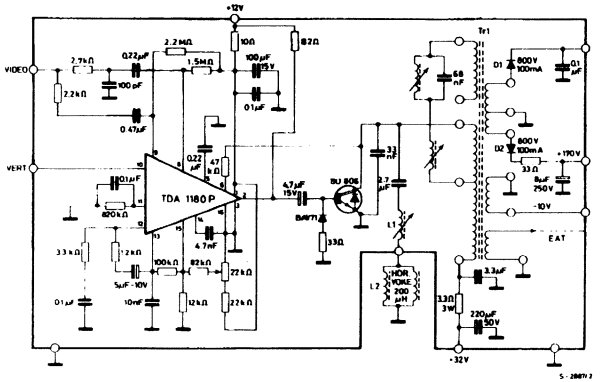


Turn-off time is the time for the collector current I_C to decrease to 100mA after the collector to emitter voltage V_{CE} has risen 3V into its flyback excursion

S-0857

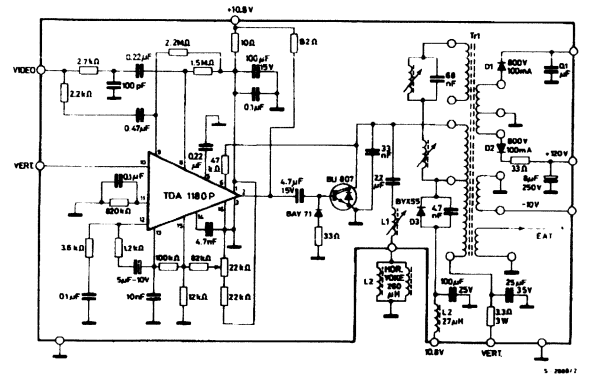
APPLICATION INFORMATION

Horizontal deflection circuit using the darlington BU806 directly driven by the TDA1180 (B & W TV set : large screen solution).



L_i = Linearity inductance 19 ÷ 39 µH.

Horizontal deflection circuit using the darlington BU807 directly driven by the TDA1180 (B & W TV set : small screen solution).



L_i = Linearity inductance 37 ÷ 67 µH.

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware.

Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is equivalent to that of the standard part, mounted with a 0.1mm mica washer.

The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by :

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Figure 1 illustrates the elements contributing to the thermal resistance of a transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance Rth(tot) is the sum of each of these elements.

The transient thermal impedance, Zth for different pulse durations can be estimated as follows :

1-for a short duration power pulse less than 1ms :

$$Z_{th} < R_{thJ\text{-}C}$$

2-for an intermediate power pulse of 5ms to 50ms :

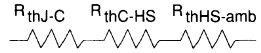
$$Z_{th} = R_{thJ\text{-}C}$$

3-for long power pulses of the order of 500ms or greater :

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Figure 1.



SGS-THOMSON MICROELECTRONICS

BU808FI
BU808DFI

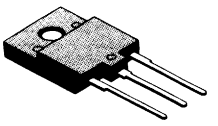
VERY HIGH VOLTAGE FAST SWITCHING POWER DARLINGTON

PRELIMINARY DATA

- HIGH VOLTAGE
- HIGH POWER
- HIGH SWITCHING SPEED
- EXCELLENT STABILITY

CONSUMER APPLICATION

- TV COLOR HORIZONTAL DEFLECTION



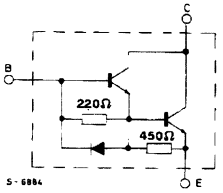
ISOWATT218

DESCRIPTION

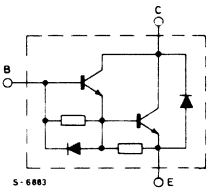
The BU808FI and BU808DFI are silicon multiepitaxial mesa NPN transistors in monolithic Darlington configuration. An integrated base-emitter speed-up diode is included in the BU808DFI. They are fast switching, high voltage devices designed for use in colour television horizontal deflection circuits.

Both devices are packaged in the fully isolated ISOWATT218.

INTERNAL SCHEMATIC DIAGRAM



BU808FI



BU808DFI

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	1400	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current (t_p < 10ms)	10	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 10ms)	6	A
P_{tot}	Total Dissipation at T_{amb} 25°C	50	W
T_{stg}	Storage Temperature	– 65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

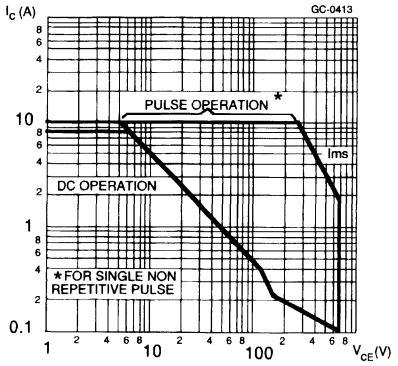
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max.	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

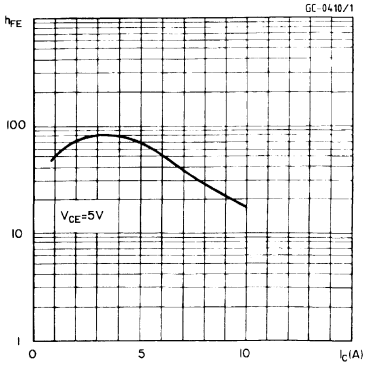
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	V_{CE} = 1400V			400	μA
I_{CEX}	Collector Cutoff Current	V_{CE} = 1000V V_{BE} = – 5V			400	μA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5V			100	mA
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 5A I_B = 0.5A			1.6	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 5A I_B = 0.5A			2	V
h_{FE}*	DC Current Gain	I_C = 5A V_{CE} = 5V I_C = 5A V_{CE} = 5V T_C = 100°C	25 15			
V_F*	Diode Forward Voltage	I_F = 5A for **BU808DFI**			3	V
	INDUCTIVE LOAD					
t_s	Storage Time	I_C = 5A I_{B1} = 0.5A V_{CC} = 150V			3	μs
t_f	Fall Time	V_{BEoff} = - 5V			0.8	μs
t_s	Storage Time	I_C = 5A I_{B1} = 0.5A V_{CC} = 150V		2		μs
t_f	Fall Time	V_{BEoff} = - 5V T_C = 100°C		0.8		μs

* Pulsed : Pulse duration = 300μs, duty cycle = 1.5%.

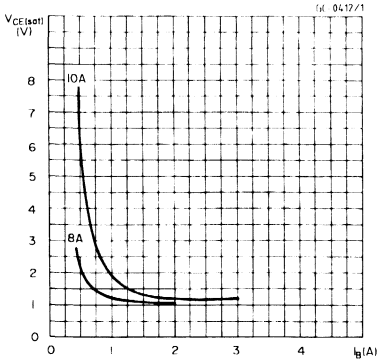
Safe Operating Areas.



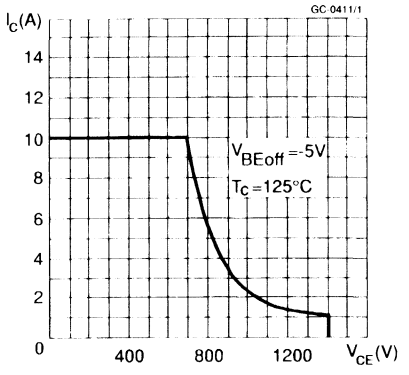
DC Current Gain.



Collector Saturation Region.



Reverse biased SOA.



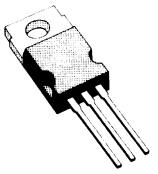
SGS-THOMSON MICROELECTRONICS

BU810

MEDIUM POWER FAST SWITCHING DARLINGTON

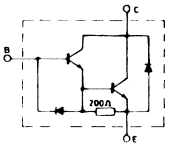
DESCRIPTION

The BU810 is a silicon epitaxial planar NPN Darlington transistor with integrated base-emitter speed-up diode, mounted in Jedec TO-220 plastic package. It is particularly suitable as output stage in medium power, fast switching applications.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base Voltage (I_E = 0)	600	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	400	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	5	V
I_C	Collector Current	7	A
I_{CM}	Collector Peak Current	10	A
I_B	Base Current	2	A
P_{tot}	Total Power Dissipation at $T_{case} \leq 25$ °C	75	W
T_{stg}	Storage Temperature	– 65 to 150	°C
T_j	Junction Temperature	150	°C

THERMAL DATA

$R_{th_{j\text{-}case}}$	Thermal Resistance Junction-case	Max	1.66	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	V_{CE} = 600 V			200	μA
I_{CEO}	Collector Cutoff Current (I_B = 0)	V_{CE} = 400 V			1	mA
I_{EBO}*	Emitter Cutoff Current (I_C = 0)	V_{EB} = 5 V			150	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage	I_C = 100 mA	400			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 2 A I_B = 20 mA I_C = 4 A I_B = 200 mA I_C = 7 A I_B = 0.7 A			2 2.5 3	V V V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	I_C = 2 A I_B = 20 mA I_C = 4 A I_B = 200 mA			2.2 3	V V
V_F*	Diode Forward Voltage	I_F = 7 A			3	V

RESISTIVE SWITCHING TIMES

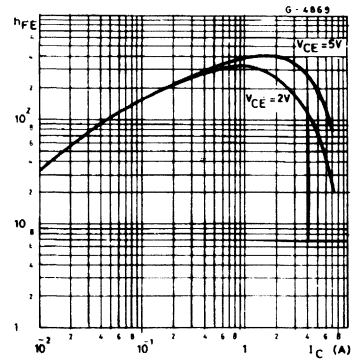
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
t_{on}	Turn-on Time	V_{CC} = 250 V I_C = 2 A I_{B1} = 20 mA $V_{BE(off)}$ = − 5 V			0.6	μs
t_s	Storage Time				1.5	μs
t_f	Fall Time				0.5	μs

INDUCTIVE SWITCHING TIMES

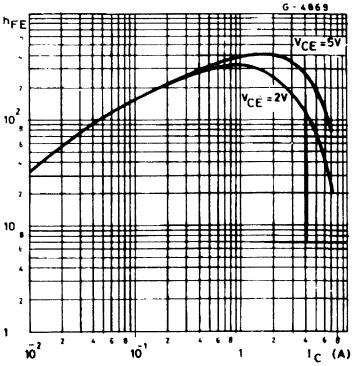
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
t_s	Storage Time	V_{Clamp} = 250 V I_C = 7 A I_{B1} = 0.7 A $V_{BE(off)}$ = − 5 V			1.5	μs
t_f	Fall Time				0.4	μs
t_s	Storage Time				1.5	μs
t_f	Fall Time				0.7	μs

* Pulsed : pulse duration = 300 ms, duty cycle = 1.5 %

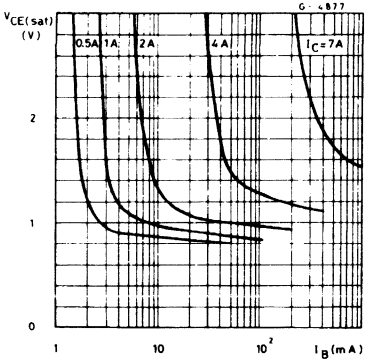
Safe Operating Areas.



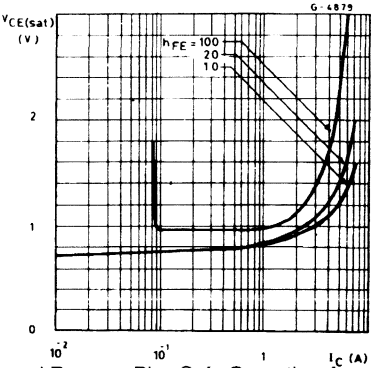
DC Current Gain.



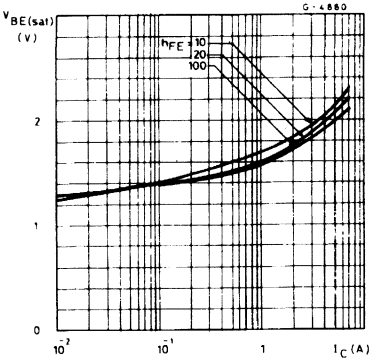
Collector–emitter Saturation Voltage.



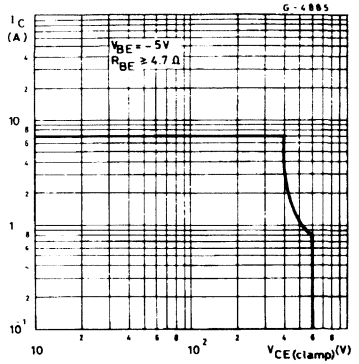
Collector–emitter Saturation Voltage.



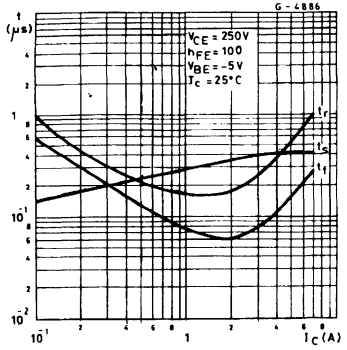
Base–emitter Saturation Voltage.



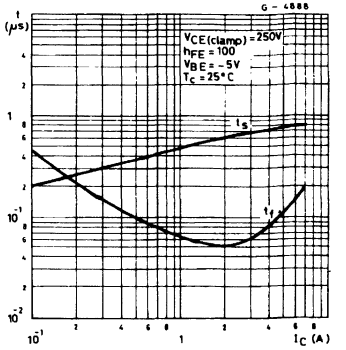
Clamped Reverse Bias Safe Operating Areas.



Saturated Switching Characteristics (resistive load).



Saturated Switching Characteristics.



SGS-THOMSON MICROELECTRONICS

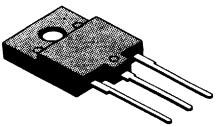
BUH313

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

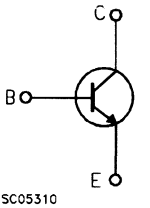
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1300	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	600	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	8	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 5 ms)	5	A
P_{tot}	Total Dissipation at T_c = 25 °C	50	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

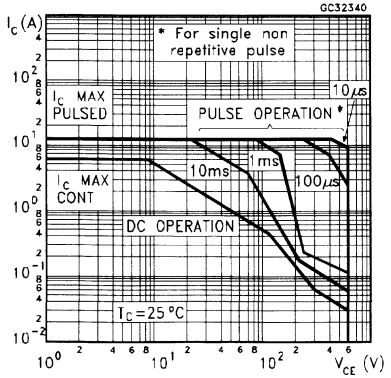
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

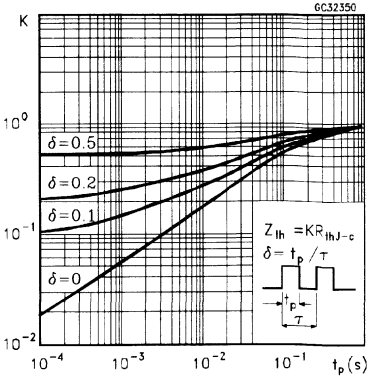
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1300 V V_{CE} = 1300 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	600			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 5 V I_C = 3 A V_{CE} = 5 V T_j = 100 °C	5.5 3.5			
 t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 3 A I_{B1} = 0.75 A I_{B2}= 1.5 A		 1.6 110	 2.4 200	 µs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 15625 Hz I_{B1} = 0.75 A I_{B2} = 1.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		 3.5 340		 µs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 31250 Hz I_{B1} = 0.75 A I_{B2} = 1.5 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		 3.5 270		 µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

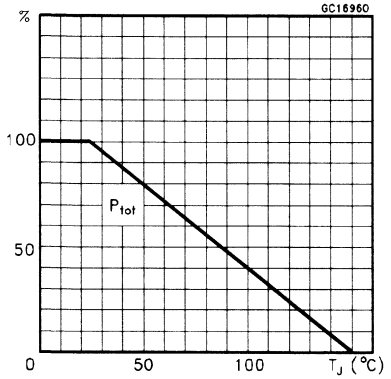
Safe Operating Areas



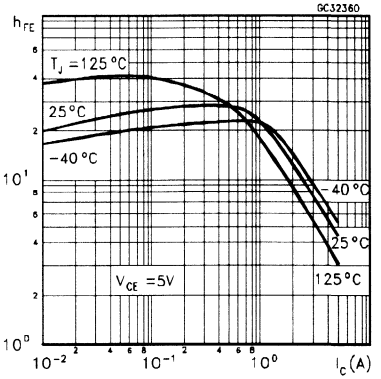
Thermal Impedance



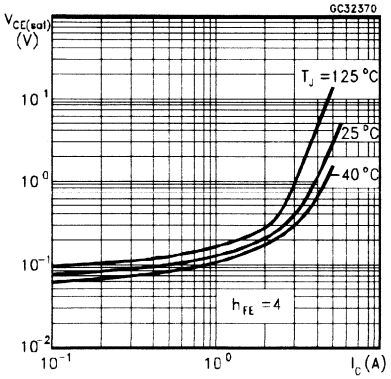
Derating Curves



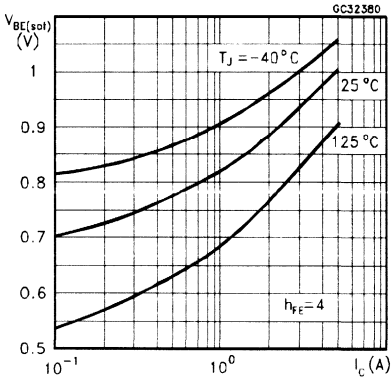
DC Current Gain



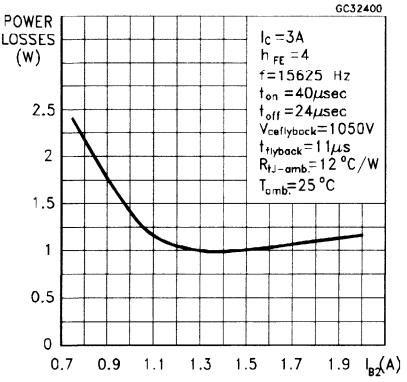
Collector-Emitter Saturation Voltage



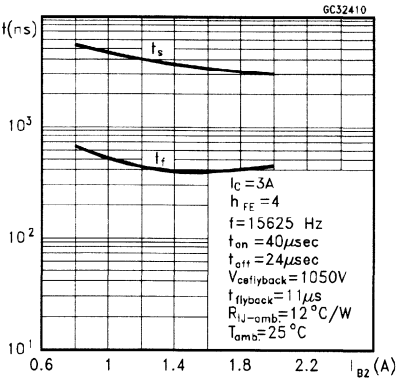
Base-Emitter Saturation Voltage



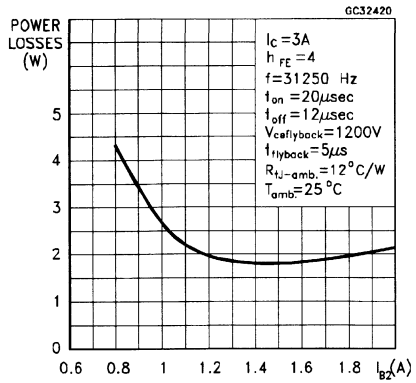
Power Losses at 16 KHz



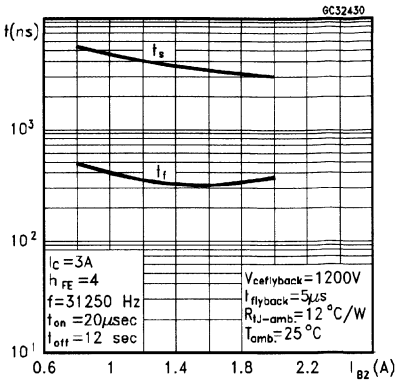
Switching Time Inductive Load at 16 KHz (see figure 2)



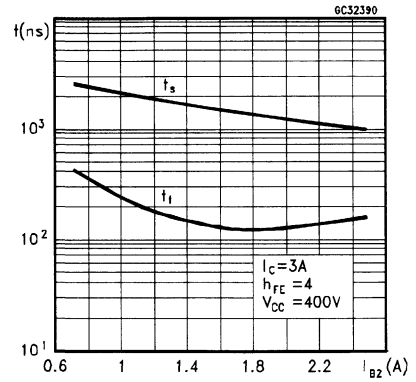
Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



Switching Time Resistive Load



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect

is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.
The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

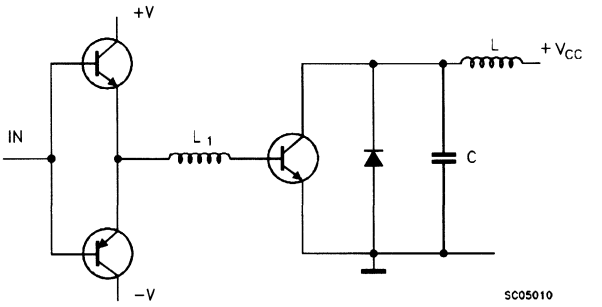
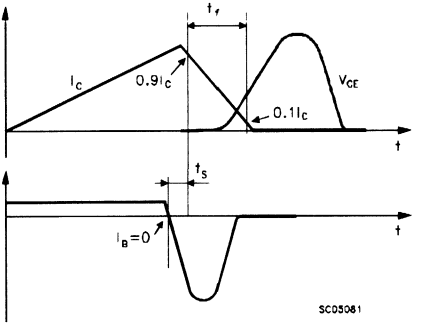


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON
MICROELECTRONICS

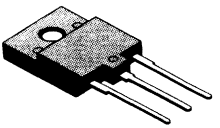
BUH313D

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

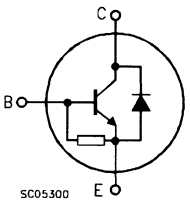
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1300	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	600	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	8	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 5 ms)	5	A
P_{tot}	Total Dissipation at T_c = 25 °C	50	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

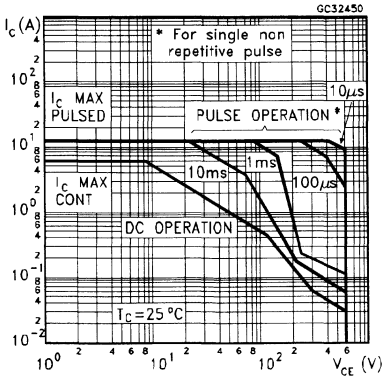
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

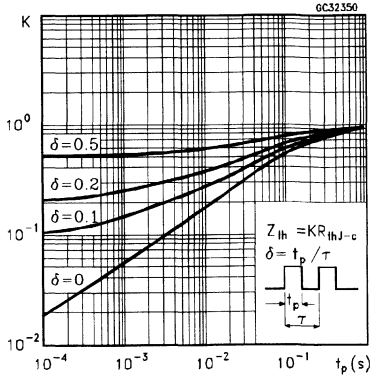
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1300 V V_{CE} = 1300 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			300	mA
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 5 V I_C = 3 A V_{CE} = 5 V T_j = 100 °C	5 3			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 3 A I_{B1} = 1 A I_{B2}= 1.5 A		1.8 200	2.7 300	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 15625 Hz I_{B1} = 1 A I_{B2} = 1.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		2.7 350		µs ns
V_F	Diode Forward Voltage	I_F = 3 A			2.5	V

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

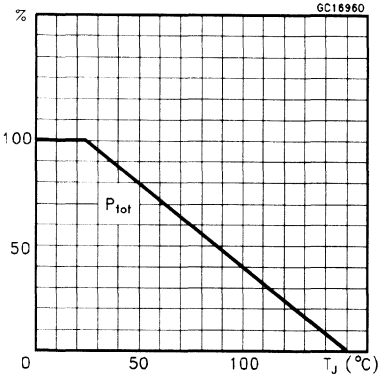
Safe Operating Areas



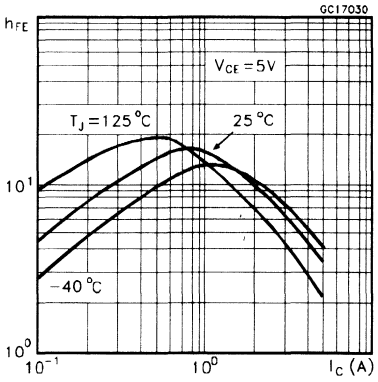
Thermal Impedance



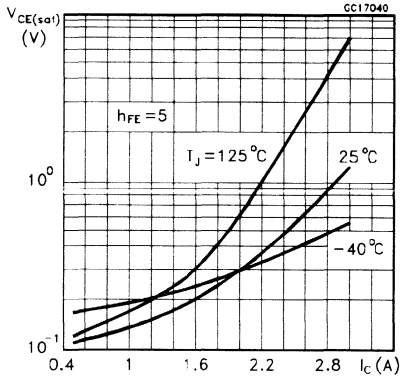
Derating Curves



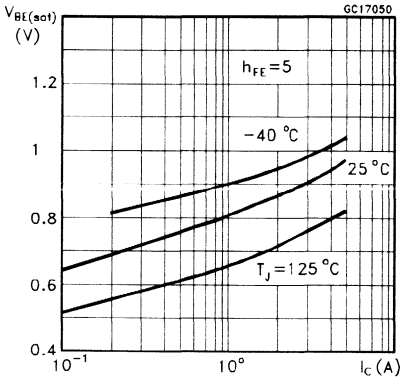
DC Current Gain



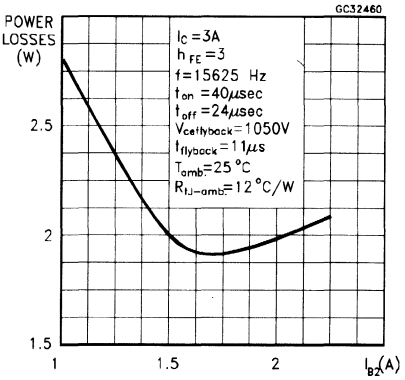
Collector-Emitter Saturation Voltage



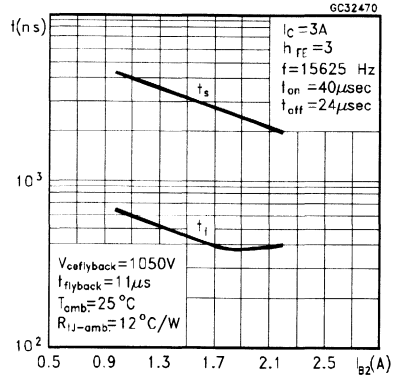
Base-Emitter Saturation Voltage



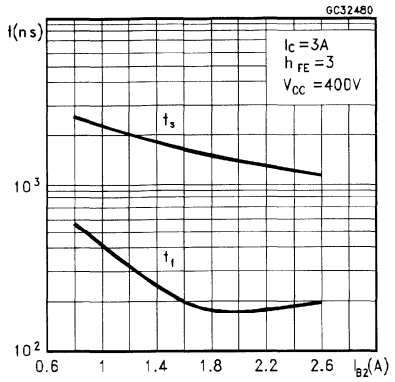
Power Losses at 16 KHz



Switching Time Inductive Load at 16 KHz (see figure 2)



Switching Time Resistive Load



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Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

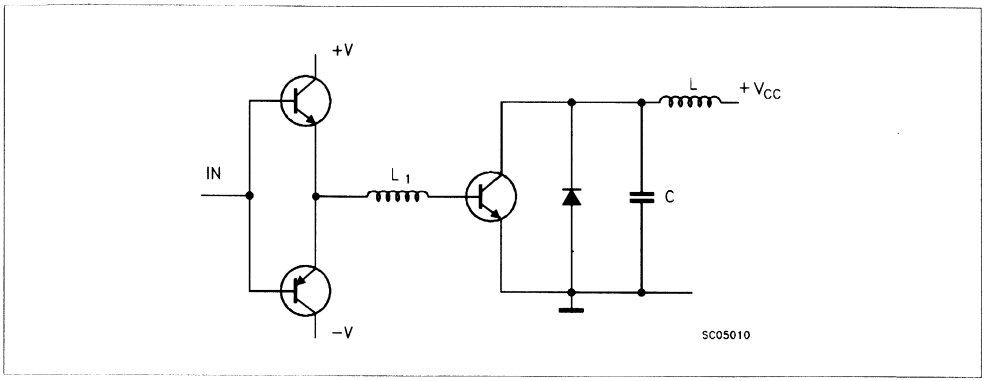
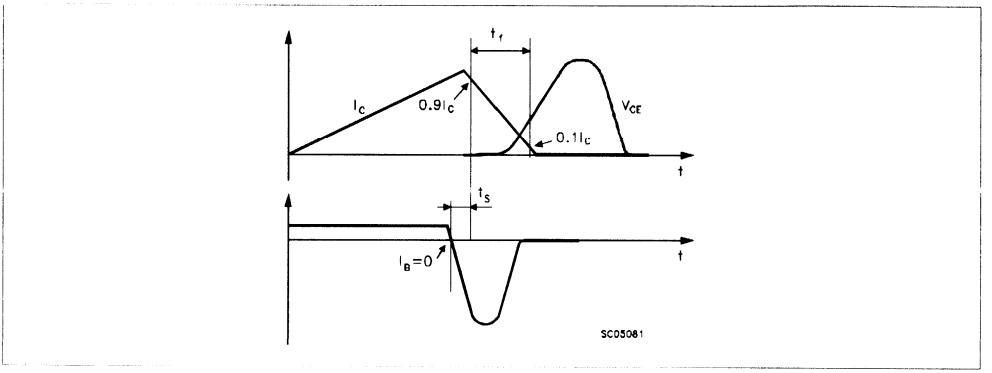


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

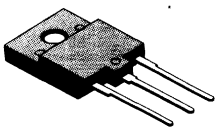
BUH315

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

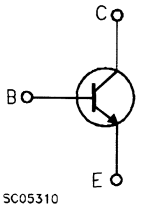
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	8	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 5 ms)	5	A
P_{tot}	Total Dissipation at T_c = 25 °C	50	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

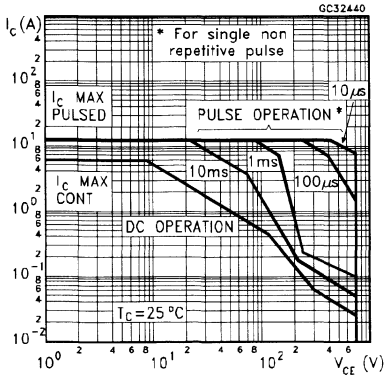
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

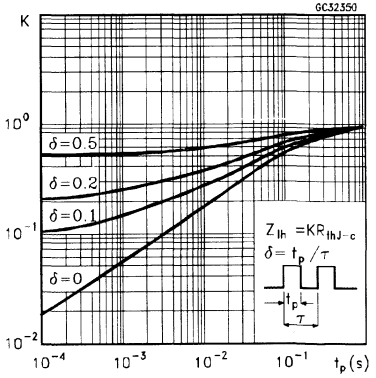
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 0.75 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 5 V I_C = 3 A V_{CE} = 5 V T_j = 100 °C	5.5 3.5			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 3 A I_{B1} = 0.75 A I_{B2}= 1.5 A		1.6 110	2.4 200	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 15625 Hz I_{B1} = 0.75 A I_{B2} = 1.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right)t$ V		3.5 340		µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 31250 Hz I_{B1} = 0.75 A I_{B2} = 1.5 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right)t$ V		3.5 270		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

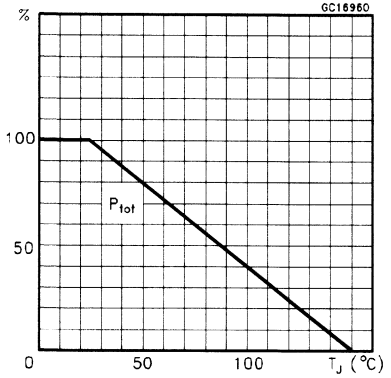
Safe Operating Areas



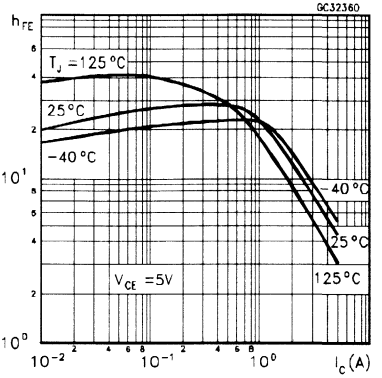
Thermal Impedance



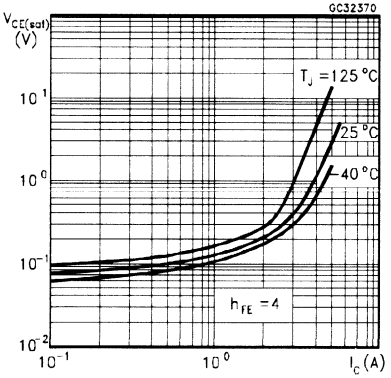
Derating Curves



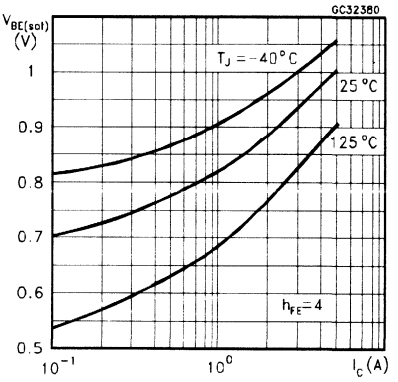
DC Current Gain



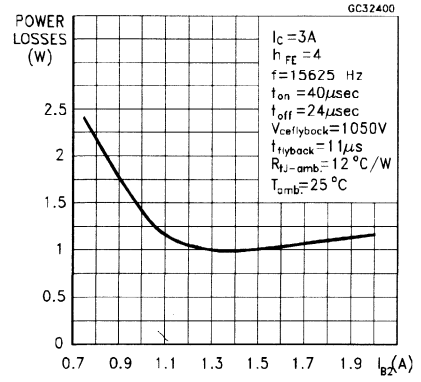
Collector-Emitter Saturation Voltage



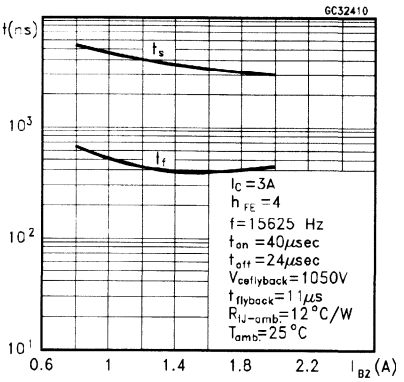
Base-Emitter Saturation Voltage



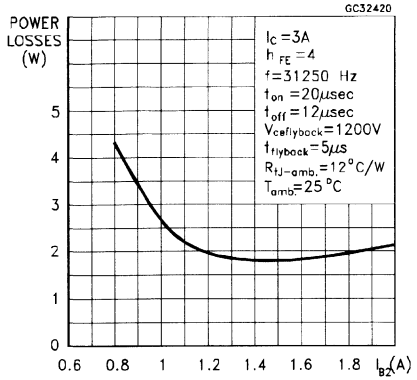
Power Losses at 16 KHz



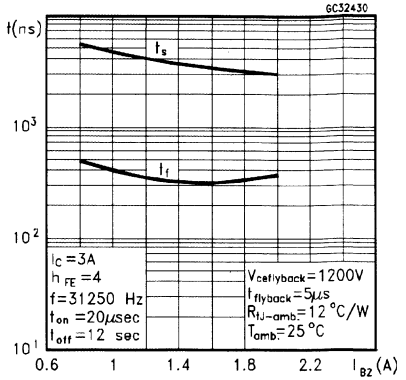
Switching Time Inductive Load at 16 KHz (see figure 2)



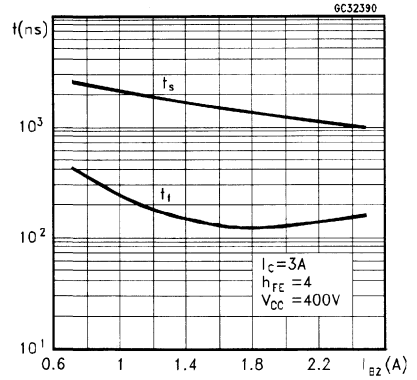
Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



Switching Time Resistive Load



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect

is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.
The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

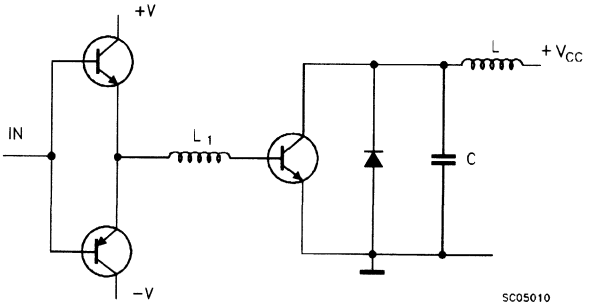
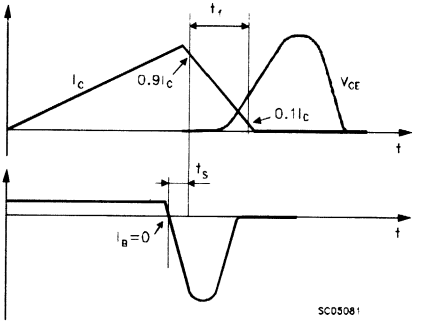


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

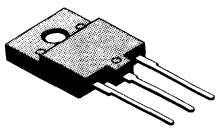
BUH315D

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

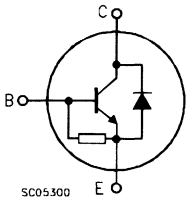
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5	V
I_C	Collector Current	5	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	8	A
I_B	Base Current	3	A
I_{BM}	Base Peak Current (t_p < 5 ms)	5	A
P_{tot}	Total Dissipation at T_c = 25 °C	50	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

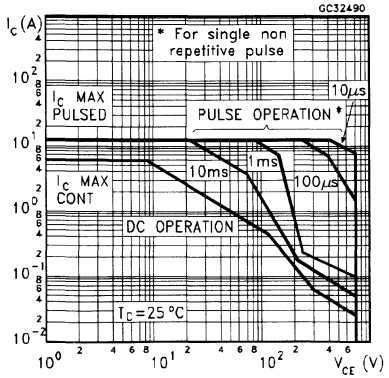
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

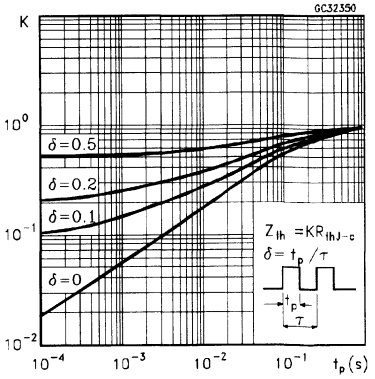
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			300	mA
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 1 A			2	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 1 A			1.5	V
h_{FE}*	DC Current Gain	I_C = 3 A V_{CE} = 5 V I_C = 3 A V_{CE} = 5 V T_j = 100 °C	3.5 2.5			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 3 A I_{B1} = 1 A I_{B2}= 1.5 A		1.8 200	2.7 300	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 3 A f = 15625 Hz I_{B1} = 1 A I_{B2} = 1.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6 t\right)$ V		2.7 350		µs ns
V_F	Diode Forward Voltage	I_F = 3 A			2.5	V

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

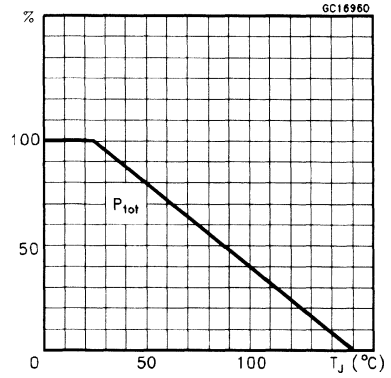
Safe Operating Areas



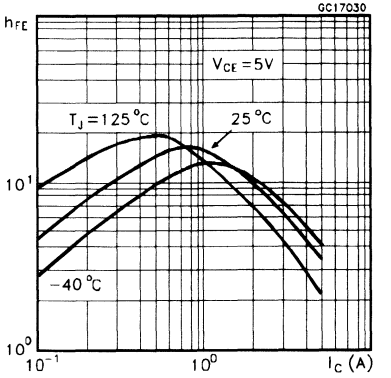
Thermal Impedance



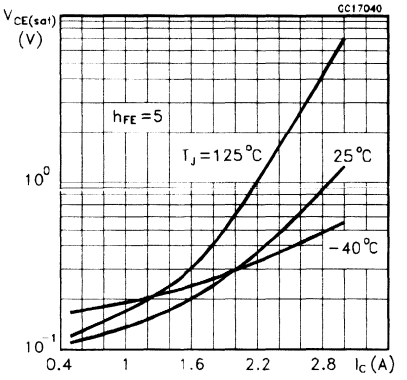
Derating Curves



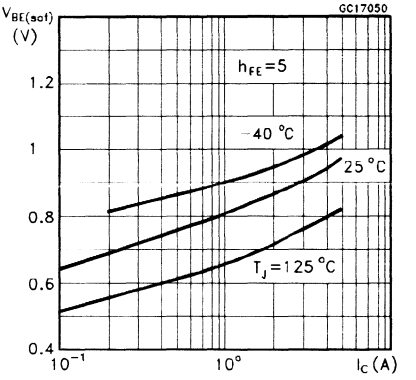
DC Current Gain



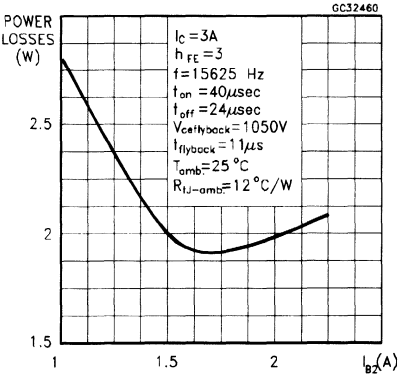
Collector-Emitter Saturation Voltage



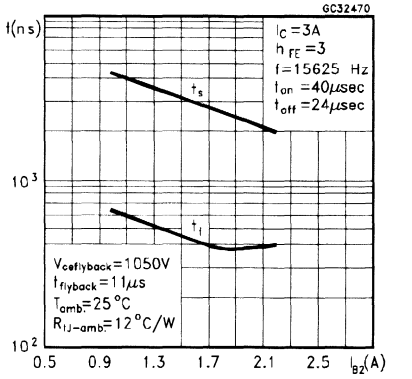
Base-Emitter Saturation Voltage



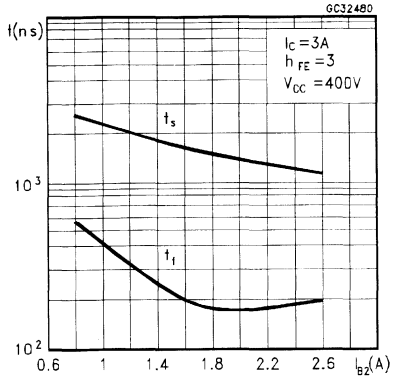
Power Losses at 16 KHz



Switching Time Inductive Load at 16 KHz (see figure 2)



Switching Time Resistive Load



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The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

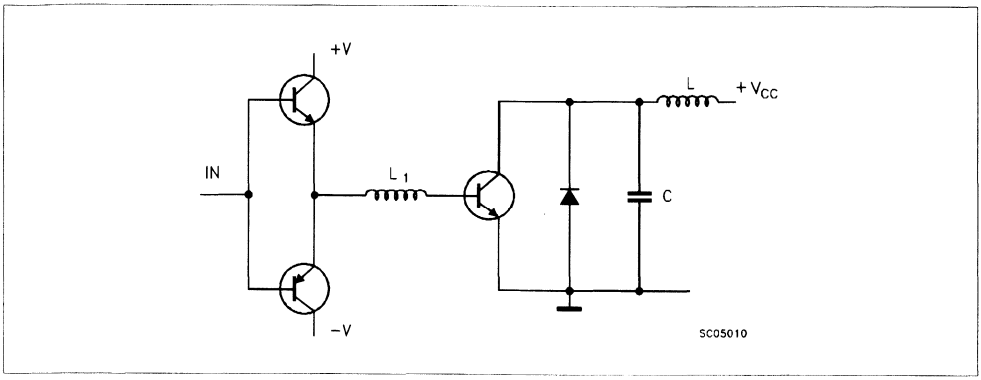
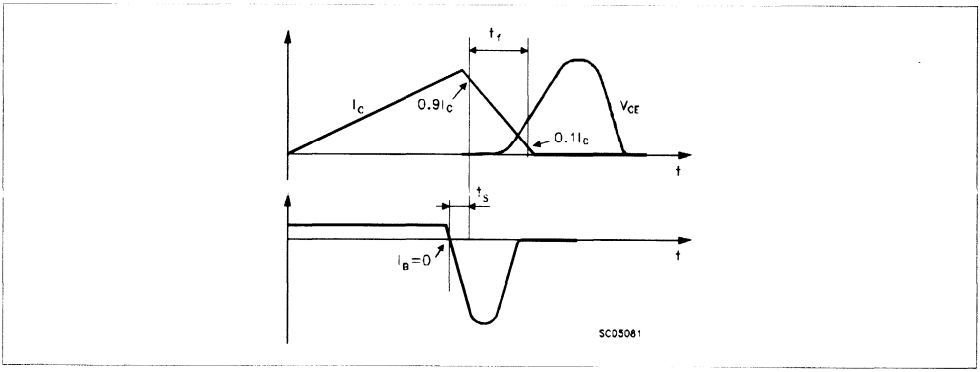


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

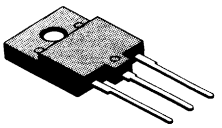
BUH417

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

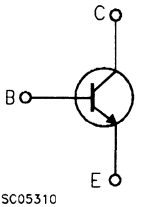
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1700	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	7	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	12	A
I_B	Base Current	4	A
I_{BM}	Base Peak Current (t_p < 5 ms)	7	A
P_{tot}	Total Dissipation at T_c = 25 °C	55	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

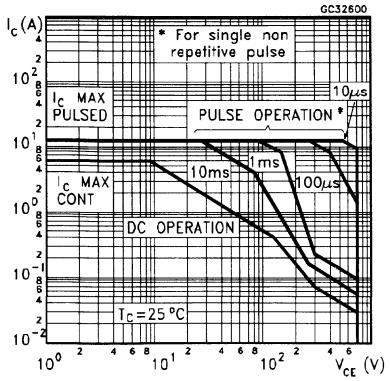
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.27	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

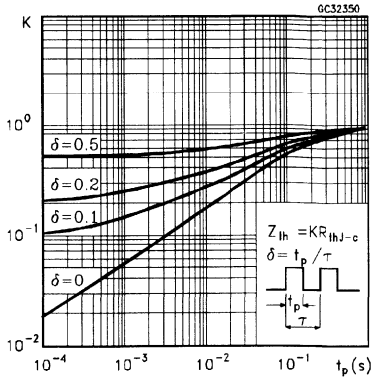
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1700 V V_{CE} = 1700 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	μA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 4 A I_B = 1 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 4 A I_B = 1 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 4 A V_{CE} = 5 V I_C = 4 A V_{CE} = 5 V T_j = 100 °C	6 4			
 t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 4 A I_{B1} = 1 A I_{B2}= 2 A		 2.1 140	 3.2 210	 μs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4 A f = 15625 Hz I_{B1} = 1 A I_{B2} = 2 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		 4.3 370		 μs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4 A f = 31250 Hz I_{B1} = 1 A I_{B2} = 2 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		 4.3 330		 μs ns

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

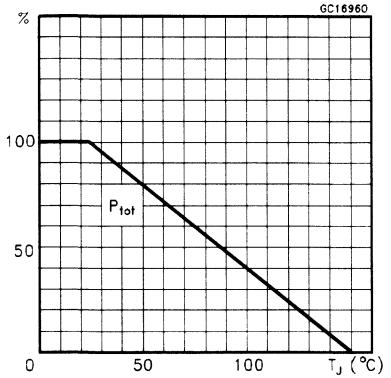
Safe Operating Areas



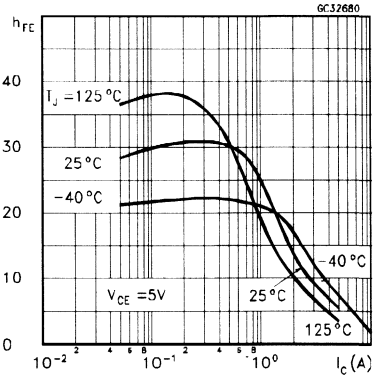
Thermal Impedance



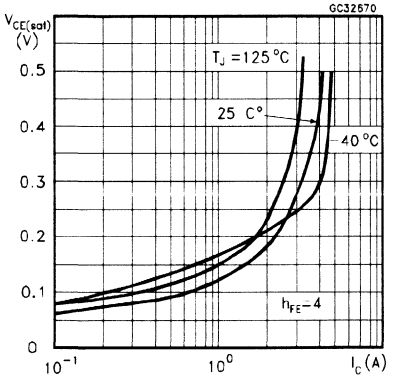
Derating Curves



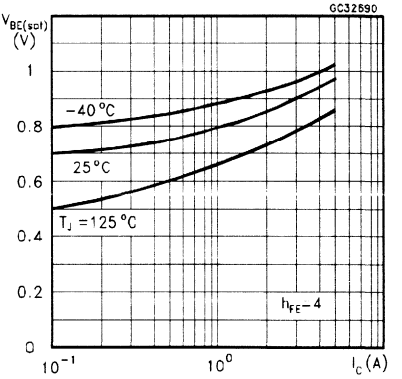
DC Current Gain



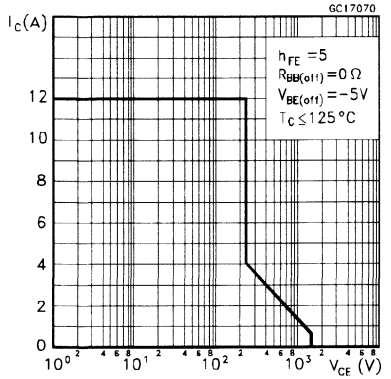
Collector-Emitter Saturation Voltage



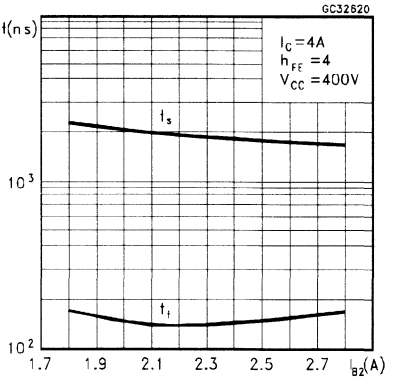
Base-Emitter Saturation Voltage



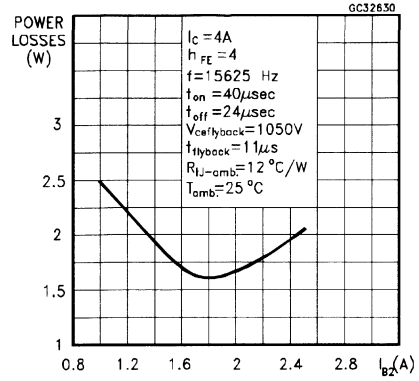
Reverse Biased SOA



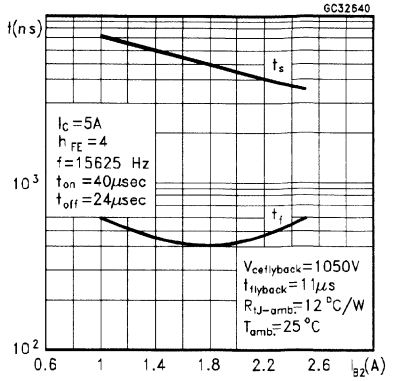
Switching Time Resistive Load



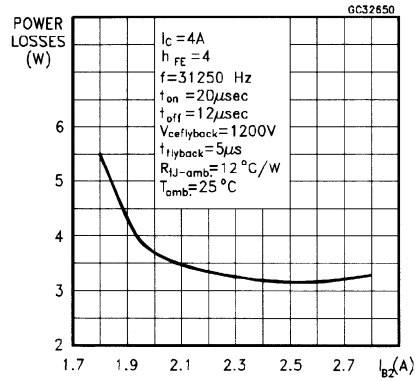
Power Losses at 16 KHz



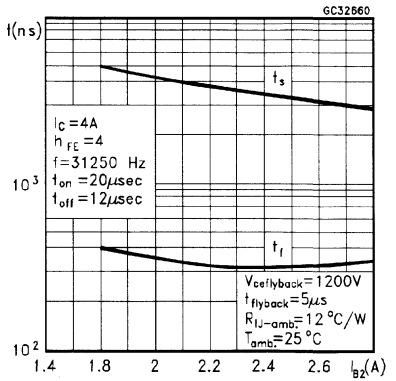
Switching Time Inductive Load at 16 KHz (see figure 2)



Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect

is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.
The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

RBSOA INFORMATION

During turn-off with an inductive load, the power transistor has to withstand high voltages and high currents simultaneously with negative base-to-emitter voltage V_{BEoff}. Very often it has to reach a working area above V_{CEO}, remaining there all the time needed for the collector current I_C to fall to zero. The safe operation for the power transistor under these conditions is specified by RBSOA (Reverse Bias Safe Operating Area) which represents the permissible I_C-V_{CE} locus within which proper operation is guaranteed. RBSOA is strongly dependent on the circuit topology and is valid only under specified drive conditions. High voltage Multiepitaxial Fastswitching transistors of the BUH series have been optimized to give improved RBSOA to suit off-line switch mode power supplies applications.

Figure 1: Test Circuits for Dynamic Characterization.

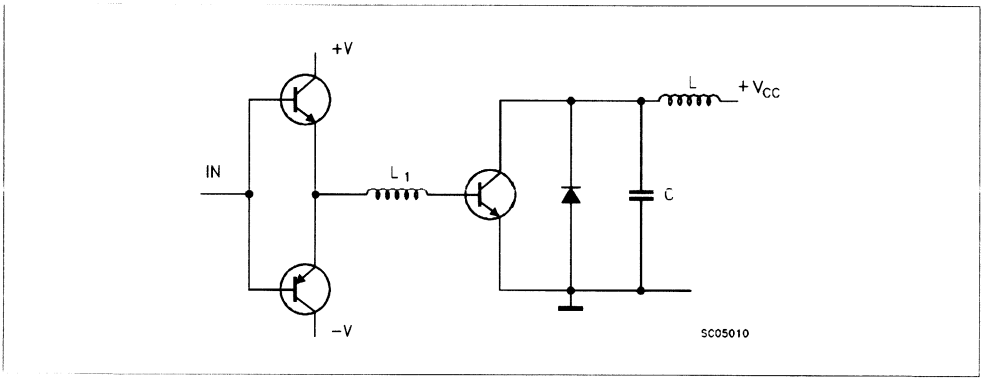
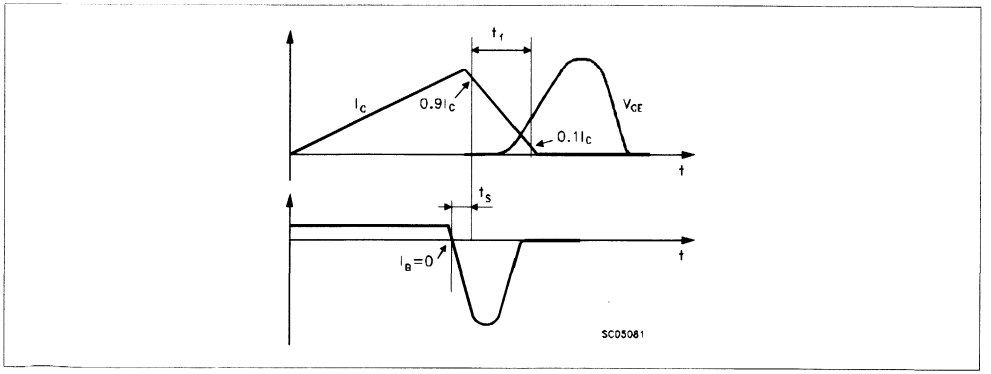


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

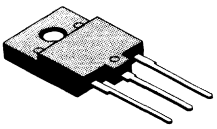
BUH515

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

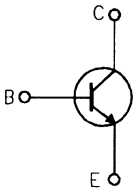
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	12	A
I_B	Base Current	5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	8	A
P_{tot}	Total Dissipation at T_c = 25 °C	60	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

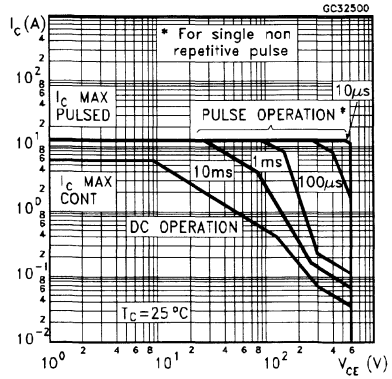
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.08	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

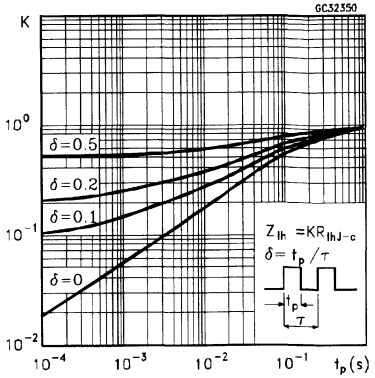
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 5 V I_C = 5 A V_{CE} = 5 V T_j = 100 °C	6 4			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 5 A I_{B1} = 1.25 A I_{B2}= 2.5 A		2.7 190	3.9 280	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 5 A f = 15625 Hz I_{B1} = 1.25 A I_{B2} = 2.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right)t$ V		2.3 350		µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 5 A f = 31250 Hz I_{B1} = 1.25 A I_{B2} = 2.5 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right)t$ V		2.3 200		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

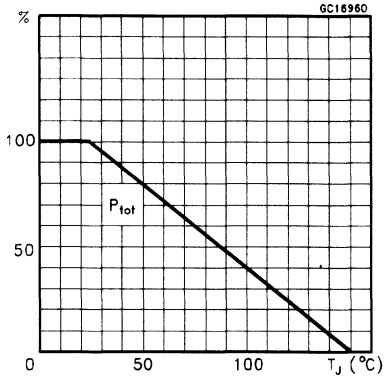
Safe Operating Areas



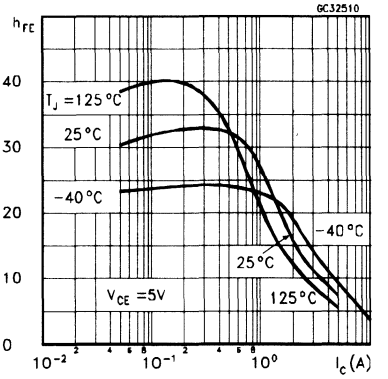
Thermal Impedance



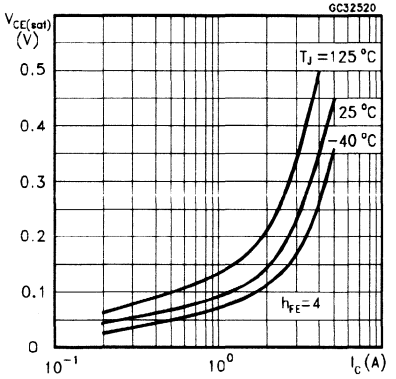
Derating Curves



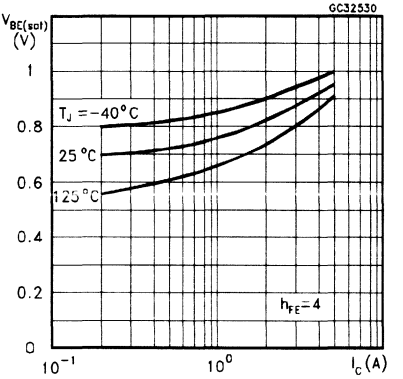
DC Current Gain



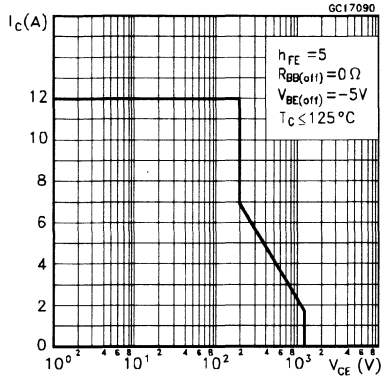
Collector-Emitter Saturation Voltage



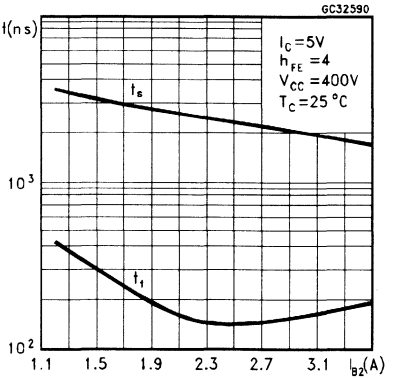
Base-Emitter Saturation Voltage



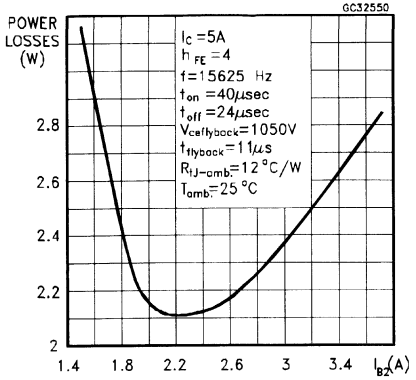
Reverse Biased SOA



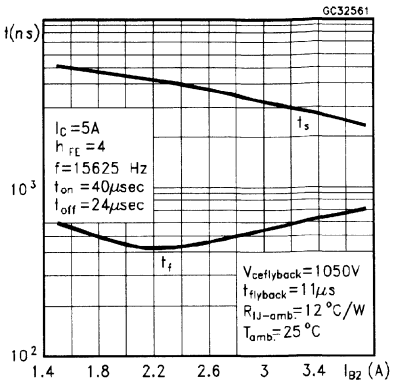
Switching Time Resistive Load



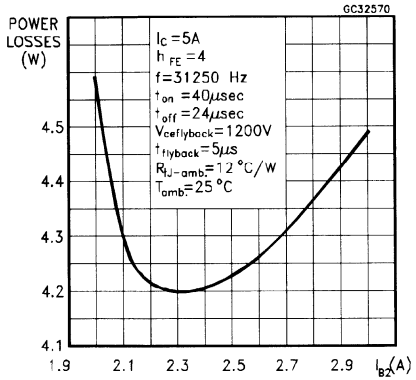
Power Losses at 16 KHz



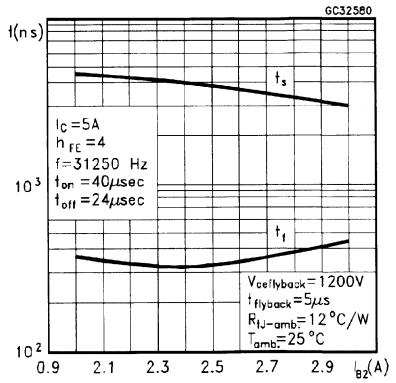
Switching Time Inductive Load at 16 KHz (see figure 2)



Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



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$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

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During turn-off with an inductive load, the power transistor has to withstand high voltages and high currents simultaneously with negative base-to-emitter voltage V_{BEoff}. Very often it has to reach a working area above V_{CEO}, remaining there all the time needed for the collector current I_C to fall to zero. The safe operation for the power transistor under these conditions is specified by RBSOA (Reverse Bias Safe Operating Area) which represents the permissible I_C-V_{CE} locus within which proper operation is guaranteed. RBSOA is strongly dependent on the circuit topology and is valid only under specified drive conditions. High voltage Multiepitaxial Fastswitching transistors of the BUH series have been optimized to give improved RBSOA to suit off-line switch mode power supplies applications.

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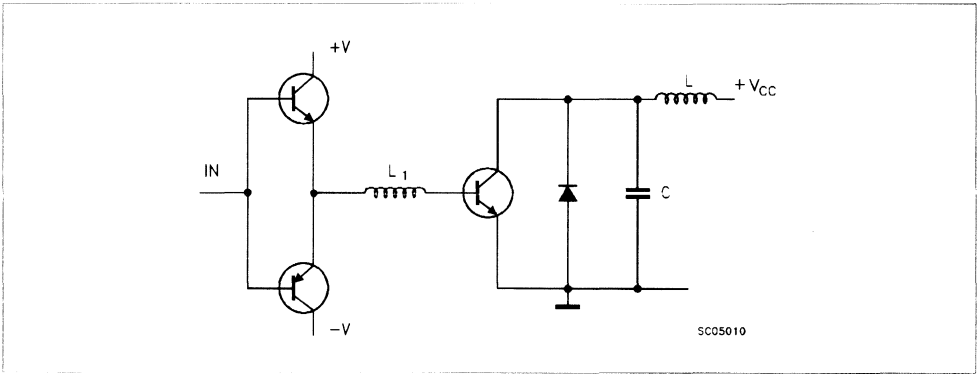
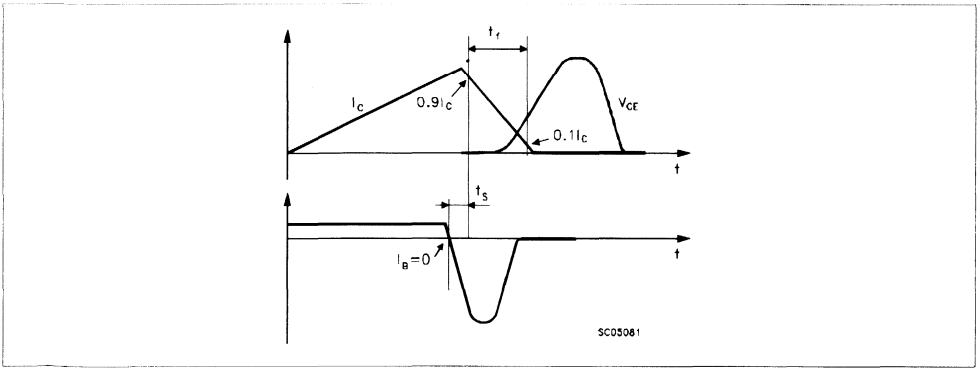


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

BUH515D

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
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- HIGH SWITCHING SPEED
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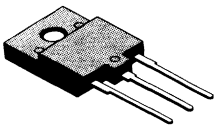
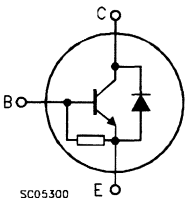
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
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V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	5	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	15	A
I_B	Base Current	5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	8	A
P_{tot}	Total Dissipation at T_c = 25 °C	60	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

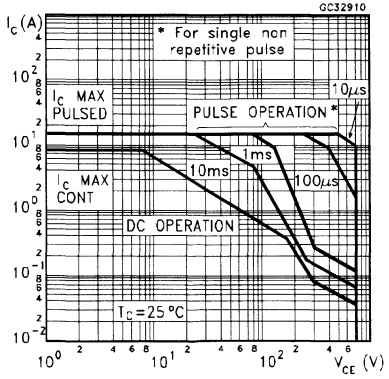
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.08	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

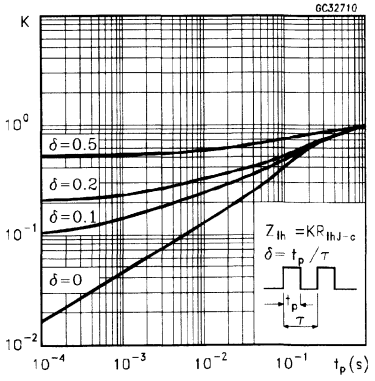
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			300	mA
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 5 V I_C = 5 A V_{CE} = 5 V T_j = 100 °C	5 3			
 t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 5 A I_{B1} = 1.25 A I_{B2}= 2.5 A		2.4 170	3.6 260	µs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 5 A f = 15625 Hz I_{B1} = 1.25 A I_{B2} = 2.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		3.5 450		µs ns
V_F	Diode Forward Voltage	I_F = 5 A			2	V

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

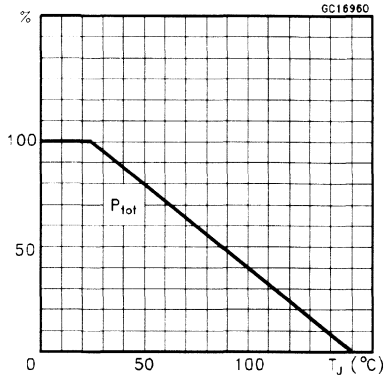
Safe Operating Areas



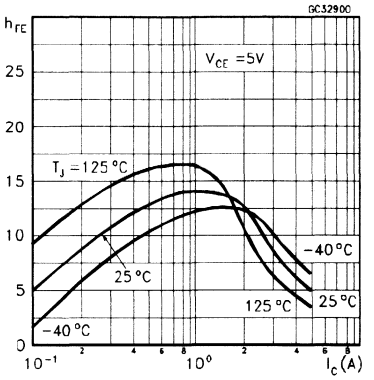
Thermal Impedance



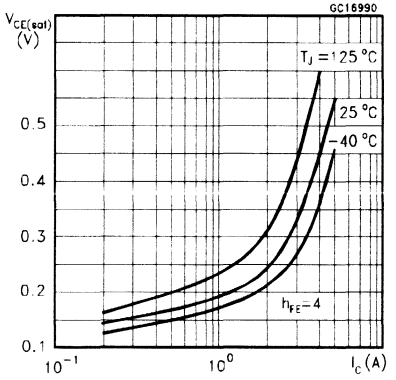
Derating Curves



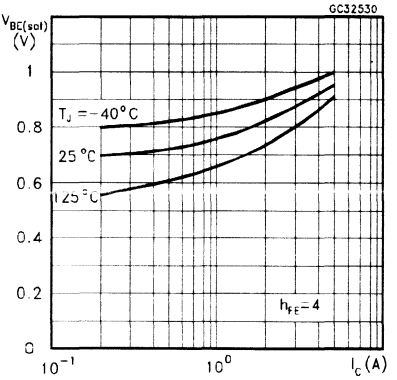
DC Current Gain



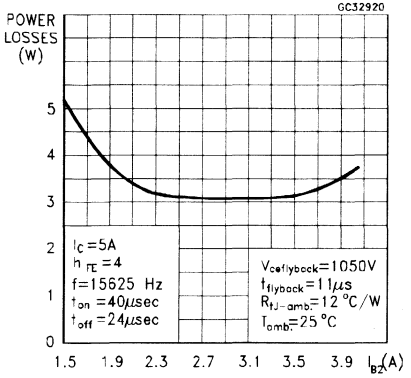
Collector-Emitter Saturation Voltage



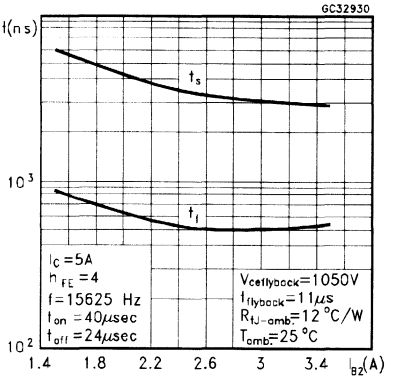
Base-Emitter Saturation Voltage



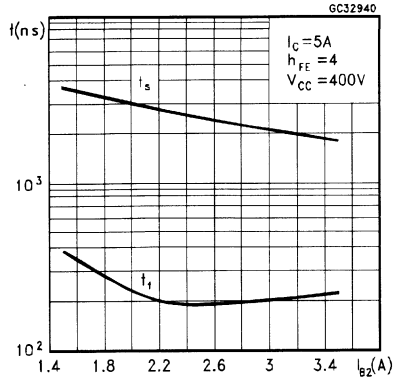
Power Losses at 16 KHz



Switching Time Inductive Load at 16 KHz (see figure 2)



Switching Time Resistive Load



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.

The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

Figure 1: Test Circuits for Dynamic Characterization.

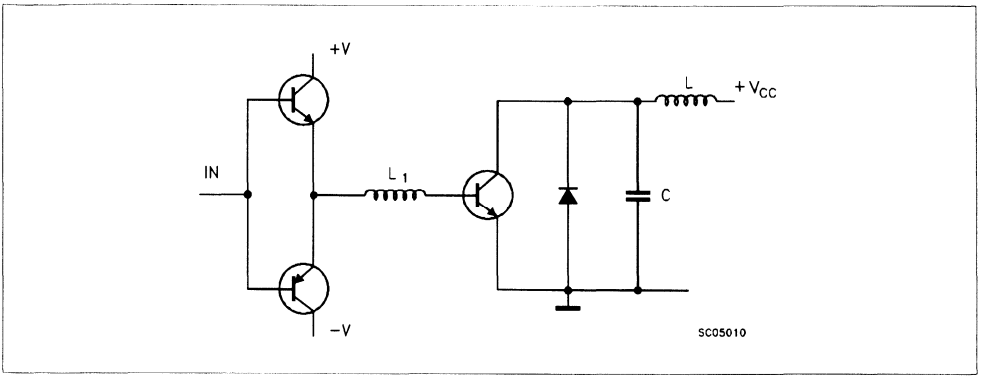
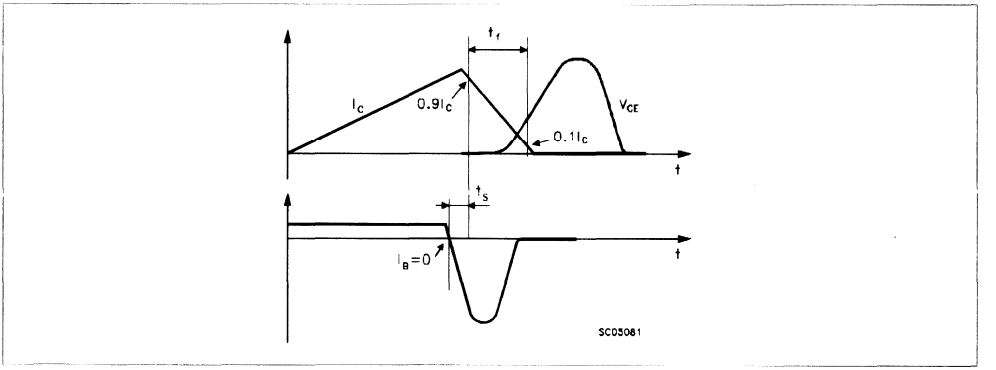


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

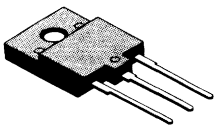
BUH517

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- FULLY INSULATED PACKAGE FOR EASY MOUNTING
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED
- COMPLETE CHARACTERIZATION OF POWER LOSSES AND SWITCHING TIMES AS A FUNCTION OF NEGATIVE BASE CURRENT FOR OPTIMUM DRIVE

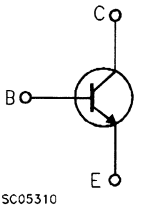
APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN STANDARD AND HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY FOR TV's AND MONITORS



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1700	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	15	A
I_B	Base Current	5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	8	A
P_{tot}	Total Dissipation at T_c = 25 °C	60	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

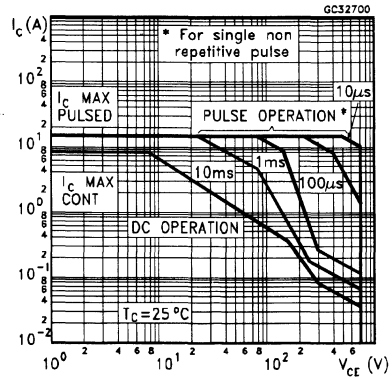
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.08	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

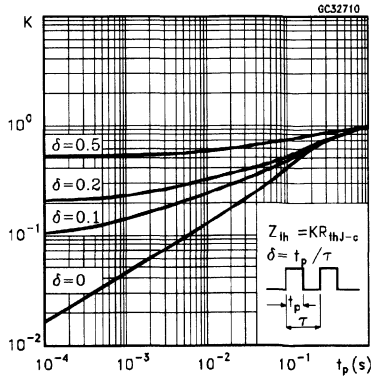
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1700 V V_{CE} = 1700 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 5 A V_{CE} = 5 V I_C = 5 A V_{CE} = 5 V T_j = 100 °C	6 4			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 5 A I_{B1} = 1.25 A I_{B2}= 2.5 A		2.7 190	3.9 280	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 5 A f = 15625 Hz I_{B1} = 1.25 A I_{B2} = 2.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		2.3 350		µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 5 A f = 31250 Hz I_{B1} = 1.25 A I_{B2} = 2.5 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		2.3 200		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

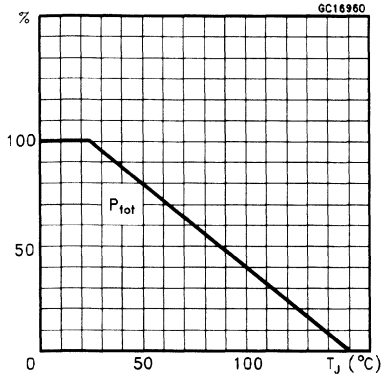
Safe Operating Areas



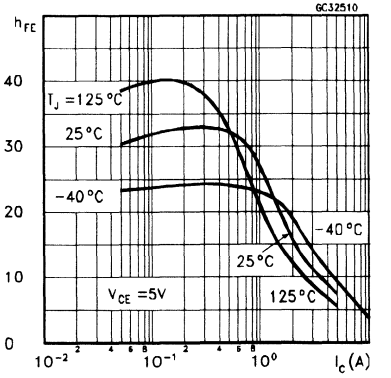
Thermal Impedance



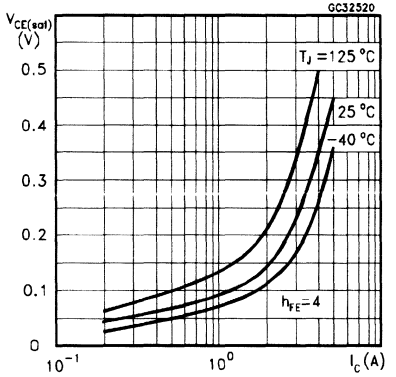
Derating Curves



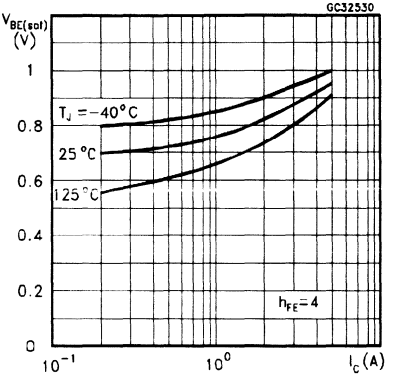
DC Current Gain



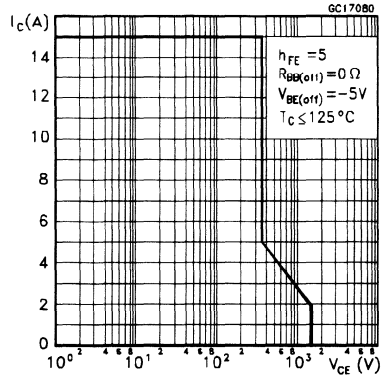
Collector-Emitter Saturation Voltage



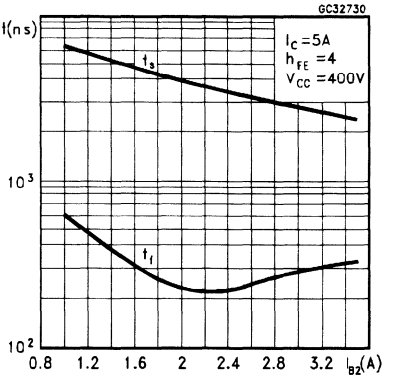
Base-Emitter Saturation Voltage



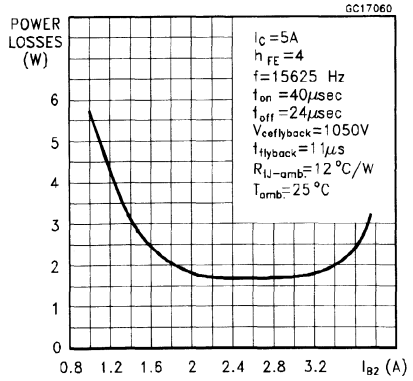
Reverse Biased SOA



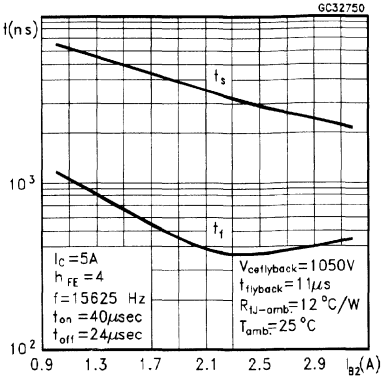
Switching Time Resistive Load



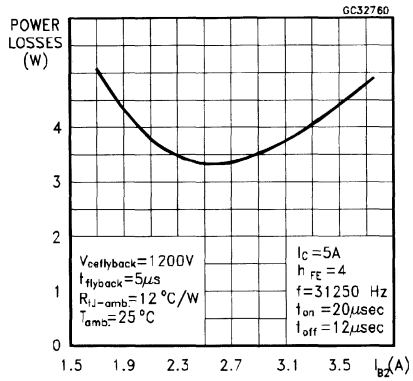
Power Losses at 16 KHz



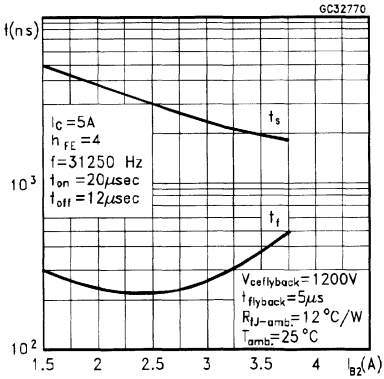
Switching Time Inductive Load at 16 KHz (see figure 2)



Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



BASE DRIVE INFORMATION

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is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.
The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

RBSOA INFORMATION

During turn-off with an inductive load, the power transistor has to withstand high voltages and high currents simultaneously with negative base-to-emitter voltage V_{BEoff}. Very often it has to reach a working area above V_{CEO}, remaining there all the time needed for the collector current I_C to fall to zero. The safe operation for the power transistor under these conditions is specified by RBSOA (Reverse Bias Safe Operating Area) which represents the permissible I_C-V_{CE} locus within which proper operation is guaranteed. RBSOA is strongly dependent on the circuit topology and is valid only under specified drive conditions. High voltage Multiepitaxial Fastswitching transistors of the BUH series have been optimized to give improved RBSOA to suit off-line switch mode power supplies applications.

Figure 1: Test Circuits for Dynamic Characterization.

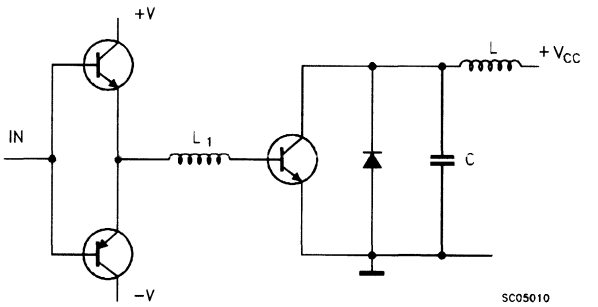
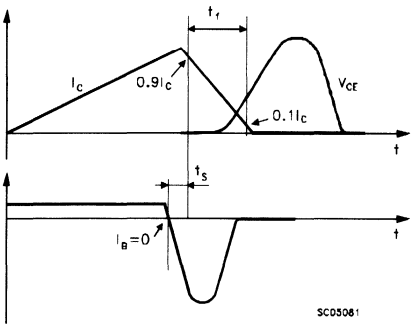


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

BUH715

CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

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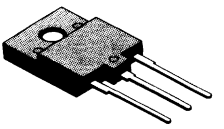
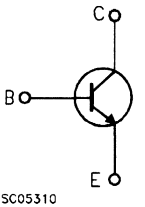


ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	10	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	20	A
I_B	Base Current	5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	10	A
P_{tot}	Total Dissipation at T_c = 25 °C	65	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

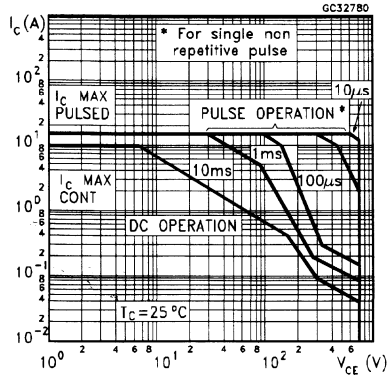
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.92	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

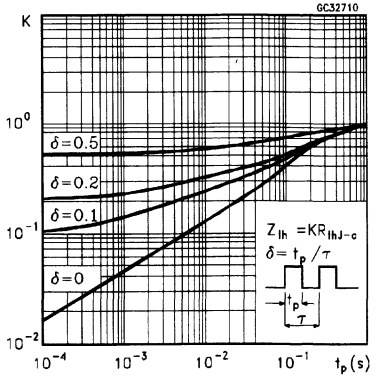
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 7 A I_B = 1.5 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 7 A I_B = 1.5 A			1.3	V
h_{FE}*	DC Current Gain	I_C = 7 A V_{CE} = 5 V I_C = 7 A V_{CE} = 5 V T_j = 100 °C	8 5			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 7 A I_{B1} = 1.5 A I_{B2}= 3.5 A		2.1 140	3.1 210	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 7 A f = 15625 Hz I_{B1} = 1.5 A I_{B2} = 3.5 A $V_{ceflyback} = 1050 \sin\left(\frac{\pi}{10} 10^6\right) t$ V		3.5 350		µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 7 A f = 31250 Hz I_{B1} = 1.5 A I_{B2} = 3.5 A $V_{ceflyback} = 1200 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		3.5 320		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

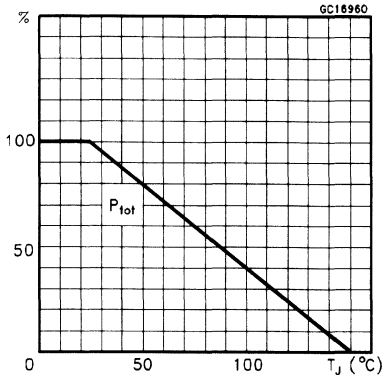
Safe Operating Areas



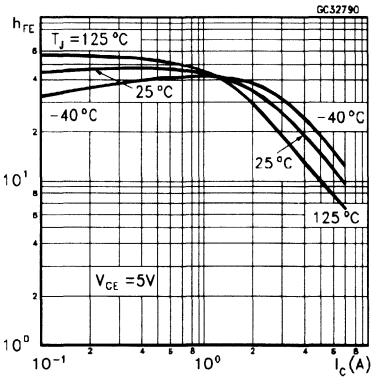
Thermal Impedance



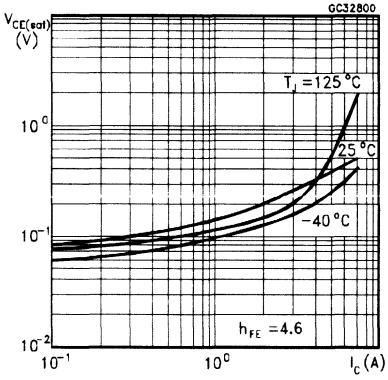
Derating Curves



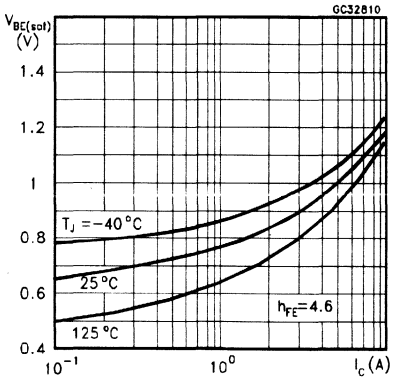
DC Current Gain



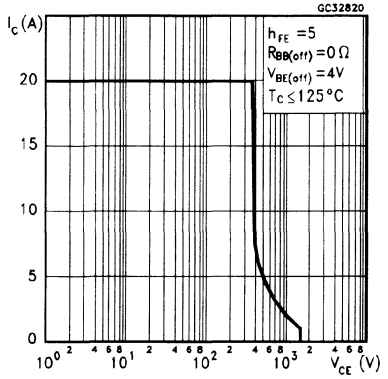
Collector-Emitter Saturation Voltage



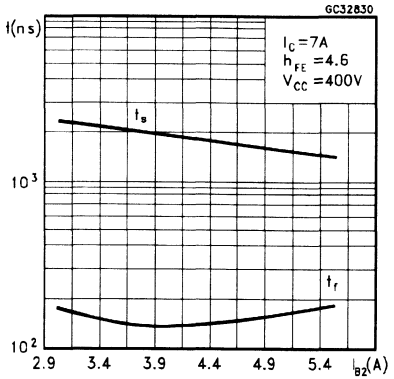
Base-Emitter Saturation Voltage



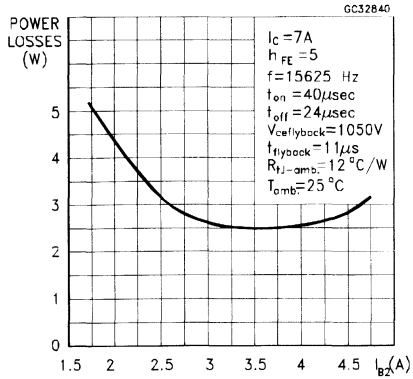
Reverse Biased SOA



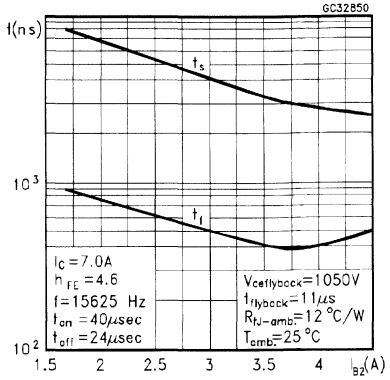
Switching Time Resistive Load



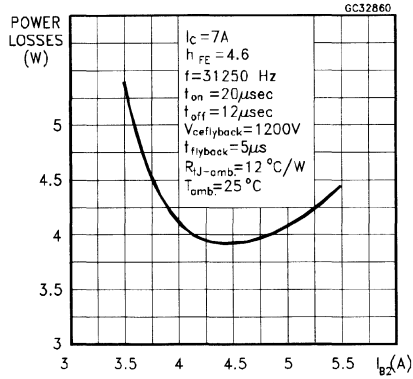
Power Losses at 16 KHz



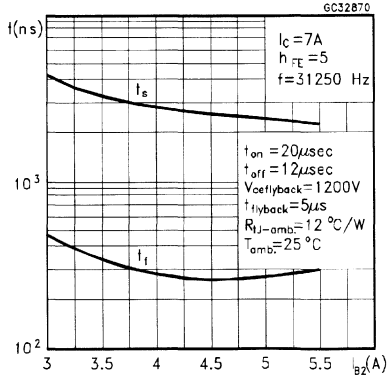
Switching Time Inductive Load at 16 KHz (see figure 2)



Power Losses at 32 KHz



Switching Time Inductive Load at 32 KHz (see figure 2)



BASE DRIVE INFORMATION

A fundamental parameter of high voltage power transistors like those used in the horizontal deflection stage is their junction temperature Tj, which, in turn, depends on the power dissipation. This parameter turns out to influence the system reliability under normal operation. Based on that, SGS-THOMSON has introduced a new dynamic, application-oriented characterization differing from the traditional data given in most datasheets.

In order to saturate the power switch and reduce conduction losses, adequate direct base current I_{B1} has to be provided for the lowest gain h_{FE} at T_j = 100 °C (line scan phase). On the other hand, negative base current I_{B2} must be provided for the transistor to be turned off (retrace phase). Most of the dissipation, especially in the deflection application, occurs at switch-off so it is essential to determine the value of I_{B2} which minimizes power losses, fall time t_f and, consequently, T_j. A new set of curves have been defined to give total power losses, t_s and t_f as a function of I_{B2} at both 16 KHz and 32 KHz scanning frequencies for choosing the optimum negative drive. The test circuit is illustrated in fig. 1.

Inductance L1 serves to control the slope of the negative base current I_{B2} in order that excess carriers in the collector recombine when base current is still present, thus avoiding any tailing phenomenon in the collector current. This effect

is, in any case, markedly reduced intrinsically by adopting the hollow emitter technology.
The values of L and C are calculated from the following equations:

$$\frac{1}{2} L (I_C)^2 = \frac{1}{2} C (V_{CEfly})^2$$

$$\omega = 2 \pi f = \frac{1}{\sqrt{L C}}$$

Where I_C= operating collector current, V_{CEfly}= flyback voltage, f= frequency of oscillation during retrace.

RBSOA INFORMATION

During turn-off with an inductive load, the power transistor has to withstand high voltages and high currents simultaneously with negative base-to-emitter voltage V_{BEoff}. Very often it has to reach a working area above V_{CEO}, remaining there all the time needed for the collector current I_C to fall to zero. The safe operation for the power transistor under these conditions is specified by RBSOA (Reverse Bias Safe Operating Area) which represents the permissible I_C-V_{CE} locus within which proper operation is guaranteed. RBSOA is strongly dependent on the circuit topology and is valid only under specified drive conditions. High voltage Multiepitaxial Fastswitching transistors of the BUH series have been optimized to give improved RBSOA to suit off-line switch mode power supplies applications.

Figure 1: Test Circuits for Dynamic Characterization.

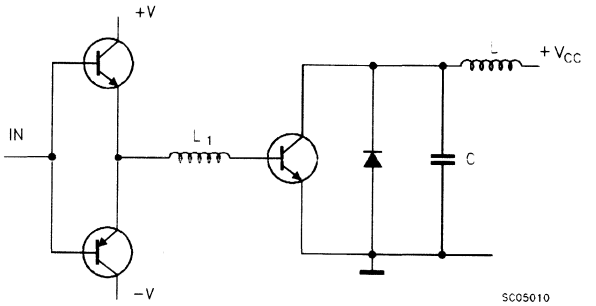
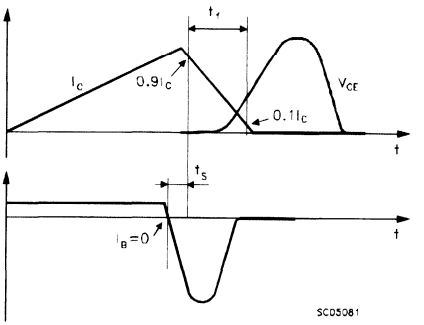


Figure 2: Switching Waveforms in a Deflection Circuit



SGS-THOMSON MICROELECTRONICS

BUH1015T

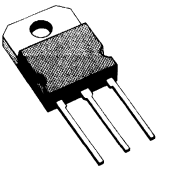
CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

ADVANCE DATA

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- LOW THERMAL RESISTANCE
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED

APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY



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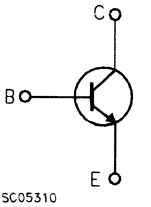
INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	16	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	22	A
I_B	Base Current	10	A
I_{BM}	Base Peak Current (t_p < 5 ms)	16	A
P_{tot}	Total Dissipation at T_c = 25 °C	160	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.78	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 10 A I_B = 2 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 10 A I_B = 2 A			1.5	V
h_{FE}*	DC Current Gain	I_C = 10 A V_{CE} = 5 V I_C = 10 A V_{CE} = 5 V T_j = 100 °C	7 5			
t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 10 A I_{B1} = 2 A I_{B2}= -5 A		2.2 110		µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 10 A f = 31250 Hz I_{B1} = 2 A I_{B2} = -5 A $V_{ceflyback} = 1350 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		4 220		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

SGS-THOMSON MICROELECTRONICS

BUH1215T

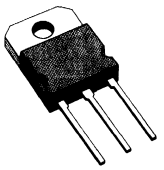
CRT HORIZONTAL DEFLECTION HIGH VOLTAGE NPN FASTSWITCHING TRANSISTOR

ADVANCE DATA

- HIGH BREAKDOWN VOLTAGE CAPABILITY
- LOW THERMAL RESISTANCE
- LOW SATURATION VOLTAGE
- HIGH SWITCHING SPEED

APPLICATIONS:

- HORIZONTAL DEFLECTION STAGE IN HIGH RESOLUTION DISPLAYS FOR TV's AND MONITORS
- SWITCHING POWER SUPPLY



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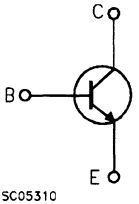
INTERNAL SCHEMATIC DIAGRAM



SC05310

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	10	V
I_C	Collector Current	19	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	26	A
I_B	Base Current	12	A
I_{BM}	Base Peak Current (t_p < 5 ms)	19	A
P_{tot}	Total Dissipation at T_c = 25 °C	200	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.63	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500 V V_{CE} = 1500 V T_j = 125 °C			1 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			100	μA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA	700			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	10			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 12 A I_B = 2.4 A			1.5	V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 12 A I_B = 2.4 A			1.5	V
h_{FE}*	DC Current Gain	I_C = 12 A V_{CE} = 5 V I_C = 12 A V_{CE} = 5 V T_j = 100 °C	7 5			
 t_s t_f	RESISTIVE LOAD Storage Time Fall Time	V_{CC} = 400 V I_C = 12 A I_{B1} = 2 A I_{B2}= -6 A		 1.5 110		 μs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 12 A f = 31250 Hz I_{B1} = 2 A I_{B2} = -6 A $V_{ceflyback} = 1350 \sin\left(\frac{\pi}{5} 10^6\right) t$ V		 4 220		 μs ns

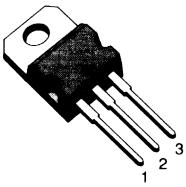
* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

SGS-THOMSON MICROELECTRONICS

BUL48

HIGH VOLTAGE NPN MULTIEPITAXIAL FASTSWITCHING TRANSISTOR

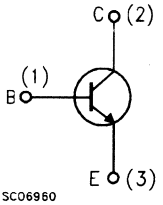
- HIGH VOLTAGE CAPABILITY
- TIGHT CONTROL OF DYNAMIC CHARACTERISTICS
- MINIMUM LOT TO LOT SPREAD FOR RELIABLE OPERATION
- LOW BASE DRIVE REQUIREMENTS
- VERY HIGH SWITCHING SPEED: t_f = 55ns (typ.) AND t_s = 1.3µs (typ.) AT I_C = 2.5A, I_{B1} = 0.5A, V_{BEoff} = -5V R_{BB} = 0Ω
- COMPLETE CHARACTERIZATION AT 125°C



TO-220

DESCRIPTION:
The BUL48 is a high voltage NPN FASTSWITCHING transistor designed to be used in lighting applications, like electronic ballasts for fluorescent lamps.
Its characteristics make it also ideal for power supplies

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)	800	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	400	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	9	V
I_C	Collector Current	7	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	11	A
I_B	Base Current	3.5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	7	A
P_{tot}	Total Dissipation at T_c = 25 °C	75	W
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

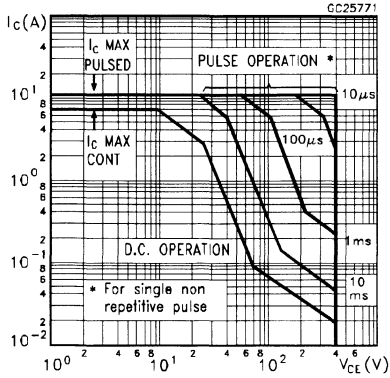
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	1.65	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

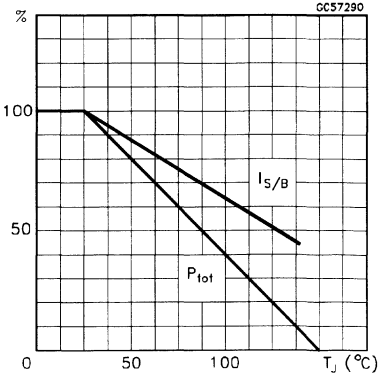
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 800 V V_{CE} = 800 V T_j = 125 °C			100 500	µA µA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{EC} = 400 V			250	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA L = 25 mH	400			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	9			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 2 A I_B = 0.5 A I_C = 3 A I_B = 0.6 A I_C = 4 A I_B = 1 A			1 1.5 1.5	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 2 A I_B = 0.5 A I_C = 3 A I_B = 0.6 A I_C = 4 A I_B = 1 A			1.2 1.5 1.5	V V V
h_{FE}*	DC Current Gain	I_C = 0.5 A V_{CE} = 3 V I_C = 1 A V_{CE} = 5 V I_C = 10 mA V_{CE} = 5 V	18 10	 30 	50 	
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 2.5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V R_{BB} = 0 Ω V_{CL} = 250 V L = 200 µH		 1.3 55	 2 100	 µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 2.5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V R_{BB} = 0 Ω V_{CL} = 250 V L = 200 µH T_j = 125 °C		 1.8 95	 	 µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

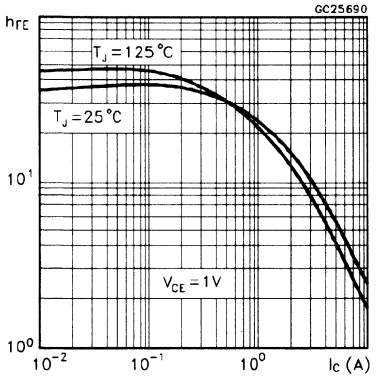
Safe Operating Area



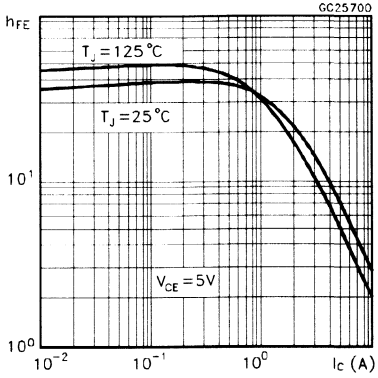
Derating Curve



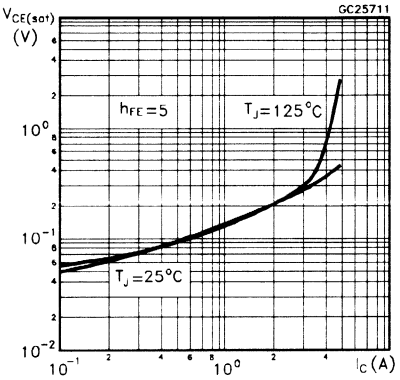
DC Current Gain



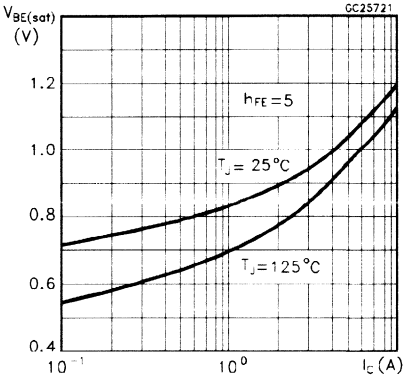
DC Current Gain



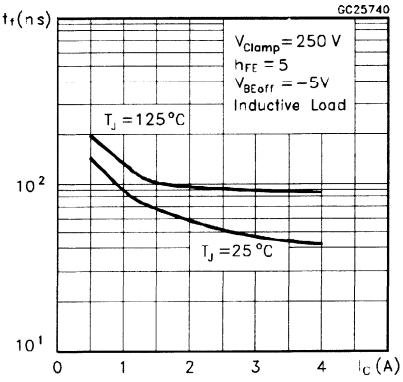
Collector Emitter Saturation Voltage



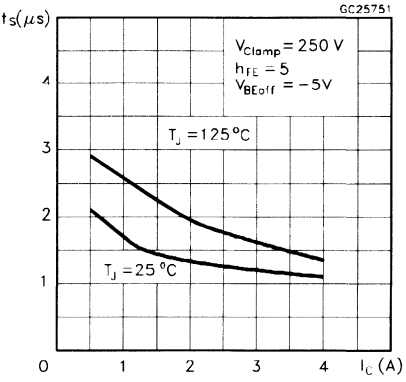
Base Emitter Saturation Voltage



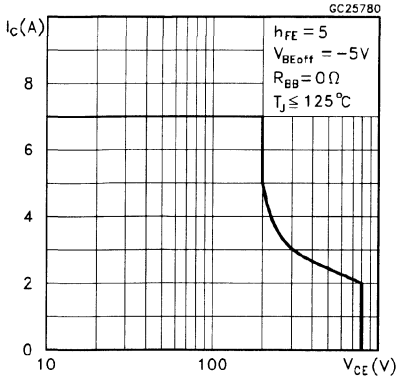
Inductive Fall Time



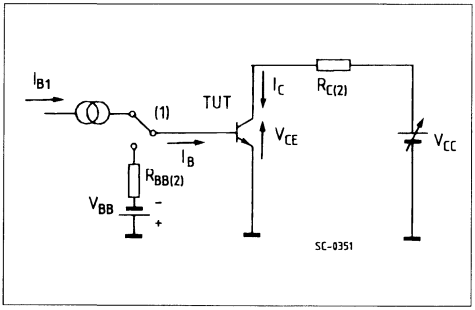
Inductive Storage Time



Reverse Biased SOA

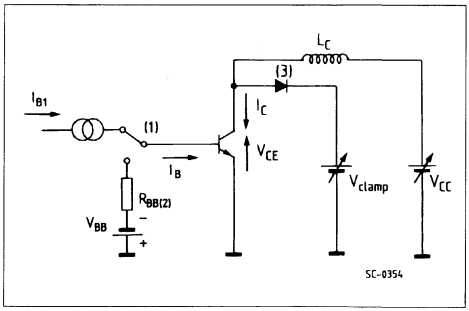


Resistive Load Switching Test Circuit



(1) Fast electronic switch
(2) Non-inductive Resistor

RBSOA and Inductive Load Switching Test Circuit



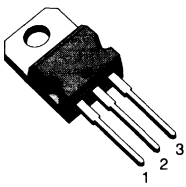
(1) Fast electronic switch
(2) Non-inductive Resistor
(3) Fast recovery rectifier

SGS-THOMSON MICROELECTRONICS

BUL410

HIGH VOLTAGE NPN MULTIEPITAXIAL FASTSWITCHING TRANSISTOR

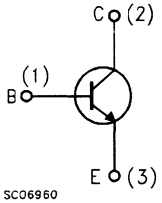
- HIGH VOLTAGE CAPABILITY
- TIGHT CONTROL OF DYNAMIC CHARACTERISTICS
- MINIMUM LOT TO LOT SPREAD FOR RELIABLE OPERATION
- LOW BASE DRIVE REQUIREMENTS
- VERY HIGH SWITCHING SPEED: t_f = 60ns (typ.) AND t_s = 1.3µs (typ.) AT I_C = 2.5A, I_{B1} = 0.5A, V_{BEoff} = -5V R_{BB} = 0Ω
- COMPLETE CHARACTERIZATION AT 125°C



TO-220

DESCRIPTION:
The BUL410 is a high voltage NPN FASTSWITCHING transistor designed to be used in lighting applications, like electronic ballasts for fluorescent lamps.
Its characteristics make it also ideal for power supplies

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)	1000	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	450	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	9	V
I_C	Collector Current	7	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	11	A
I_B	Base Current	3.5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	7	A
P_{tot}	Total Dissipation at T_c = 25 °C	75	W
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

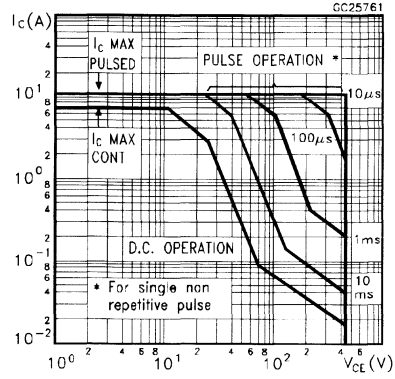
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	1.65	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

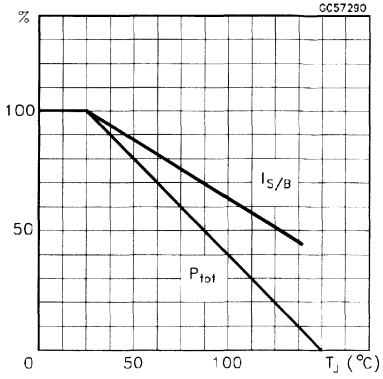
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1000 V V_{CE} = 1000 V T_j = 125 °C			100 500	µA µA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{EC} = 450 V			250	µA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA L = 25 mH	450			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	9			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 2 A I_B = 0.5 A I_C = 3 A I_B = 0.6 A I_C = 4 A I_B = 1 A			1 1.5 1.5	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 2 A I_B = 0.5 A I_C = 3 A I_B = 0.6 A I_C = 4 A I_B = 1 A			1.2 1.5 1.5	V V V
h_{FE}*	DC Current Gain	I_C = 1 A V_{CE} = 5 V I_C = 2 A V_{CE} = 5 V I_C = 10 mA V_{CE} = 5 V	15 8 10		55 40	
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 2.5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V R_{BB} = 0 Ω V_{CL} = 250 V L = 200 µH		1.3 60	2 110	µs ns
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 2.5 A I_{B1} = 0.5 A $V_{BE(off)}$ = -5 V R_{BB} = 0 Ω V_{CL} = 250 V L = 200 µH T_j = 125 °C		1.8 100		µs ns

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

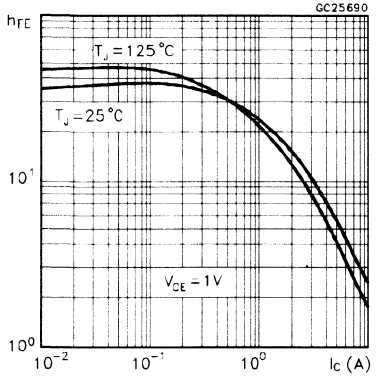
Safe Operating Area



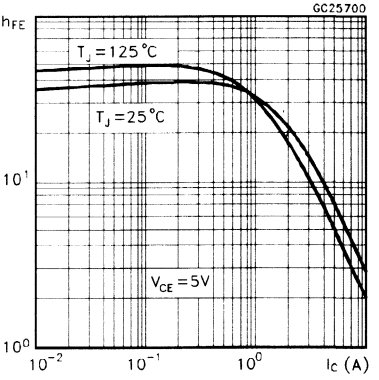
Derating Curve



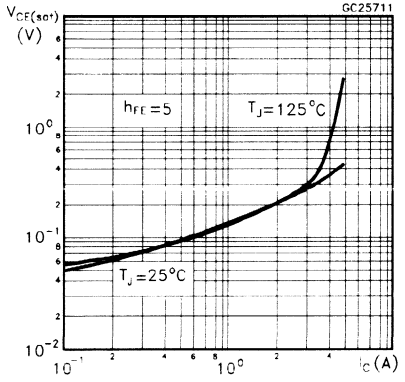
DC Current Gain



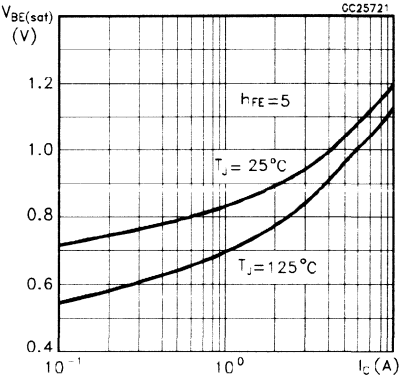
DC Current Gain



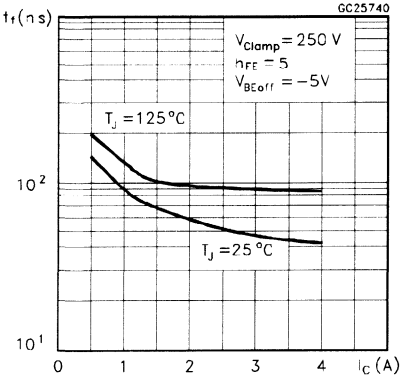
Collector Emitter Saturation Voltage



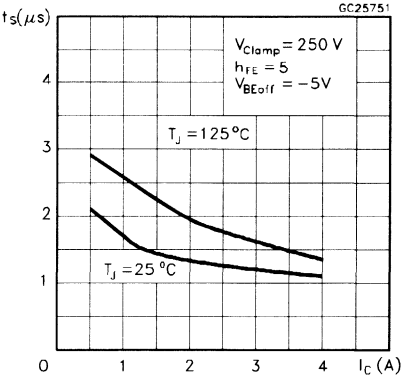
Base Emitter Saturation Voltage



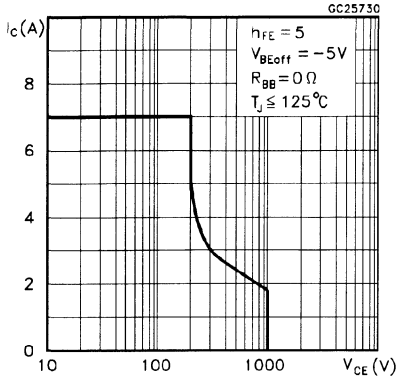
Inductive Fall Time



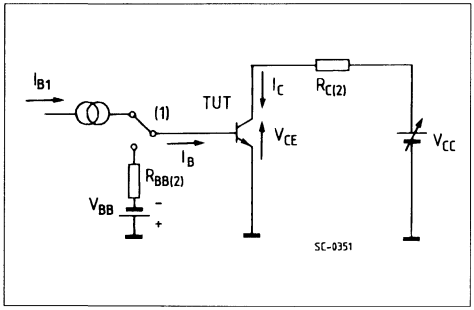
Inductive Storage Time



Reverse Biased SOA

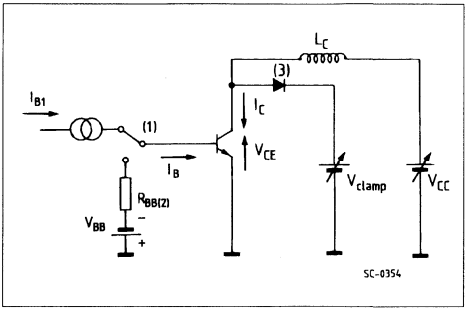


Resistive Load Switching Test Circuit



(1) Fast electronic switch
(2) Non-inductive Resistor

RBSOA and Inductive Load Switching Test Circuit



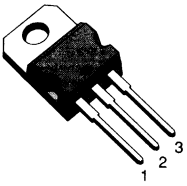
(1) Fast electronic switch
(2) Non-inductive Resistor
(3) Fast recovery rectifier

SGS-THOMSON MICROELECTRONICS

BUL510

HIGH VOLTAGE NPN MULTIEPITAXIAL FASTSWITCHING TRANSISTOR

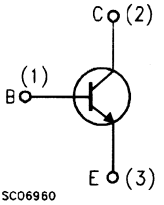
- HIGH VOLTAGE CAPABILITY
- TIGHT CONTROL OF DYNAMIC CHARACTERISTICS
- MINIMUM LOT TO LOT SPREAD FOR RELIABLE OPERATION
- LOW BASE DRIVE REQUIREMENTS
- VERY HIGH SWITCHING SPEED: t_f = 80 ns (typ.) AND t_s = 2.2 µs (typ.) AT I_C = 4 A, I_{B1} = 0.8 A, I_{B2} = -1.6A
- COMPLETE CHARACTERIZATION AT 125°C



TO-220

DESCRIPTION:
The BUL510 is a high voltage NPN FASTSWITCHING transistor designed to be used in lighting applications, like electronic ballasts for fluorescent lamps.
Its characteristics make it also ideal for power supplies.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)	1000	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	450	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	9	V
I_C	Collector Current	8	A
I_{CM}	Collector Peak Current (t_p < 5 ms)	12	A
I_B	Base Current	3.5	A
I_{BM}	Base Peak Current (t_p < 5 ms)	7	A
P_{tot}	Total Dissipation at T_c = 25 °C	80	W
T_{stg}	Storage Temperature Range	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

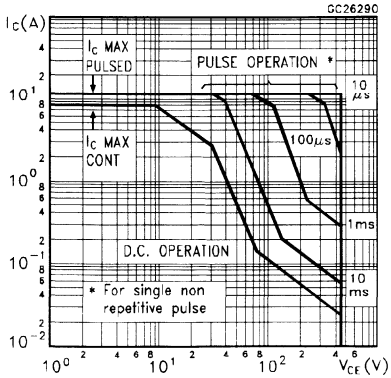
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	1.56	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-Ambient	Max	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

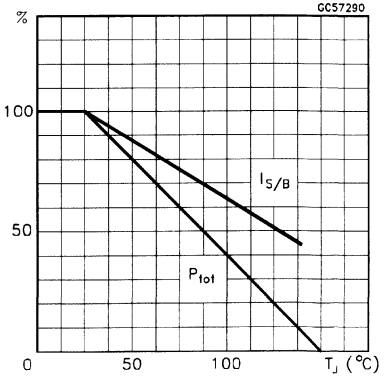
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1000 V V_{CE} = 1000 V T_j = 125 °C			100 500	μA μA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = 450 V			250	μA
$V_{CEO(sus)}$	Collector-Emitter Sustaining Voltage	I_C = 100 mA L = 25 mH	450			V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	I_E = 10 mA	9			V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 3 A I_B = 0.6 A I_C = 4 A I_B = 0.8 A I_C = 5 A I_B = 1.25 A			0.8 1 1.5	V V V
$V_{BE(sat)}$*	Base-Emitter Saturation Voltage	I_C = 3 A I_B = 0.6 A I_C = 5 A I_B = 1.25 A			1.2 1.5	V V
h_{FE}*	DC Current Gain	I_C = 1 A V_{CE} = 5 V I_C = 10 mA V_{CE} = 5 V	15 10		45	
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4 A V_{CL} = 300 V I_{B1} = 0.8 A I_{B2} = -1.6 A L = 200 μH		2.2 80	3.4 150	 μs ns
 t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4 A V_{CL} = 300 V I_{B1} = 0.8 A I_{B2} = -1.6 A L = 200 μH T_j = 125 °C		3 120		 μs ns

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %

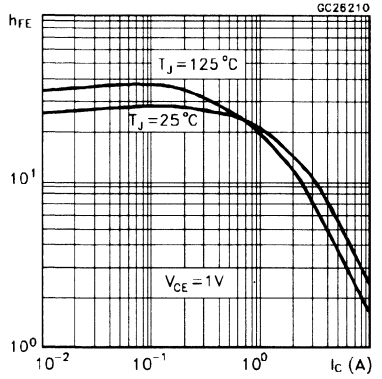
Safe Operating Areas



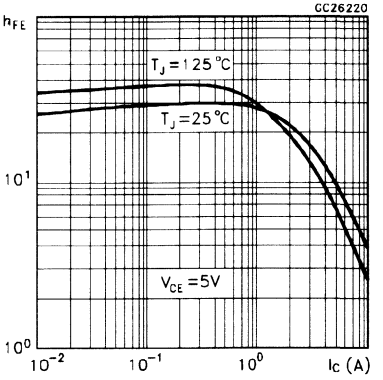
Derating Curves



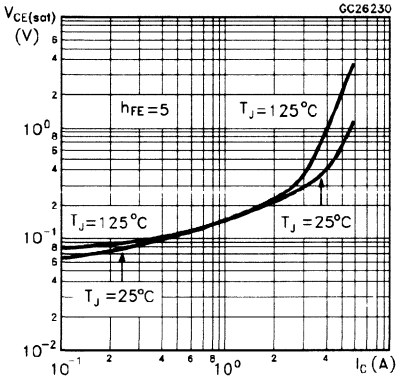
DC Current Gain



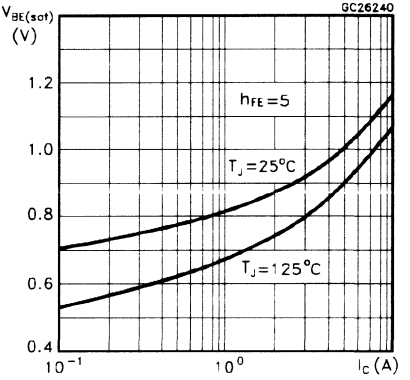
DC Current Gain



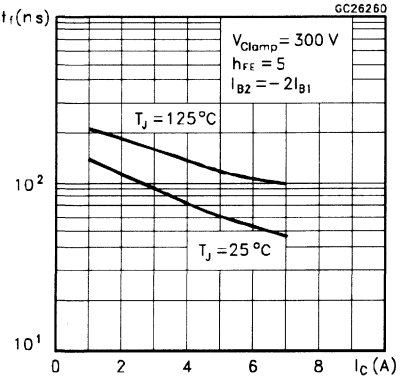
Collector Emitter Saturation Voltage



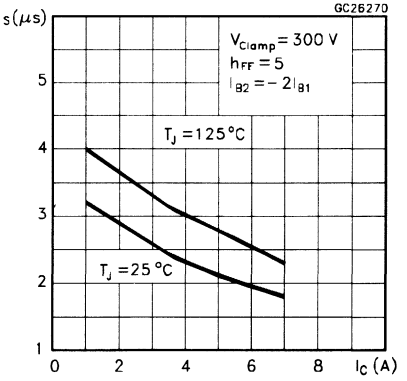
Base Emitter Saturation Voltage



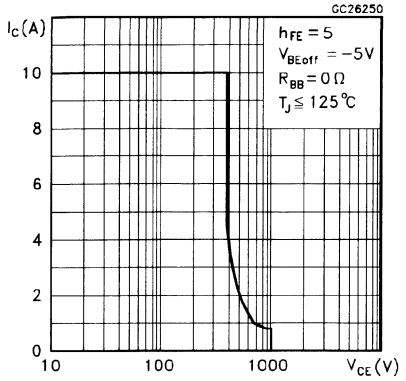
Inductive Fall Time



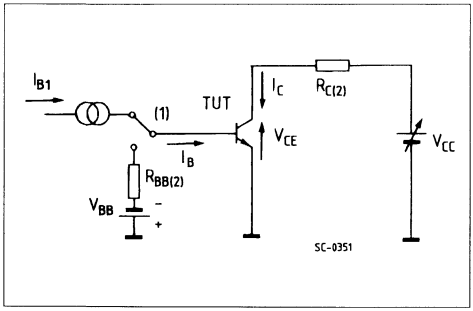
Inductive Storage Time



Reverse Biased SOA

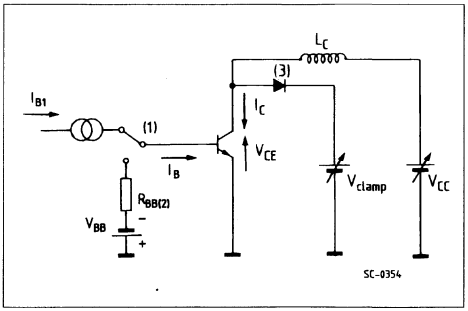


Resistive Load Switching Test Circuit



(1) Fast electronic switch
(2) Non-inductive Resistor

RBSOA and Inductive Load Switching Test Circuit



(1) Fast electronic switch
(2) Non-inductive Resistor
(3) Fast recovery rectifier

FASTSWITCH HOLLOW–EMITTER NPN TRANSISTOR

- HIGH SWITCHING SPEED NPN POWER TRANSISTOR
- HOLLOW EMITTER TECHNOLOGY
- HIGH VOLTAGE FOR OFF-LINE APPLICATIONS
- 50kHz SWITCHING SPEED
- LOW COST DRIVE CIRCUITS
- LOW DYNAMIC SATURATION

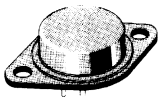
APPLICATIONS

- SMPS
- TV AND MONITOR DEFLECTION

DESCRIPTION

This hollow emitter FASTSWITCH NPN power transistor is specially designed for 220V (and 117V with input doubler) off-line switching power supply applications. It can also be used for 117V three phase mains off-line switching power supplies. Hollow emitter transistors can operate at up to 50kHz with simple drive circuits which helps to simplify design and improve reliability. The superior switching performance reduces dissipation and consequently lowers the equipment operating temperature. This transistor is suitable for applications in half bridge and full bridge high power converters, 900W to 1800W. The high switching speed of this transistor together with its high voltage and current rating, make it ideal for horizontal deflection circuits in large screen colour televisions and monitors. When used in conjunction with a low voltage Power MOSFET in emitter switch configuration, they can operate at up to 100kHz.

This hollow emitter FASTSWITCH transistor is available in the metal can TO-3 package.



TO-3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SGSF664	Unit
V_{CES}	Collector - Emitter Voltage (V_{BE} = 0)	1200	V
V_{CEO}	Collector - Emitter Voltage (I_B = 0)	600	V
V_{EBO}	Emitter - Base Voltage (I_C = 0)	7	V
I_C	Collector Current	20	A
I_{CM}	Collector Peak Current (t_p < 5ms)	30	A
I_B	Base Current	14	A
I_{BM}	Base Peak Current (t_p < 5ms)	24	A
P_{tot}	Total Dissipation at T ≤ 25°C	250	W
T_{stg}	Storage Temperature – 65 to	175	°C
T_j	Junction Temperature	175	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	V_{CE} = 1200V			400	µA
I_{CEO}	Collector Cutoff Current (I_B = 0)	V_{CE} = 380V V_{CE} = 600V			400 4	µA mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 7V			2	mA
$V_{CEO\ (sus)}$*	Collector Emitter Sustaining Voltage	I_C = 0.2A	600			V
$V_{CE\ (sat)}$*	Collector Emitter Saturation Voltage	I_C = 12A I_B = 2.4A I_C = 7A I_B = 1A			1.5 1.5	V V
$V_{BE\ (sat)}$*	Base Emitter Saturation Voltage	I_C = 12A I_B = 2.4A I_C = 7A I_B = 1A			1.5 1.5	V V

RESISTIVE LOAD

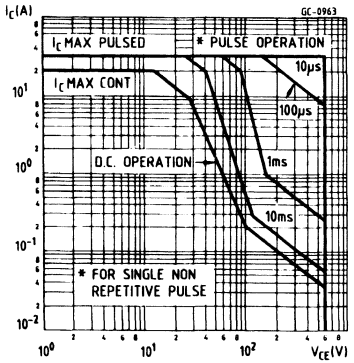
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Time	I_C = 12A V_{CC} = 250V I_{B1} = 2.4A I_{B2} = − $2I_{B1}$		0.6	1.2	µs
t_s	Storage Time			2.45	3.5	µs
t_f	Fall Time			0.12	0.4	µs
t_{on}	Turn-on Time	I_C = 12A V_{CC} = 250V I_{B1} = 2.4A I_{B2} = − $2I_{B1}$ with Antisaturation Network		0.6		µs
t_s	Storage Time			1.7		µs
t_f	Fall Time			0.12		µs
t_{on}	Turn-on Time	I_C = 12A V_{CC} = 250V I_{B1} = 2.4A $V_{BE(off)}$ = − 5V		0.6		µs
t_s	Storage Time			1.3		µs
t_f	Fall Time			0.2		µs

INDUCTIVE LOAD

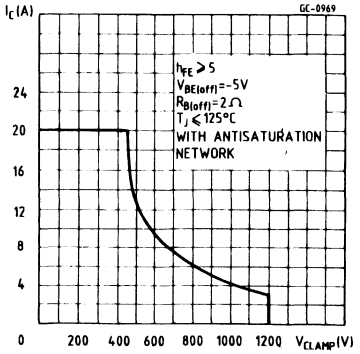
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_s	Storage Time	I_C = 12A h_{FE} = 5 V_{CL} = 450V $V_{BE(off)}$ = − 5V L = 300µH $R_{B(off)}$ = 0.5Ω		1.5	3	µs
t_f	Fall Time			0.12	0.25	µs
t_s	Storage Time	I_C = 12A h_{FE} = 5 V_{CL} = 450V $V_{BE(off)}$ = − 5V L = 300µH $R_{B(off)}$ = 0.5Ω T_c = 100°C			4.3	µs
t_f	Fall Time				0.35	µs

* Pulsed : Pulse duration = 300µs, duty cycle = 1.5%

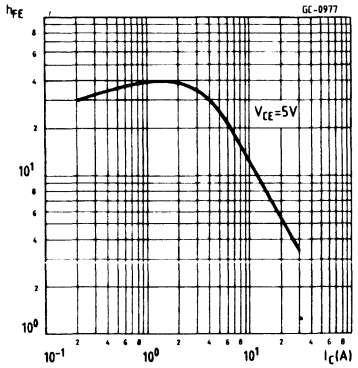
Safe Operating Areas



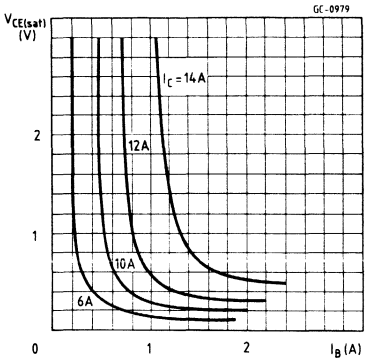
Reverse Biased Safe Operating Area



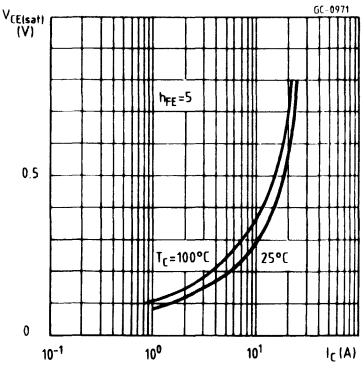
DC Current Gain



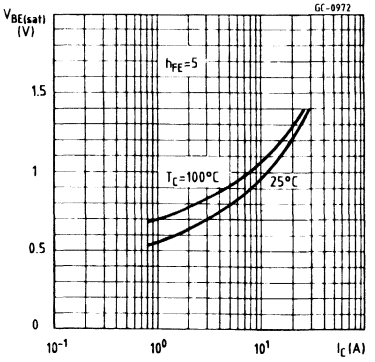
Collector-emitter Saturation Voltage



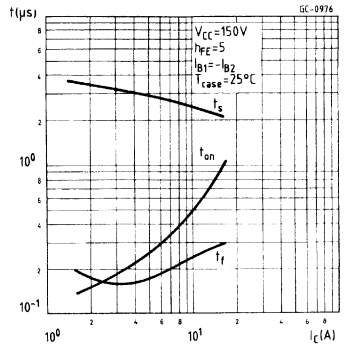
Collector-emitter Saturation Voltage



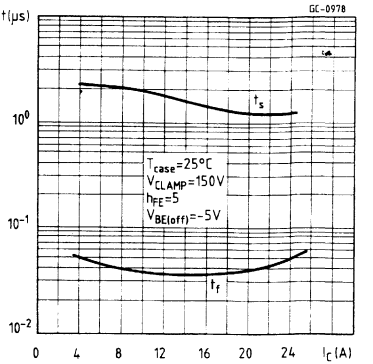
Base-emitter Saturation Voltage



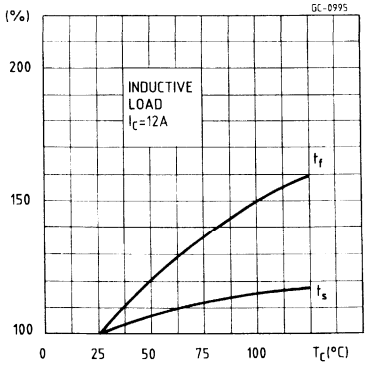
Resistive Load Switching Times



Inductive Load Switching Times



Switching Times Percentance Variation



FASTSWITCH HOLLOW–EMITTER NPN TRANSISTOR

- HIGH SWITCHING SPEED NPN POWER TRANSISTOR
- HOLLOW EMITTER TECHNOLOGY
- HIGH VOLTAGE FOR OFF-LINE APPLICATIONS
- 50kHz SWITCHING SPEED
- LOW COST DRIVE CIRCUITS
- LOW DYNAMIC SATURATION

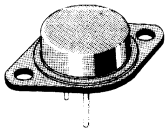
APPLICATIONS

- SMPS
- TV AND MONITOR DEFLECTION

DESCRIPTION

This hollow emitter FASTSWITCH NPN power transistor is specially designed for 220V (and 117V with input doubler) off-line switching power supply applications. It can also be used for 117V three phase mains off-line switching power supplies. The superior switching performance reduces dissipation and consequently lowers the equipment operating temperature. This transistor is suitable for applications in half bridge and full bridge high power converters, 700W to 1500W. The high switching speed of this transistor, together with its high voltage and current rating, make it ideal for horizontal deflection circuits in large screen colour televisions and monitors. When used in conjunction with a low voltage Power MOSFET in emitter switch configuration, they can operate at up to 100kHz.

This hollow emitter FASTSWITCH transistor is available in the metal can TO-3 package.



TO-3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SGSF665	Unit
V_{CES}	Collector - Emitter Voltage (V_{BE} = 0)	1300	V
V_{CEO}	Collector - Emitter Voltage (I_B = 0)	600	V
V_{EBO}	Emitter - Base Voltage (I_C = 0)	7	V
I_C	Collector Current	20	A
I_{CM}	Collector Peak Current (t_p < 5ms)	30	A
I_B	Base Current	14	A
I_{BM}	Base Peak Current (t_p < 5ms)	24	A
P_{tot}	Total Dissipation at T ≤ 25°C	250	W
T_{stg}	Storage Temperature – 65 to	175	°C
T_j	Junction Temperature	175	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.6	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	V_{CE} = 1300V			400	μA
I_{CEO}	Collector Cutoff Current (I_B = 0)	V_{CE} = 380V V_{CE} = 600V			400 4	μA mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 7V			2	mA
$V_{CEO\ (sus)}$*	Collector Emitter Sustaining Voltage	I_C = 0.2A	600*			V
$V_{CE\ (sat)}$*	Collector Emitter Saturation Voltage	I_C = 10A I_B = 2A I_C = 6A I_B = 0.9A			1.5 1.5	V V
$V_{BE\ (sat)}$*	Base Emitter Saturation Voltage	I_C = 10A I_B = 2A I_C = 6A I_B = 0.9A			1.5 1.5	V V

RESISTIVE LOAD

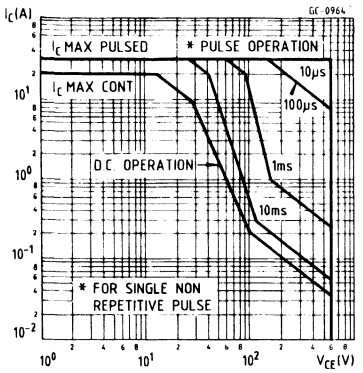
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Time	I_C = 10A V_{CC} = 250V I_{B1} = 2A I_{B2} = − 2 I_{B1}		0.6	1.2	μs
t_s	Storage Time			2.45	3.5	μs
t_f	Fall Time			0.12	0.4	μs
t_{on}	Turn-on Time	I_C = 10A V_{CC} = 250V I_{B1} = 2A I_{B2} = − 2 I_{B1} With Antisaturation Network		0.6		μs
t_s	Storage Time			1.7		μs
t_f	Fall Time			0.12		μs
t_{on}	Turn-on Time	I_C = 10A V_{CC} = 250V I_{B1} = 2A $V_{BE(off)}$ = − 5V		0.6		μs
t_s	Storage Time			1.3		μs
t_f	Fall Time			0.2		μs

INDUCTIVE LOAD

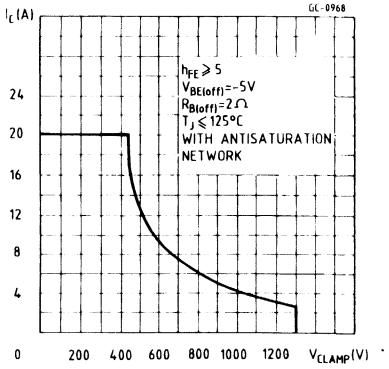
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_s	Storage Time	I_C = 10A h_{FE} = 5 V_{CL} = 450V $V_{BE(off)}$ = − 5V L = 300μH $R_{B(off)}$ = 0.5Ω		1.5	3	μs
t_f	Fall Time			0.12	0.25	μs
t_s	Storage Time	I_C = 10A h_{FE} = 5 V_{CL} = 450V $V_{BE(off)}$ = − 5V L = 300μH $R_{B(off)}$ = 0.5Ω T_C = 100°C			4.3	μs
t_f	Fall Time				0.35	μs

* Pulsed : Pulse duration = 300μs, duty cycle = 1.5%

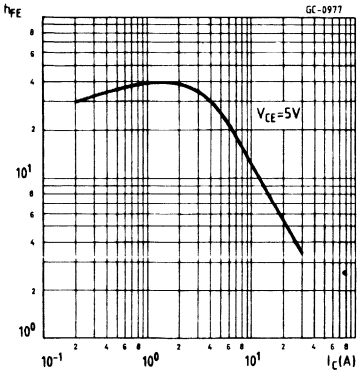
Safe Operating Areas



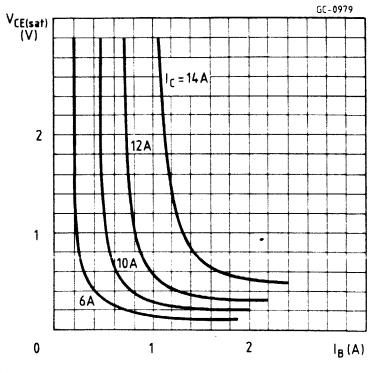
Reverse Biased Safe Operating Area



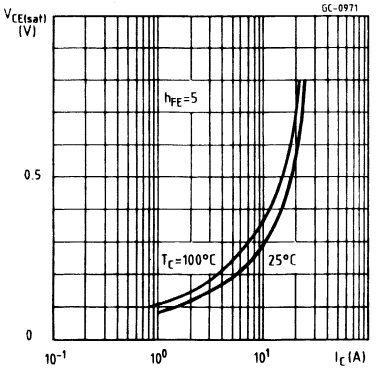
DC Current Gain



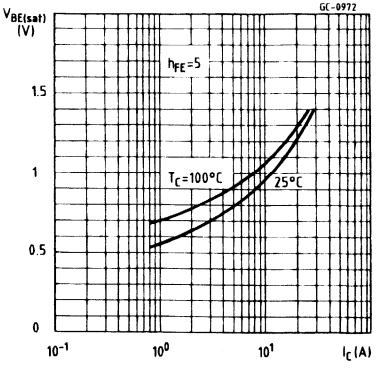
Collector-emitter Saturation Voltage



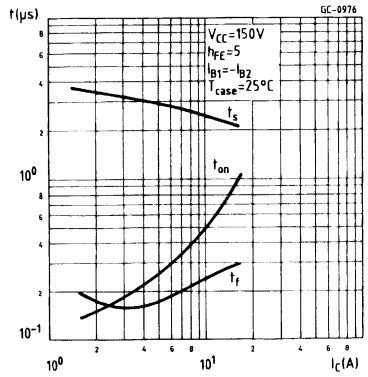
Collector-emitter Saturation Voltage



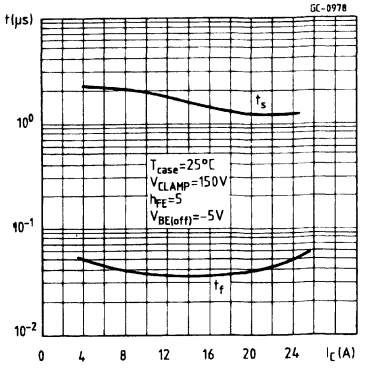
Base-emitter Saturation Voltage



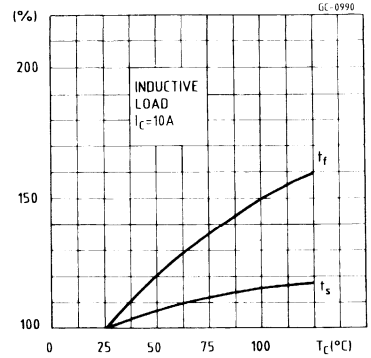
Resistive Load Switching Times



Inductive Load Switching Times



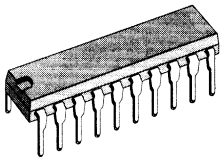
Switching Times Percentance Variation



CHROMA

PAL DECODER AND VIDEO PROCESSOR

- RGB OUTPUTS
- SINGLE CHIP CHROMA AND LUMINANCE PROCESSOR
- DC CONTROL BRIGHTNESS, CONTRAST, AND SATURATION
- FEW EXTERNAL COMPONENTS
- FAST BLANKING INPUT FOR OSD INSERTION
- SUPER SANDCASTLE INPUT



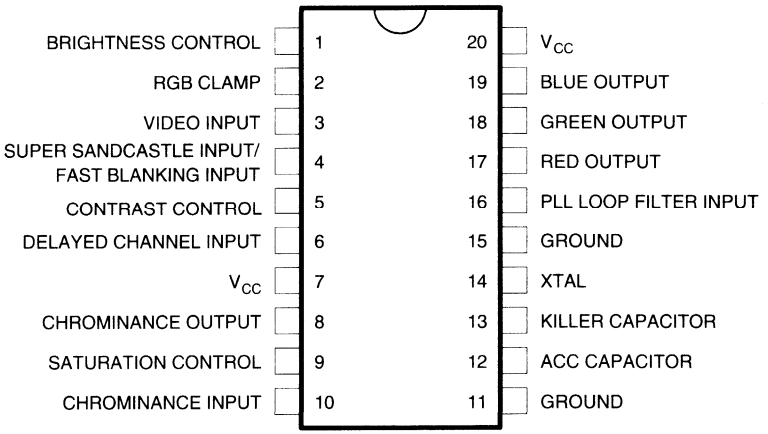
DIP20
(Plastic Package)

ORDER CODE : TDA8217

DESCRIPTION

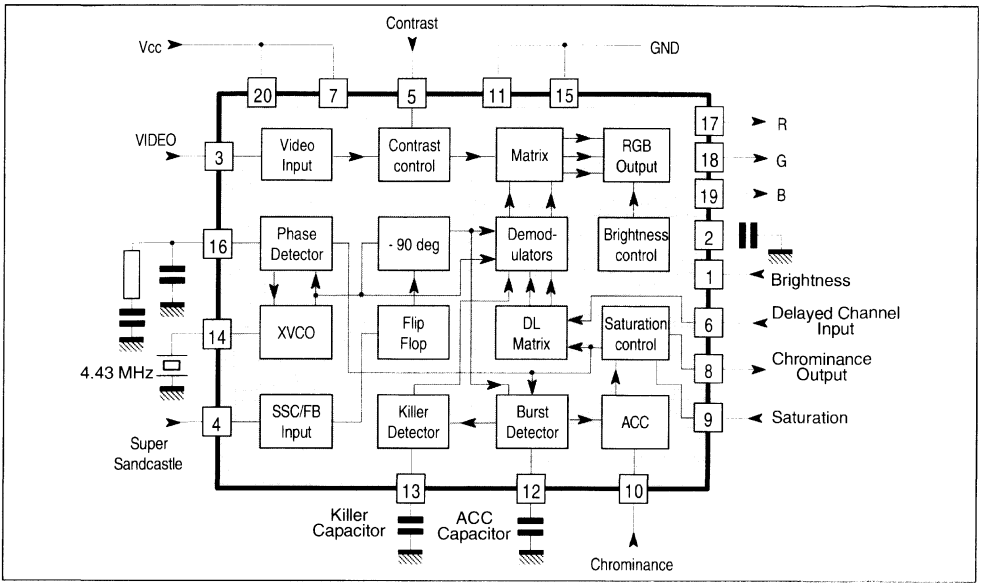
The TDA8217 is a monolithic integrated color decoder for the PAL standard. It includes in a 20 pins IC all the functions required for the identification and demodulation of PAL signals, and all the videoprocessor functions up to the drive of the video stages. Used with TDA8213 (video & sound IF system) and TDA8214A (H/V deflection circuit), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



8217-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	12	V
T_{OPER}	Operating temperature	0 , + 70	°C
T_{STG}	Storage temperature	-55 , + 150	°C

8217-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH\ (j\text{-}a)}$	Junction to ambient thermal resistance	Max.	80	°C/W

8217-02.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		8	9	10	V
I_{CC}	Supply Current	No Load		30	50	mA
P_D	Total Power Dissipation	No Load		270	450	mW
LUMINANCE INPUT (Pin 3)						
	Input Level before Clipping (Black to White)				500	mV_{PP}
	DC Operating Voltage	No Input Signal	2.5	2.8	3.1	V
	Input Current	During Burst Period Out of Burst Period	± 50	± 100	± 150 5	µA µA
CHROMINANCE INPUT (Pin 10)						
	Input Level before Clipping				900	mV_{PP}
	ACC Control Range	Change of Burst Signal over whole ACC Control Range < 1dB	30			dB
	Minimum Burst Signal Amplitude within the ACC Control Range		30			mV_{PP}

8217-03.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMINANCE INPUT (Pin 10) (continued)						
	Input Impedance		6	8	12	kΩ
	DC Operating Voltage	No Input Signal	2.3	2.8	3.3	V
SSC INPUT (Pin 4)						
	Burst Gate Threshold		7.0	7.5	8.0	V
	Line Blanking Threshold		3.1	3.6	3.9	V
	Frame Blanking Threshold / Fast Blanking		0.5	1	1.5	V
	Input Current				60	µA
CONTRAST CONTROL INPUT (Pin 5) (See Figure 1)						
	Input Current				10	µA
	Contrast Control Range		20			dB
SATURATION CONTROL INPUT (Pin 9) (See Figure 2)						
	Input Current				10	µA
	Tracking between Luminance and Chrominance Signals over 10 dB Contrast Control				2	dB
BRIGHTNESS CONTROL INPUT (Pin 1) (See Figure 3)						
	Input Current				10	µA
ACC CAPACITOR (Pin 12)						
	Charging Current	During Burst Gate Period		100		µA
	Discharging Current	During Burst Gate Period			10	µA
	Leakage Current	Out of Burst Gate Period			5	µA
KILLER CAPACITOR (Pin 13)						
	Color off Voltage	No Chroma Signal		5.6		V
	Color on Voltage			6		V
	PAL flip-flop inhibition level			3.2		V
	Control Current			150		µA
	Leakage Current				5	µA
	Voltage with Nominal Input Signal		6.4	6.5	7.0	V
PLL LOOP FILTER (Pin 16)						
	Control Current			800		µA
	Leakage Current				5	µA
SUBCARRIER OUTPUT (Pin 8)						
	Output Burst Amplitude	Within ACC Control Range	1.6	2.4	3.0	V_{PP}
DELAYED CHANNEL INPUT (Pin 6)						
	DC Operating Voltage	No Input Signal	2.0	2.2	2.4	V
	Input impedance		6	8	12	kΩ
RGB OUTPUTS (Pins 17-18-19)						
	Output Signal Amplitude (Black to White)	0.35V B to W, Signal @ Pin 3, Contrast @ 4.2V, Sat. @ 1.6V, Brig. @ 3.5V	2.80	3.15	3.50	V
	Blue Channel Output Amplitude (no Y)	300 mV_{PP} (B-Y), Signal with 200mV_{PP} Burst Amplitude at pin 10, Contrast @ 4.2V, Sat. @ 4.2V, Brig. @ 3.5V	3.5	3.9	4.3	V_{PP}
	Individual Output Sinking Current				2	mA

8217-04.TBL

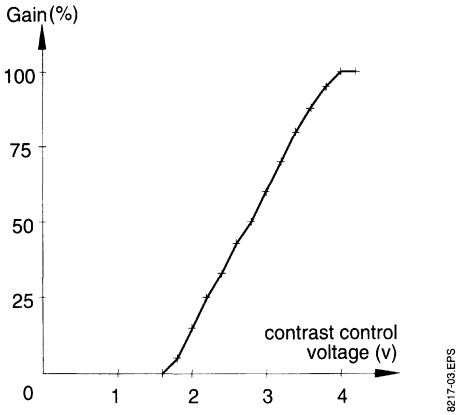
DC AND AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 9V , T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RGB OUTPUTS (Pins 17-18-19)						
	Maximum Peak White Level		7.4	7.8	8.2	V
	Blanking Level		1.0	1.2	1.4	V
	Black Level Differential Error				300	mV
	Relative Variation in Black Level with Various Saturation, Contrast and Brightness Control Level				10	mV
	Black Level Thermal Drift			0.5		mV/°C
	Differential Black Level Drift over 40°C Temperature Range			5		mV
	Frequency Response(-3dB)			5		MHz
XTAL (Pin 14)						
	Catching Range		± 500	± 700		Hz
RGB CLAMP CAPACITOR (Pin 2)						
	Control Current		50	100	150	µA
	Leakage Current				5	µA

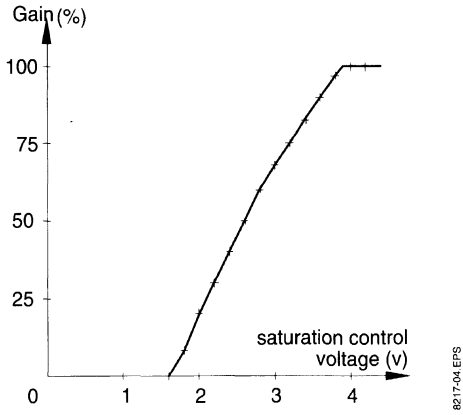
8217-05.TBL

Figure 1 : Contrast Control Voltage Range



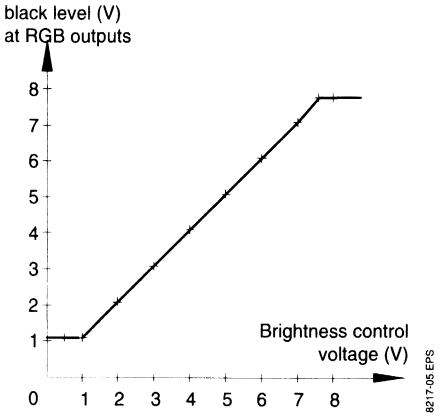
8217-03.EPS

Figure 2 : Saturation Control Voltage Range



8217-04.EPS

Figure 3 : Brightness Control Voltage Range



INPUT / OUTPUT PIN CONFIGURATION

Figure 4 : Pins 1 - 2 Configuration

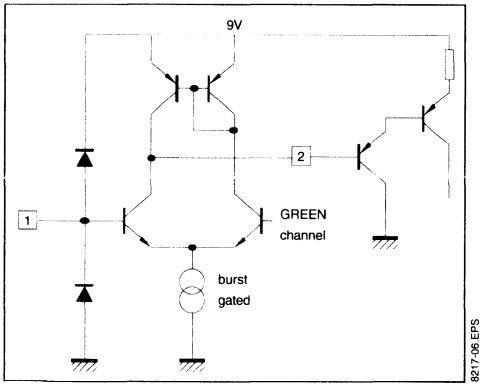


Figure 5 : Pin 3 Configuration

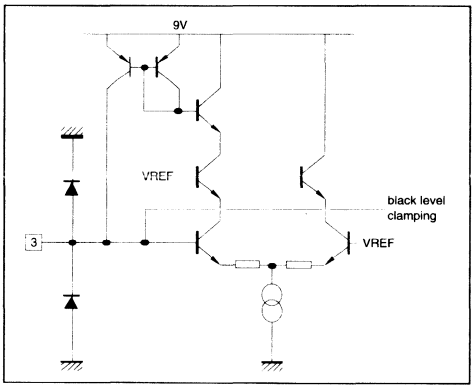
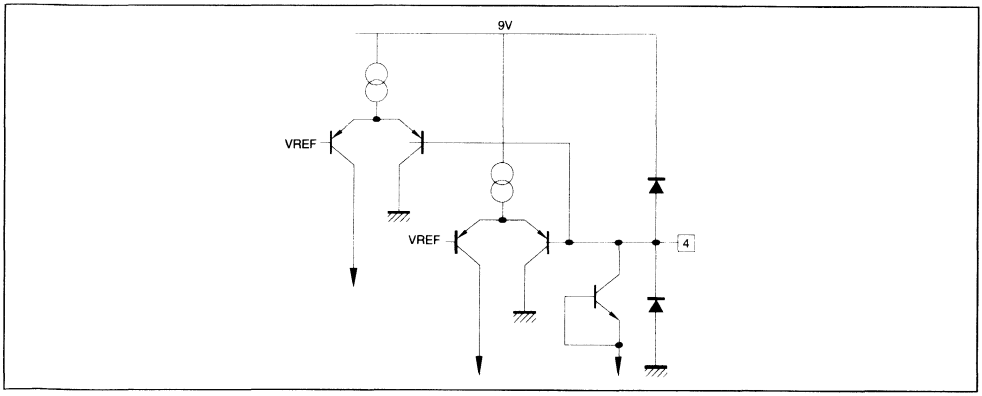


Figure 6 : Pin 4 Configuration



INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 7 : Pin 5 Configuration

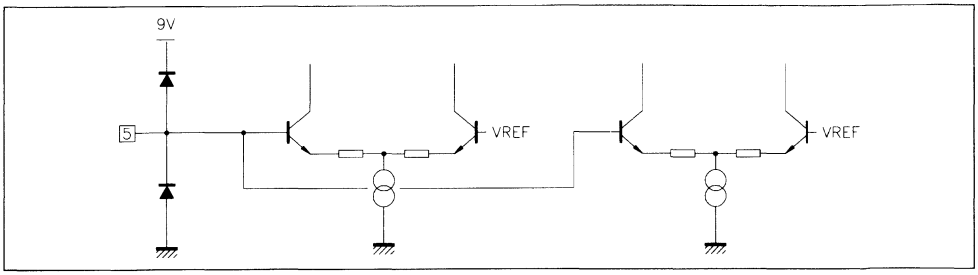


Figure 8 : Pin 6 Configuration

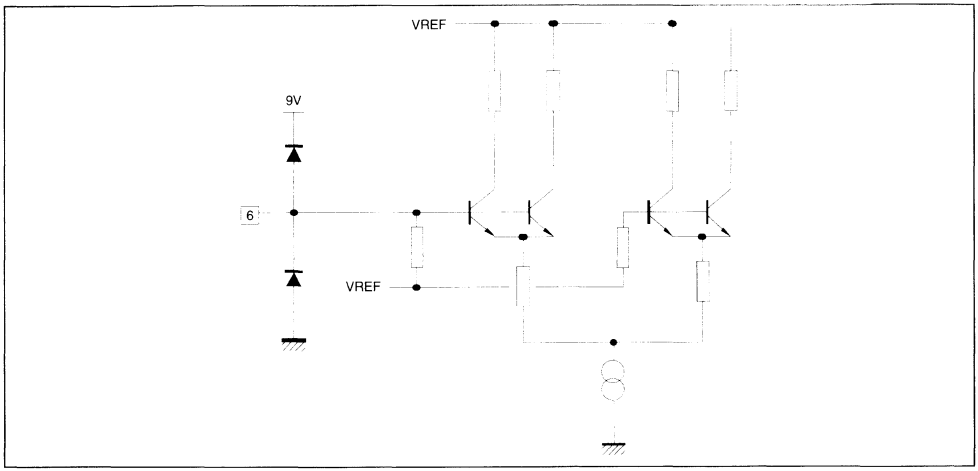


Figure 9 : Pin 8 Configuration

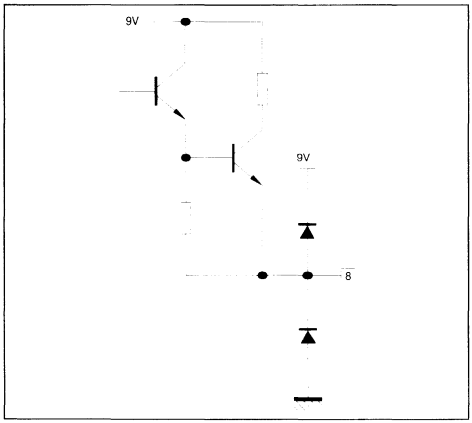
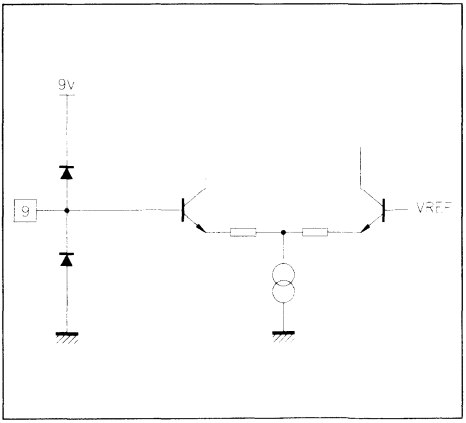


Figure 10 : Pin 9 Configuration



INPUT / OUTPUT PIN CONFIGURATION (continued)

Figure 11 : Pin 10 Configuration

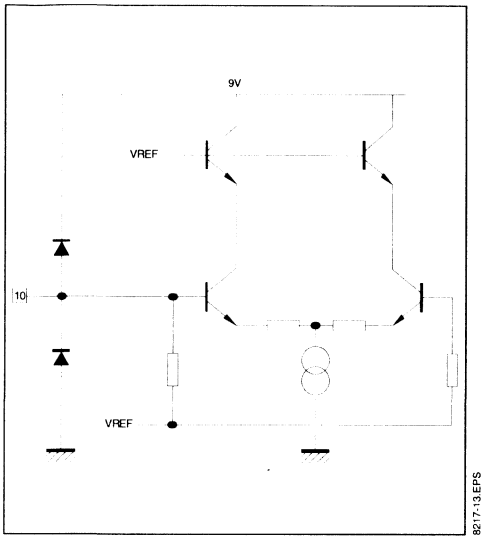


Figure 12 : Pin 12 Configuration

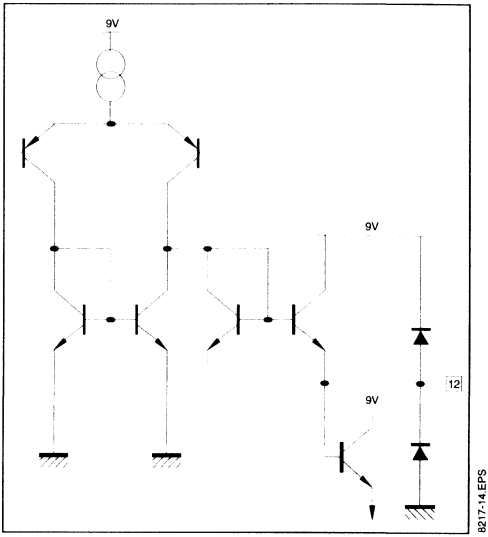


Figure 13 : Pin 13 Configuration

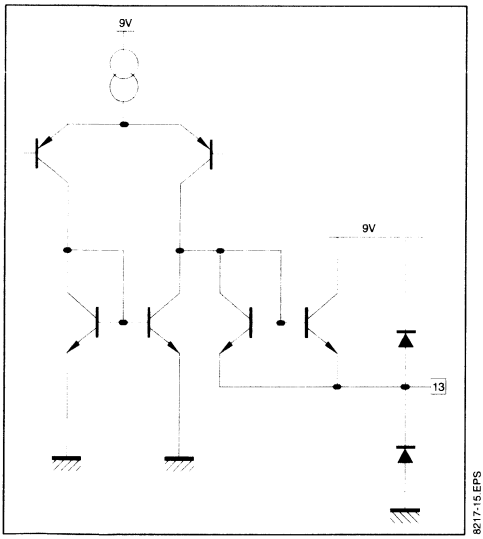


Figure 14 : Pin 14 Configuration

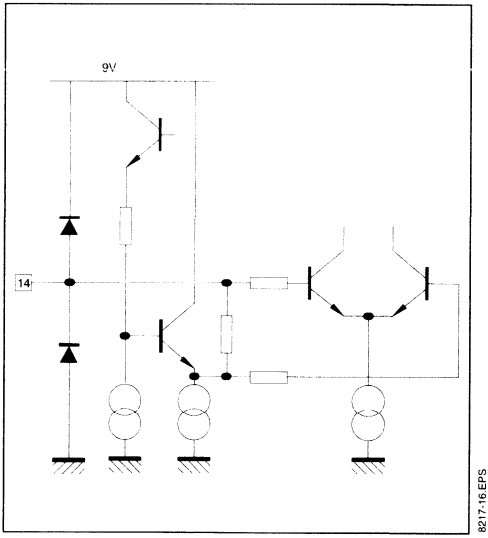


Figure 15 : Pin 16 Configuration

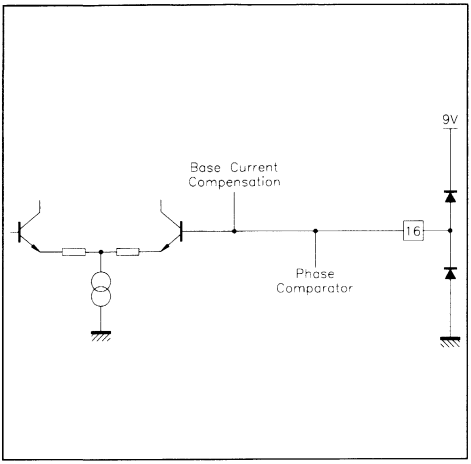
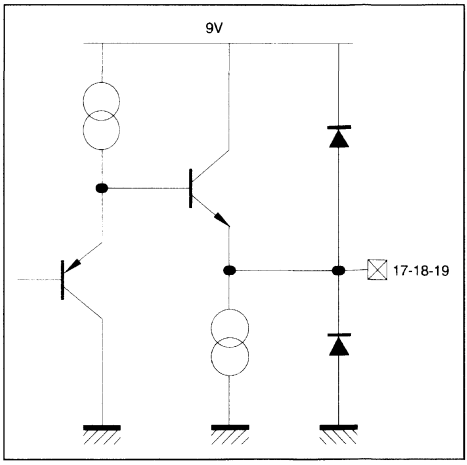
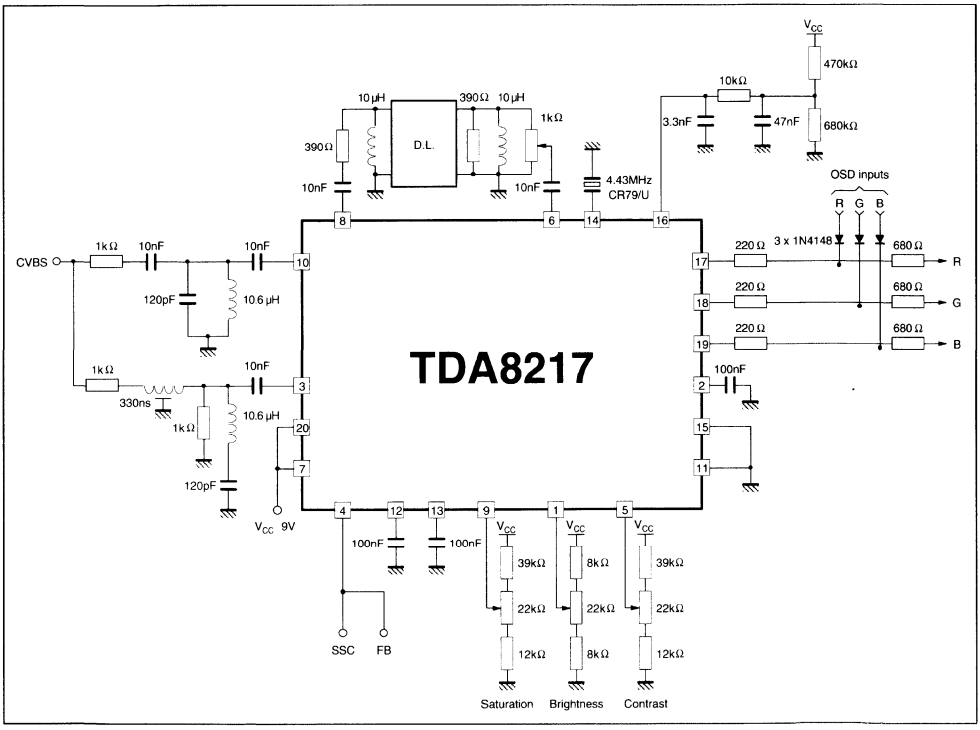


Figure 16 : Pins 17 - 18 - 19 Configuration



APPLICATION DIAGRAM (with OSD capability)



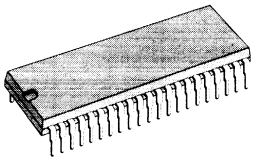
TEA5040S

WIDE BAND VIDEO PROCESSOR

- DIGITAL CONTROL OF BRIGHTNESS, SATURATION AND CONTRAST ON TV SIGNALS AND R, G, B INTERNAL OR EXTERNAL SOURCES
- BUS DRIVE OF SWITCHING FUNCTIONS
- DEMATRIXING OF R, G, B SIGNALS FROM Y, R-Y, B-Y, TV MODE INPUTS
- MATRIXING OF R, G, B SOURCES INTO Y, R-Y, B-Y SIGNALS
- AUTOMATIC DRIVE AND CUT-OFF CONTROLS BY DIGITAL PROCESSING DURING FRAME RETRACE
- PEAK AND AVERAGE BEAM CURRENT LIMITATION
- ON-CHIP SWITCHING FOR R, G, B INPUT SELECTION
- ON-CHIP INSERTION OF INTERNAL OR EXTERNAL R, G, B SOURCES

DESCRIPTION

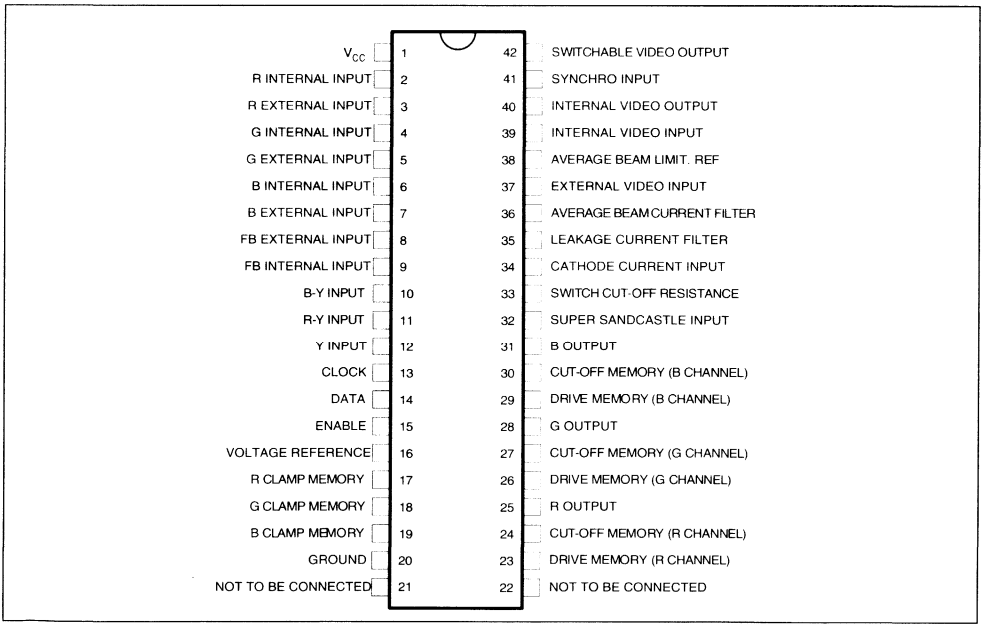
The TEA5040S is a serial bus-controlled videoprocessing device which integrates a complex architecture fulfilling multiple functions.



SDIP42
(Plastic Package)

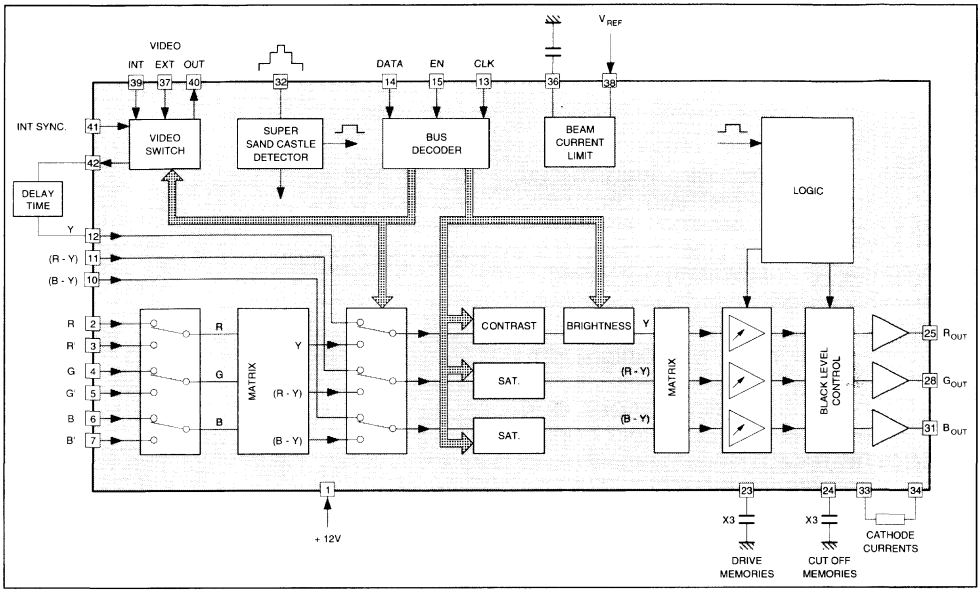
ORDER CODE : TEA5040S

PIN CONNECTIONS



5040S-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

Brief Description

This integrated circuit incorporates the following features :

- a synchro and two video inputs
- a fixed video output
- a switchable video output
- normal Y, R-Y, B-Y TV mode inputs
- double set of R, G, B inputs
- brightness, contrast and saturation controls as well on a R, G, B picture as on a normal TV picture
- digital control inputs by means of serial bus
- peak beam current limitation
- average beam current limitation
- automatic drive and cut-off controls

Block Diagram Description

BUS DECODER

A 3 lines bus (clock, data, enable) delivered by the microcontroller of the TV-set enters the videoprocessor integrated circuit (pins 13-14-15). A control system acts in such a way that only a 9-bit word is taken into account by the videoprocessor. Six of the bits carry the data, the remaining three carry the address of the subsystem.

Function	Address	Number of Bits
Brightness Control	0	5
Contrast Control	1	5
Colour on/off Selection	2	1
Insertion Allowed	3	1
Sync/Async Mode	4	1
Int/Ext Video Switching	5	1
B-Y Saturation Control	6	6
R-Y Saturation Control	7	6

Table below depicts 9-bit words required for various functions.

Subsystem's Configuration		Data Bits LSB....MSB	Add. Bits LSB....MSB
BRIGHTNESS	Min. Max.	X00000 X11111	000
CONTRAST	Min. max.	X00000 X11111	100
COLOUR ON/OFF	Off On	XXXXX0 XXXXX1	010
INSERTION	Allowed Not Allow.	XXXXX0 XXXXX1	110
SYNC/ASYNC MODE	Sync. Async.	XXXX0X XXXX1X	001
VIDEO INT/EXT	Ext. Int.	XXXXX0 XXXXX1	101
SATURATION B-Y	Min. Max.	000000 111111	011
SATURATION R-Y	Min. Max.	000000 1111	111

A demultiplexer directs the data towards latches which drive the appropriate control. More detailed information about serial bus operation is given in the following chapter.

Video Switch

The video switch has three inputs :
- an internal video input (pin 39),
- an external video input (pin 37),
- a synchro input (pin 41),

and two outputs :
- an internal video output (pin 40),
- a switchable video output (pin 42)

The 1Vpp composite video signal applied to the internal video input is multiplied by two and then appears as a 2Vpp low impedance composite video signal at the output. This signal is used to deliver a 1Vpp/75Ω composite video signal to the peri-TV plug.

The switchable video output can be any of the three inputs. When the Int/Ext one active bit word is high (address number 5), the internal video input is selected. If not, either a regenerated synchro pulse or the external video signal is directed towards this output depending on the level of the Sync/Async one active bit word (address number 4). As this output is to be connected to the synchro integrated circuit, RGB information derived from an external source via the Peri-TV plug can be displayed on the screen, the synchronization of the TV-set being then made with an external video signal.

When RGB information is derived from a source integrated in the TV-set, a teletext decoder for example, the synchronization can be made either on the internal video input (in case of synchronous data) or on the synchro input (in case of asynchronous data).

R, G, B Inputs

There are two sets of R, G, B inputs : one is to be connected to the peri-TV plug (Ext R, G, B), the second one to receive the information derived from the TV-set itself (Int R, G, B).

In order to have a saturation control on a picture coming from the R, G, B inputs too, it is necessary to get R-Y, B-Y and Y signals from R, G, B information : this is performed on the first matrix that receives the three 0.9Vp (100% white) R, G, B signals and delivers the corresponding Y, R-Y, B-Y signals. These ones are multiplied by 1.4 in order to make the R-Y and B-Y signals compatible with the R-Y and B-Y TV mode inputs. The desired R, G, B inputs are selected by means of 3 switches controlled by the two fast blanking signal inputs. A high level on FB external pin selects the external RGB sources. The three selected inputs are clamped in order to give the required DC level at the output of this first matrix. The three not selected inputs are clamped on a fixed DC level.

Y, R-Y, B-Y Inputs

The 2Vpp composite video signal appearing at the switchable output of the video switch (pin 42) is driven through the subcarrier trap and the luminance delay line with a 6 dB attenuation to the Y input (1Vpp ; pin 12). In order to make this 1Vpp (synchro to white) Y signal compatible with the 1Vpp (black to white) Y signal delivered by the first matrix, it is necessary to multiply it by a coefficient of 1.4.

R, G, B Insertion Pulse (fast blanking)

A R, G, B source has also to provide an insertion pulse. Since this integrated circuit can be directly

connected to two different sources, it is necessary then to have two separate insertion pulse inputs (pin 8-9). Fast blanking can be inhibited by a one active bit word. The two fast blanking inputs carry out an OR function to insert R, G, B sources into TV picture. The external fast blanking (FB ext.) selects the appropriate R, G, B source.

Controls

The four brightness, contrast and saturation control functions are direct digitally controlled without using digital-to-analog converters.

The contrast control of the Y channel is obtained by means of a digital potentiometer which is an attenuator including several switchable cells directly controlled by a 5 active bit word (address number 1). The brightness control is also made by a digital potentiometer (5 active bit word, address number 0). Since a + 3dB contrast capability is required, the Y signal value could be up to 0.7Vpp nominal. For both functions, the control characteristics are quasi-linear.

In each R-Y and B-Y channel, a six-cell digital attenuator is directly controlled by a 6 active bit word (address number 6 and 7). The tracking needed to keep the saturation constant when changing the contrast has to be done externally by the microcontroller. Furthermore, colour can be disabled by blanking R-Y and B-Y signals using one active bit word (address number 2) to drive the one-chip colour ON/OFF switch.

Second Matrix, Clamp, Peak Clipping, Blanking

The second matrix receives the Y, R-Y and B-Y signals and delivers the corresponding R, G, B signals. As it is required to have the capability of + 6dB saturation, an internal gain of 2 is applied on both R-Y and B-Y signals.

A low clipping level is included in order to ensure a correct blanking during the line and frame retraces. A high clipping level ensures the peak beam current limitation. These limitations are correct only if the DC bias of the three R, G, B signals are precise enough. Therefore a clamp has been added in each channel in order to compensate for the inaccuracy of the matrix.

Sandcastle Detector And Counter

The three level supersandcastle is used in the circuit to deliver the burst pulse (CLP), the horizontal pulse (HP), and the composite vertical and horizontal blanking pulse (BLI). This last one is regenerated in the counter which delivers a new composite pulse (BL) in which the vertical part lasts 23 lines when the vertical part of the supersandcastle lasts more than 11 lines.

The TEA5040S cannot work properly if this minimum duration of 11 lines is not ensured.

The counter delivers different pulses needed circuit and especially the line pulses 17 to 23 used in the automatic drive and cut-off control system.

Automatic Drive And Cut-off Control System

Cut-off and drive adjustments are no longer required with this integrated circuit as it has a sample and hold feedback loop incorporating the final stages of the TV-set. This system works in a sequential mode. For this purpose, special pulses are inserted in G, R and B channels. During the lines 17, 18 and 19, a "drive pulse" is inserted respectively in the green, red and blue channels. The line 20 is blanked on the three channels. During the lines 21, 22 and 23, a "quasi cut-off pulse" is inserted respectively in the green, red and blue guns.

The resulting signal is then applied to the input of a voltage controlled amplifier. In the final stages of the TV-set, the current flowing in each green, red and blue cathode is measured and sent to the videoprocessor by a current source.

The three currents are added together in a resistor matrix which can be programmed to set the ratio between the three currents in order to get the appropriate colour temperature. The output of the matrix forms a high impedance voltage source which is connected to the integrated circuit (pin 34). Same measurement range between drive and cut-off is achieved by internally grounding an external low impedance resistor during lines 17, 18 and 19.

This is due to the fact that the drive currents are about one hundred times higher than the cut-off and leakage currents.

Each voltage appearing sequentially on the wire pin 34 is then a function of specific cathode current :

- When a current due to a drive pulse occurs, the voltage appearing on the pin 34 is compared within the IC with an internal reference, and the result of the comparison charges or discharges an external appropriate drive capacitor which stores the value during the frame. This voltage is applied to a voltage controlled amplifier and the system works in such a way that the pulse current drive derived from the cathode is kept constant.
- During the line 20, the three guns of the picture tube are blanked. The leakage current flowing out of the final stages is transformed into a voltage

which is stored by an external leakage capacitor to be used later as a reference for the cut-off current measurement.
- When a current due to a cut-off pulse occurs, the voltage appearing on the pin 34 is compared within the IC to the voltage present on the leakage memory. An appropriate external capacitor is then charged or discharged in such a way that the difference between each measured current and the leakage current is kept constant, and thus the quasi cut-off current is kept constant.

Average Beam Current Limitation

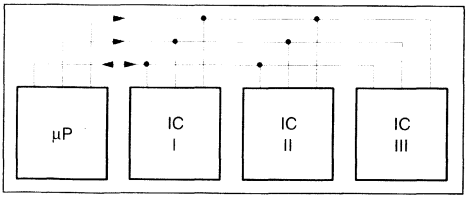
The total current of the three guns is integrated by means of an internal resistor and an external capacitor (pin 36) and then compared with a programmable voltage reference (pin 38). When 70% of the maximum permitted beam current is reached, the drive gain begins to be reduced ; to do so, the amplitude of the inserted pulse is increased.

In order to keep enough contrast, the maximum drive reduction is limited to 6dB. If it is not sufficient, the brightness is suppressed.

SPECIFICATION FOR THE THOMSON BI-DIRECTIONAL DATA BUS

This is a bi-directional 3-wire (ENABLE, CLOCK, DATA) serial bus. The DATA line transmission is bi-directional whereas ENABLE and CLOCK lines are only microprocessor controlled. The ENABLE and CLOCK lines are only driven by the microcomputer.

Figure 1



It is possible to select several IC from the microprocessor via the bus. The identification of each particular IC is achieved by the length of the word (number of data bits/clock pulses), meaning that each IC responds with its own particular word length.

The number is determined while ENABLE is low and by counting the negative clock edges. As soon as the high edge of the ENABLE signal is applied, the number is fixed (see Figure 2).

The reply word lenght from any of the IC on the bi-directional line is four bits. If it is found insufficient then the reply word can be expanded to include two repetitive reply sequences one after the other.

The bi-directional transmission is enabled if :
- the IC has been previously addressed at the positive going edge of the enable pulse.
- ENABLE remains high,
  and DATA is available only during the period when the clock remains low.
- number of identification bits : n
  1...n : data from the microcomputer
- number of bi-directional clocks : 4
  1...M : data to the microcomputer

The four bit reply word (synchronized with the clock coming from the microcontroller) from the addressed IC to the microcontroller is sent only once. Subsequent clock pulses present on the clock line will be ignored by the IC in question. The data sent to the microcontroller can generally be suppressed completely or partially, but in the case of the videoprocessor, a minimum reply word lenght of 1 has to be maintained (see Figure 3).

This implies that a bi-directional bus that incorporates other IC's together with a videoprocessor IC is then also limited by the minimum reply word restriction of 1.

The data word from the microcompter is divided into :
- addresses within the IC
- data

The data word to the microcomputer is divided into
- two data bits,
- two address bits

After the operating voltage is applied, the first transmission will be used as a reset command, i.e. the data word will not be detected.
- number of identification bits : n
  1...n : data from the microcomputer
- number of bi-directional clocks : 1
  1 : data the microcomputer (which is the minimum number for the videoprocessor)

Figure 2

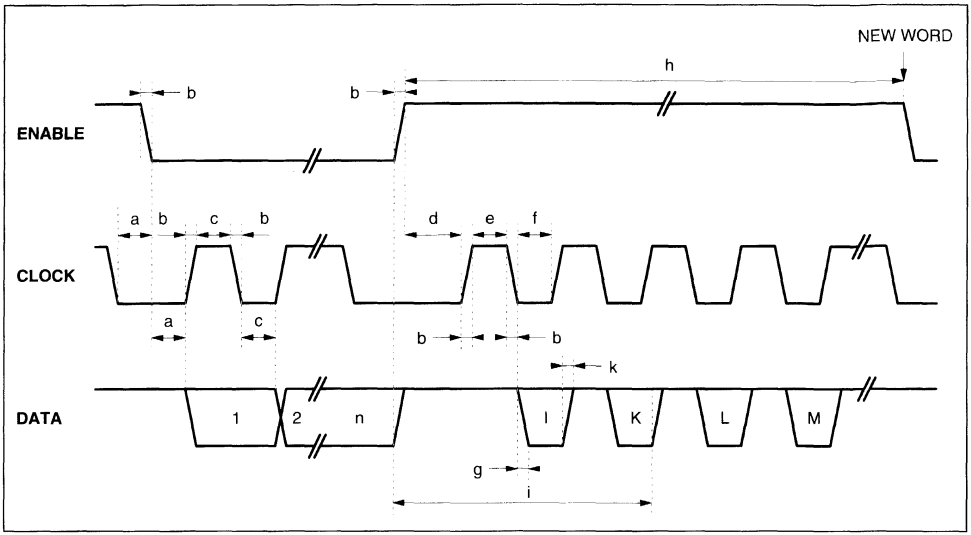
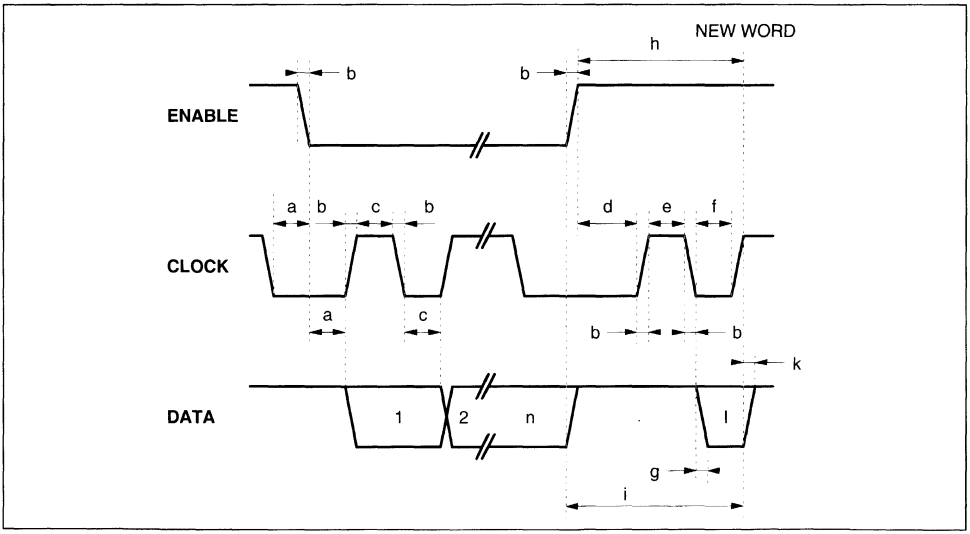


Figure 3



BI-DIRECTIONAL DATA BUS

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING Identification nr-9 (9 video processor address) (see figures 2-3)					
a		5			µs
b		0			µs
c		5			µs
d		70			µs
e	N/A				
f	N/A				
g	N/A				
h	new word to same IC new word to other IC	24 70			ms µs

5040S-01.TBL

ABSOLUTE MAXIMUM RATINGS

T_{AMB} = 25°C (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	14			V
T_{OPER}	Operating Temperature Range	0, + 60			°C
T_{STG}	Storage Temperature Range	– 25, + 125			°C

5040S-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction-ambiant Thermal Resistance	Typ.	60	°C/W

5040S-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{AMB} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	10.8	12	12.5	V
I_{CC}	Supply Current Pin 1		80	104	mA
VIDEO SWITCH					
	External Video Input (75Ω source impedance)				
V_{37}	Signal Amplitude Pin 37		1	1.4	Vpp
I_{37}	Input Current Pin 37		10	30	µA
	Internal Video Input (300Ω source impedance)				
V_{39}	Signal Amplitude Pin 39		1	1.4	Vpp
I_{39}	Input Current Pin 39		10	30	µA
	Synchro Input				
	Output Signal Amplitude Pin 42 (for a 0.5V input signal on pin 41)	0.5	0.6		V
	Internal Video Output Pin 40				
	Dynamic	2.7			Vpp
	DC Level (bottom of synchro pulse)	1		2	V
	Gain between Pin 39 (for 1Vpp on pin 39) and Pin 40	5	6	7	dB
	Crosstalk between Pin 37 and Pin 40)			– 50	dB
	Bandwidth (– 1dB)	6			MHz
	Switchable Video Output Pin 42				
	Dynamic (pin 37 or pin 39 selected)	2.7			Vpp
	Gain between Pins 37 and 42 (for 1VPP on pin 37)	5		7	dB
	Gain between Pins 39 and 42 (for 1VPP on pin 39)	5			dB
	Crosstalk between Pins 37 or 39 with Pin 42			– 50	dB
	Bandwidth (– 1dB)			– 50	MHz

5040S-04.TBL

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TV MODE INPUTS					
	Luminance Input Pin 12				
Y	Signal Amplitude (100% white)		1	1.5	V_{pp}
V_{12}	DC Level (on black level)		4		V
I_{12}	Input Current			10	µA
	R-Y Input Pin 11				
R-Y	Signal Amplitude (75% saturation)		1.05	1.47	V_{pp}
V_{11}	DC Level (on black level)		4.7		V
I_{11}	Input Current			2	µA
	B-Y Input Pin 10				
B-Y	Signal Amplitude (75% saturation)		1.33	1.86	V_{pp}
V_{10}	DC Level (on black level)		4.7		V
I_{10}	Input Current			2	µA
RGB INPUTS PINS 2-3-4-5-6-7					
	Signal Amplitude (100% saturation without synchro pulse)		0.7	1	V_{pp}
	DC Level (on black level)		3.2		V
	Input Current			3	µA
FAST BLANKING INPUTS PINS 8-9					
	TV/RGB Mode Threshold	0.5		0.9	V
	Switching Time		70		ns
	Switching Time Delay		70		ns
CLAMP MEMORY OUTPUT PINS 17-18-19					
	Voltage Range	8	10	11	V
	Input Current			2	µA
REFERENCE PARAMETER					
V_{REF}	Reference Voltage Pin 16		4		V
SANDCASTLE INPUT PIN 32					
	Blanking Threshold	1	1.4	1.8	V
	Burst Gate Threshold	6.4	6.9	7.6	V
	Line Retrace Threshold	3.1	3.4	3.8	V
	Input Current Pin 32 Grounded			100	µA
DRIVE AND CUT-OFF MEMORY OUTPUT PINS 23-24-26-27-29-30					
	Drive Leakage Current Pins 23-26-29			1	µA
	Cut-off Leakage Current Pins 24-27-30			1	µA
	Minimum Active Level Pins 24-27-30		4		V
LEAKAGE CURRENT MEMORY OUTPUT PIN 35					
	Voltage Range	3			V
	Input Current (during picture pin 35 = 5V)			0.5	µA
	Charging Output Impedance			500	Ω
	Minimum Voltage (pin 34 grounded)		3		V
CATHODE CURRENTS INPUT PIN 34					
	Output Current during the Line Trace (pin 34 grounded)			10	µA
	Voltage during Lines 17, 18, 19	0.26	0.35	0.50	V
	Voltage Difference during Lines 21, 22, 23 and during Line 20		0.4		V

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ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
CATHODE CURRENTS INPUT PIN 34 (continued)						
	Voltage Amplitude on Cathode Currents Input for Drive Decrease					
V_{34}	Threshold 10% on Drive/cut-off	1V on Pin 38 2V on Pin 38		0.7 1.4		V V
	Voltage Amplitude on Cathode Currents Input for Brightness					
V_{34}	Decrease Threshold	1V on Pin 38 2V on Pin 38		1 2		V V
IMPEDANCE SWITCH PIN 33)						
	Saturation Impedance [for 5mA] (open during lines 20, 21, 22, 23)			250		Ω
REFERENCE VOLTAGE INPUT FOR THE AVERAGE BEAM CURRENT LIMITER PIN 38						
V_{38}	Reference Voltage		0		5	V
I_{38}	Input Current (V_{38} = 1V)				– 20	V
AVERAGE BEAM CURRENT FILTER PIN 36 VOLTAGE RANGE						
	0 < V34 < 7V		6			V
RGB OUTPUTS R (PIN 25), G (PIN 28), B (PIN 31)						
	Inserted Levels					
	Low Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)			45		%
	High Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)			115		%
	Drive Inserted Level Referred to quasi Cut-off Inserted Level (without beam limitation, V_{38} = 6V, V_{34} grounded)			35		%
	Bandwidth (– 3dB) (TV mode and R, G, B mode)			10		MHz
	Crosstalk for any of the 11 Inputs Pins 2-3-4-5-6-7-10-11-12-37-39 on any of the 5 Outputs Pins 25-28-31-40-42 (range : DC to 1MHz)				– 50	dB
	Brightness					
	Nominal Brightness Referred to quasi Cut-off Inserted Level (bit word "10000" address = 0)			– 25		%
	Total Brightness Range (100 % = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			78		%
	Maximum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			38		%
	Minimum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			– 40		%
	Differential Brightness between any two Channels (TV mode, colour off, pins 10-11-12 AC grounded, 0.5 (W/B) signal on Pin 12, maximum contrast = 100% on RGB outputs)			2		%
	Variation of the Differential Brightness (in the whole saturation control range (including colour off))			0.5		%
	Contrast : Max. Contrast Attenuation		11			dB
	Saturation					
	Max. Saturation			6		dB
	Max. Saturation Attenuation		20			dB
	Colour off Attenuation		40			dB

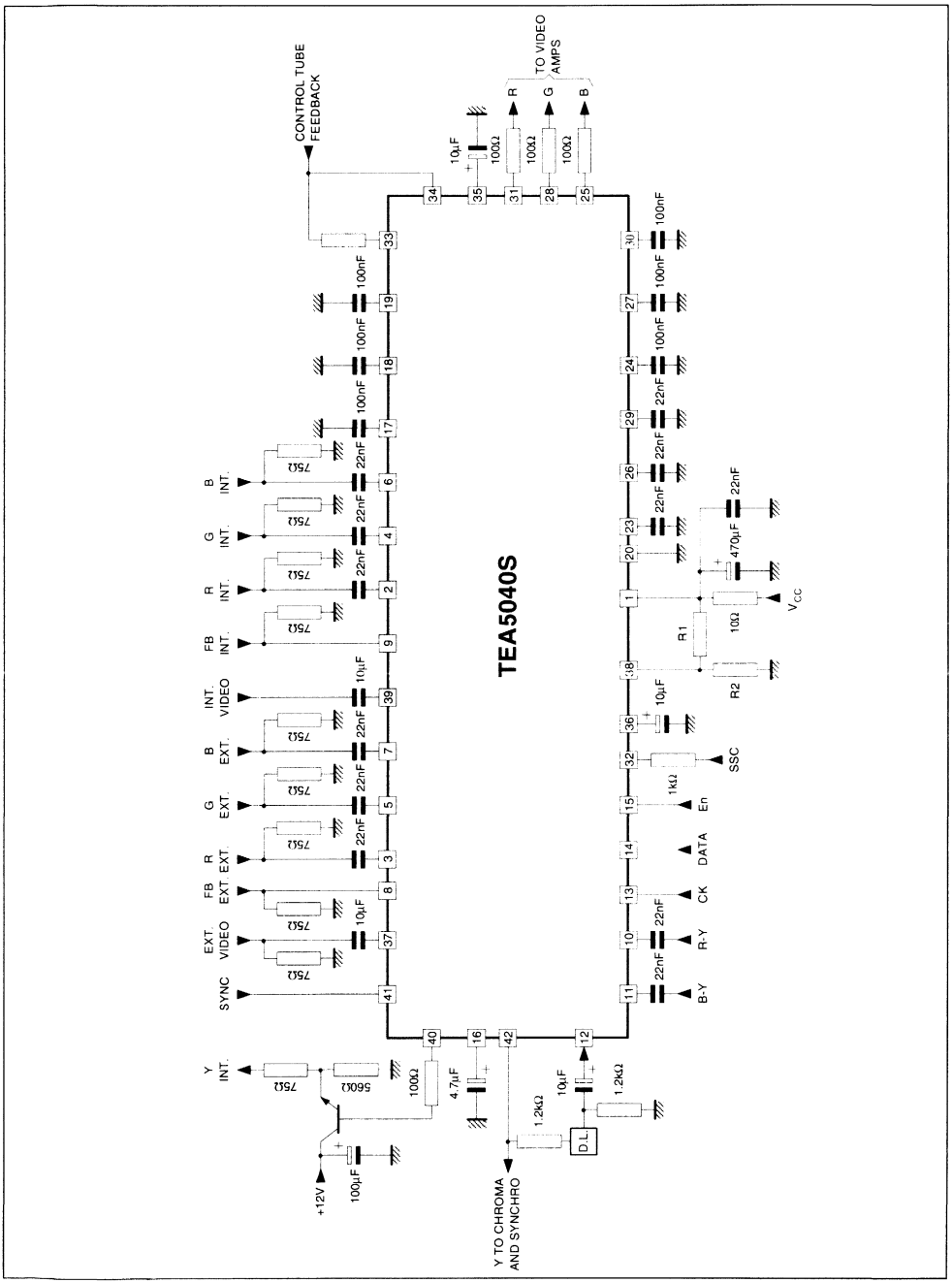
5040S-06.TBL

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
RGB OUTPUTS R (PIN 25), G (PIN 28), B (PIN 31) (continued)					
	Output Signal Amplitude Pins 25-28-31 (blanking to high clipping) • Y input : 0.7V B/W • 0dB Contrast, Bit Word = 010110, Address = 1 • Maximum Brightness • Maximum Drive Efficiency (Pins 23-26-29 grounded) • No Average Beam Current Limitation (Pin 38 to 6V)		6.2		V
	Black to White Output Voltage Y Input : 0.5V (B/W) Maximum Contrast (Pin 38 to 6V, Pins 23-26-29 grounded)		3.6		V
	Drive Efficiency Ratio : $\frac{V_{OUT} \text{ (Pins 23–26–29 grounded)}}{V_{OUT} \text{ (Pins 23–26–29 to } V_{CC})}$ (no average beam current limitation Pin 38 to 6V)		3.6		
	Black Level Control (variable DC voltage from 4V to V_{CC} on Pins 24-27-30)	4.3			V
BUS INPUTS PINS 13-14-15					
V_{HL}	High Level	3.5			V
V_{LL}	Low Level			1	V

5040S-07.TBL

APPLICATION CIRCUIT



SGS-THOMSON MICROELECTRONICS

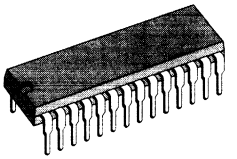
TEA5640E

MULTISTANDARD COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL AND NTSC OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

DESCRIPTION

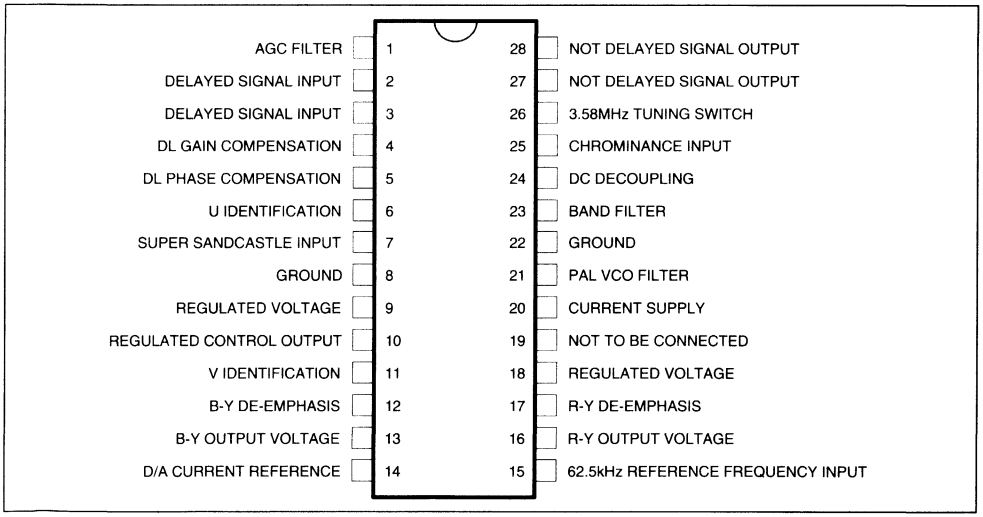
The TEA5640E is a multistandard TV decoder for PAL-SECAM NTSC1 (3.58MHz) and NTSC2 (4.43MHz). The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are four numerical frequency locked loops that allow the elimination of PAL and NTSC crystals. The circuit uses an external reference frequency of 62.5kHz generally provided by the frequency synthesis tuner of the TV set.



DIP28
(Plastic Package)

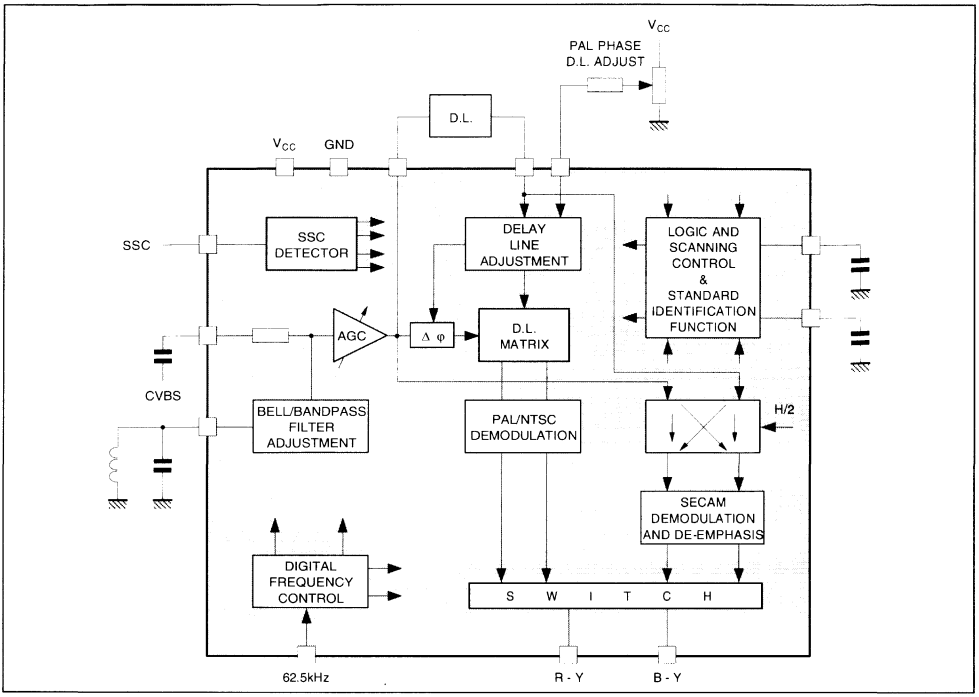
ORDER CODE : TEA5640E

PIN CONNECTIONS



5640E-01.EPS

BLOCK DIAGRAM (simplified)



FEATURES

- Full automatic multistandard switching :
  The circuit includes a scanning control system that provides all the switchings required for the automatic standard recognition. This system is synchronized by the frame pulse.
- No crystal requirement :
  The PAL and NTSC frequencies are synthesized originally by the external reference frequency of 62.5kHz and data stored in the ROM.
- Automatic gain adjustment of the bell filter :
  By switching an internal capacitor network included in a digital loop.
- Automatic gain adjustment of the delay line compensations :
  This adjustment is made on the burst and is refreshed every line retrace
- Automatic adjustment for PAL and NTSC oscillator :
  This oscillator has a digital and an analogic loop. the PAL and NTSC frequencies are memorized in a ROM connected to the digital loop. The digital loop gives the right frequency and the analogic one holds the phase.
- Automatic adjustment of F0R and F0B in SECAM :
  These frequencies are programmed in the ROM and are sent to two other digital loops when SECAM standard is selected.
- Automatic difference phase error compensation in PAL mode.
  The PAL VCO is locked on the burst and during the line, on the blue picture content (0° axis color vector).

STANDARD SWITCHING AND INHIBITION

NTSC inhibition
NTSC 1 and 2 standards can be inhibited by connecting pin 6 to the ground.

3.58 MHz filter switching :
Pin 26 can be used to switch external filters when NTSC 1 is selected (For example luma filter).

SECAM recognition :

- When SECAM on, Pin 12 and Pin 17 DC voltages are lower than 5V.
- For other standards, Pin 12 and Pin 17 DC voltages are regulated V_{CC} (typical 8V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0, +70	°C
T_{stg}	Storage Temperature		– 40, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

5640E-02.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12V ; With Normalized Color Bar Pattern Input Signal (75%)
Subcarrier Level : 320mV_{PP}
Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
SUPPLIES						
V_{REG}	Regulated Voltage I_{10} = 4mA	Pins 9-18	7.5	8	8.5	V
I_{CC}	Supply Current	Pin 9 + Pin 18		90	120	mA
I_9	Supply Current	Pin 9			90	mA
I_{18}	Supply Current	Pin 18			27	mA
V_{I2L}	DC Voltage at I_{20} = 15mA	Pin 20		0.8		V
I_{10}	Input Current	Pin 10	2	4	5	mA
	Transfer Characteristic (I_{10} = 4.0mA)			250		mA/V
CURRENT REFERENCE (Pin 14)						
V_{14}	DC Voltage (I_{14} = 0.77mA)		1.2	1.4	1.6	V
INTERNAL BIAS (Pin 24)						
V_{24}	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2mA)			90	110	Ω
REFERENCE CLOCK INPUT (f = 62.5kHz ± 6Hz, Pin 15)						
I_{15L}	Low Level Input Current (V_{15} = 2.1V)		– 20	– 10	– 5	µA
I_{15H}	High Level Input Current (V_{15} = 3.2V)			5	10	µA
V_{15L}	Low Level Input Voltage	R_{Source} = 68kΩ			1	V
V_{15H}	High Level Input Voltage	R_{Source} = 68kΩ	4			V
	Voltage Threshold			2.8		V
SUPER SANDCASTLE DETECTOR (Pin 7)						
V_B	Blanking Threshold		0.5	0.75	0.9	V
V_L	Line Threshold		1.6	1.8	1.9	V
V_6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I_7	Input Current (V_7 = 1.75V)		– 20		0	µA
	Max Input Voltage Pin 7				6.0	V
CHROMINACE INPUT (Pin 25)						
V_{25}	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	V_{PP}
	Impedance		0.8	1		kΩ

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ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
AUTOMATIC GAIN CONTROL						
	SECAM MODE					
	0dB Reference Voltage for Measurement on Pins 27-28 (chroma input voltage V_{25} = 320mV$_{PP}$)		50	150	250	mV$_{PP}$
	AC Voltage Variation on Pins 27-28	V_{25} = + 6dB V_{25} = − 24dB	− 3 − 5		+ 3 + 2	dB dB
	PAL/NTSC MODE WITH IDENTIFICATION					
	0dB Reference Voltage for Measurement on Pins 13-16 (chroma input voltage V_{25} = 320mV$_{PP}$)					
	AC Voltage Variation on Pins 13-16	V_{25} = + 6dB V_{25} = − 24dB	− 3 − 5		+ 3 + 2	dB dB
DEMODULATOR PART						
	GENERALITIES					
V_{13}	B-Y Output DC Voltage	Pin 13	2.7	3.3	4	V
V_{16}	R-Y Output DC Voltage	Pin 16	3.0	3.5	4.2	V
	Maximum Sink Current	Pins 13-16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50µA)			250		Ω
	R-Y Output AC Impedance (± 50µA)			250		Ω
	Blanking Level Offset (% of the pp output signal)				± 2	%
SECAM MODE						
V_{BYS}	B-Y AC Voltage		1.0	1.34	1.6	V$_{PP}$
V_{RYS}	R-Y AC Voltage		0.8	1.05	1.3	V$_{PP}$
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mV$_{PP}$
	Max overshoot on output SECAM signals (see test conditions Note 2)				5	%
	SECAM Rise Time (see test conditions Note 1)				800	ns
PAL MODE						
V_{BYP}	B-Y AC Voltage		1.0	1.34	1.6	V$_{PP}$
V_{RYP}	R-Y AC Voltage		0.8	1.05	1.3	V$_{PP}$
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mV$_{PP}$
PAL/SECAM OUTPUT BALANCE						
RYPS	R-Y Output				± 2	dB
BYPS	B-Y Output				± 2	dB
NTSC 4.43						
V_{BYN2}	B-Y AC Voltage		1.0	1.34	1.6	V$_{PP}$
V_{RYN2}	R-Y AC Voltage		0.8	1.05	1.3	V$_{PP}$
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			50		mV$_{PP}$

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Notes :

1. **Rise Time Test Conditions**
   - SECAM Color Bar Patterns 75%
   - Generator TEKTRONIX 143
   - Standard Application without any output load
   - Measure between 10% and 90% on the major transition (Green Violet)
2. **Overshoot Test Conditions**
   - Idem than for Rise Time
   - Ratio between the value of the overshoot and the peak-to-peak value of the transition after overshoot (on the flat level)

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
NTSC 3.58					
V_{BYN1}	B-Y AC Voltage	1.0		1.6	V_{PP}
V_{RYN1}	R-Y AC Voltage	0.8		1.3	V_{PP}
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		50		mV_{PP}
DE-EMPHASIS (Pins 12-17)					
	DC Voltage SECAM Mode (blanking level)		3.5	4.0	V
	Impedance SECAM Mode		11		kΩ
	DC Voltage PAL NTSC Mode		V_{REG}		V
	Impedance PAL Mode		70		kΩ
REFERENCE OSCILLATOR PLL					
	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz
BAND FILTER (Pin 23)					
	Impedance SECAM Mode	3.7	4.7	5.7	kΩ
	Impedance PAL/NTSC Mode	0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)		20		pF
	Maximum Switchable Internal Capacitance (all standards)		50		pF
ΔF	Internal Oscillator Frequency Range for (L = 10μH, C = 68pF)	590			kHz
	requency Offset, After Automatic Adjustement			± 10	kHz
UNDELAYED SIGNAL OUTPUTS (Pins 27-28)					
V_{27}, V_{28}	DC Voltage		1.6		V
I_{27}, I_{28}	Sink Current	1			mA
	Impedance		30		Ω
IDENTIFICATION					
	BURST ATTENUATION RANGE / NOMINAL LEVEL				
	SECAM Mode (line identification) PAL Mode NTSC Modes	30 30 20			dB dB dB
	SECAM MODE				
V_{26}	Pin 26 Voltage (unloaded)	6.9	7.8	8.5	V
V_{26}	Pin 26 Impedance	5	13	25	kΩ
	PAL AND NTSC 4.43 MODES				
V_{26}	Pin 26 Voltage (unloaded)	3.6	4.2	4.9	V
V_{26}	Pin 26 Impedance	2	6	15	kΩ
	NTSC 3.58 MODE				
V_{26}	Pin 26 Voltage (unloaded)		0.0	0.3	V
V_{26}	Pin 26 Impedance		0.1	1	kΩ
TINT CONTROL (NTSC Modes)					
	Range of Phase Change for $V_{Pin\ 5}$ Changing from 2 to 4.5V		± 40		degree
V_5	DC Voltage for 0 Degree TINT Change Pin 5		3.5		V
I_5	Input Current Pin 5	0.08		0.2	mA
NTSC DETECTION					
	Detection Threshold Pin 6	3	3.5	4	V
	NTSC Mode Inhibition Threshold	0.5		2.5	V
	Leakage Current			0.5	μA

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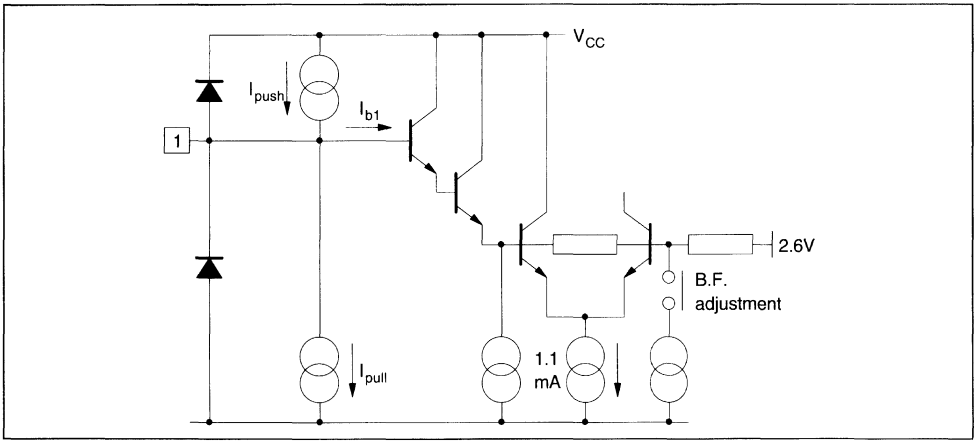
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DELAYED SIGNAL INPUT (Pins 2-3)					
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
DELAY LINE ATTENUATION COMPENSATION					
	Range of Automatic Attenuation Compensation	– 3	– 9	– 15	dB
DELAY LINE PHASE SHIFT COMPENSATION					
	Range of Phase Shift Compensation with a 100kΩ Potentiometer (see application diagram)	± 30			degree
ALTERNATION LINE DETECTION PAL OR SECAM (Pin 11)					
V_{TH-H}	High Differential Threshold ($V_{TH-H} = V_{11H} - V_{24}$)	200		350	mV
V_{TH-L}	Low Differential Threshold ($V_{TH-L} = V_{11L} - V_{24}$)	– 350		– 200	mV
	Leakage Current Threshold ($V_{11} = V_{24} + 1V$)			0.5	µA

5640E-06.TBL

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

Pin 1



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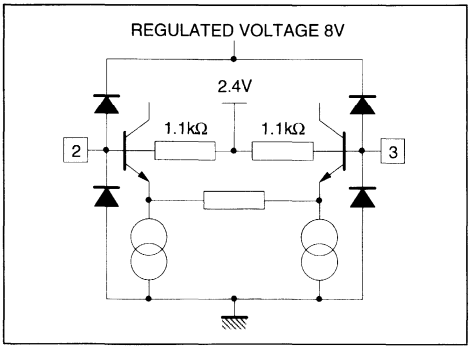
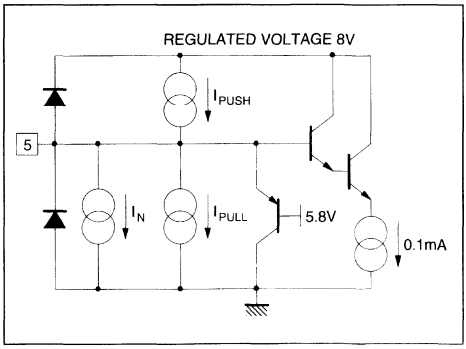
Pins 2-3



5640E-04.EPS

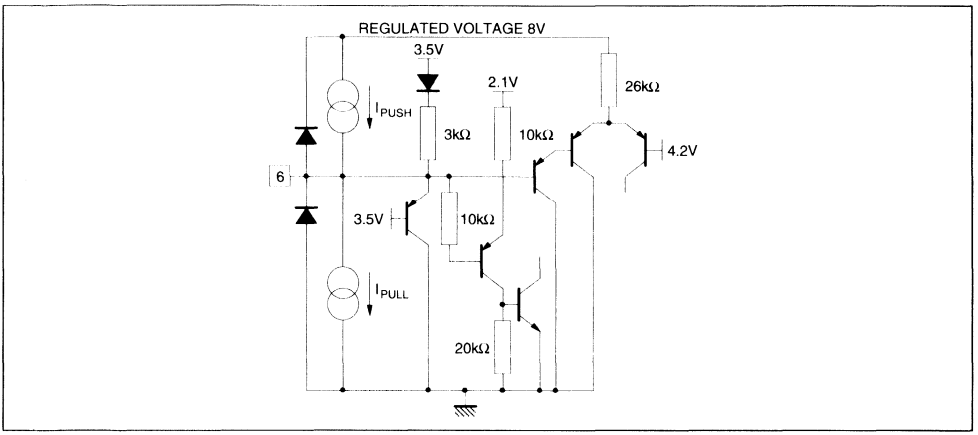
Pin 5



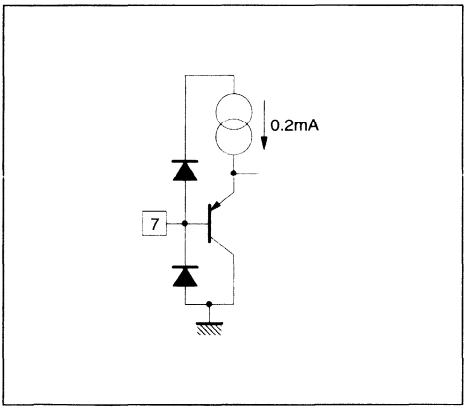
5640E-05.EPS

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

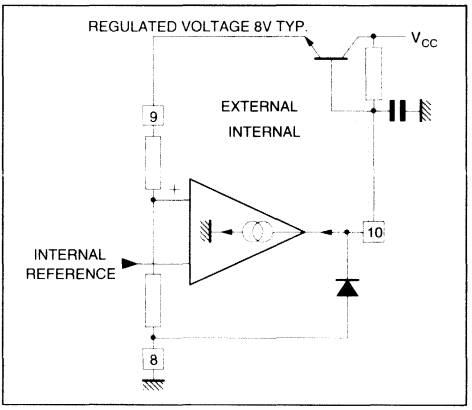
Pin 6



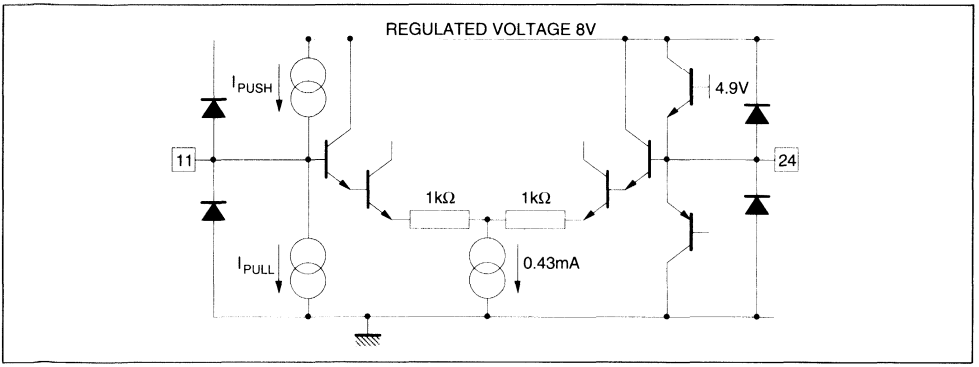
Pin 7



Pins 8-9-10

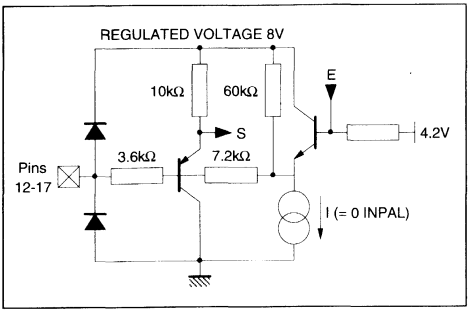


Pins 11-24

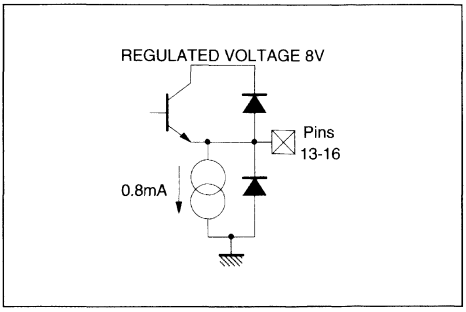


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

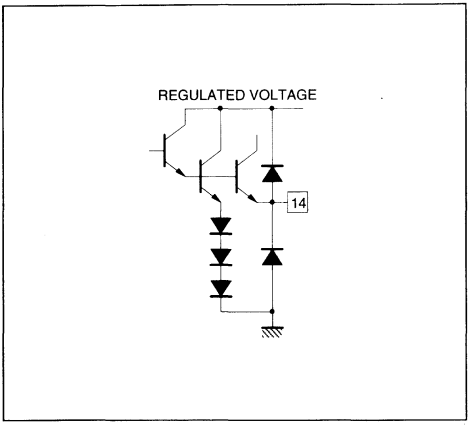
Pins 12-17



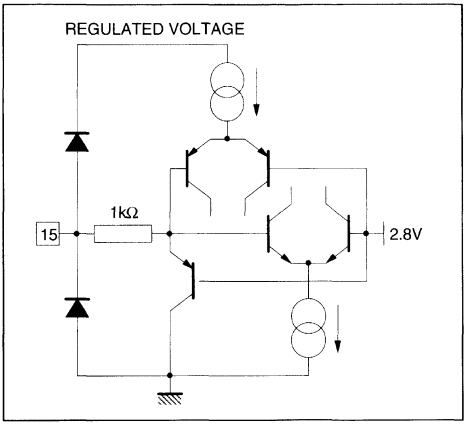
Pins 13 - 16



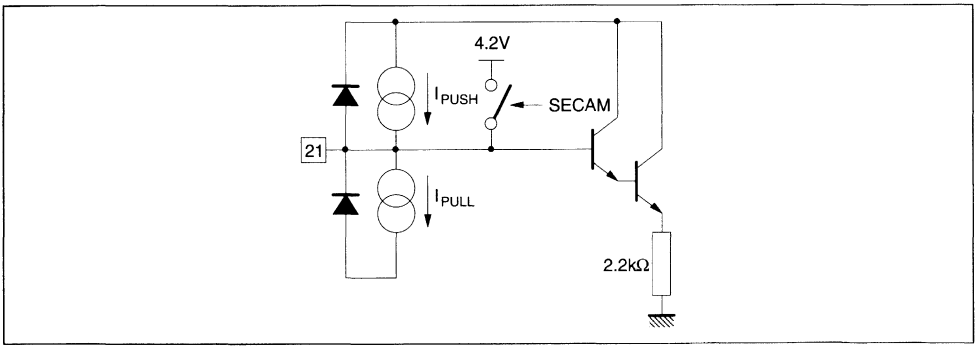
Pin 14



Pin 15

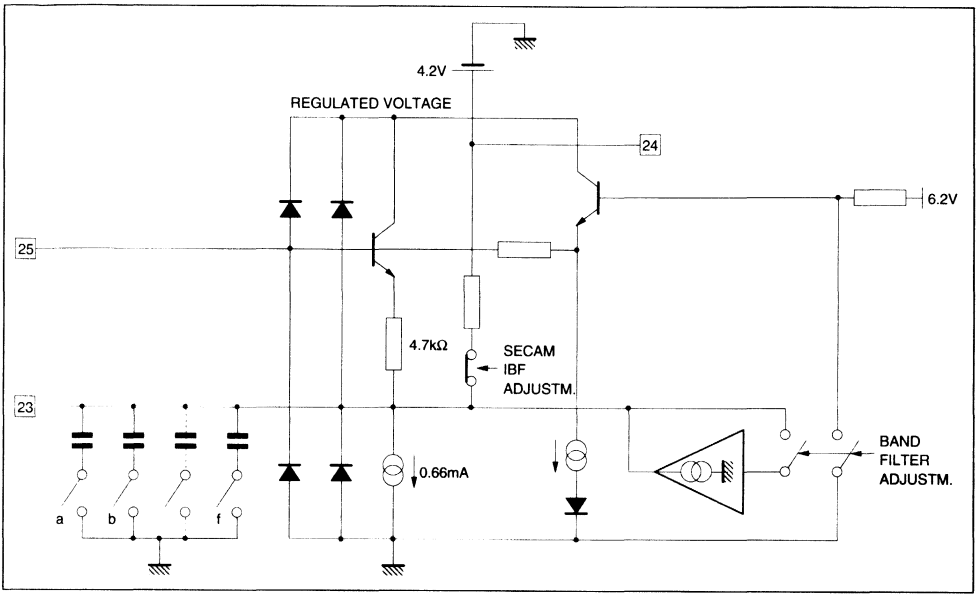


Pin 21

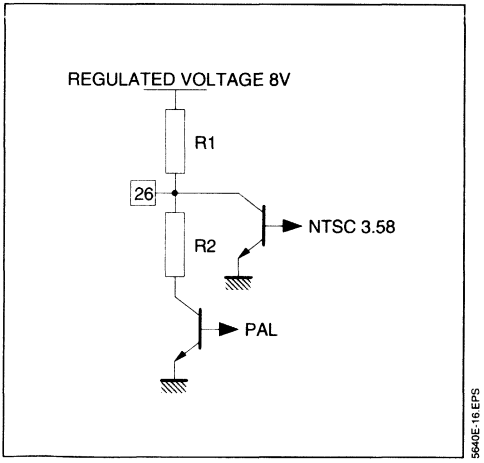


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

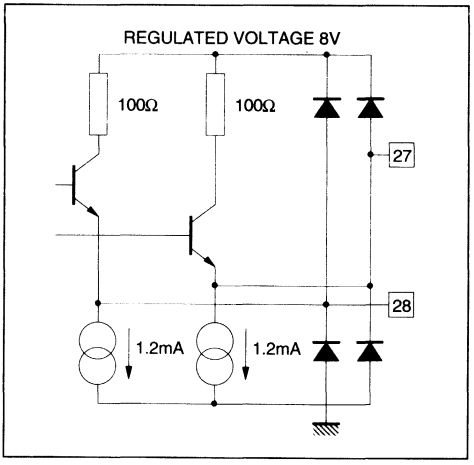
Pins 23-24-25



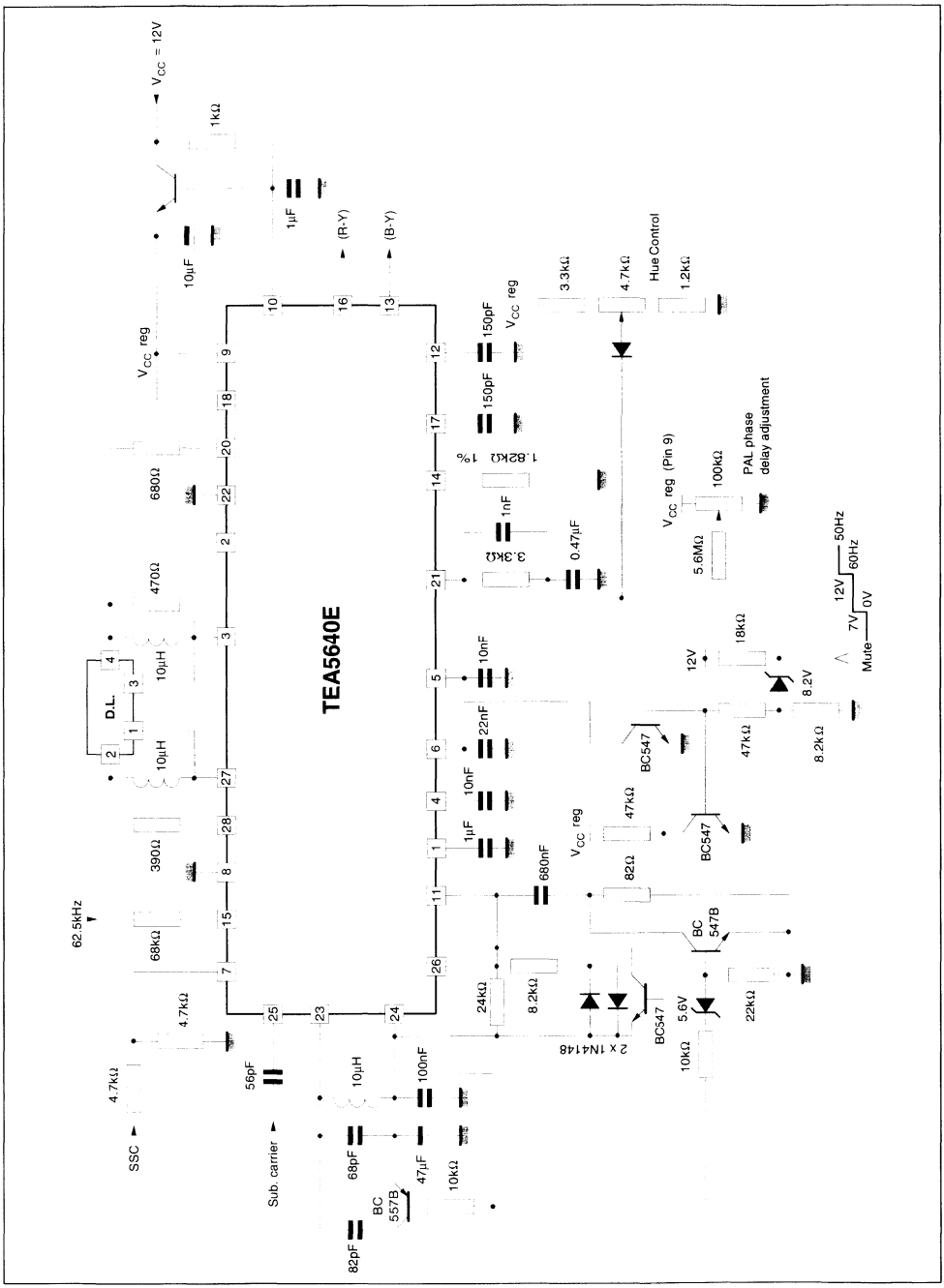
Pin 26



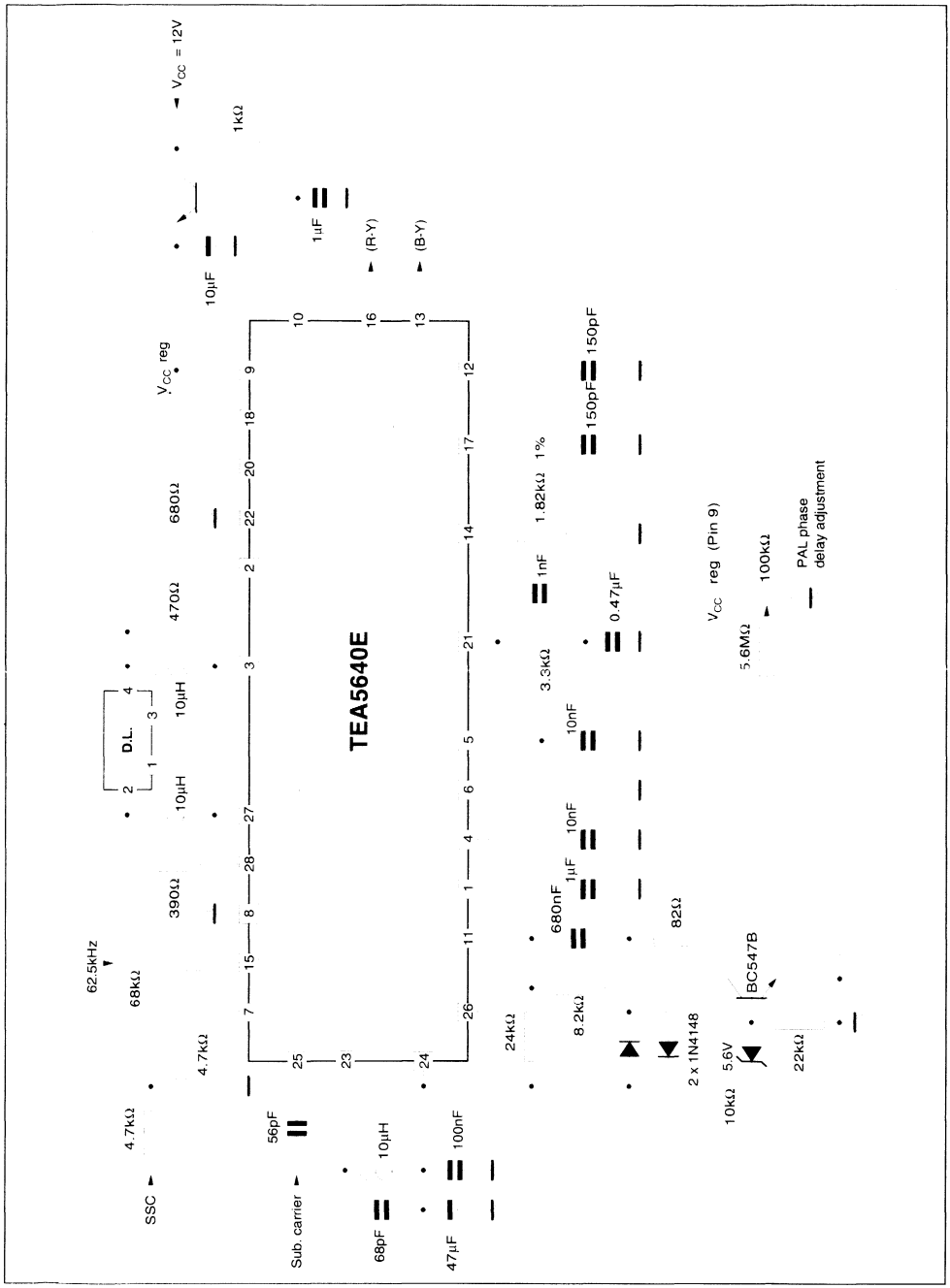
Pins 27 - 28



TYPICAL APPLICATION FOR PAL/SECAM/NTSC1/NTSC2



TYPICAL APPLICATION FOR PAL/SECAM

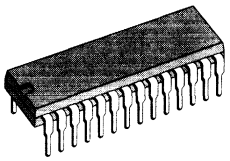


PAL/SECAM COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

DESCRIPTION

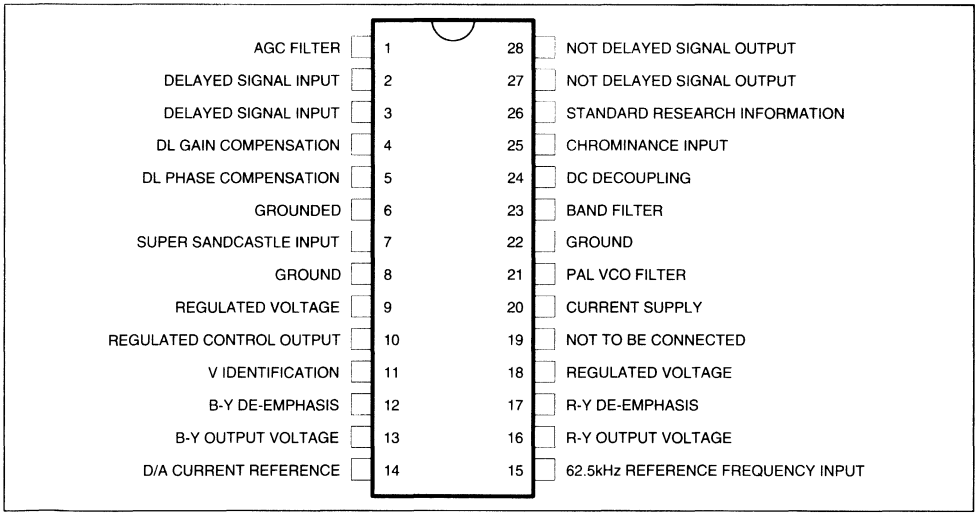
The TEA5640F is a multistandard TV decoder for PAL-SECAM. The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are four numerical frequency locked loops that allow the elimination of PAL crystals. The circuit uses an external reference frequency of 62.5kHz generally provided by the frequency synthesis tuner of the TV set.



DIP28
(Plastic Package)

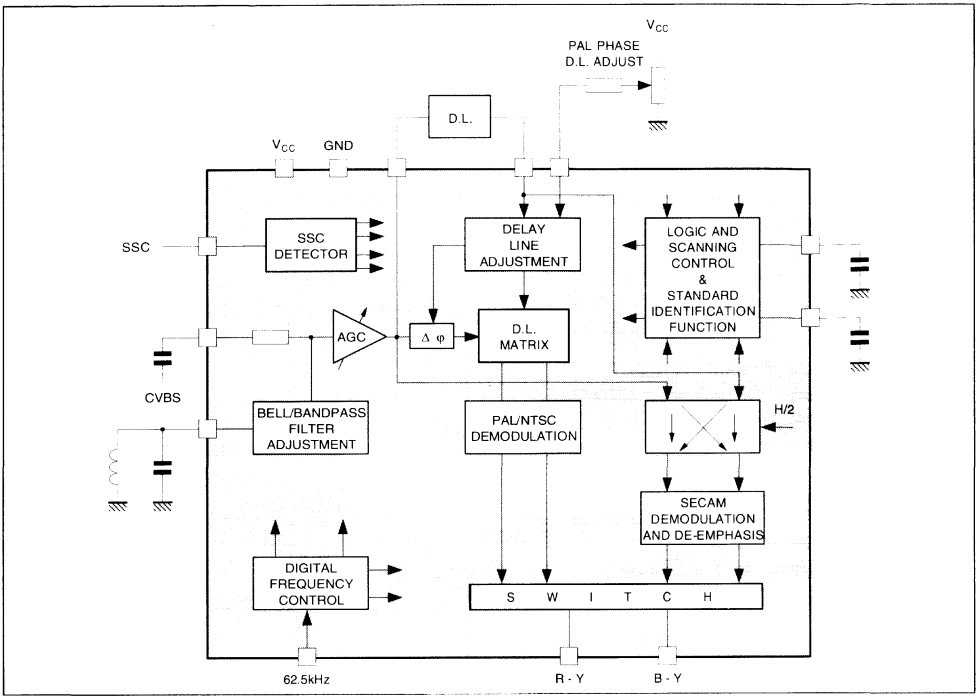
ORDER CODE : TEA5640F

PIN CONNECTIONS



5640F-01.EPS

BLOCK DIAGRAM (simplified)



FEATURES

- Full automatic multistandard switching :
  The circuit includes a scanning control system that provides all the switchings required for the automatic standard recognition. This system is synchronized by the frame pulse.
- No crystal requirement :
  The PAL frequencies are synthesized originally by the external reference frequency of 62.5kHz and data stored in the ROM.
- Automatic gain adjustment of the bell filter :
  By switching an internal capacitor network included in a digital loop.
- Automatic gain adjustment of the delay line compensations :
  This adjustment is made on the burst and is refreshed every line retrace
- Automatic adjustment for PAL oscillator :
  This oscillator has a digital and an analogic loop. the PAL frequencies are memorized in a ROM connected to the digital loop. The digital loop gives the right frequency and the analogic one holds the phase.
- Automatic adjustment of F0R and F0B in SECAM :
  These frequencies are programmed in the ROM and are sent to two other digital loops when SECAM standard is selected.
- Automatic difference phase error compensation in PAL mode.
  The PAL VCO is locked on the burst and during the line, on the blue picture content (0° axis color vector).

STANDARD SWITCHING AND INHIBITION

SECAM recognition :

- When SECAM on, Pin 12 and Pin 17 DC voltages are lower than 5V.
- For other standards, Pin 12 and Pin 17 DC voltages are regulated V_{CC} (typical 8V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0, +70	°C
T_{stg}	Storage Temperature		- 40, +150	°C

5640F-01 TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

5640F-02 TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12V ; With Normalized Color Bar Pattern Input Signal (75%)
Subcarrier Level : 320mV_{PP}
Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
SUPPLIES						
V_{REG}	Regulated Voltage I_{10} = 4mA	Pins 9-18	7.5	8	8.5	V
I_{CC}	Supply Current	Pin 9 + Pin 18		90	120	mA
I_9	Supply Current	Pin 9			90	mA
I_{18}	Supply Current	Pin 18			27	mA
V_{I2L}	DC Voltage at I_{20} = 15mA	Pin 20		0.8		V
I_{10}	Input Current	Pin 10	2		5	mA
	Transfer Characteristic (I_{10} = 4.0mA)			250		mA/V
CURRENT REFERENCE (Pin 14)						
V_{14}	DC Voltage (I_{14} = 0.77mA)		1.2	1.4	1.6	V
INTERNAL BIAS (Pin 24)						
V_{24}	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2mA)			90	110	Ω
REFERENCE CLOCK INPUT (f = 62.5kHz ± 6Hz, Pin 15)						
I_{15L}	Low Level Input Current (V_{15} = 2.1V)		- 20	- 10	- 5	µA
I_{15H}	High Level Input Current (V_{15} = 3.2V)			5	10	µA
V_{15L}	Low Level Input Voltage	R_{Source} = 68kΩ			1	V
V_{15H}	High Level Input Voltage	R_{Source} = 68kΩ	4			V
	Voltage Threshold			2.8		V
SUPER SANDCASTLE DETECTOR (Pin 7)						
V_B	Blanking Threshold		0.5	0.75	0.9	V
V_L	Line Threshold		1.6	1.8	1.9	V
V_6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I_7	Input Current (V_7 = 1.75V)		- 20		0	µA
	Max Input Voltage Pin 7				6.0	V
CHROMINACE INPUT (Pin 25)						
V_{25}	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	V_{PP}
	Impedance		0.8	1		kΩ

5640F-03 TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
AUTOMATIC GAIN CONTROL						
	SECAM MODE					
	0dB Reference Voltage for Measurement on Pins 27-28 (chroma input voltage V_{25} = 320mV$_{PP}$)		50	150	250	mV$_{PP}$
	AC Voltage Variation on Pins 27-28	V_{25} = + 6dB V_{25} = – 24dB	– 3 – 5		+ 3 + 2	dB dB
	PAL/NTSC MODE WITH IDENTIFICATION					
	0dB Reference Voltage for Measurement on Pins 13-16 (chroma input voltage V_{25} = 320mV$_{PP}$)					
	AC Voltage Variation on Pins 13-16	V_{25} = + 6dB V_{25} = – 24dB	– 3 – 5		+ 3 + 2	dB dB
DEMODULATOR PART						
	GENERALITIES					
V_{13}	B-Y Output DC Voltage	Pin 13	2.7	3.3	4	V
V_{16}	R-Y Output DC Voltage	Pin 16	3	3.5	4.2	V
	Maximum Sink Current	Pins 13-16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50µA)			250		Ω
	R-Y Output AC Impedance (± 50µA)			250		Ω
	Blanking Level Offset (% of the pp output signal)				± 2	%
SECAM MODE						
V_{BYS}	B-Y AC Voltage		1.0	1.34	1.6	V$_{PP}$
V_{RYS}	R-Y AC Voltage		0.8	1.05	1.3	V$_{PP}$
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mV$_{PP}$
	Max overshoot on output SECAM signals (see test conditions Note 2)				5	%
	SECAM Rise Time (see test conditions Note 1)				800	ns
PAL MODE						
V_{BYP}	B-Y AC Voltage		1.0	1.34	1.6	V$_{PP}$
V_{RYP}	R-Y AC Voltage		0.8	1.05	1.3	V$_{PP}$
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mV$_{PP}$
PAL/SECAM OUTPUT BALANCE						
RYPS	R-Y Output				± 2	dB
BYPS	B-Y Output				± 2	dB
DE-EMPHASIS (Pins 12-17)						
	DC Voltage SECAM Mode (blanking level)			3.5	4.0	V
	Impedance SECAM Mode			11		kΩ
	DC Voltage PAL Mode			V_{REG}		V
	Impedance PAL Mode			70		kΩ

5640F-04.TBL

Notes :

1. **Rise Time Test Conditions**
   - SECAM Color Bar Patterns 75%
   - Generator TEKTRONIX 143
   - Standard Application without any output load
   - Measure between 10% and 90% on the major transition (Green Violet)
2. **Overshoot Test Conditions**
   - Idem than for Rise Time
   - Ratio between the value of the overshoot and the peak-to-peak value of the transition after overshoot (on the flat level)

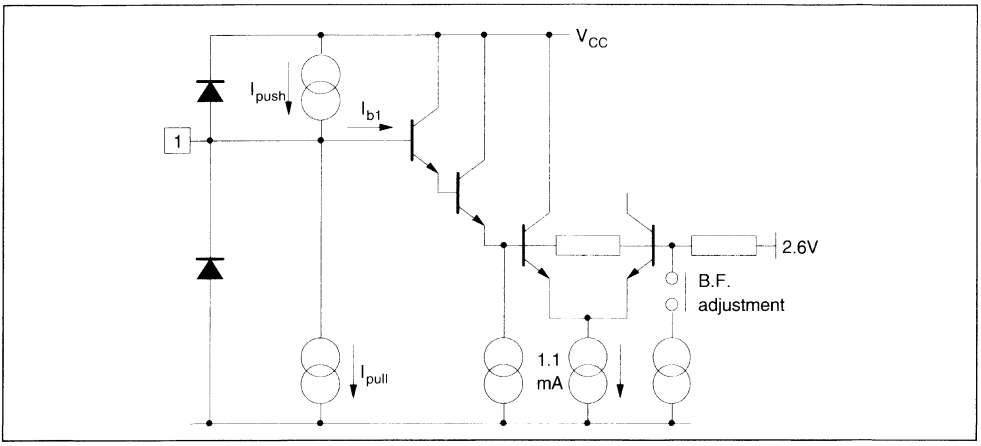
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
REFERENCE OSCILLATOR PLL					
	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz
BAND FILTER (Pin 23)					
	Impedance SECAM Mode	3.7	4.7	5.7	
	Impedance PAL Mode	0.85	1.1	1.35	
	Minimum Switchable Internal Capacitance (all standards)		20		
	Maximum Switchable Internal Capacitance (all standards)		50		
ΔF	Internal Oscillator Frequency Range for (L = 10µH, C = 68pF)	590			
	Frequency Offset, After Automatic Adjustement			± 10	
UNDELAYED SIGNAL OUTPUTS (Pins 27-28)					
V_{27}, V_{28}	DC Voltage		1.6		V
I_{27}, I_{28}	Sink Current	1			mA
	Impedance		30		Ω
IDENTIFICATION					
	BURST ATTENUATION RANGE / NOMINAL LEVEL				
	SECAM Mode (line identification) PAL Mode	30 30			dB dB
	SECAM MODE				
V_{26}	Pin 26 Voltage (unloaded)	6.9	7.8	8.5	V
	Pin 26 Impedance	5	13	25	kΩ
	PAL MODE				
V_{26}	Pin 26 Voltage (unloaded)	3.6	4.2	4.9	V
	Pin 26 Impedance	2	6	15	kΩ
DELAYED SIGNAL INPUT (Pins 2-3)					
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
DELAY LINE ATTENUATION COMPENSATION					
	Range of Automatic Attenuation Compensation	– 3	– 9	– 15	dB
DELAY LINE PHASE SHIFT COMPENSATION					
	Range of Phase Shift Compensation with a 100kΩ Potentiometer (see application diagram)	± 30			degree
ALTERNATION LINE DETECTION PAL OR SECAM (Pin 11)					
V_{TH-H}	High Differential Threshold ($V_{TH-H} = V_{11H} - V_{24}$)	200		350	mV
V_{TH-L}	Low Differential Threshold ($V_{TH-L} = V_{11L} - V_{24}$)	– 350		– 200	mV
	Leakage Current Threshold ($V_{11} = V_{24} + 1V$)			0.5	µA

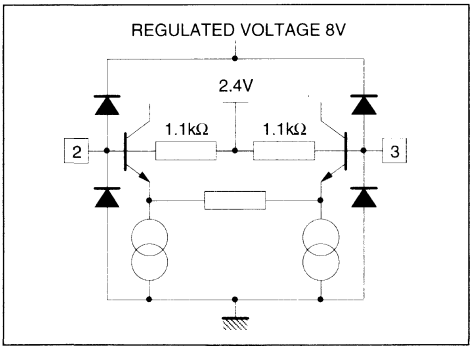
5640F-05.TBL

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

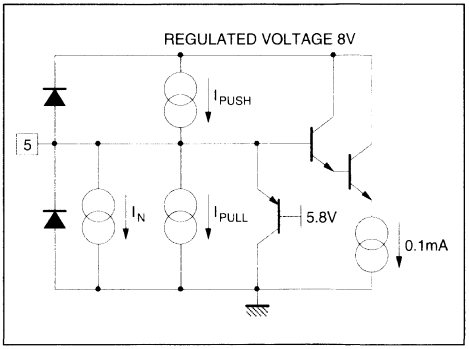
Pin 1



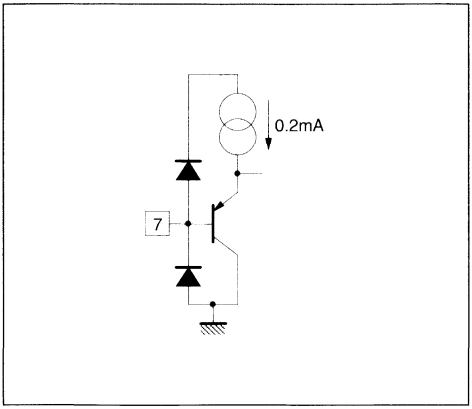
Pins 2-3



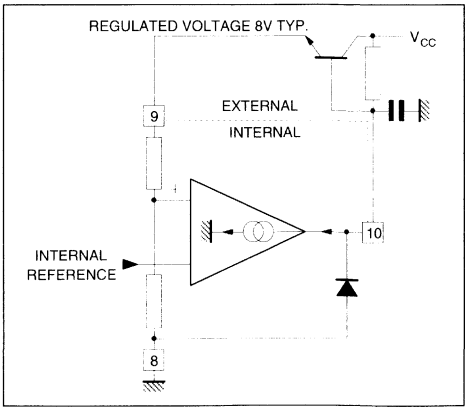
Pin 5



Pin 7

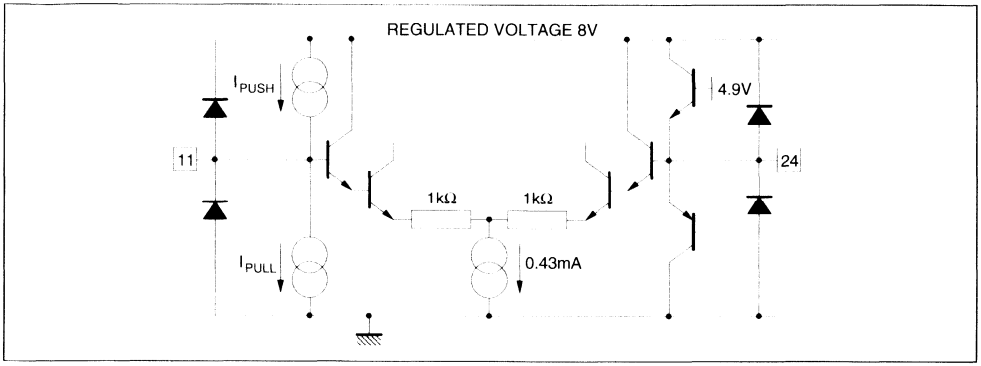


Pins 8-9-10

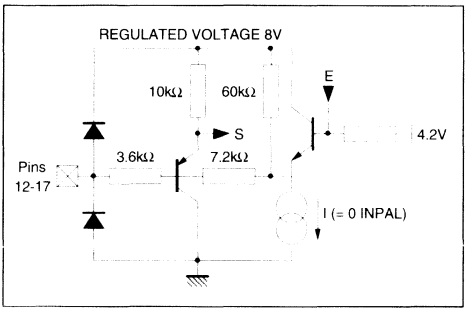


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

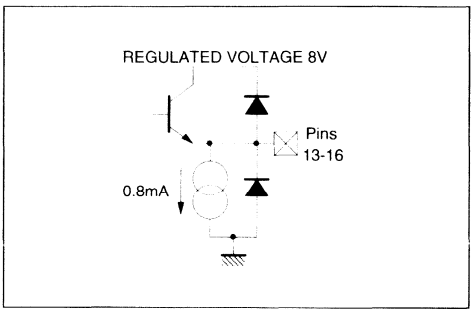
Pins 11-24



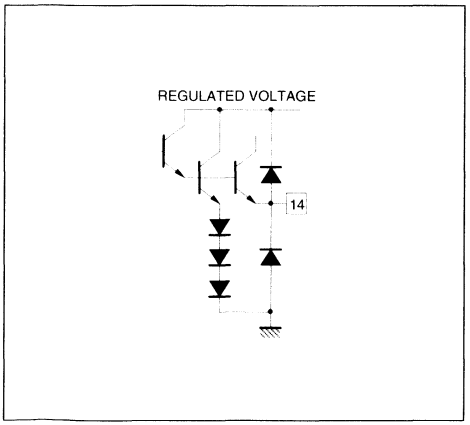
Pins 12-17



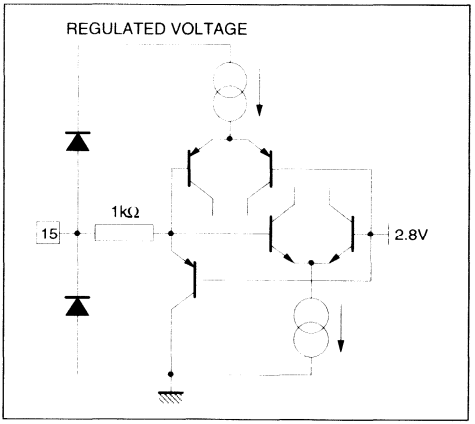
Pins 13 - 16



Pin 14

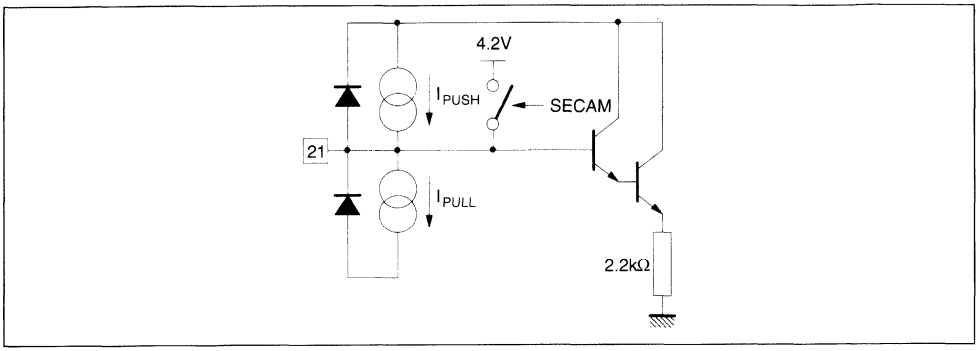


Pin 15

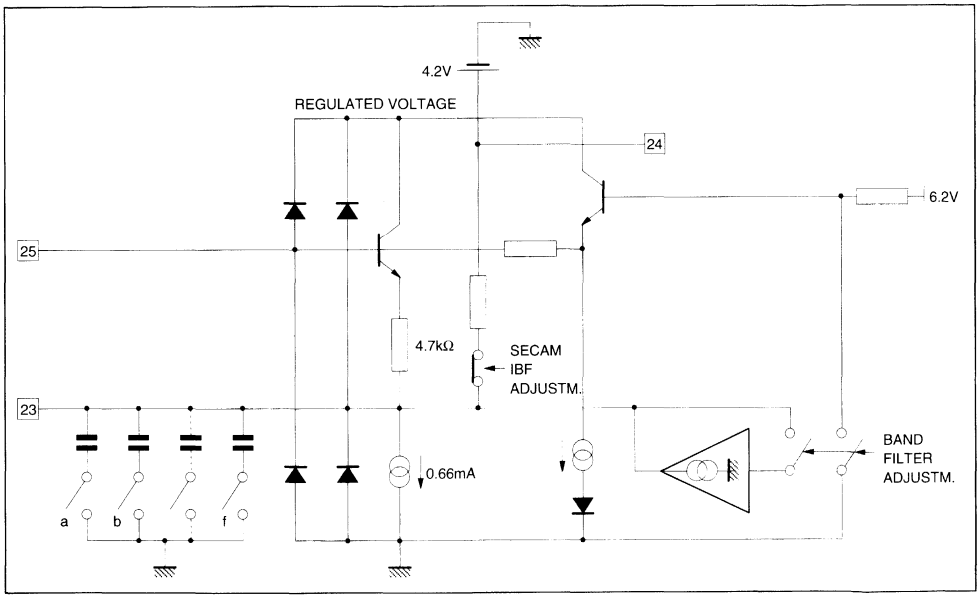


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Pin 21

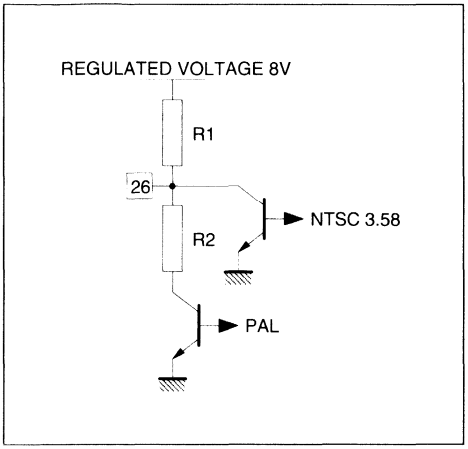


Pins 23-24-25

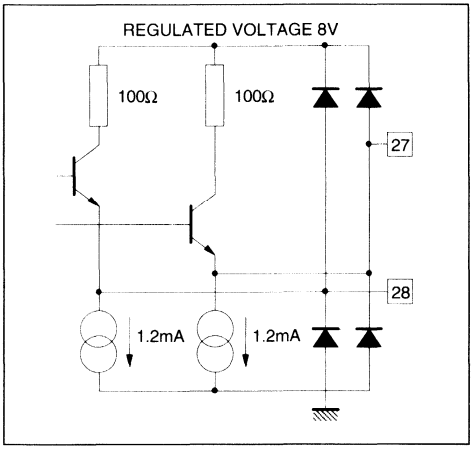


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

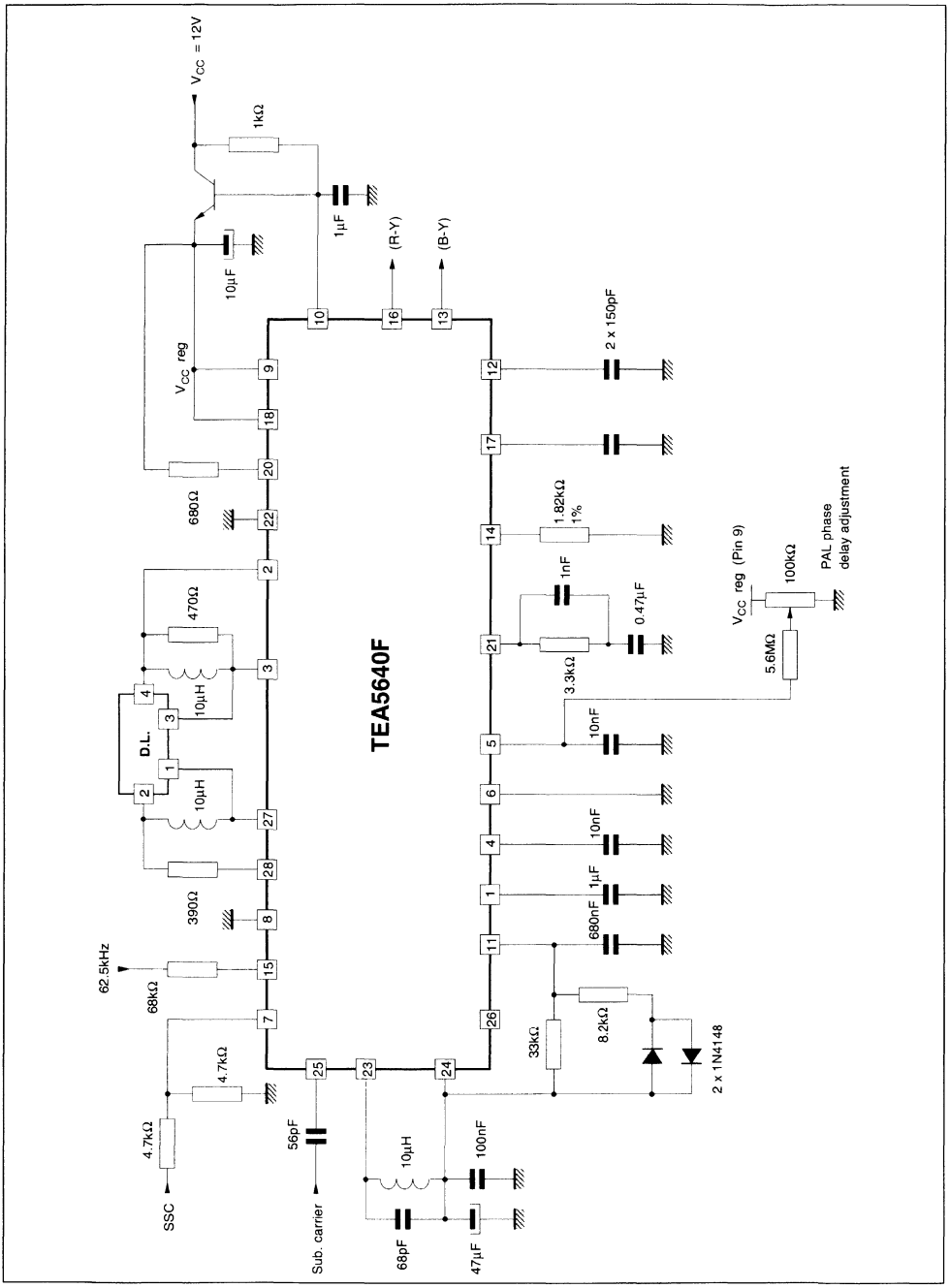
Pin 26



Pins 27 - 28



TYPICAL APPLICATION for PAL/SECAM

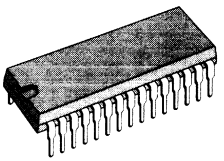


SGS-THOMSON MICROELECTRONICS

TEA5652

WIDE BAND VIDEO PROCESSOR

- Y, R-Y, B-Y INPUTS
- 2 RGB AND FAST BLANKING SOURCES
- RGB SOURCES MATRIXING INTO Y, R-Y, B-Y
- ANALOG CUT-OFF CONTROLS
- ANALOG CONTROLS FOR : BRIGHTNESS, CONTRAST, SATURATION ON ALL INPUT SIGNALS
- BEAM CURRENT LIMITER
- 62.5kHz GENERATOR (FOR TEA5640)
- INTERNAL INDEXATION BETWEEN SATURATION AND CONTRAST



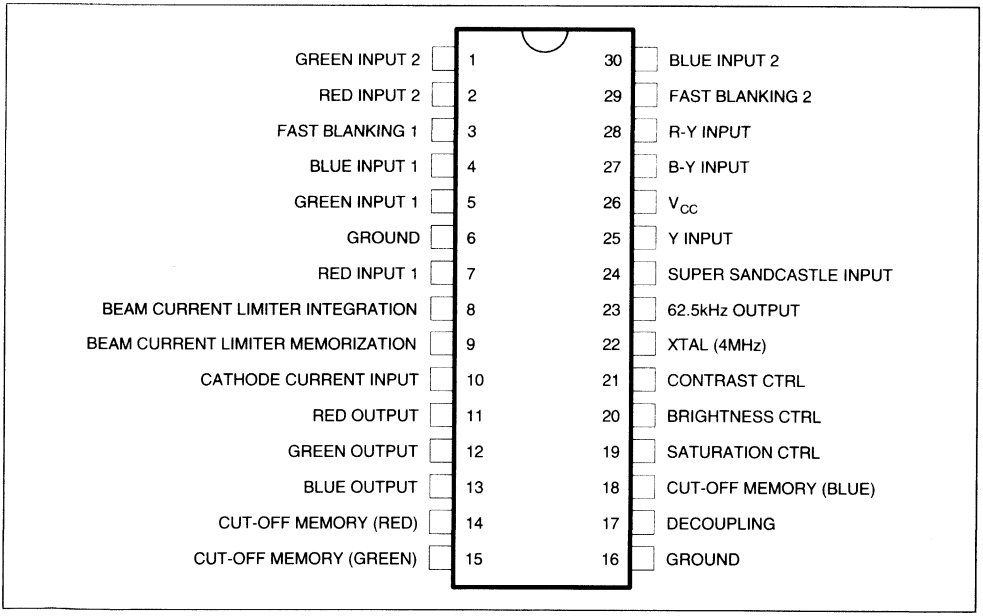
SHRINK30
(Plastic Package)

ORDER CODE : TEA5652S

DESCRIPTION

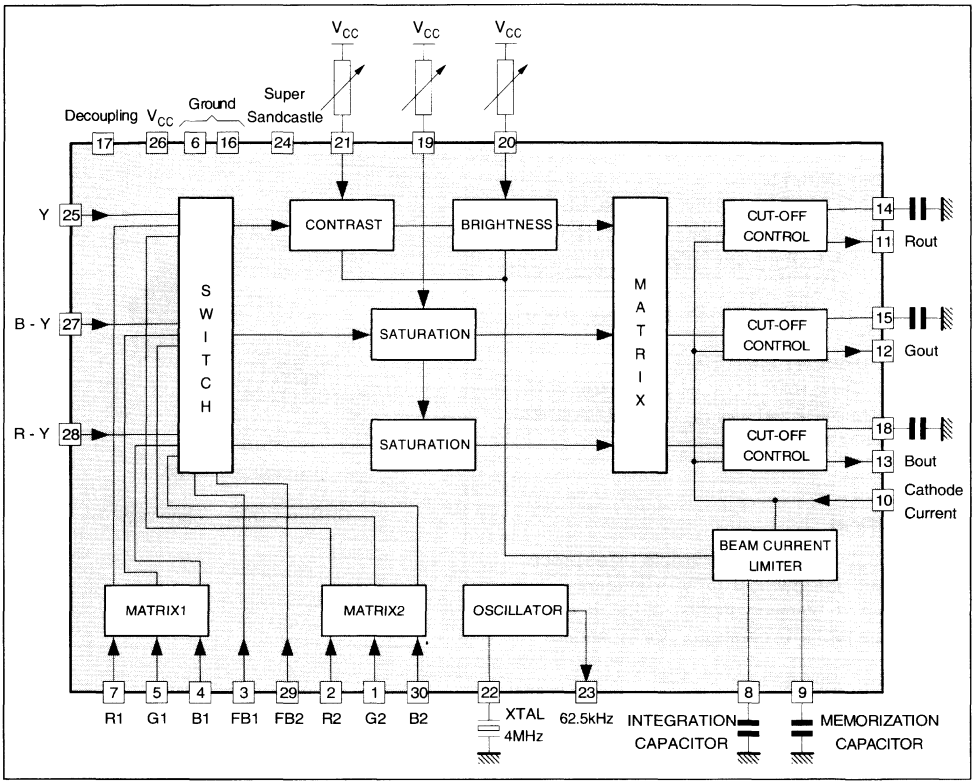
The TEA5652 is a wide band flexible video processor intended for low-cost CTV. It integrates two RGB and fast blanking inputs, a beam current limiter and a 62.5kHz generator (for TEA5640).

PIN CONNECTIONS



5652-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

This circuit includes the following features.

- One Y, R-Y, B-Y input
- Two R, G, B sources with their associated fast blankings
- Analog inputs for contrast brightness and saturation controls both on TV and RGB pictures.
- Saturation contrast indexation internally made.
- Analog cut-off controls.
- Start beam current limiter.
- Average beam current limiter.
- 62.5kHz generator to drive TEA5640 multistandard chroma decoder.

CLAMPING SYSTEM

Because the clamp information are selected after fast blanking switch it is necessary to clamp source by source line after line.

So during frame retrace the Y, R-Y, B-Y source is sampled during the burst gate of every line.

During the frame one source is selected by line : one line Y, R-Y, B-Y, one line RGB1, one line RGB2.

Analog Controls

Brightness, contrast and saturation are controlled by analog inputs.

The indexation between saturation and contrast is achieved internally.

Analog Cut-off Controls
The IC incorporates a standard sequential analog cut-off controls.
The controls are achieved sequentially during the four lines following the end of the frame retrace.

Beam Current Limiter (see Figures 1 and 2)
A new beam current limiter is used in this circuit. It provides the following features.
- a short time constant (one frame)
- no brightness and contrast variation during the frame
- a limitation of peak magnitudes

62.5kHz Generator
This function is devoted to deliver the 62.5kHz frequency reference to the chroma decoder TEA5640 from a 4MHz crystal. By this way the TEA5652 and TEA5640 can achieve a complete multistandard luma-chroma application.

Beam Current Limiter Capacitors Setting

C1 CALCULATION
C1 is the capacitor which integrates the cathode current during the frame :

$$C1 = \frac{1.15 \times I_{CATH} \times T_{AV}}{100 \times V_{TH}}$$

I_{CATH} : Average current per cathode
T_{AV} : Averaging duration =
Frame period - Frame retrace duration
~ 18.5ms for 50Hz operation
V_{TH} : Beam current limiter threshold voltage
~ 2.5V for V_{CC} = 8V
example : for $I_{cathode}$ = 800µA **C1 = 68nF**

C2 SETTING
The value of the memorization capacitor is determined to obtain good picture stability from one frame to following one.
We advice a value of 680nF for standard operation.

Figure 1 : Beam Current Limiter Block Diagram

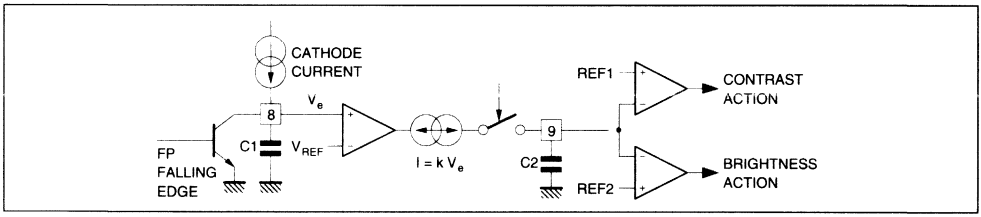
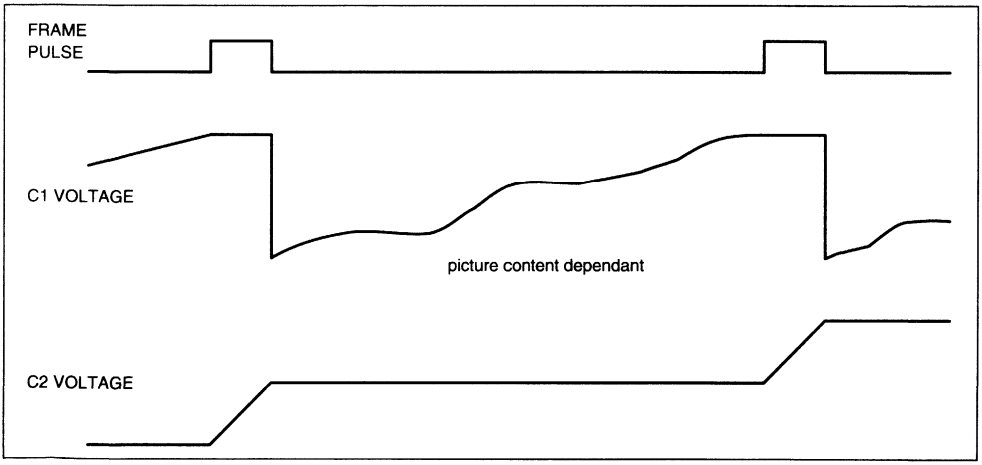


Figure 2 : Beam Current Limiter Waveforms



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12.6	V
T_{amb}	Operating Ambient Temperature	0, +70	°C

5652-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Juntion-ambient Thermal Resistance	70	°C/W

5652-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY SECTION (Pin 26)						
V_{CC}	Supply Voltage		7.5	8	8.5	V
I_{CC}	Supply Current	no loads on outputs		55	80	mA
Y-CVBS INPUT (Pin 25)						
CVBS	Signal Amplitude	100% white CVBS signal		0.5	0.75	Vpp
DC Y A	DC Level			1.7		V
I_{CLPY}	Positive Clamp Current			180		µA
I_{CLNY}	Negative Clamp Current			180		µA
$I_{LEAK\ Y}$	Leakage Current				1	µA
R-Y INPUT (Pin 28)						
R-Y A	Signal Amplitude	75% color bar pattern		1.05	1.47	Vpp
DC R-Y	DC Level			2.7		V
I_{CLPR}	Positive Clamp Current			180		µA
I_{CLNR}	Negative Clamp Current			180		µA
$I_{LEAK\ A}$	Leakage Current				1	µA
B-Y INPUT (Pin 27)						
B-Y A	Signal Amplitude	75% color bar pattern		1.3	1.86	Vpp
DC B-Y	DC Level			2.7		V
I_{CLPB}	Positive Clamp Current			180		µA
I_{CLNB}	Negative Clamp Current			180		µA
$I_{LEAK\ B}$	Leakage Current				1	µA
R-G-B INPUTS (Pins 1-2-4-5-7-30)						
RGB A	Signal Amplitude	100% amplitude		0.7	1	Vpp
DC RGB	DC Level			2.6		V
I_{CLP}	Positive Clamp Current			180		µA
I_{CLN}	Negative Clamp Current			180		µA
I_{LEAK}	Leakage Current				1	µA
FAST BLANKING INPUTS (Pins 3-29)						
FBLL	TV/RGB Low Level				0.5	V
FBHL	TV/RGB High Level		0.95		3	V
Z_{IN} FB	Input Impedance			1		kΩ
T_{ON} FB	Switching Delay Time On			40		nsec
T_{OFF} FB	Switching Delay Time Off			40		nsec

5652-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTRAST CONTROL (Pin 21)						
Typ. CONT	Nominal Value	Maximum contrast		0		dB
Min. CONT	Minimum Value			-16		dB
DC Max. C	DC Level for Contrast Max.			4.2		V
DC Min. C	DC Level for Contrast Min.			1.2		V
$I_{CONT\ C}$	Input Current				2	µA
SATURATION CONTROL (Pin 19)						
Max. SAT	Over Saturation Value			6		dB
Off SAT	Color Off Value	Referred to over saturation value		-45		dB
DC Nom. S	DC Level for Nominal Saturation			2.75		V
DC Max. S	DC Level for Over Saturation			4.25		V
DC Min. S	DC Level for Minimum Saturation			1.5		V
$I_{CONT\ S}$	Input Current				2	µA
BRIGHTNESS CONTROL (Pin 20)						
$I_{CONT\ B}$	Input Current				2	µA
BRIG	Brightness Range	Referred to nominal input levels (350mV B/W)		± 40		%
DC Max. B	DC Level for Maximum Brightness			4		V
DC Min. B	DC Level for Minimum Brightness			2		V
RGB OUTPUTS (Pins 11-12-13)						
High CLIP	High Clipping Level	Refered to minimal black level		185		%
	Blanking Voltage			0.5		V
	Typical Output B/W	Contrast max. - B/W input 350mV		1.6		V
	Minimum DC Level Cut-off Inserted	Cut-off caps DC voltage = 2.5V		1.7		V
	Maximum DC Level Cut-off Inserted	Cut-off caps DC voltage = V_{CC}		4.8		V
Y BAND	Y Bandwidth	-3dB attenuation	8	15		MHz
B-Y BAND	B-Y Bandwidth	-3dB attenuation	8	10		MHz
R-Y BAND	R-Y Bandwidth	-3dB attenuation	8	10		MHz
RGB BAND	RGB Bandwidth	-3dB attenuation	8	15		MHz
CROSSTALK						
CRRY	RGB/YUV Crosstalk	0 - 5MHz		45		dB
CRYR	RGB1/RGB2 Crosstalk	0 - 5MHz		45		dB
AUTOMATIC CUT-OFF (Pins 10-14-15-18)						
LEA REF	Leakage Current Reference Voltage			2		V
COF REF	Cut-off Reference	Refered to leakage current reference measured on Pin 10		+350		mV
I_{COP}	Capacitor Cut-off Positive Clamping Current			100		µA
I_{CON}	Capacitor Cut-off Negative Clamping Current			100		µA
BS REF	Start Beam Current Detection Reference Voltage	Pin 10		2.5		V
I_{LEAK}	Low Voltage Output Current	V_{10} = 0V		200		µA

5652-04 TBL

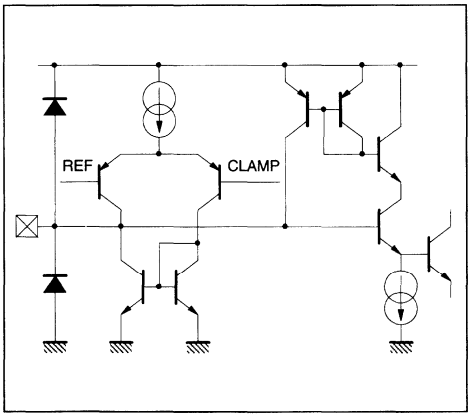
ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AVERAGE BEAM CURRENT LIMITER (Pin 8)						
	Max. Contrast Action	First action (decreasing)		-5		dB
	Max. Brightness Action	After contrast decreasing		80		%
V_{C1TH}	C1 Threshold Voltage			2.5		V
	C1 Discharging Current			10		mA
	Current Ratio between Pin 10 and 8			100		
C2 Y	C2 Min. Voltage	$V_{C1} < V_{C1TH}$		2.2		V
C2 I_C	Max. C2 Charging Current	V_{C1} = 6V		50		µA
C2 T_C	C2 Threshold Voltage for Contrast Action			2.6		V
C2 T_B	C2 Threshold Voltage for Brightness Action			3.2		V
SUPERSANDCASTLE INPUT (Pin 24)						
FT	Frame Threshold			0.7		V
LT	Line Threshold			1.9		V
BGT	Burst Gate Threshold			4		V
I_{OUT} SSC	Output Current	V_{24} = 0V		30		µA
XTAL (Pin 22)						
DC XTAL	DC Level			2.4		V
Z_S XTAL	Output Impedance			400		Ω
62.5kHz OUTPUT (Pin 23)						
Z_S	Output Impedance			250		Ω
DC H	DC Level High			6		V
DC L	DC Level Low			1.3		V
DC	Duty Cycle			100		%

5652-05.TBL

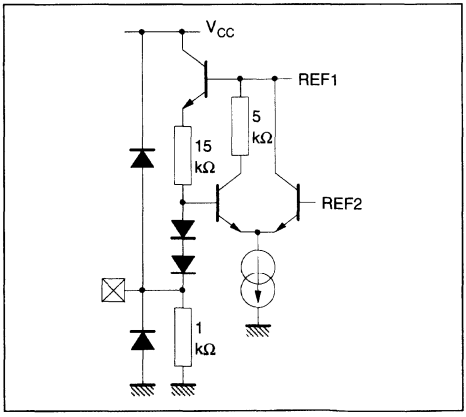
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

Figure 3 : Pins 1-2-4-5-7-30



5652-05.EPS

Figure 4 : Pins 3-29



5652-06.EPS

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Figure 5 : Pins 8-9

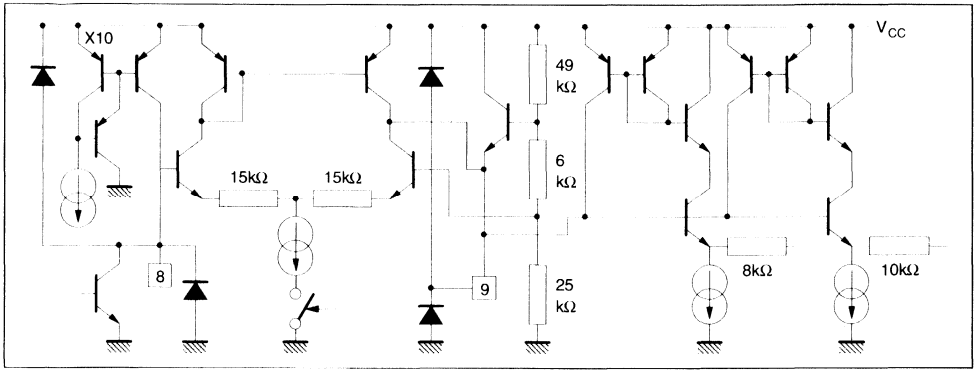


Figure 6 : Pins 10-14-15-18

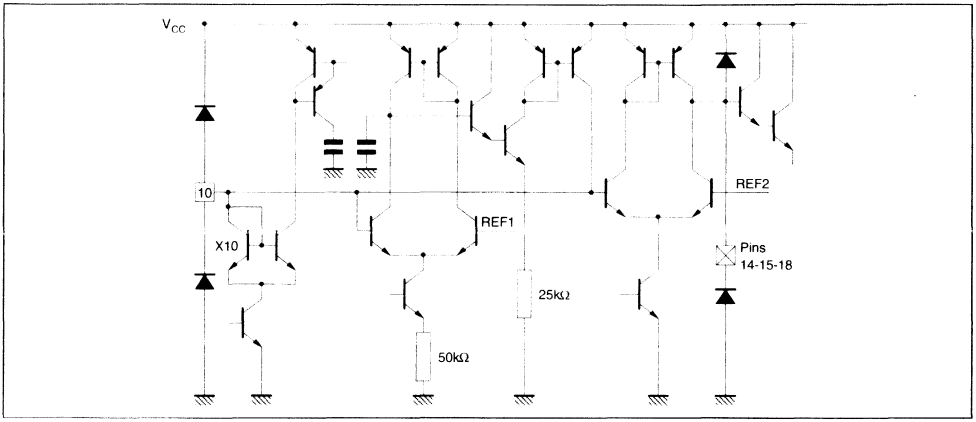


Figure 7 : Pin 19

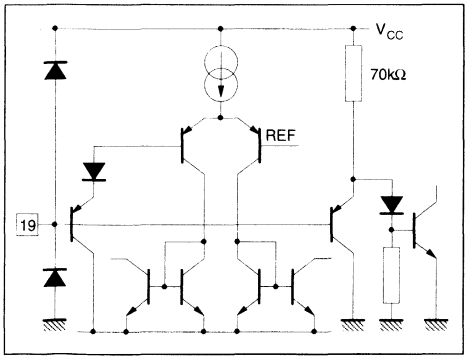
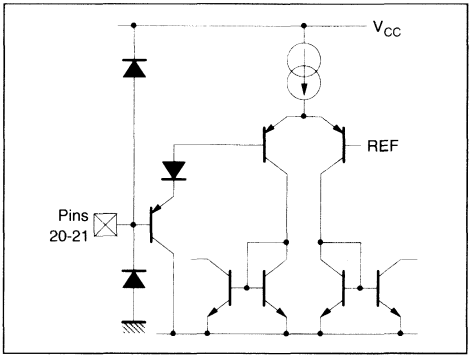


Figure 8 : Pins 20-21



INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

Figure 9 : Pin 22

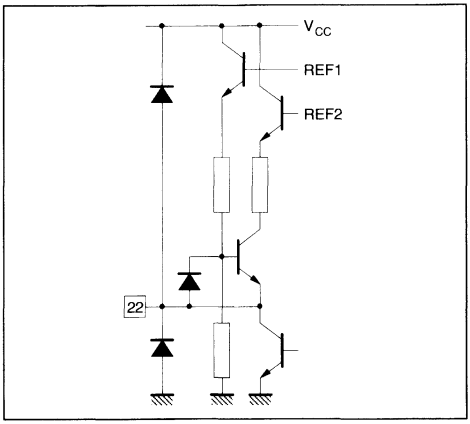


Figure 10 : Pin 23

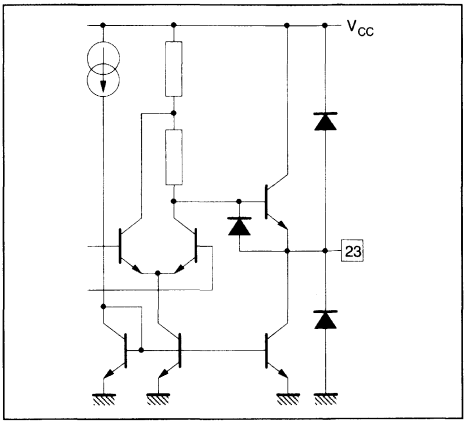


Figure 11 : Pin 24

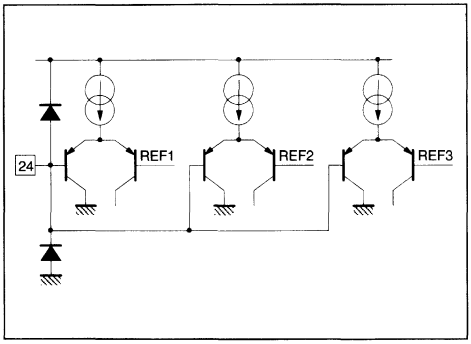


Figure 12 : Pin 25

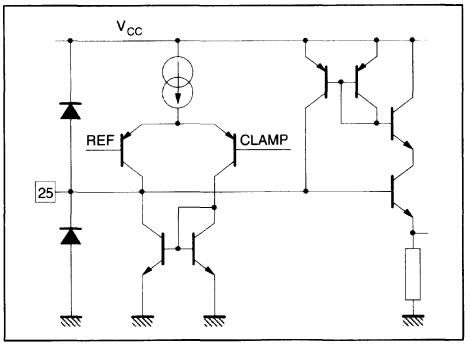


Figure 13 : Pins 26-17

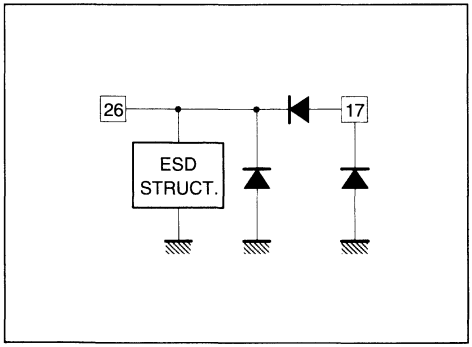


Figure 14 : Pins 27-28

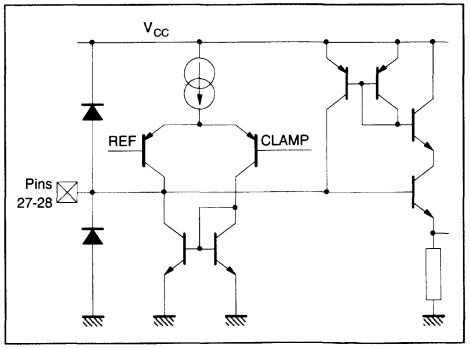


Figure 19 : Beam Current Limiter Action
Contrast Variation = f(V_{BCL2})

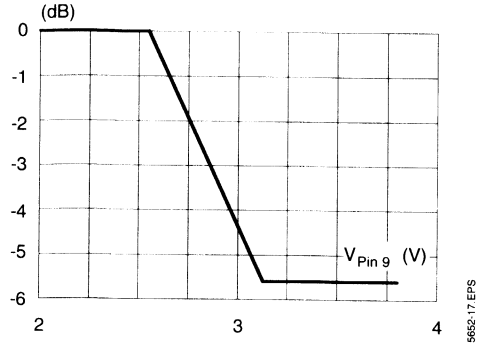


Figure 20 : Beam Current Limiter Action
Brightness Variation = f(V_{BCL2})

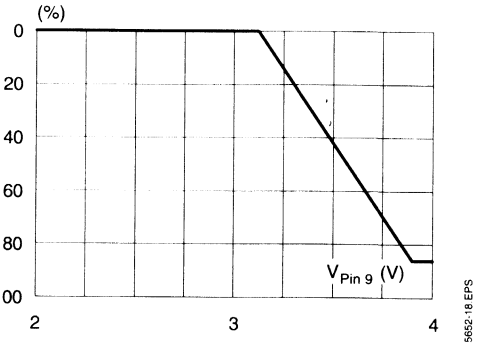


Figure 21 : Contrast Variation

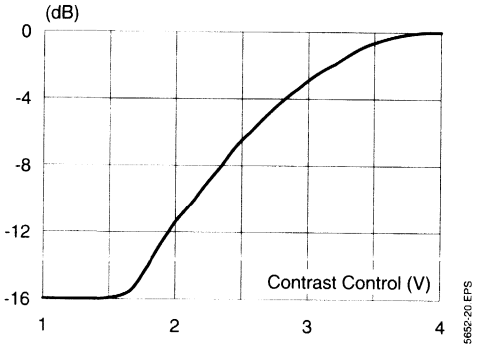


Figure 22 : Saturation Variation

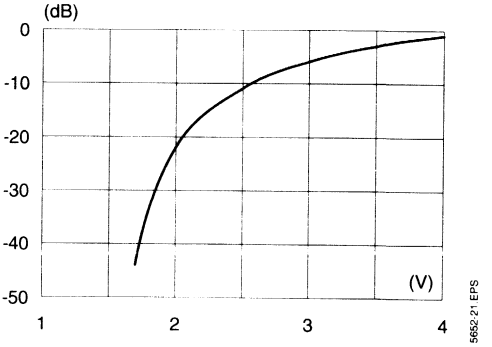
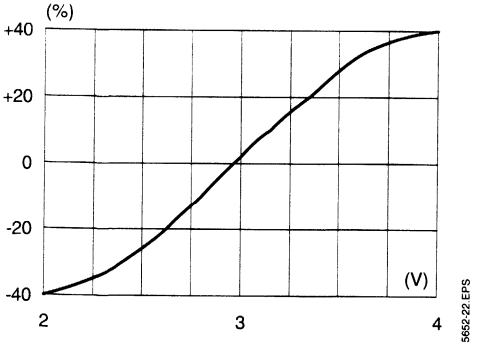
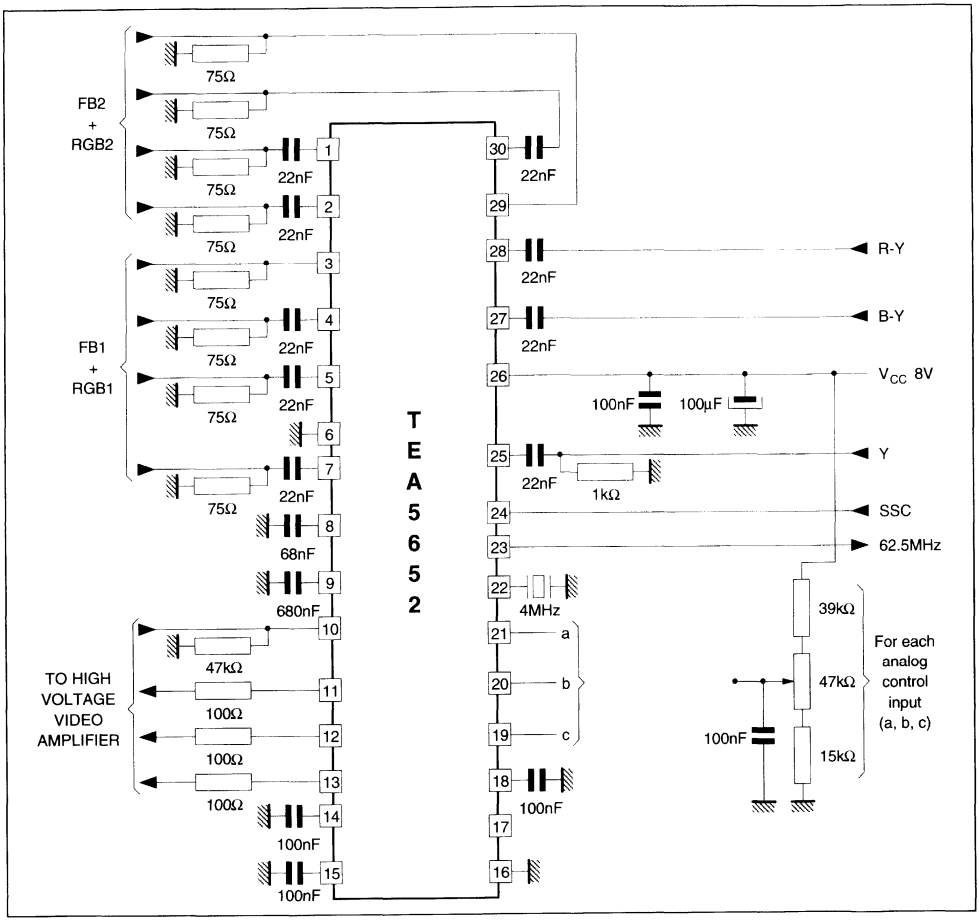


Figure 23 : Brigthness Variation



TYPICAL APPLICATION

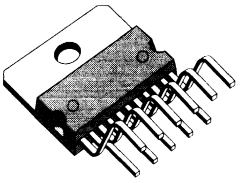


SGS-THOMSON MICROELECTRONICS

TEA5101A

RGB HIGH VOLTAGE VIDEO AMPLIFIER

- BANDWIDTH : 10MHz TYPICAL
- RISE AND FALL TIME : 50ns TYPICAL
- CRT CATHODES CURRENT OUTPUTS FOR PARALLEL OR SEQUENTIAL CUT-OFF OR DRIVE ADJUSTMENT
- FLASHOVER PROTECTION
- POWER DISSIPATION : 3.5W
- ESD PROTECTED



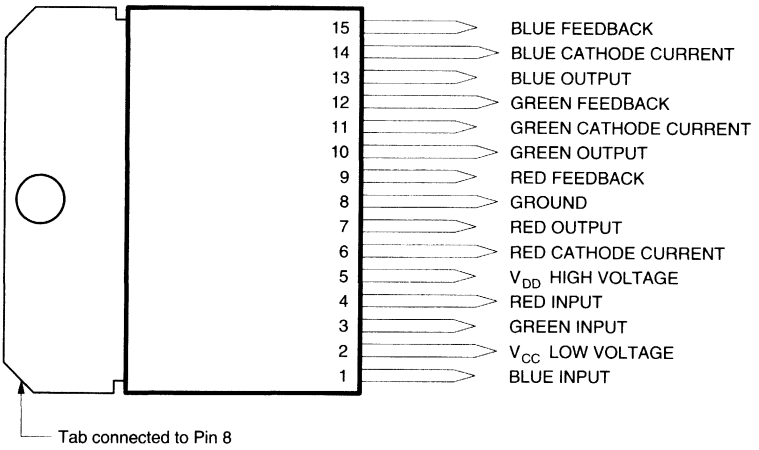
MULTIWATT 15
(Plastic Package)

ORDER CODE : TEA5101A

DESCRIPTION

The TEA5101A includes three video amplifiers designed with a high voltage DMOS/bipolar technology. It drives directly the three CRT cathodes. The device is protected against flashovers. Due to its three cathode current outputs, the TEA5101A can be used with both parallel and sequential sampling applications.

PIN CONNECTIONS (top view)



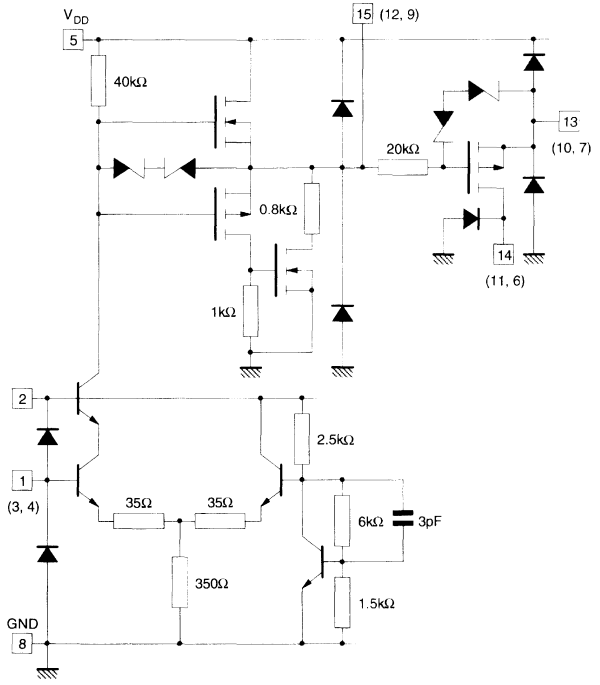
5101A-01.EPS

PIN FUNCTION

N°	Function	Description
1	Blue Input	Input of the "blue" amplifier. It is a virtual ground with 3.8 V bias voltage, 15 microamperes input bias current with 14kΩ input resistance.
2	V_{CC}	Low voltage power supply, typically 12V.
3	Green Input	See pin 1.
4	Red Input	See pin 1.
5	V_{DD}	High voltage power supply, typically 200V.
6	Red Cathode Current	Provides the video processor with a copy of the DC current flowing into the red cathode, for automatic cut-off or gain adjustment. If this control is not used, pin 6 must be grounded.
7	Red Output	Output driving the red cathode. Pin 7 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
8	Ground	Also connected to the heat sink.
9	Red Feedback	Output driving the feedback resistor network for the red amplifier.
10	Green Output	See pin 7.
11	Green Cathode Current	See pin 6.
12	Green Feedback	See pin 9.
13	Blue Output	See pin 7.
14	Blue Cathode Current	See pin 6.
15	Blue Feedback	See pin 9.

5101A-01.TBL

BLOCK DIAGRAM OF EACH CHANNEL



5101A-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply High Voltage	Pin 5	250	V
V_{CC}	Supply Low Voltage	Pin 2	35	V
I_O I_O	Output Current to V_{DD} to Ground	Pins 7 - 10 - 13	 Protected 8	 mA
I_F I_F	Output Current to V_{DD} to Ground	Pins 9 - 12 - 15	 45 45	 mA mA
I_j	Input Current	Pins 1 - 3 - 4	60	mA
T_j	Junction Temperature		150	°C
T_{oper}	Operating Ambient Temperature		0 to 70	°C
T_{stg}	Storage Temperature		– 55 to + 150	°C

5101A-02 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction Case Thermal Resistance	Max.	3	°C/W
$R_{th(j-a)}$	Typical Junction Ambient Thermal Resistance	Typ.	35	°C/W

5101A-03 TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C ; V_{CC} = 12V ; V_{DD} = 200V ; AV = 50 (unless otherwise specified)

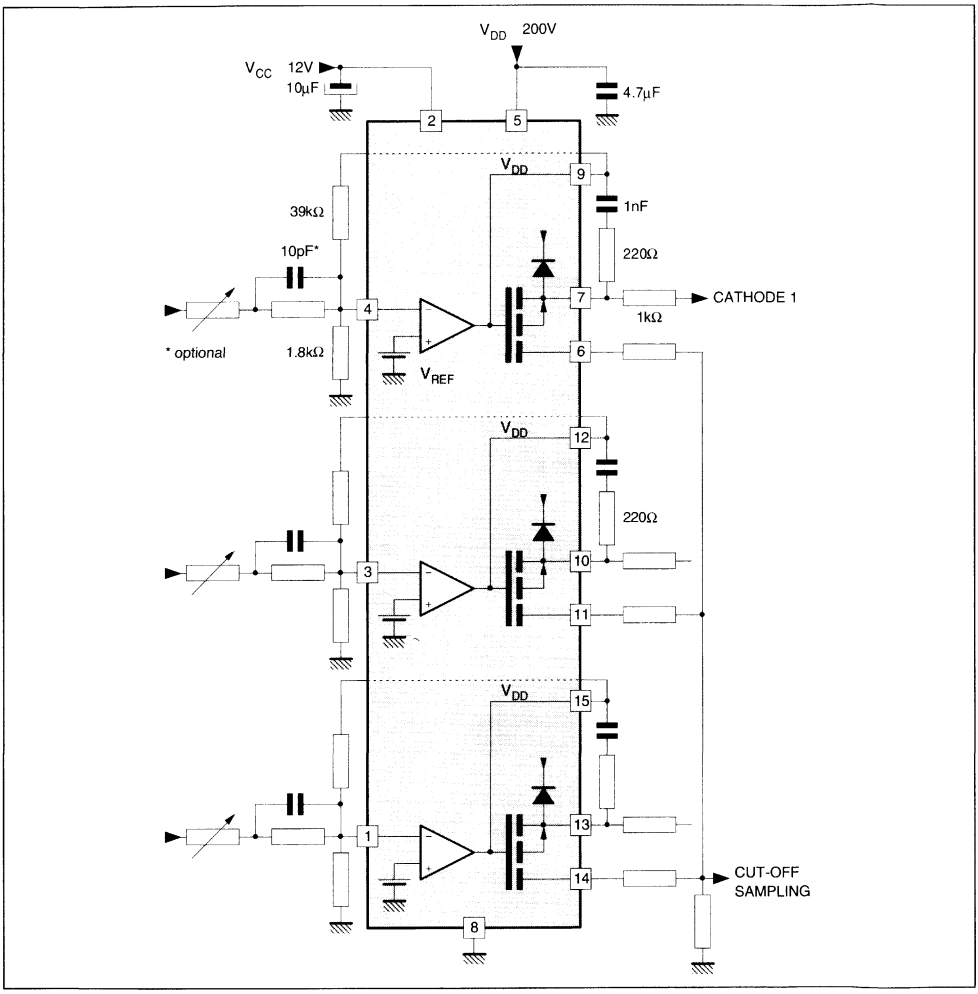
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	High Supply Voltage	Pin 5		200	220	V
V_{CC}	Low Supply Voltage	Pin 2	10	12	15	V
I_{DD}	High Voltage Supply Internal DC Current (V_{out} 100V) (without the current due to the feedback network)	Pin 5		8	12	mA
I_{CC}	Low Voltage Supply DC Current	Pin 2	19	33	47	mA
V_{sath}	Output Saturation Voltage (High level) I_O = – 10 µA	Pins 7-10-13		3	10	V
R_{ON}	Output Mos Transistor (Low level) R_{ON} @ I_O = 3 mA	Pins 7-10-13		1.7		kΩ
BW	Bandwidth (– 3db) (measured on CRT cathodes) (C_{LOAD} : 10pF – R Protect = 1kΩ – V_{out} = 100V) Δ V_{out} : 50 V_{PP} Δ V_{out} : 100 V_{PP}			 10 8		 MHz MHz
T_R - T_F	Rise Time and Fall Time : measured between 10% and 90% of output pulse (C_{LOAD} : 10 pF – R Protect = 1 kΩ – V_{out} = 100 V) Δ V_{out} : 100 V_{PP}			50		ns
G_O	Open Loop Gain		47	50		dB
P	Internal Power Dissipation (see calculation below)			3.5		W
V_{REF}	Internal Voltage Reference	Pins 1-3-4	3.55	3.8	4.05	V
	Internal Reference Voltage Difference Between 2 Channels				5	%
	Voltage Reference Temperature Coefficient			– 5		mV/°C
I_{IB}	Input Bias Current (V_{out} : 100 V)	Pins 1-3-4		15		µA
R_I	Input Resistance			14		kΩ

5101A-04 TBL

TYPICAL APPLICATION

The TEA5101A consists of three independent amplifiers. Each of them includes :

- A differential amplifier, the gain of which is fixed by external feedback resistors,
- A voltage reference,
- A PMOS transistor providing a copy of the cathode current,
- A protection diode against CRT arc discharges.



APPLICATION INFORMATION

PC BOARD LAYOUT

The best performances of the high voltage video amplifier will be obtained only with a carefully designed PC board. Output to input capacitances are of particular importance.

For a single amplifier, the input-output capacitance, in parallel with the relatively high feedback resistance, creates a pole in the closed-loop transfer function. A low parasitic capacitance (0.3pF) feedback resistor and HF isolated printed wires are necessary. Further more, capacitive coupling from the output of an amplifier toward the input of another one may induce excessive crosstalk.

POWER DISSIPATION

The power dissipation consists of a static part and a dynamic part. The static dissipation varies with the output voltage. With V_{DD} = 200V, P_{stat} = 2.6W typ(3.5W max) at V_{OUT} = 100V, 1.5W typ at 150V and 3W typ at 50V (with R feedback = 39kΩ).

V_{OUT} first value (100V) will be the reference.

The dynamic dissipation depends on the signal spectrum and the load capacitance.

- Dynamic power with a typical picture with 150 V_{pp} modulation is typically 1W.
- For a sine wave, dynamic dissipation per amplifier is $P_d = F \times C_l \times V_{opp} \times V_{dd} \times 0.8$.

The load capacitance C_L includes CRT and board capacitance (10pF), and amplifier output capacitance (8pF) : total C_L value is about 20pF. For a 5MHZ, 50 V_{pp} sine wave and a 20pF load capacitance, the maximum dynamic power is 2.5W.

- Generally, the maximum dynamic power is reached with a white noise (tuner noise).
- Typical value is about 2W.

Total dissipation is typically 3.6W (2.6W + 1W). With a maximum static dissipation of 3.5W, total dissipation is :

- 4.5W with a typical picture (UER pattern)
- 5.5W with white noise

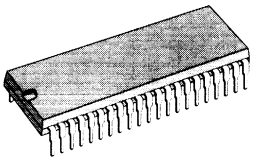
SGS-THOMSON MICROELECTRONICS

STV2102A

PAL LUMA-CHROMA & DEFLECTION PROCESSOR

PRELIMINARY DATA

- RGB AND FAST BLANKING INPUTS
- AUTOMATIC CUT-OFF CONTROL
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR



SHRINK 42
(Plastic Package)

ORDER CODE : STV2102A

DESCRIPTION

The STV2102A is a PAL chroma decoder, video and H/V deflection processor for CTV.

Used with the TDA8222, this IC permits a complete low cost solution with external output stages.

It is pin compatible with STV2110A PAL/SECAM processor.

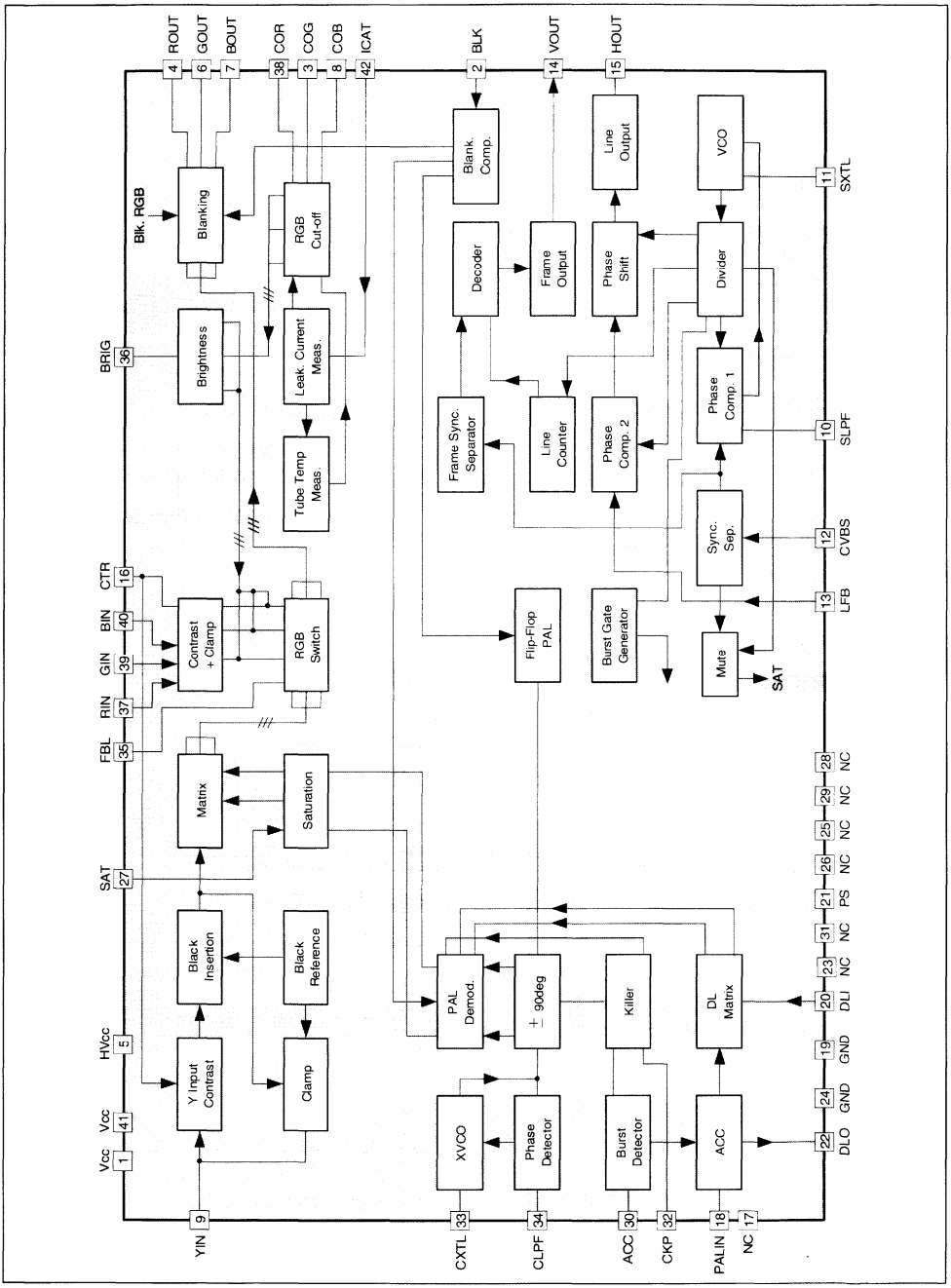
PIN CONNECTIONS

SUPPLY VOLTAGE	**Vcc**	1	42	**ICAT**	CATHODE CURRENT
BLANKING INPUT	**BLK**	2	41	**Vcc**	SUPPLY VOLTAGE INPUT
GREEN CUT-OFF CAPACITOR	**COG**	3	40	**BIN**	BLUE INPUT
RED OUTPUT	**ROUT**	4	39	**GIN**	GREEN INPUT
HORIZONTAL Vcc	**HVcc**	5	38	**COR**	RED CUT-OFF CAPACITOR
GREEN OUTPUT	**GOUT**	6	37	**RIN**	RED INPUT
BLUE OUTPUT	**BOUT**	7	36	**BRIG**	BRIGHTNESS CONTROL
BLUE CUT-OFF CAPACITOR	**COB**	8	35	**FBL**	FAST BLANKING INPUT
LUMINANCE SIGNAL INPUT	**YIN**	9	34	**CLPF**	CHROMA LOOP FILTER
SCANNING LOOP FILTER	**SLPF**	10	33	**CXTL**	CHROMA XTAL
SCANNING XTAL	**SXTL**	11	32	**CKP**	PAL KILLER CAPACITOR
COMPOSITE VIDEO SIGNAL	**CVBS**	12	31	**NC**	NOT CONNECTED
LINE FLYBACK INPUT	**LFB**	13	30	**ACC**	ACC CONTROL CAPACITOR
VERTICAL OUTPUT	**VOUT**	14	29	**NC**	NOT CONNECTED
HORIZONTAL OUTPUT	**HOUT**	15	28	**NC**	NOT CONNECTED
CONTRAST CONTROL	**CTR**	16	27	**SAT**	SATURATION CONTROL
NOT CONNECTED	**NC**	17	26	**NC**	NOT CONNECTED
PAL CHROMA INPUT	**PALIN**	18	25	**NC**	NOT CONNECTED
GROUND	**GND**	19	24	**GND**	GROUND
DELAY CHROMA INPUT	**DLI**	20	23	**NC**	NOT CONNECTED
CHROMA STANDARD	**PS**	21	22	**DLO**	CHROMA OUTPUT

2102A-01 EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

DEFLECTION

Synchronization Separator

The synchronization separator is based on the bottom of synchronization pulses alignment to an internal reference voltage. An external capacitor permits to align synchro. pulses, two external resistors determines the detection threshold of synchro pulses. The frame synchronization pulses are locked to a 32µs reference signal to perfect interlacing.

Horizontal Scanning

The horizontal scanning frequency is obtained from a 500kHz VCO. The circuit uses two phase-locked loops (PLL). The first one controls the frequency; the second one, fully integrated, controls the relative phase of the synchronization and the line flyback signals.

The first PLL has two times constants : a long time constant during the picture to have a good noise immunity, a short time constant at the beginning of the frame to recapture faster the phase in case of VCR video signal. More over, the PLL is in short time constant three lines before frame pulses occured, it permits to ensure good interlacing when the video signal comes from a VCR tape with high phase error.

The horizontal output signal is 28µs width. On starting up, horizontal pulses are enabled at V_{CC} = 6.8V. On shutting down, horizontal pulses are inhibited for V_{CC} = 6.2V.

Vertical Scanning

The windows for the frame sync detection are generated by a count down system. The selection of the windows is determined by the IC status :

- video identification off - window : 248/314
- video identification on - window : 248/352

When a sync pulse is detected inside the window a 10.5 lines long pulse is provided to V_{OUT} pin.

The count down system provides also the needed signals for the time constant switch, the line PLL inhibition and service signals to the rest of the IC.

CHROMA

ACC Amplifier, DL Matrix Demodulator

The correct chroma subcarrier input, issued from bandpass or bell filter, is internally selected with the standard. The ACC amplifier envolves three stages : the first one select the correct input, the second one the -6dB in picture (PAL mode), the third one is controled by the ACC voltage.

The dynamic range is over than 30dB.

The chrominance output signal is fed to the delay line :

- the adding and substracting direct and delayed signals are performed by the DL matrix function. Two synchronous demodulators multiplies the (B-Y) signal with the 0 degree phase 4.43MHz reference signal and the (R-Y) signal with the alternate ± 90 deg. 4.43MHz phase reference signal.

4.43MHz Phase Locked Loop

The oscillating frequency of the 4.43MHz crystal oscillator is controlled by the output voltage of the loop filter. The phase detector will lock the 90 degree reference signal to the direct burst signal. A 90 degree phase shifter permits to recover the 0 degree reference signal. A flip-flop driven by line pulses permits to generate the alternate ± 90 degree signal.

ACC Control and Color Killer

PAL mode :

the direct burst signal is demodulated with the ± 90 degree reference signal. The demodulation result is used by ACC control and killer function.

If the demodulation result is always positive, the killer capacitor is charged and the standard is identified (color ON). When demodulation result is always negative, the killer capacitor voltage reaches the flip-flop inhibition level, so the alternance sequence is reversed and the capacitor is charged again.

In case of no video signal, both killer capacitors voltage are maintained about $V_{CC}/2$, below the color off threshold.

The ACC control voltage is obtained by the peak detection of the demodulated burst.

VIDEO

Input Stage

The luminance input is controlled by the contrast control stage which range is 20dB.

The luminance and color difference signals are added in the video matrix circuit to obtain the color signals.

The color signals are sent to an RGB switch which will drive to the outputs either internal RGB signals or external RGB signals.

Automatic Cut-off Control

The black levels of the RGB outputs are controlled with the cut-off loops during three line periods after the frame retrace. The cut-off measurements are sequentially achieved during these three lines. The leakage current measurement is achieved during the frame retrace and memorized on an internal capacitor, thus the circuit is able to extract the cut-off current from the total current measurement.

Warm-up Detector

At the start-up, the cut-off loops are switch off, a white level is inserted on the luminance signal until a cathode current is detected. Then the cut-off loops are released.

RGB Inputs

To avoid the black level of the inserted signal differing from the black level of the normal video signal, the external RGB are clamped to the black level of the luminance signal. Therefore, an AC coupling is required for the RGB inputs.

The RGB inputs are controlled by a 12dB range contrast control stage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
HV_{CC}	Horizontal Supply Voltage (Pin 5)	12	V
V_{CC}	Video & Chroma Supply Voltage (Pins 1-41)	HV_{CC} + 0.5	V
H_{OUT}	Horizontal Output (Pin 15)	12	V
T_{stg}	Storage Temperature	-55, +150	°C
T_{oper}	Operating Temperature	0, +70	°C

2102A-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	60	°C/W

2102A-02.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HV_{CC}	Scanning Supply Voltage (Pin 5)		8.1	9	9.9	V
V_{CC}	Video & Chroma Supply Voltage (Pins 1-41)		8.1	9	9.9	V
I_{cch}	Scanning Supply Current (pin 5)	No load		25	35	mA
$I_{ccv\&c}$	Video & Chroma Supply Current (Pins 1-41)	No load		45	55	mA
P_D	Total Power Dissipation	No load		630	890	mW
LUMINANCE INPUT (Pin 9)						
V_{BW9}	Input Voltage			350	490	mV_{PP}
V_{DC9}	DC Level	No input signal		2.6		V
I_g	Input Current	• During burst period • Out of burst period		±150	 1	µA µA
G_9	Luma Gain			7.4		
BW467	Bandwidth (Y to R, G, B outputs)	-3dB		6		MHz
CONTRAST CONTROL (Pin 16)						
V_{16}	Contrast Control Voltage			2 to 4		V
$V_{16\ (Max.)}$	Allowed Control Voltage				5	V
G_{16}	Contrast Control Range			20		dB
I_{16}	Input Current				10	µA
BRIGHTNESS CONTROL (Pin 36)						
V_{36}	Brightness Control Voltage			1.8 to 4.3		V
$V_{36\ (Max.)}$	Allowed Control Voltage				5	V
I_{36}	Input Current				10	µA

2102A-03.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

($HV_{CC} = V_{CC} = 9V$, $T_{amb} = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SATURATION CONTROL INPUT (Pin 27)						
V_{27}	Saturation Control Voltage			2 to 4		V
$V_{27\,(Max.)}$	Allowed Control Voltage				5	V
G_{27}	Saturation Control Range			-50		dB
V_{27M}	Mute Level				0.5	V
I_{27}	Input Current				10	µA
RGB OUTPUTS (Pins 4-6-7)						
$V_{BW\ 4\text{-}6\text{-}7}$	Output Signal Amplitude (black to white)	• 0.35V B to W @ Pin 9 • Contrast @ 4V • Sat. & Brig. @ 3V		2.6		V
$I_{4\text{-}6\text{-}7}$	Individual Output Sinking Current			2		mA
$VM_{4\text{-}6\text{-}7}$	Maximum Peak White Level			7.8		V
$V_{blank\ 4\text{-}6\text{-}7}$	Blanking Level			0.5		V
$V_{CO\ min.}$	Minimum Level of Inserted Cut-off Lines			2.5		V
$V_{CO\ max.}$	Maximum Level of Inserted Cut-off Lines			4.5		V
	Relative Variation in Black Level with Various CONT. SAT. BRIG between the 3 channels				20	mV
ΔV_{temp}	Black Level Thermal Drift			0.5		mV/°C
	Tracking between Luminance and Chrominance Signals over 10dB Contrast Control				2	dB
RGB INPUTS (Pins 37-39-40)						
$V_{BW37\text{-}39\text{-}40}$	Input Amplitude (B to W)			0.7	2	V
$V_{clamp\ 37\text{-}39\text{-}40}$	Clamp Level	Contrast max		1.8		V
$I_{37\text{-}39\text{-}40}$	Control Current			±150		µA
$I_{i37\text{-}39\text{-}40}$	Leakage Current				1	µA
$BW_{37\text{-}39\text{-}40}$	Bandwidth	-3dB		8		MHz
G_{CTR}	RGB Contrast Control Range			14		dB
$G_{37\text{-}39\text{-}40}$	RGB Gain			3.7		
FAST BLANKING INPUT (Pin 35)						
$V_{TH1\text{-}35}$	First Threshold (switching)			0.7		V
$V_{TH2\text{-}35}$	Second Threshold (blanking)			2.1		V
T_{switch}	Switching Delay			50		ns
T_{blank}	Blanking Delay			100		ns
CATHODE CURRENT INPUT (Pin 42)						
V_{REF42}	Leakage Current Reference Voltage			1.75		V
ΔV_{REF42}	CO Reference refered to Leakage Current Reference			250		mV
I_{42}	Output Current		150			µA
V_{sb42}	Start-beam Current Detection Reference Voltage			2.4		V
AUTOMATIC CUT-OFF (Pin 3-8-38)						
	Cut-off Capacitor Clamping Current			± 100		µA

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMINANCE INPUT (Pin 18)						
V_{18}	Input Level			0.3	1.0	V_{PP}
$V_{burst-18}$	Minimum Burst Signal Amplitude within the ACC Control Range			30		mV_{PP}
G_{ACC}	ACC Control Range	Change of burst over whole ACC Control Range < 1dB		30		dB
R_{18}	Input Impedance			8		kΩ
V_{DC-18}	DC Level	No input signal		3.5		V
ACC CAPACITOR (Pin 30)						
I_{30}	Charging Current	During burst gate period		250		µA
I_{i30}	Leakage Current	Out of burst gate period			1	µA
PLL LOOP FILTER (Pin 34)						
I_{34}	Control Current			400		µA
CHROMAXTAL (Pin 33)						
CR_{33}	Catching Range			±700		Hz
SUBCARRIER OUTPUT (Pin 22)						
$V_{burst-22}$	Output Burst Amplitude	Within ACC Control Range		2		Vpp
KILLER CAPACITOR (Pin 32)						
V_{OFF-32}	Color off Threshold			5.0		V
V_{ON-32}	Color on Threshold			5.4		V
V_{INH-32}	PAL Flip-flop Inhibition Level			3.2		V
I_{32}	Control Current			250		µA
V_{nom-32}	Voltage with Nominal Input Signal			6.0		V
DELAYED CHANNEL INPUT (Pin 20)						
V_{DC-20}	DC Level	No input Signal		2.2		V
R_{20}	Input Impedance			8		kΩ
COMPOSITE VIDEO BASE BAND SIGNAL (Pin 12)						
V_{REF-12}	Clamp Voltage	I_{12} = - 1µA	1.6	1.85	2.1	V
V_{12}	Video Input Signal (sync to white)			1		V_{PP}
I_{12}	Sync Threshold			12		µA
SCANNING XTAL (Pin 11)						
F_{11}	Frequency after Divider			15.625		kHz
CR_{11}	Frequency Control Range after Divider			±700		Hz
PLL LOOP FILTER (Pin 10)						
I_{low-10}	Output Current	Long time constant		0.15		mA
$I_{high-10}$	Output Current	Short time constant		0.40		mA
DELAYED LINE FLYBACK INPUT (Pin 13)						
V_{TH-13}	Threshold			0.6		V
V_{13}	Allowed Voltage Range		- 0.4		HV_{CC}	V
I_{13}	Input Current	V_{13} < 0.6V			5	µA

DC AND AC ELECTRICAL CHARACTERISTICS (continued)
(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIRECT BLANKING INPUT (Pin 2)						
V_{TH-2}	Threshold			0.6		V
V_2	Allowed Voltage Range		- 0.4		HV_{CC}	V
I_2	Input Current	V_2 < 0.6V			5	µA
HORIZONTAL OUTPUT (Pin 15)						
T_{15}	Output Pulse Width		26	28	29	µs
V_{low-15}	Output Voltage (open collector)	I_{15} = 10mA		1.5		V
$V_{5\ start}$	HV_{CC} Start Threshold			6.8		V
$V_{5\ stop}$	HV_{CC} Stop Threshold			6.2		V
Δt_{15}	φ2 Phase Range			12		µs
VERTICAL OUTPUT (Pin 14)						
T_{14}	Output Pulse Width			10.5		line
T_{sync1}	Frame Synchro. Window (search)			248 to 352		line
V_{low-14}	Output Voltage (open collector)			1		V

2102A-06.TBL

Figure 1 : Contrast Control Curve

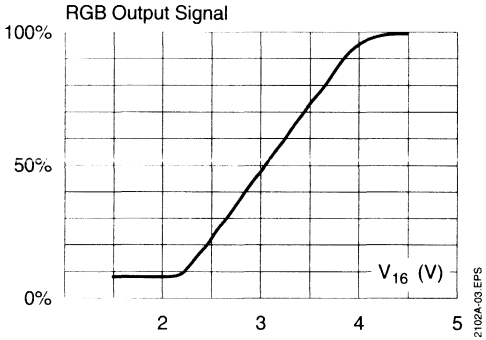


Figure 2 : Saturation Control Curve

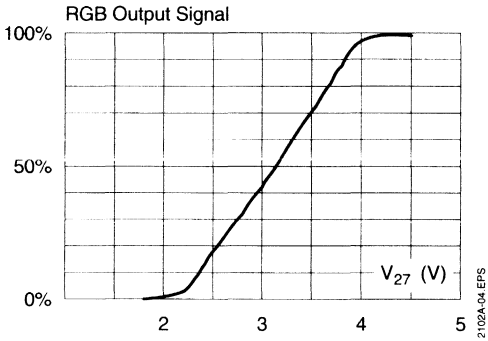


Figure 3 : Difference between Black Level and measuring Level at RGB Outputs as a function of the Brightness Control Input

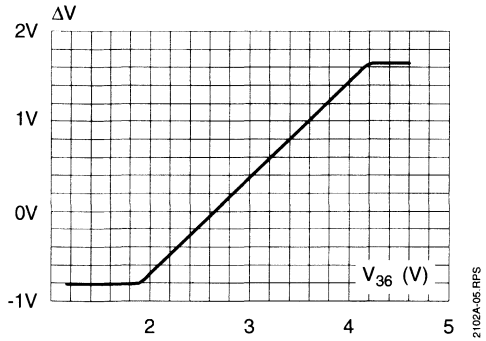


Figure 4 : Pins 3-8-38-42 (COG, COB, COR, ICAT)

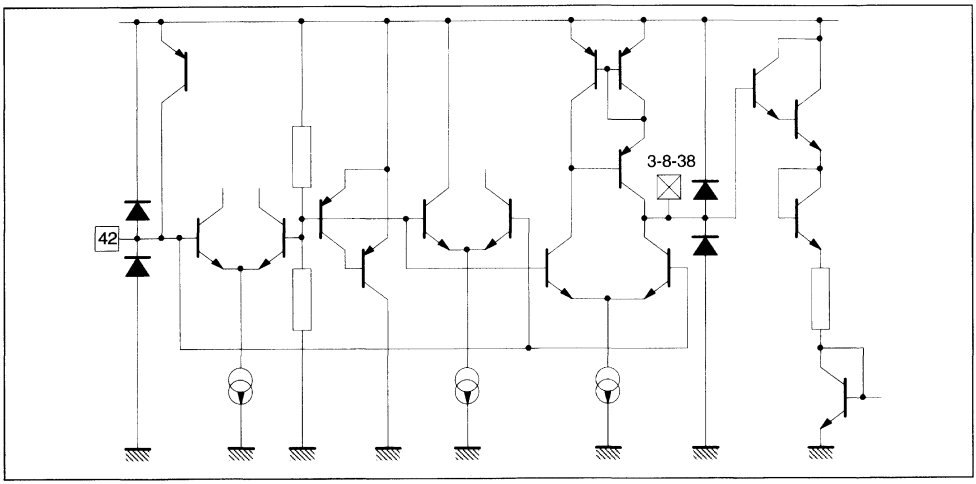


Figure 5 : Pins 37-39-40 (RIN, GIN, BIN)

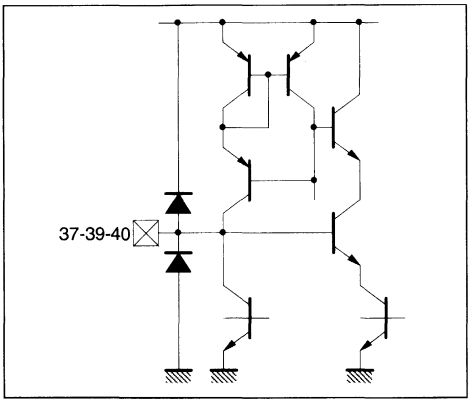


Figure 6 : Pins 4-6-7 (ROUT, GOUT, BOUT)

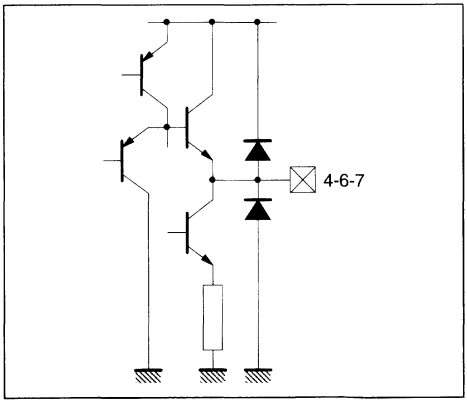


Figure 7 : Pin 9 (YIN)

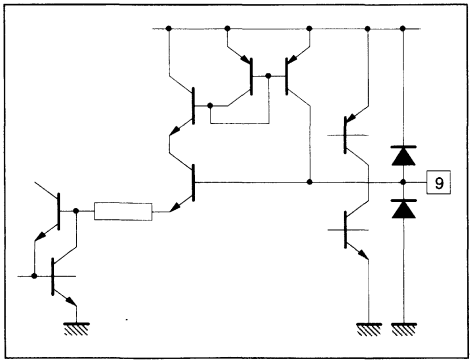


Figure 8 : Pin 10 (SLPF)

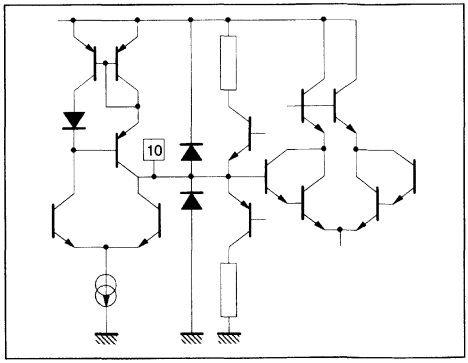


Figure 9 : Pin 11 (SXTL)

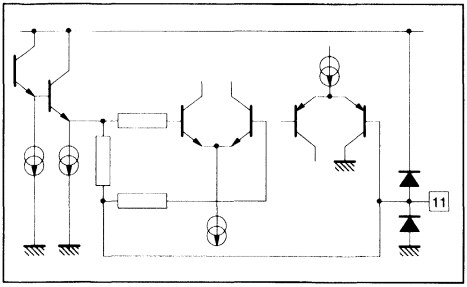


Figure 10 : Pin 12 (CVBS)

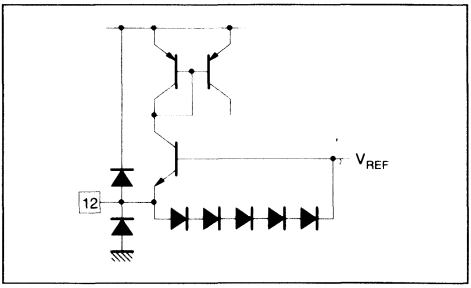


Figure 11 : Pins 2-13 (BLK, LFB)

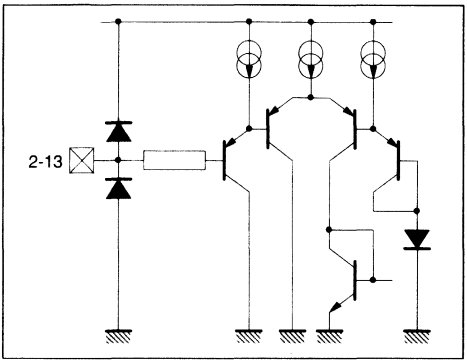


Figure 12 : Pins 14 (VOUT)

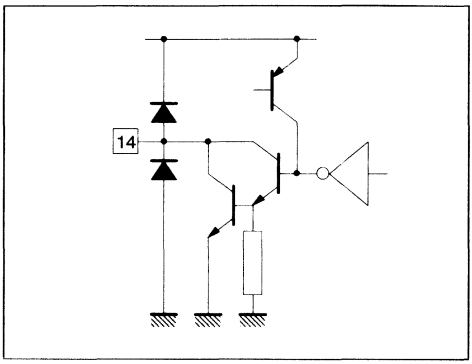


Figure 13 : Pin 15 (HOUT)

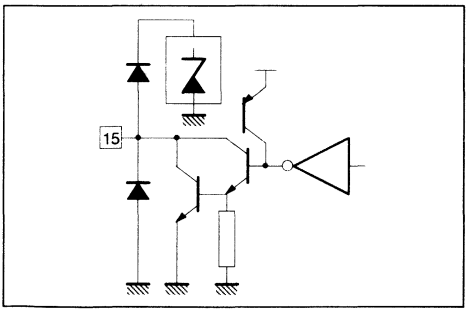


Figure 14 : Pins 16-27 (CTR, SAT)

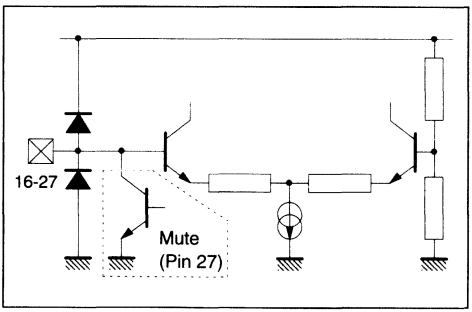


Figure 15 : Pin 20 (DLI)

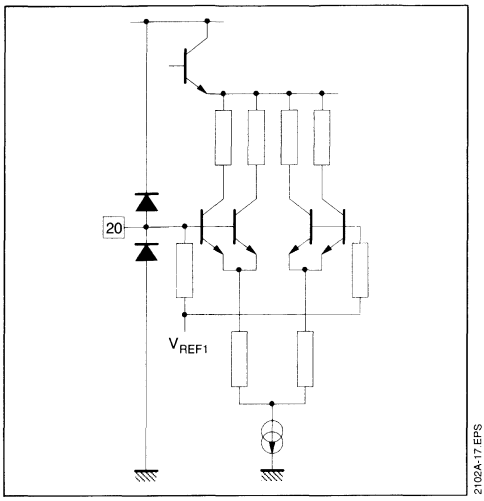


Figure 16 : Pin 21 (PS)

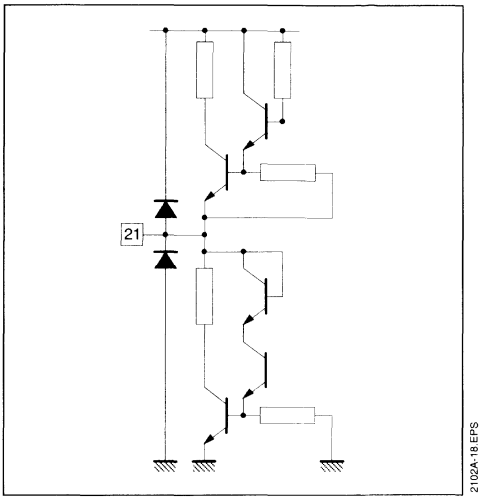


Figure 17 : Pin 18 (PALIN)

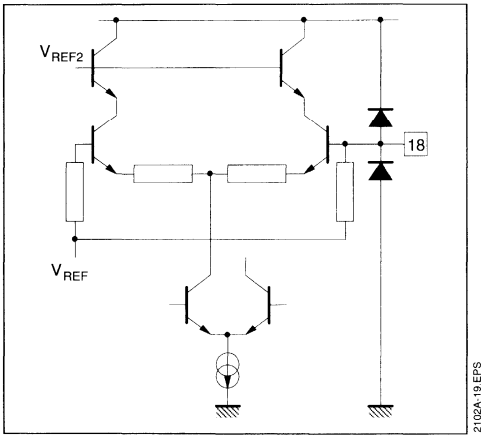


Figure 18 : Pin 32 (CKP)

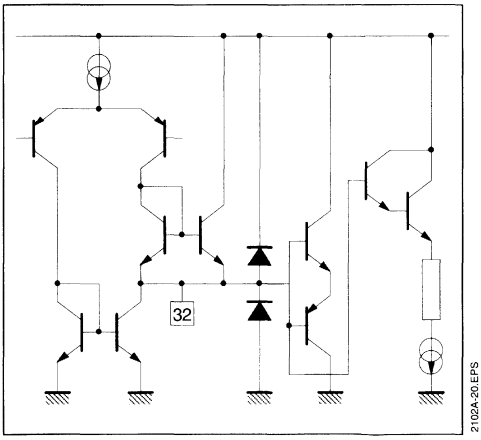


Figure 19 : Pin 22 (DLO)

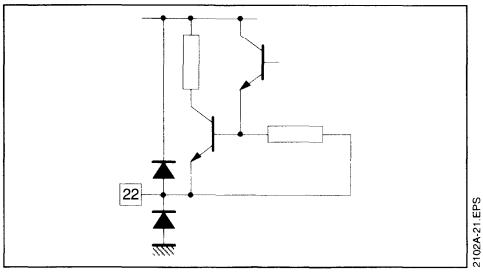


Figure 20 : Pin 36 (BRIG)

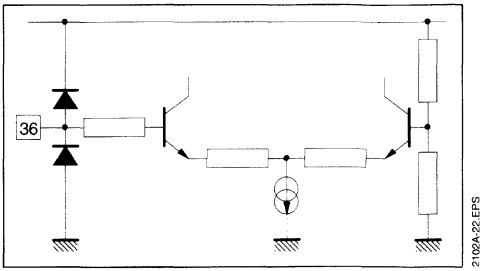


Figure 21 : Pin 30 (ACC)

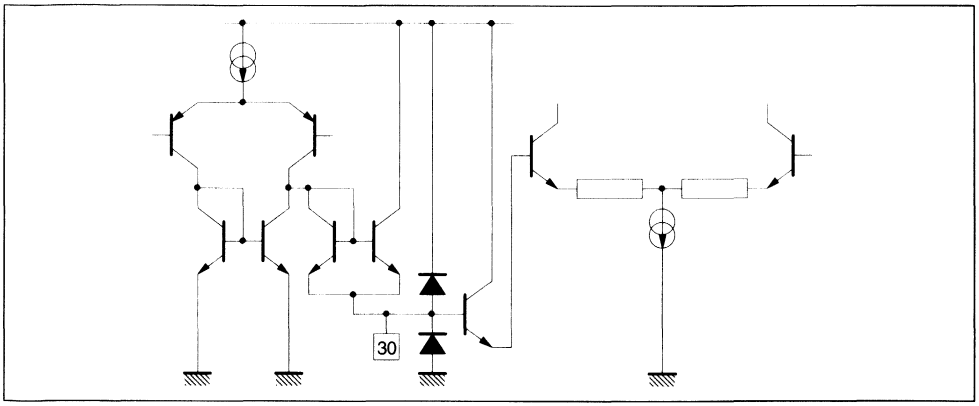


Figure 22 : Pin 33 (CXTL)

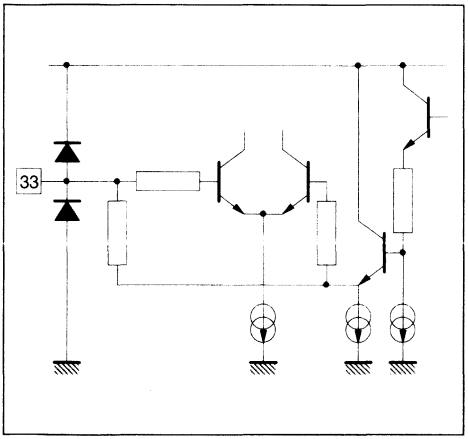


Figure 23 : Pin 34 (CLPF)

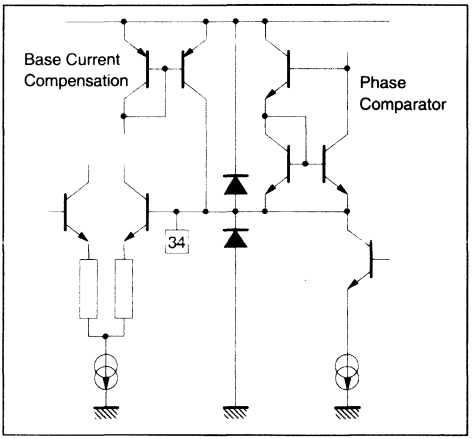
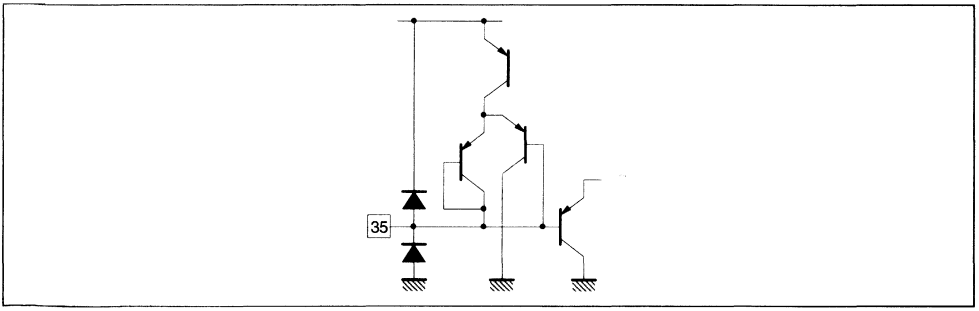
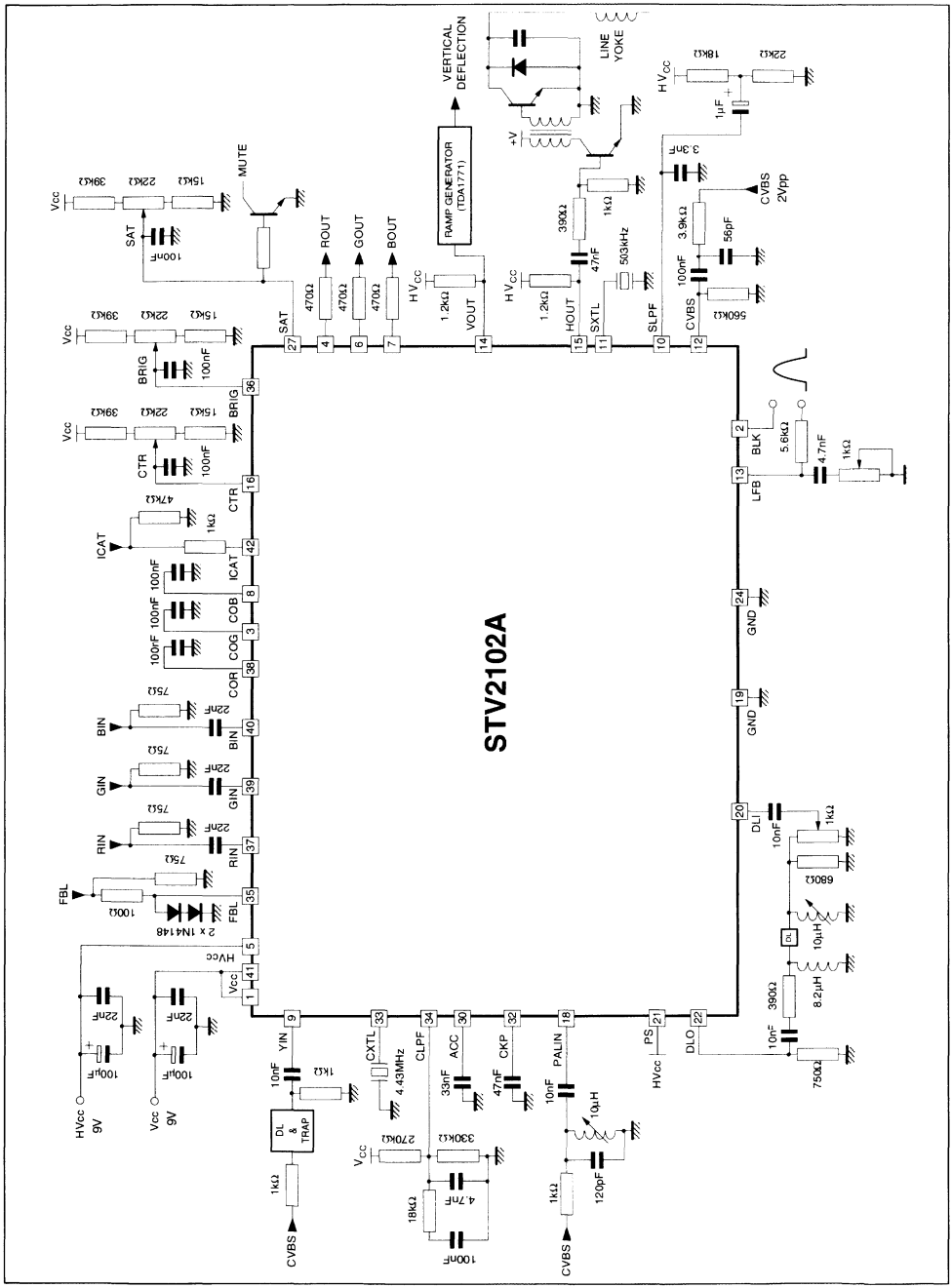


Figure 24 : Pin 35 (FBL)



APPLICATION DIAGRAM



2102A-27.EPS

SGS-THOMSON MICROELECTRONICS

STV2110A

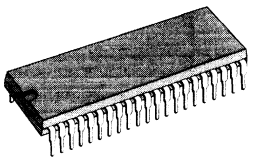
PAL-SECAM LUMA-CHROMA & DEFLECTION PROCESSOR

PRELIMINARY DATA

- RGB AND FAST BLANKING INPUTS
- AUTOMATIC CUT-OFF CONTROL
- DC-CONTROLLED BRIGHTNESS, CONTRAST AND SATURATION
- CERAMIC 500kHz VCO FOR LINE DEFLECTION
- CHROMA STANDARD AUTOMATIC IDENTIFICATION
- BIDIRECTIONAL I/O FOR CHROMA STANDARD
- PHASE-LOCKED REFERENCE OSCILLATOR USING A STANDARD 4.43MHz
- OSD CAPABILITY ON OUTPUTS
- VIDEO IDENTIFICATION GENERATOR

Used with the TDA8222, this IC permits a complete low cost solution with external output stages.

It is pin compatible with STV2102 PAL only processor.



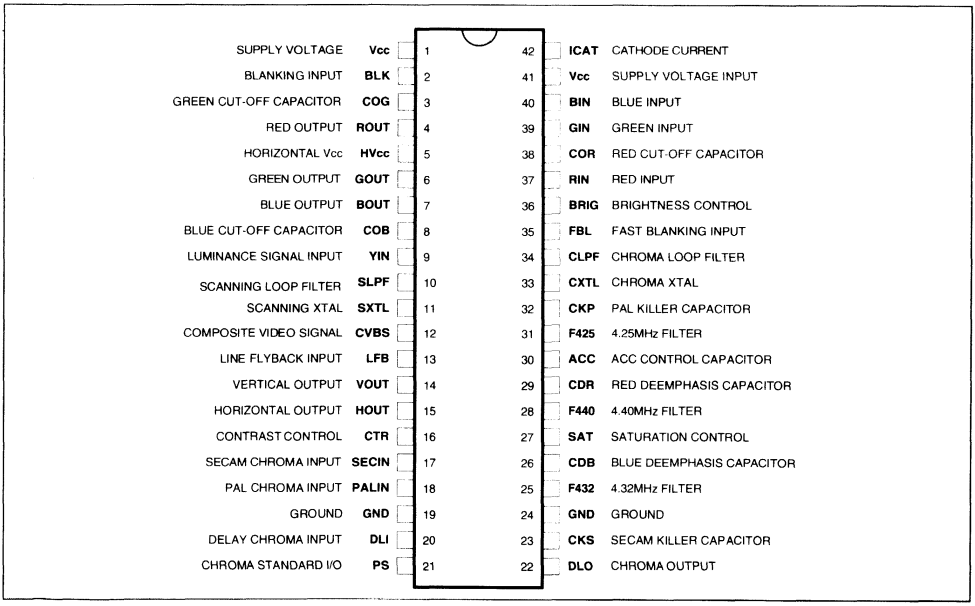
SHRINK 42
(Plastic Package)

ORDER CODE : STV2110A

DESCRIPTION

The STV2110A is a PAL-SECAM chroma decoder, video and H/V deflection processor for CTV.

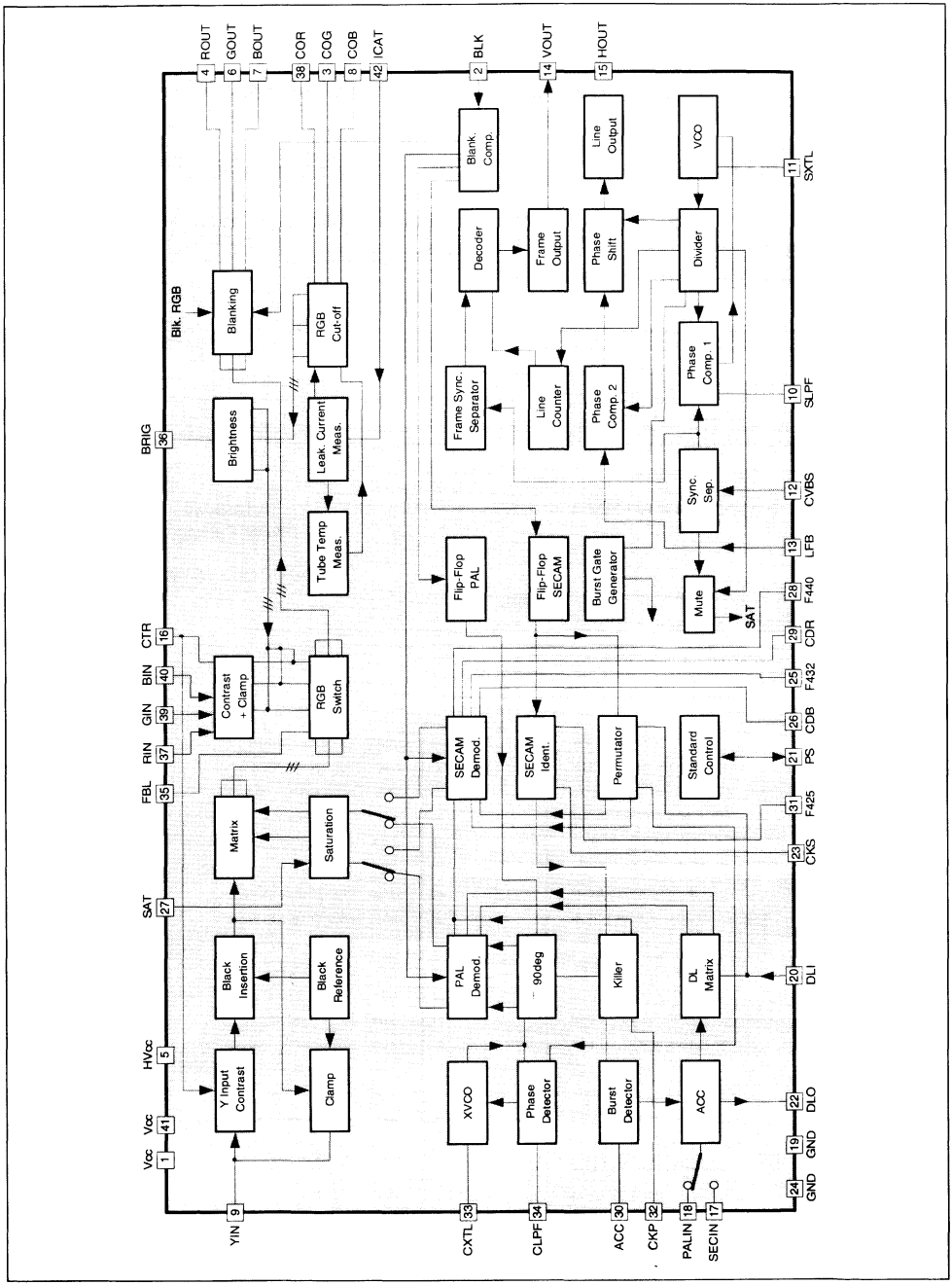
PIN CONNECTIONS



2110-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



2110-02.EPS

FUNCTIONAL DESCRIPTION

DEFLECTION

Synchronization Separator

The synchronization separator is based on the bottom of synchronization pulses alignment to an internal reference voltage. An external capacitor permits to align synchro. pulses, two external resistors determines the detection threshold of synchro pulses. The frame synchronization pulses are locked to a 32µs reference signal to perfect interlacing.

Horizontal Scanning

The horizontal scanning frequency is obtained from a 500kHz VCO. The circuit uses two phase-locked loops (PLL). The first one controls the frequency; the second one, fully integrated, controls the relative phase of the synchronization and the line flyback signals.

The first PLL has two times constants : a long time constant during the picture to have a good noise immunity, a short time constant at the beginning of the frame to recapture faster the phase in case of VCR video signal. More over, the PLL is in short time constant three lines before frame pulses occured, it permits to ensure good interlacing when the video signal comes from a VCR tape with high phase error.

The horizontal output signal is 28µs width. On starting up, horizontal pulses are enabled at V_{CC} = 6.8V. On shutting down, horizontal pulses are inhibited for V_{CC} = 6.2V.

Vertical Scanning

The windows for the frame sync detection are generated by a count down system. The selection of the windows is determined by the IC status :

- video identification off - window : 248/314
- video identification on - window : 248/352

When a sync pulse is detected inside the window a 10.5 lines long pulse is provided to V_{OUT} pin.

The count down system provides also the needed signals for the time constant switch, the line PLL inhibition and service signals to the rest of the IC.

CHROMA

ACC Amplifier, DL Matrix, Permutator and Demodulator

The correct chroma subcarrier input, issued from bandpass or bell filter, is internally selected with the standard. The ACC amplifier envolves three stages : the first one select the correct input, the second one the -6dB in picture (PAL mode), the third one is controled by the ACC voltage.

The dynamic range is over than 30dB.

The chrominance output signal is fed to the delay line.

- PAL mode :
  the adding and substracting direct and delayed signals are performed by the DL matrix function. Two synchronous demodulators multiplies the (B-Y) signal with the 0 degree phase 4.43MHz reference signal and the (R-Y) signal with the alternate ± 90 deg. 4.43MHz phase reference signal.
- SECAM mode :
  the permutator separates the two (B-Y) and (R-Y) subcarriers. These signals are demodulated by two FM demodulators with two external L, C centered on $f_{O(blue)}$ = 4.25MHz and $f_{O(red)}$ = 4.406MHz.

4.43MHz Phase Locked Loop

The oscillating frequency of the 4.43MHz crystal oscillator is controlled by the output voltage of the loop filter. The phase detector will lock the 90 degree reference signal to the direct burst signal. A 90 degree phase shifter permits to recover the 0 degree reference signal. A flip-flop driven by line pulses permits to generate the alternate ± 90 degree signal.

ACC Control and Color Killer

PAL mode :
the direct burst signal is demodulated with the ± 90 degree reference signal. The demodulation result is used by ACC control and killer function.

SECAM mode :
ACC control is done by a X^2 demodulator. For identification the burst signals of the red and blue lines are demodulated by the external LC connected on Pin 31, it is centered at 4.32MHz. This give positive and negative signals which are inverted by the signal coming out of the SECAM flip-flop.

In both standard, if the demodulation result is always positive, the killer capacitor is charged and the standard is identified (color ON). When demodulation result is always negative, the killer capacitor voltage reaches the flip-flop inhibition level, so the alternace sequence is reversed and the capacitor is charged again.

In case of no video signal, both killer capacitors voltage are maintained about $V_{CC}/2$, below the color off threshold.

In PAL or SECAM, the ACC control voltage is obtained by the peak detection of the demodulated burst.

Automatic Standard Identification

The circuit is alternately forced in each mode during two fields (PAL mode, SECAM mode disabled or SECAM mode, PAL mode disabled).

If PAL signal is identified, the alternate PAL/SECAM sequency is locked in PAL mode.

To have a SECAM identification, the circuit must memorizes a first SECAM identification, than test the PAL mode and confirm a second SECAM identification. The SECAM identification will take from four to six fields.

Output Pin 21, named PS, is high level in PAL mode and low level in SECAM mode.

Forced standard : Pin 21 can be used for the purpose :
- Pin 21 to HVCC : PAL mode
- Pin 21 to ground : SECAM mode

VIDEO

Input Stage

The luminance input is controlled by the contrast control stage which range is 20dB.

The luminance and color difference signals are added in the video matrix circuit to obtain the color signals.

The color signals are sent to an RGB switch which will drive to the outputs either internal RGB signals or external RGB signals.

Automatic Cut-off Control

The black levels of the RGB outputs are controlled with the cut-off loops during three line periods after the frame retrace. The cut-off measurements are sequentially achieved during these three lines. The leakage current measurement is achieved during the frame retrace and memorized on an internal capacitor, thus the circuit is able to extract the cut-off current from the total current measurement.

Warm-up Detector

At the start-up, the cut-off loops are switch off, a white level is inserted on the luminance signal until a cathode current is detected. Then the cut-off loops are released.

RGB Inputs

To avoid the black level of the inserted signal differing from the black level of the normal video signal, the external RGB are clamped to the black level of the luminance signal. Therefore, an AC coupling is required for the RGB inputs.

The RGB inputs are controlled by a 12dB range contrast control stage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
HV_{CC}	Horizontal Supply Voltage (Pin 5)	12	V
V_{CC}	Video & Chroma Supply Voltage (Pins 1-41)	HV_{CC} + 0.5	V
H_{OUT}	Horizontal Output (Pin 15)	12	V
T_{stg}	Storage Temperature	-55, +150	°C
T_{oper}	Operating Temperature	0, +70	°C

2110-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	60	°C/W

2110-02.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HV_{CC}	Scanning Supply Voltage (Pin 5)		8.1	9	9.9	V
V_{CC}	Video & Chroma Supply Voltage (Pins 1-41)		8.1	9	9.9	V
I_{cch}	Scanning Supply Current (pin 5)	No load		25	35	mA
$I_{ccv\&c}$	Video & Chroma Supply Current (Pins 1-41)	No load		45	55	mA
P_D	Total Power Dissipation	No load		630	890	mW

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

($HV_{CC} = V_{CC} = 9V$, $T_{amb} = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LUMINANCE INPUT (Pin 9)						
V_{BW9}	Input Voltage			350	490	mV_{PP}
V_{DC9}	DC Level	No input signal		2.6		V
I_g	Input Current	• During burst period • Out of burst period		±150	1	µA µA
G_9	Luma Gain			7.4		
BW467	Bandwidth (Y to R, G, B outputs)	-3dB		6		MHz
CONTRAST CONTROL (Pin 16)						
V_{16}	Contrast Control Voltage			2 to 4		V
$V_{16\,(Max.)}$	Allowed Control Voltage				5	V
G_{16}	Contrast Control Range			20		dB
I_{16}	Input Current				10	µA
BRIGHTNESS CONTROL (Pin 36)						
V_{36}	Brightness Control Voltage			1.8 to 4.3		V
$V_{36\,(Max.)}$	Allowed Control Voltage				5	V
I_{36}	Input Current				10	µA
SATURATION CONTROL INPUT (Pin 27)						
V_{27}	Saturation Control Voltage			2 to 4		V
$V_{27\,(Max.)}$	Allowed Control Voltage				5	V
G_{27}	Saturation Control Range			-50		dB
V_{27M}	Mute Level				0.5	V
I_{27}	Input Current				10	µA
RGB OUTPUTS (Pins 4-6-7)						
$V_{BW\ 4\text{-}6\text{-}7}$	Output Signal Amplitude (black to white)	• 0.35V B to W @ Pin 9 • Contrast @ 4V • Sat. & Brig. @ 3V		2.6		V
$I_{4\text{-}6\text{-}7}$	Individual Output Sinking Current			2		mA
$VM_{4\text{-}6\text{-}7}$	Maximum Peak White Level			7.8		V
$V_{blank\ 4\text{-}6\text{-}7}$	Blanking Level			0.5		V
$V_{CO\ min.}$	Minimum Level of Inserted Cut-off Lines			2.5		V
$V_{CO\ max.}$	Maximum Level of Inserted Cut-off Lines			4.5		V
	Relative Variation in Black Level with Various CONT. SAT. BRIG between the 3 channels				20	mV
ΔV_{temp}	Black Level Thermal Drift			0.5		mV/°C
	Tracking between Luminance and Chrominance Signals over 10dB Contrast Control				2	dB
RGB INPUTS (Pins 37-39-40)						
$V_{BW37\text{-}39\text{-}40}$	Input Amplitude (B to W)			0.7	2	V
$V_{clamp\ 37\text{-}39\text{-}40}$	Clamp Level	Contrast max		1.8		V
$I_{37\text{-}39\text{-}40}$	Control Current			±150		µA
$I_{i37\text{-}39\text{-}40}$	Leakage Current				1	µA
$BW_{37\text{-}39\text{-}40}$	Bandwidth	-3dB		8		MHz
G_{CTR}	RGB Contrast Control Range			14		dB
$G_{37\text{-}39\text{-}40}$	RGB Gain			3.7		

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

($HV_{CC} = V_{CC} = 9V$, $T_{amb} = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FAST BLANKING INPUT (Pin 35)						
V_{TH1-35}	First Threshold (switching)			0.7		V
V_{TH2-35}	Second Threshold (blanking)			2.1		V
T_{switch}	Switching Delay			50		ns
T_{blank}	Blanking Delay			100		ns
CATHODE CURRENT INPUT (Pin 42)						
V_{REF42}	Leakage Current Reference Voltage			1.75		V
ΔV_{REF42}	CO Reference refered to Leakage Current Reference			250		mV
I_{42}	Output Current		150			µA
V_{sb42}	Start-beam Current Detection Reference Voltage			2.4		V
AUTOMATIC CUT-OFF (Pin 3-8-38)						
	Cut-off Capacitor Clamping Current			± 100		µA
PAL CHROMINANCE INPUT (Pin 18)						
V_{18}	Input Level			0.3	1.0	V_{PP}
$V_{burst-18}$	Minimum Burst Signal Amplitude within the ACC Control Range			30		mV_{PP}
G_{ACC}	ACC Control Range	Change of burst over whole ACC Control Range < 1dB		30		dB
R_{18}	Input Impedance			8		kΩ
V_{DC-18}	DC Level	No input signal		3.5		V
SECAM CHROMINANCE INPUT (Pin 17)						
V_{17}	Input Level			0.3	1.0	V_{PP}
$V_{burst-17}$	Minimum Burst Signal Amplitude within the ACC Control Range			30		mV_{PP}
R_{17}	Input Impedance			20		kΩ
V_{DC-17}	DC Level	No input signal		3.5		V
ACC CAPACITOR (Pin 30)						
I_{30}	Charging Current	During burst gate period		250		µA
I_{i30}	Leakage Current	Out of burst gate period			1	µA
PLL LOOP FILTER (Pin 34)						
I_{34}	Control Current			400		µA
CHROMAXTAL (Pin 33)						
CR_{33}	Catching Range			±700		Hz
SUBCARRIER OUTPUT (Pin 22)						
$V_{burst-22}$	Output Burst Amplitude (PAL mode)	Within ACC Control Range		2		Vpp
PAL KILLER CAPACITOR (Pin 32)						
V_{OFF-32}	Color off Threshold			5.0		V
V_{ON-32}	Color on Threshold			5.4		V
V_{INH-32}	PAL Flip-flop Inhibition Level			3.2		V
I_{32}	Control Current			250		µA
V_{nom-32}	Voltage with Nominal Input Signal			6.0		V

2110-05.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SECAM KILLER CAPACITOR (Pin 23)						
V_{OFF-23}	Color off Threshold			5.6		V
V_{ON-23}	Color on Threshold			6		V
V_{INH-23}	SECAM Flip-flop Inhibition Level			3.2		V
I_{23}	Control Current			250		µA
V_{nom-23}	Voltage with Nominal input Signal			7.3		V
DELAYED CHANNEL INPUT (Pin 20)						
V_{DC-20}	DC Level	No input Signal		2.2		V
R_{20}	Input Impedance	PAL standard SECAM standard		8 20		kΩ kΩ
4.25MHz AND 4.40MHz FILTER (Pins 28-31)						
$V_{DC\ 28-31}$	DC Level	No input signal		2.3		V
R_{28-31}	Input Impedance			20		kΩ
RED AND BLUE DEEMPHASIS CAPACITORS (Pins 26-29)						
$V_{DC-26-29}$	DC Level	No input signal		6.4		V
R_{26-29}	Input Impedance			6		kΩ
4.32MHz FILTER (Pin 25)						
V_{DC-25}	DC Level	No input signal		3.5		V
R_{25}	Input Impedance			40		kΩ
FORCING/STANDARD IDENTIFICATION (Pin 21)						
	Max.Current on PS Output	PAL SECAM	+ 5 - 5			mA mA
	DC Output Voltage	PAL SECAM		7.5 1.5		V V
	DC input Voltage	PAL SECAM		HV_{CC} 0.0		V V
COMPOSITE VIDEO BASE BAND SIGNAL (Pin 12)						
V_{REF-12}	Clamp Voltage	I_{12} = - 1µA	1.6	1.85	2.1	V
V_{12}	Video Input Signal (sync to white)			1		V_{PP}
I_{12}	Sync Threshold			12		µA
SCANNING XTAL (Pin 11)						
F_{11}	Frequency after Divider			15.625		kHz
CR_{11}	Frequency Control Range after Divider			±700		Hz
PLL LOOP FILTER (Pin 10)						
I_{low-10}	Output Current	Long time constant		0.15		mA
$I_{high-10}$	Output Current	Short time constant		0.40		mA
DELAYED LINE FLYBACK INPUT (Pin 13)						
V_{TH-13}	Threshold			0.6		V
V_{13}	Allowed Voltage Range		- 0.4		HV_{CC}	V
I_{13}	Input Current	V_{13} < 0.6V			5	µA

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(HV_{CC} = V_{CC} = 9V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIRECT BLANKING INPUT (Pin 2)						
V_{TH-2}	Threshold			0.6		V
V_2	Allowed Voltage Range		- 0.4		HV_{CC}	V
I_2	Input Current	V_2 < 0.6V			5	µA
HORIZONTAL OUTPUT (Pin 15)						
T_{15}	Output Pulse Width		26	28	29	µs
V_{low-15}	Output Voltage (open collector)	I_{15} = 10mA		1.5		V
$V_{5\ start}$	HV_{CC} Start Threshold			6.8		V
$V_{5\ stop}$	HV_{CC} Stop Threshold			6.2		V
Δt_{15}	φ2 Phase Range			12		µs
VERTICAL OUTPUT (Pin 14)						
T_{14}	Output Pulse Width			10.5		line
T_{sync1}	Frame Synchro. Window (search)			248 to 352		line
V_{low-14}	Output Voltage (open collector)			1		V

2110-07.TBL

Figure 1 : Contrast Control Curve

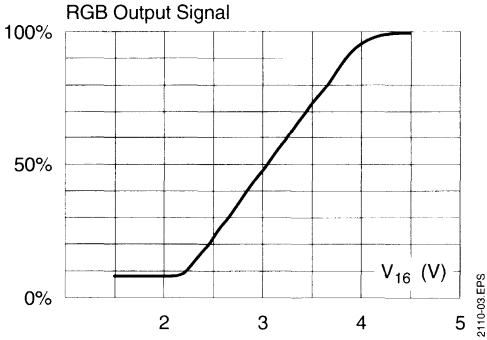


Figure 2 : Saturation Control Curve

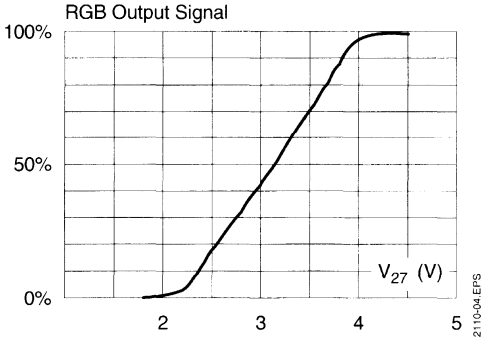


Figure 3 : Difference between Black Level and measuring Level at RGB Outputs as a function of the Brightness Control Input

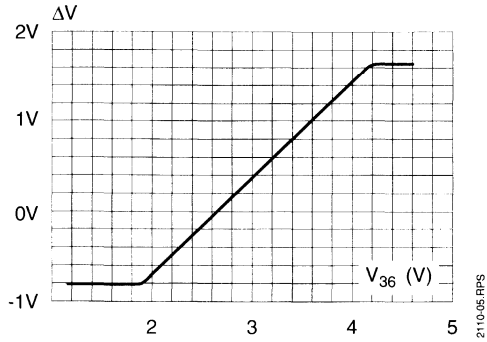


Figure 4 : Pins 3-8-38-42 (COG, COB, COR, ICAT)

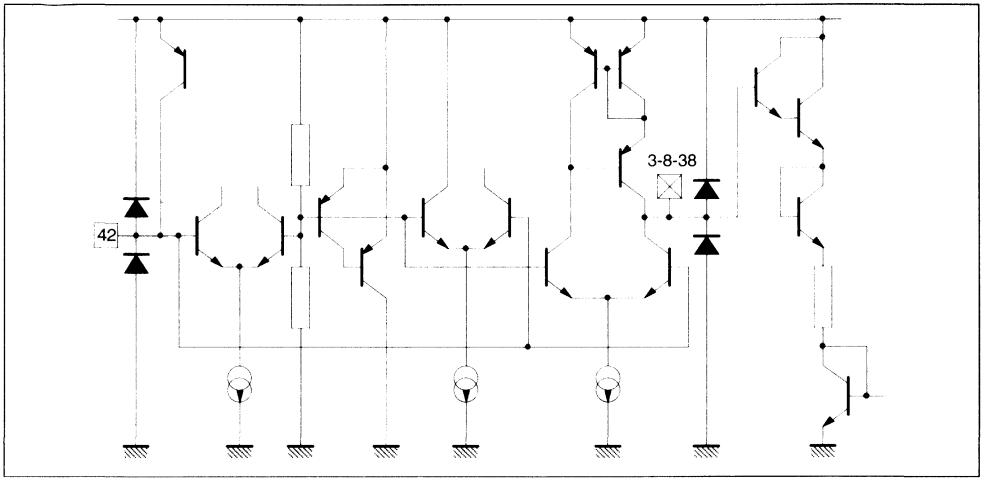


Figure 5 : Pins 37-39-40 (RIN, GIN, BIN)

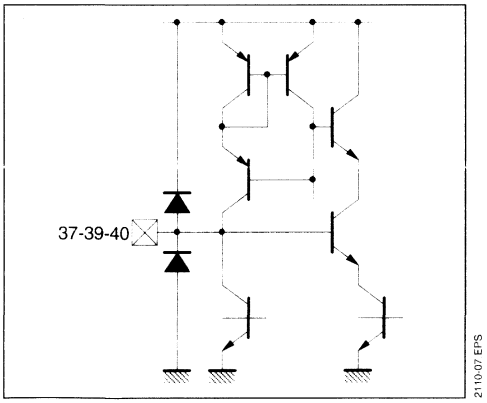


Figure 6 : Pins 4-6-7 (ROUT, GOUT, BOUT)

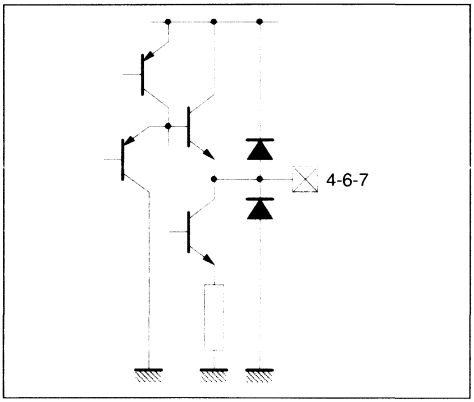


Figure 7 : Pin 9 (YIN)

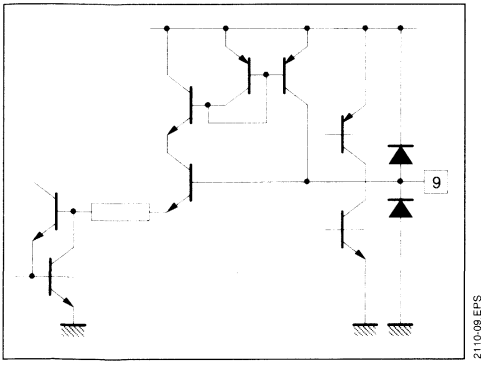


Figure 8 : Pin 10 (SLPF)

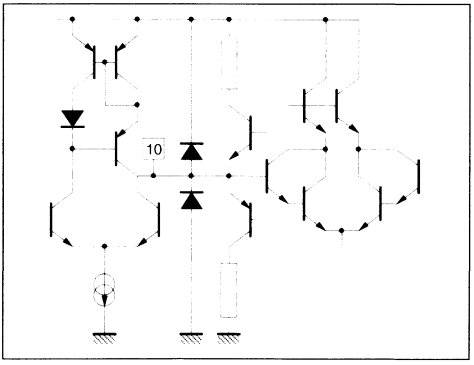


Figure 9 : Pin 11 (SXTL)

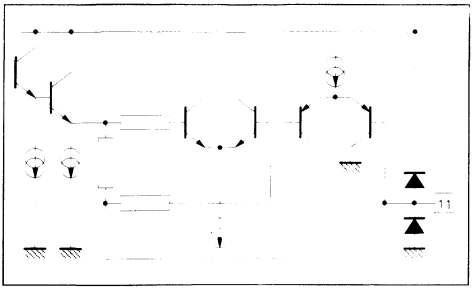


Figure 10 : Pin 12 (CVBS)

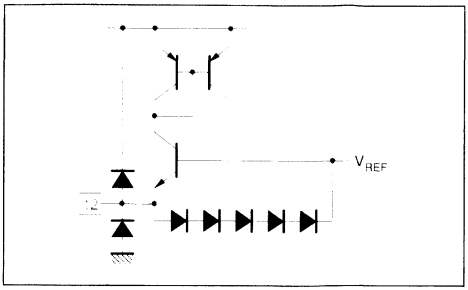


Figure 11 : Pins 2-13 (BLK, LFB)

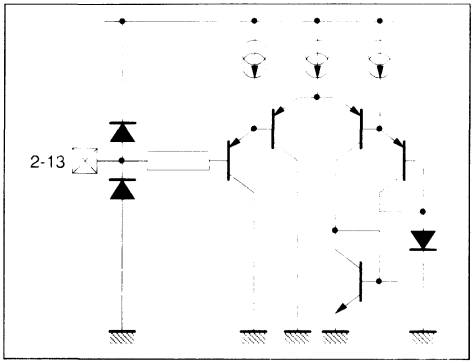


Figure 12 : Pins 14 (VOUT)

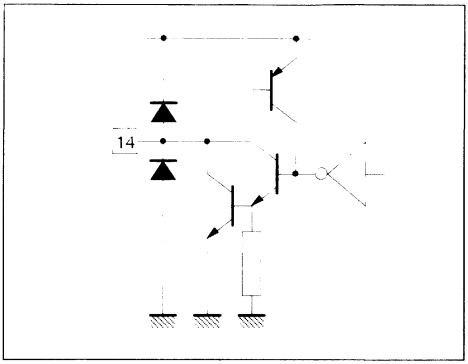


Figure 13 : Pin 15 (HOUT)

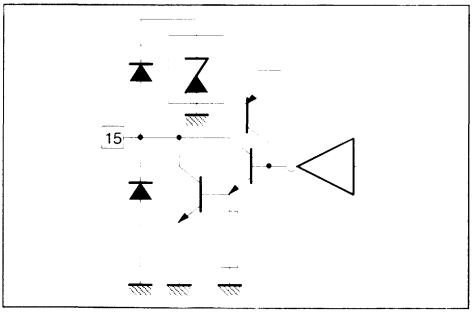


Figure 14 : Pins 16-27 (CTR, SAT)

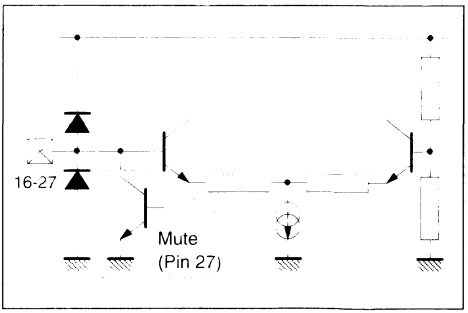


Figure 15 : Pin 20 (DLI)

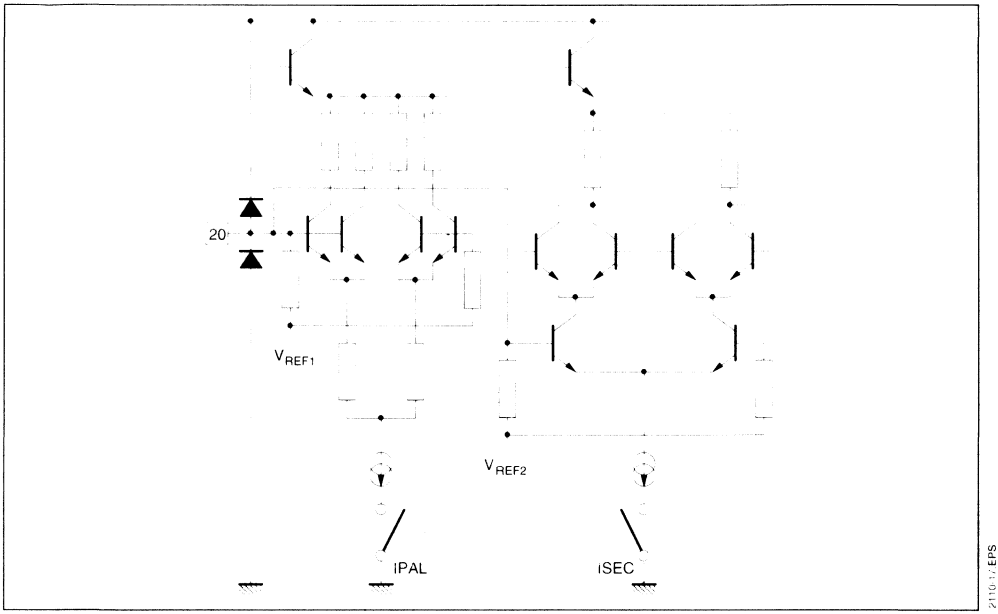


Figure 16 : Pin 21 (PS)

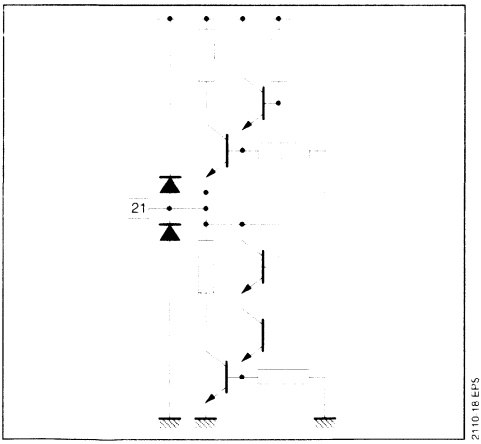


Figure 17 : Pin 25 (F432)

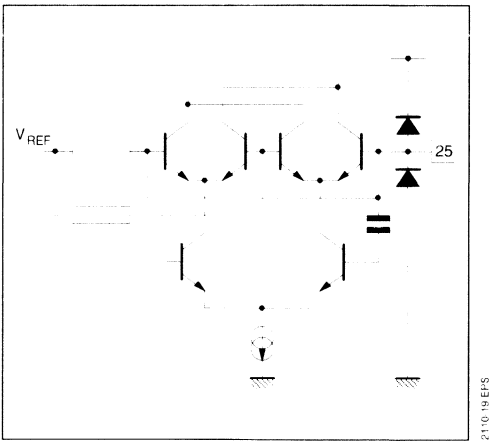


Figure 18 : Pins 17-18 (SECIN, PALIN)

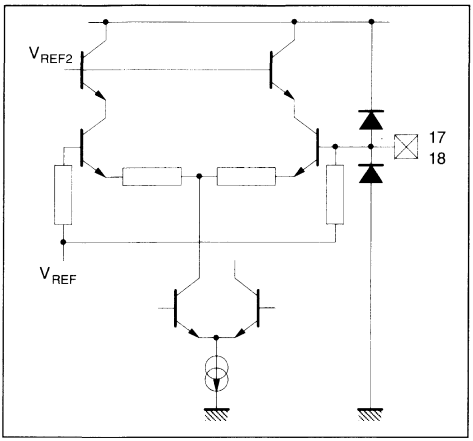


Figure 19 : Pins 28-31 (F440, F425)

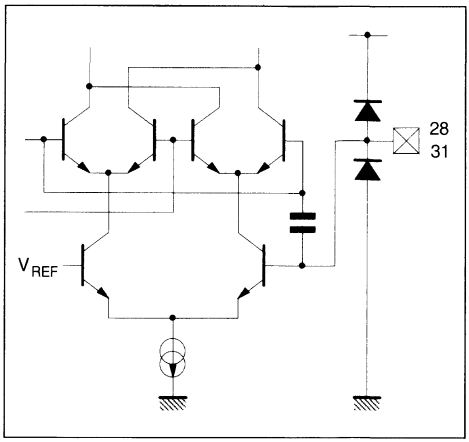


Figure 20 : Pins 26-29 (CDB, CDR)

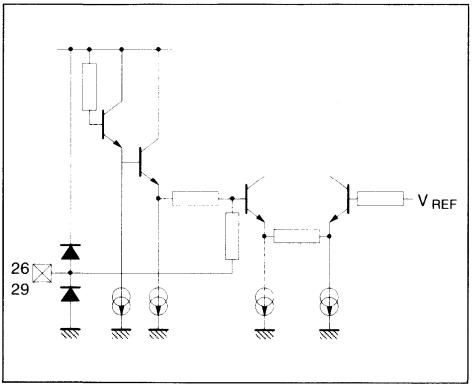


Figure 21 : Pins 23-32 (CKS, CKP)

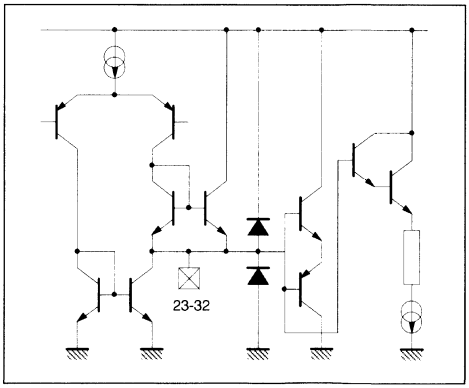


Figure 22 : Pin 22 (DLO)

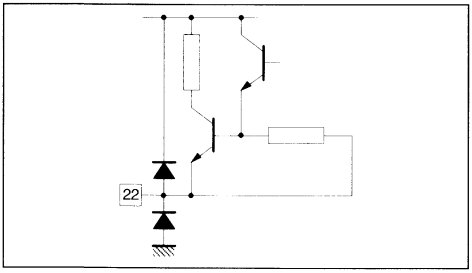


Figure 23 : Pin 36 (BRIG)

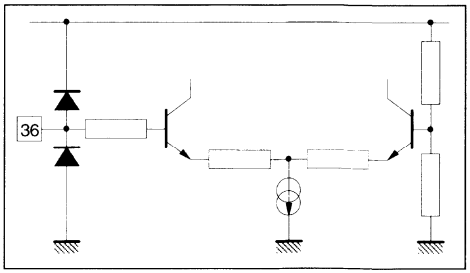


Figure 24 : Pin 30 (ACC)

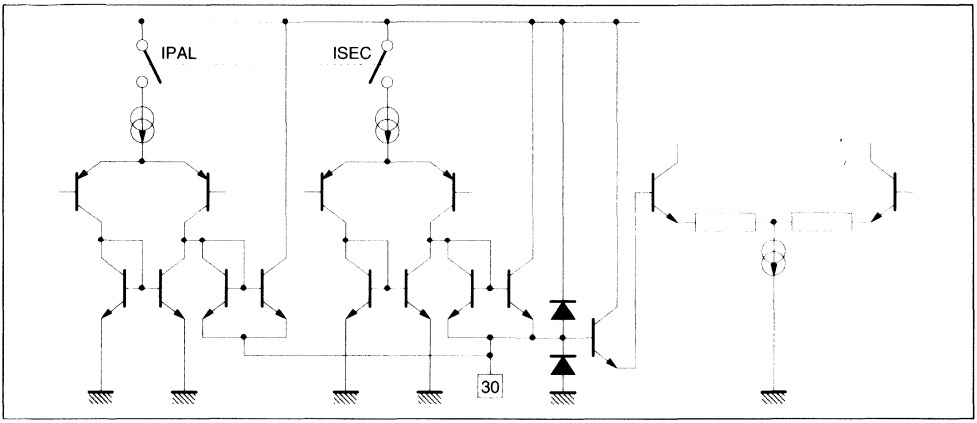


Figure 25 : Pin 33 (CXTL)

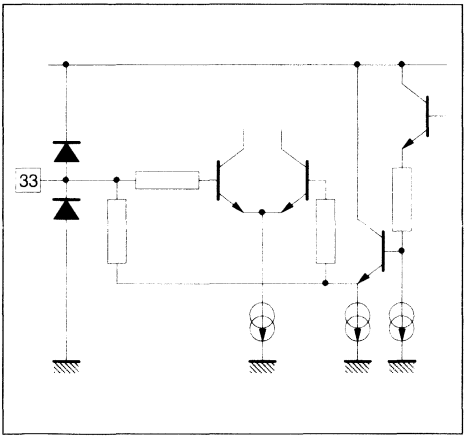


Figure 26 : Pin 34 (CLPF)

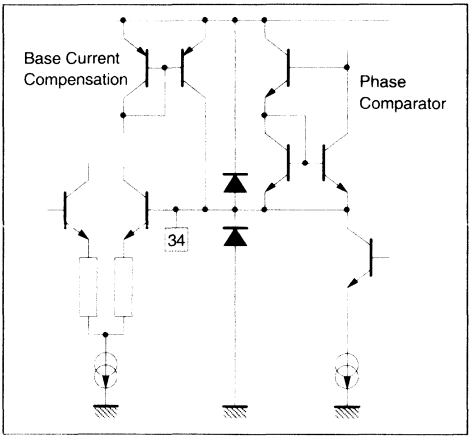
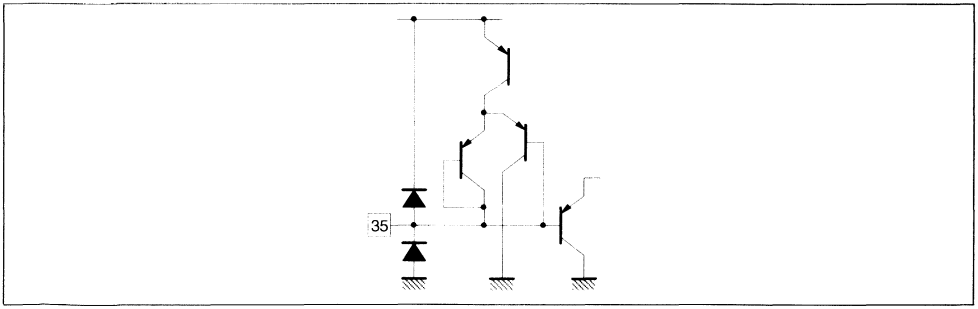
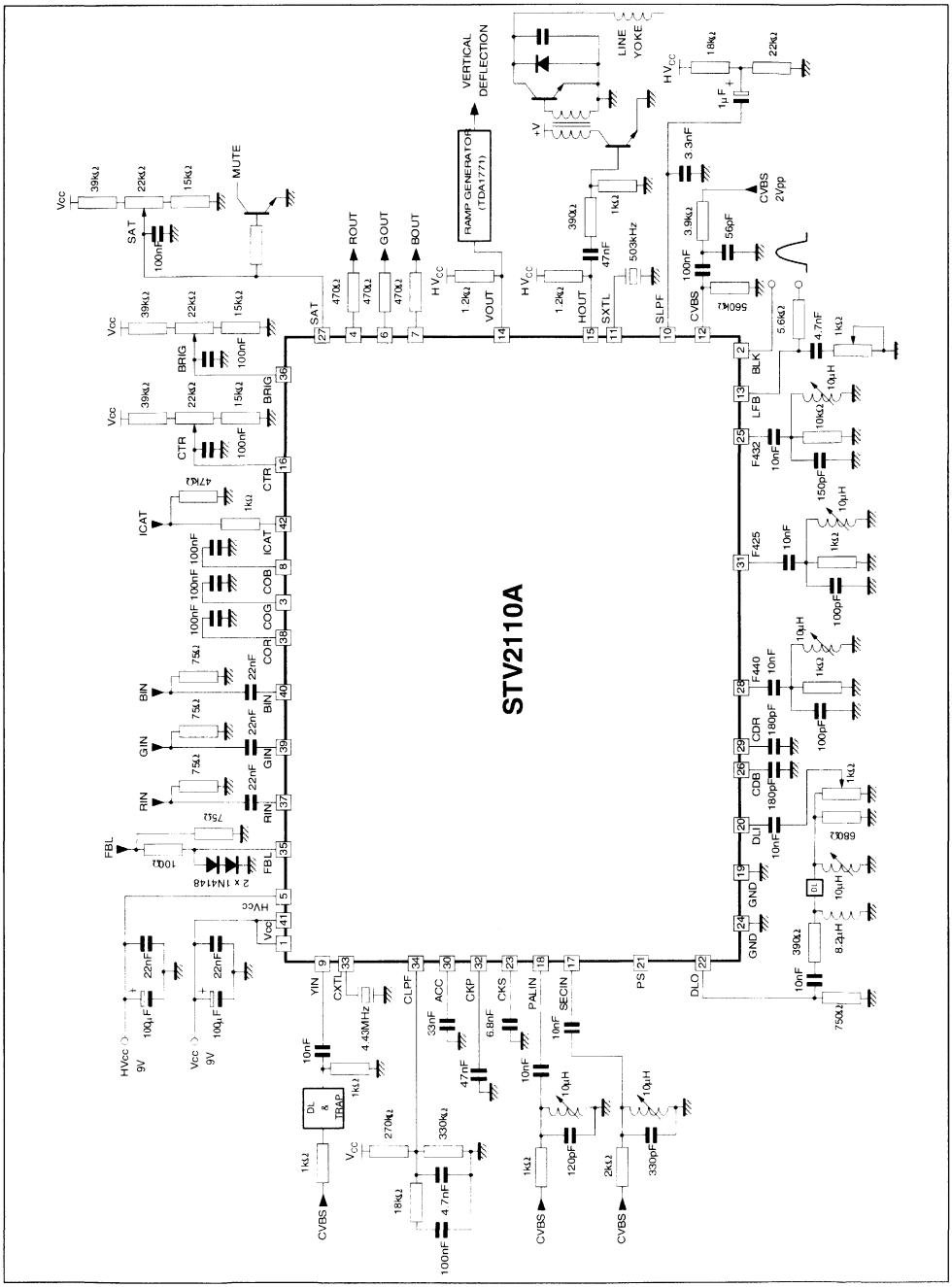


Figure 27 : Pin 35 (FBL)



APPLICATION DIAGRAM



2110-30.EPS

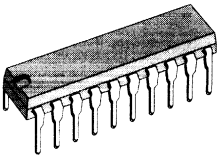
INTERMEDIATE FREQUENCY (IF)

SGS-THOMSON MICROELECTRONICS

TDA8190

TV SOUND CHANNEL WITH DC CONTROLS

- SEPARATE VCR INPUT AND OUTPUT PINS
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION



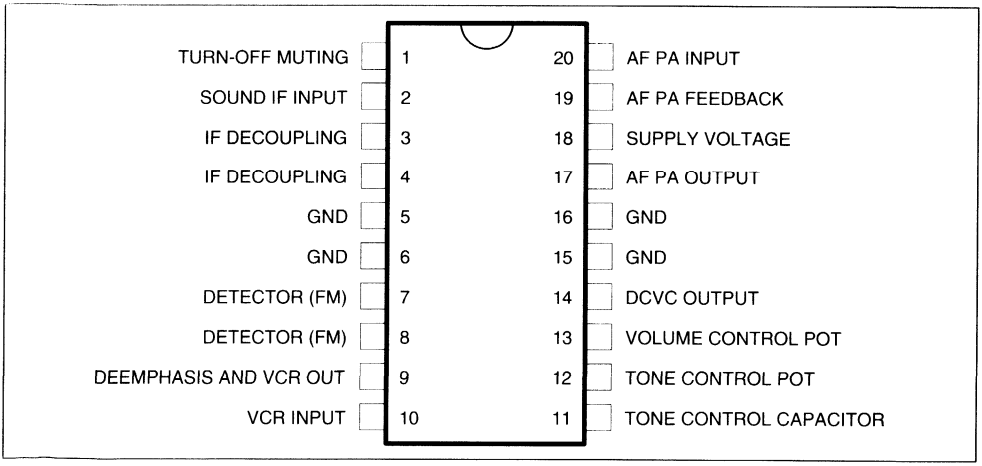
DIP20
(Plastic Package)

ORDER CODE : TDA8190

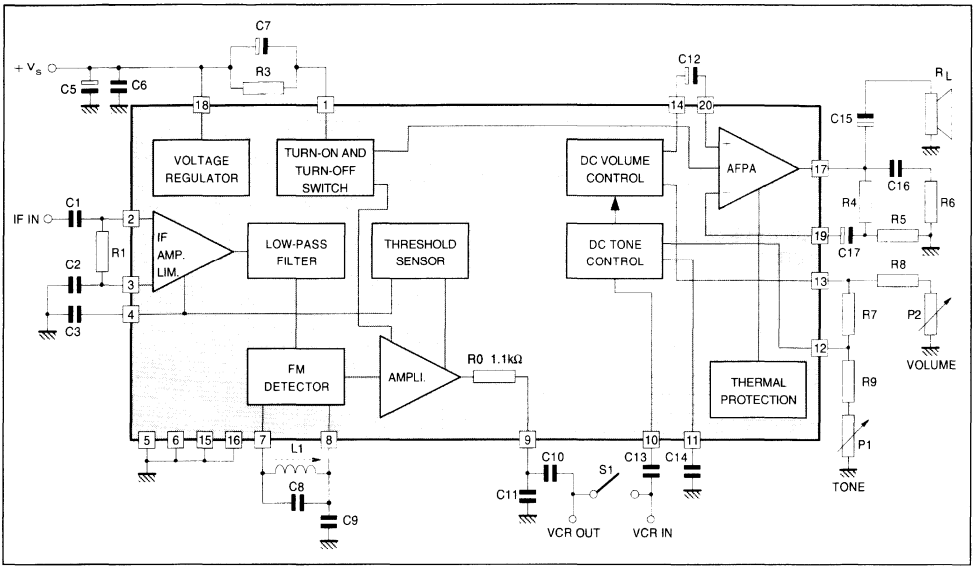
DESCRIPTION

The TDA8190 is a complete TV sound channel with DC tone and volume controls plus separate VCR input and output connections. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA8190 are : IF amplifier limiter, active low-pass filter, AF pre-amplifier and power amplifier, turn-off muting, mute circuit and thermal protection. High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 18)	28	V
V_l	Voltage at Pin 1	$\pm V_s$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg} - T_j	Storage and Junction Temperature	– 40 to 150	°C

8190-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W*

8190-02.TBL

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 24V, S1 : on, $\Delta f = \pm$ 25kHz, V_i = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_s	Supply Voltage (pin 18)	P_2 = 12kΩ	10.8		27	V
V_o	Quiescent Output Voltage (pin 17)	P_2 = 12kΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12kΩ, R_1 = 270kΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12kΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12kΩ		32		mA
IF AMPLIFIER AND DETECTOR						
$V_{i\,(threshold)}$	Input Limiting Voltage at Pin 2 (–3dB)	V_o = 4 V_{rms}		50	100	µV
V_9	Recovered Audio Voltage (pin 9)	$\Delta f = \pm$ 7.5kHz, P_2 = 12kΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3, V_i = 1mV, V_o = 4V_{RMS}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0, P_2 = 12kΩ		30		kΩ
C_i	Input Capacitance (pin 2)	Δf = 0, P_2 = 12kΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888nF	0.75	1.1	1.5	kΩ
DC VOLUME CONTROL						
K_v	Volume Attenuation (resistance control)	P_2 = 0Ω P_2 = 4.3kΩ P_2 = 12kΩ	20	0 26 88	32	dB dB dB
V_c	Control Voltage	K = 0dB K = 26dB K = 88dB		0 1.3 2.6		V V V
$\frac{\Delta K_V}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} = 25 to 85°C, P_2 = 4.3kΩ		– 0.05		dB/°C
DC TONE CONTROL						
K_T	Tone Cut	S1 : Off, V_{10} = 200 mV P_1 = 12kΩ to 100Ω, f_{AF} = 10kHz		14		dB
AUDIO FREQUENCY AMPLIFIER						
P_o	Output Power (d = 10 %)	V_s = 24 V, R_L = 16 Ω V_s = 12 V, R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3dB)	P_o = 1W, R_L = 16Ω, S1 : Off, V_{10} = 200mV, V_o = 4V_{RMS}, @400 Hz	15	50		kHz
SVR	Supply Voltage Rejection	P_2 = 12kΩ, Δf = 0, f_{ripple} = 120Hz		26		dB
V. C. R.						
d	Total Harmonic Distortion of Pin 9 Output Signal	$\Delta f = \pm$ 7.5kHz, V_i = 1mV		0.5		%
SVR	Supply Voltage Rejection at Output Pin 9	Δf = 0, f_{ripple} = 120Hz, P_2 = 12kΩ		66		dB
$\frac{S+N}{N}$	Signal to Noise Ratio at Output Pin 9	Δf = 25 kHz, $V_i \geq$ 1 mV		70		dB
V_{10}	Input Voltage (playback)	V_o = 4 V_{rms}, P_2 = 0, S1 : Off	50	70	100	mV
R_{10}	Input Resistance (playback)	S1 : Off	10			kΩ
	Total Harmonic Distortion for 20dB Overload of V_{10}	S1 : Off, V_{10} = 1V_{rms}, V_o = 4V_{rms}		0.5	3	%

8190-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

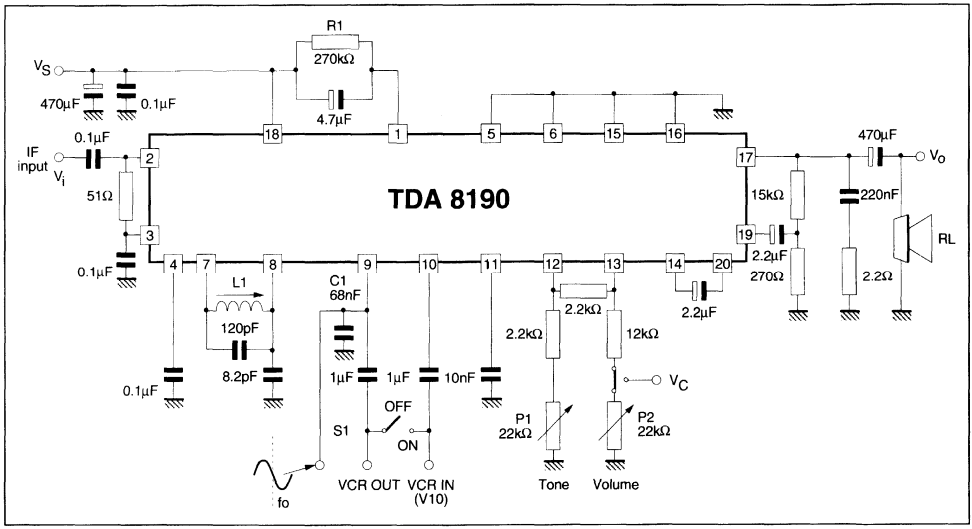
(refer to the test circuit, V_S = 24V, S1 : on, $\Delta f = \pm$ 25kHz, V_I = 1mV, P_1 = 12kΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OVERALL CIRCUIT						
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_i \geq$ 1mV, V_o = $4V_{rms}$, Δf = 0		70		dB
d	Distortion (*)	P_o = 50mW, $\Delta f = \pm$ 7.5Hz V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = $4V_{rms}$ @ no V_1 ; V_1 = 0	100			dB
Δf	Deviation Sensitivity	P_2 = 0, V_o = $4V_{rms}$		3	6	kHz

8190-04.TBL

* Test Bandwidth = 20kHz.

TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

V_S = 24V, Q_O = 60, f_O = 4.5MHz, V_{IN} = 1mV, f_m = 400Hz, Δf = ±25kHz, P_1 = 12kΩ, R_L = ∞, S1 = on

Figure 1 : Relative Audio Output Voltage and Output Noise versus Input Signal

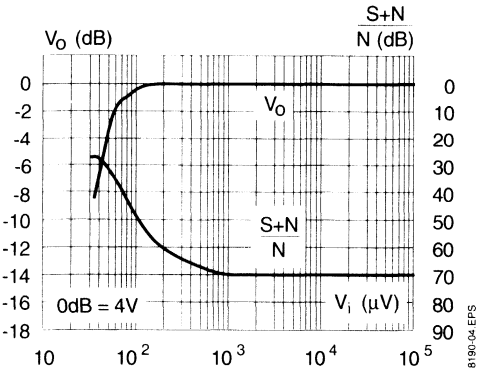


Figure 2 : Output Voltage Alternation versus DC Volume Control Resistance (a) or versus DC Volume Control Voltage (b)

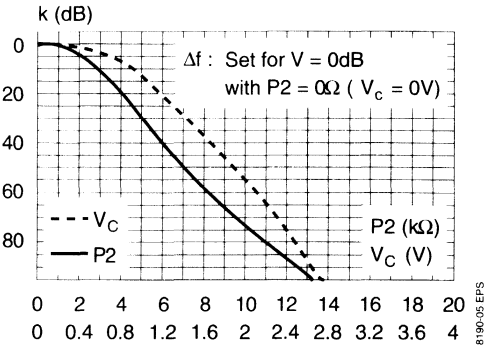


Figure 3 : DC Tone Control Cut-off the High Audio Frequencies for some Values of Resistance adjusted by P1

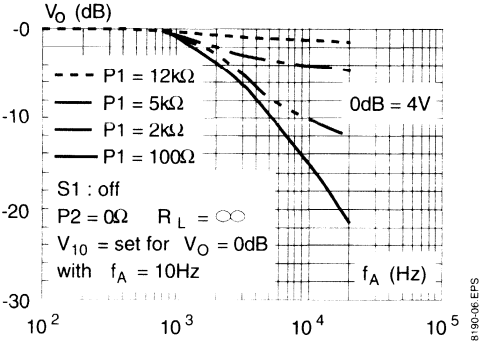


Figure 4 : Amplitude Modulation Rejection versus Input Signal

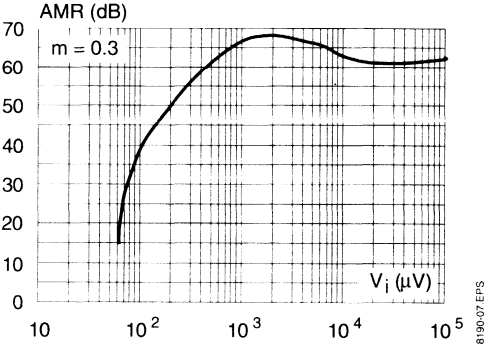


Figure 5 : ΔAMR versus Timing Frequency Change

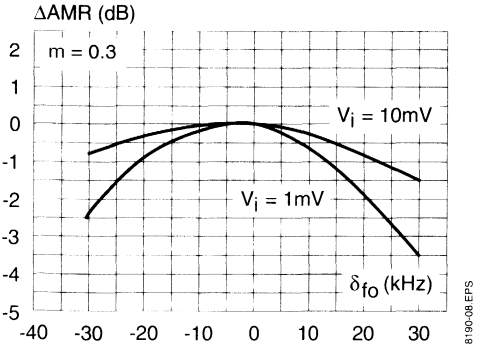


Figure 6 : Recovered Audio Voltage versus Unloaded Q-factor of the Detector Coil

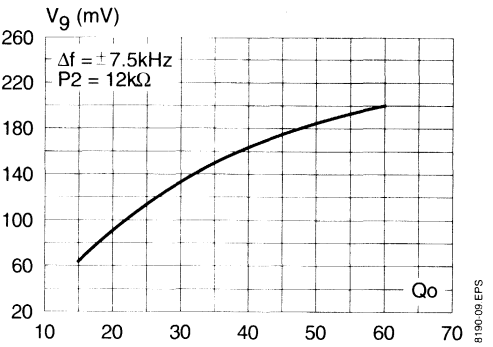


Figure 7 : Distortion versus Unloaded Q-factor of the Detector Coil

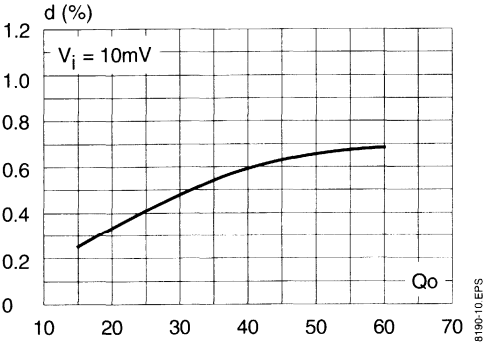


Figure 8 : Distortion versus Frequency Variation

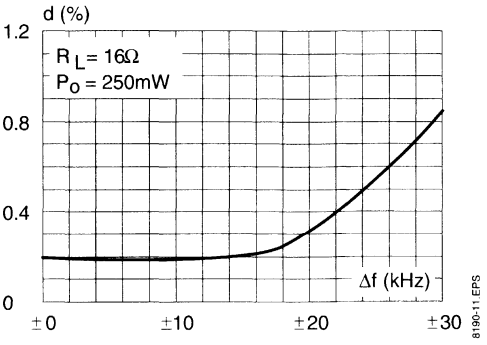


Figure 9 : Distortion versus Tuning Frequency Change

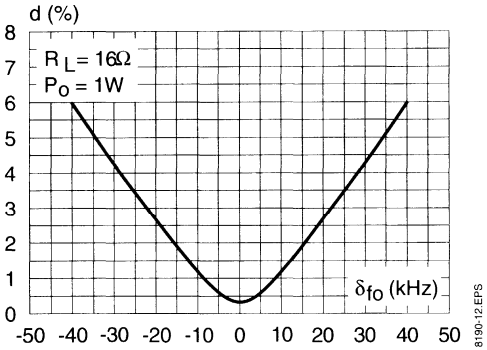


Figure 10 : Distortion versus Output Power

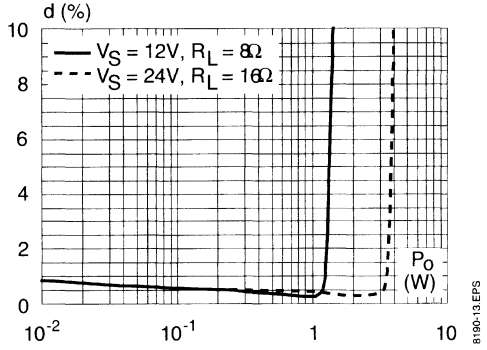


Figure 11 : Audio Amplifier Frequency Response

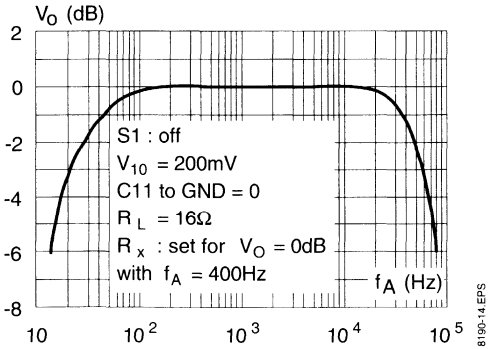


Figure 12 : Output Power versus Supply Voltage

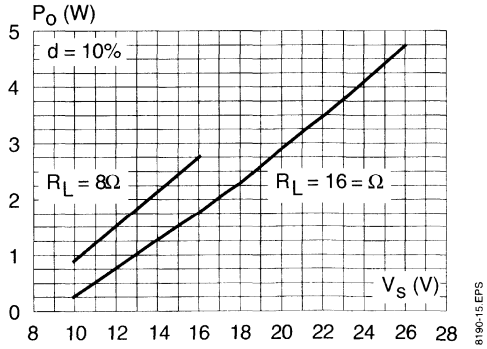


Figure 13 : Power Dissipation versus Supply Voltage (sine wave operation)

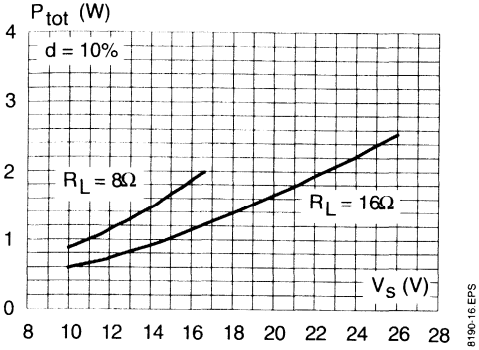


Figure 14 : Power Dissipation and Efficiency versus Output Power

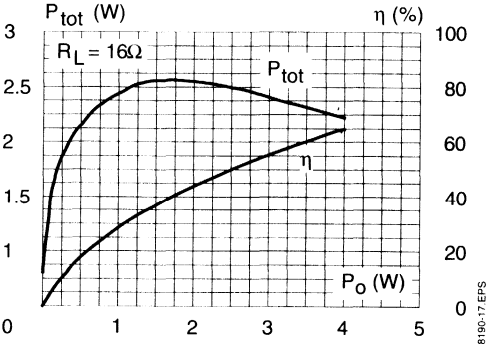
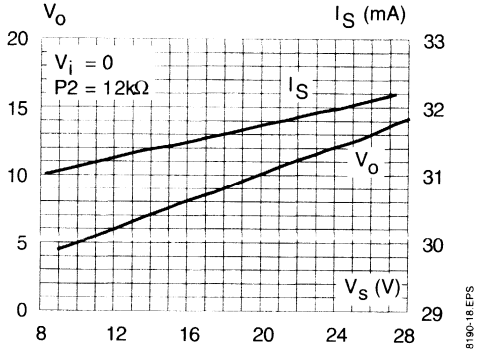


Figure 15 : Quiescent Drain and Quiescent Output Voltage versus Supply Voltage



APPLICATION INFORMATION

(refer to the block diagram)

IF Amplifier-limiter

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50µV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50µV. (see VCR facility too).

Low-pass Filter, Fm Detector And Amplifier

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40 dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and} \quad X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f_2}{f_1} = \sqrt{1 + \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1K, is available the recovered audio signal as auxiliary output.

DC Tone Control

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by :

X_{C11} = 6.8K, typically.

Pin 11 - At this pin is tied the tone capacitor.

Pin 12 - Is the DC Tone Control input.

DC Volume Control

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

Audio Frequency Power Amplifier and Thermal Protection

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_V = 20 \text{ Log } \frac{R5 + R4}{R5} \text{ (dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16 load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

Turn-on And Turn-off Switch

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turninig on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage V_S V_1 and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching..

- Pin 1 is the turn-on and turn-off muting input.

Supply

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 Q_o = 60	12 Q_o = 80	10 Q_o = 70
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C. F		Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

8190-05.TBL

Figure 16 : Application Circuit

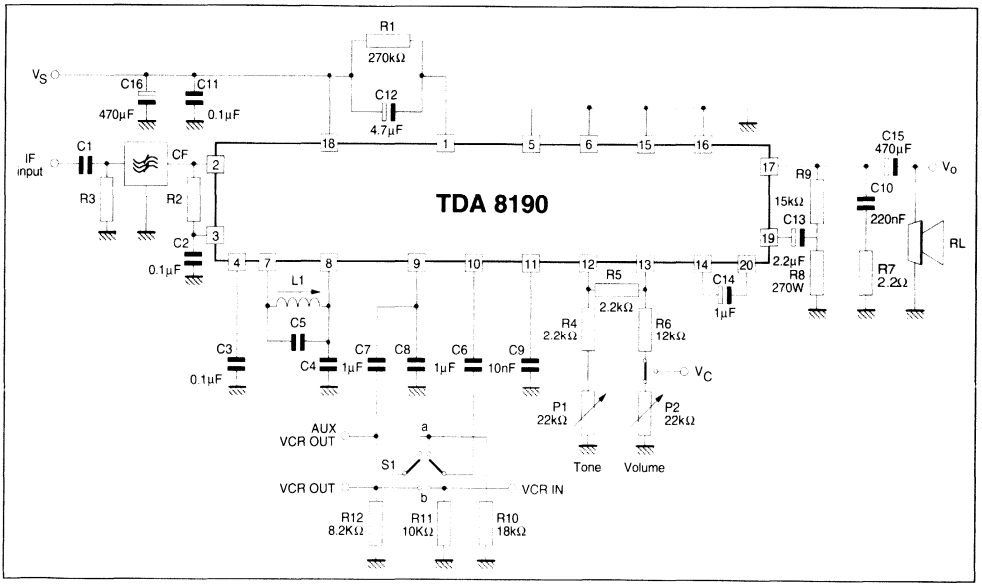
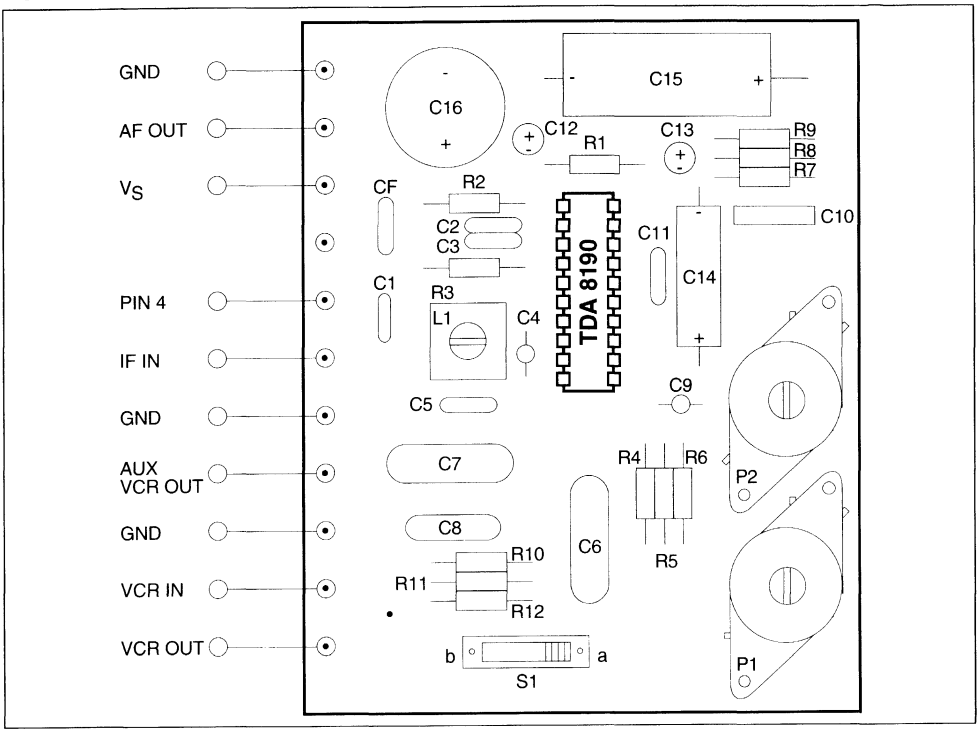


Figure 17 : PC Board and Components Layout of the Circuit of Figure 16 (1 : 1 scale)

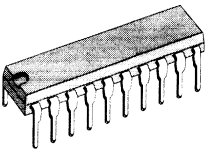


SGS-THOMSON MICROELECTRONICS

TDA8191

TV SOUND CHANNEL

- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- DC VOLUME CONTROL
- PERITELEVISION FACILITY
- 4W OUTPUT POWER
- LOW DISTORTION
- THERMAL PROTECTION
- TURN-ON AND TURN-OFF MUTING



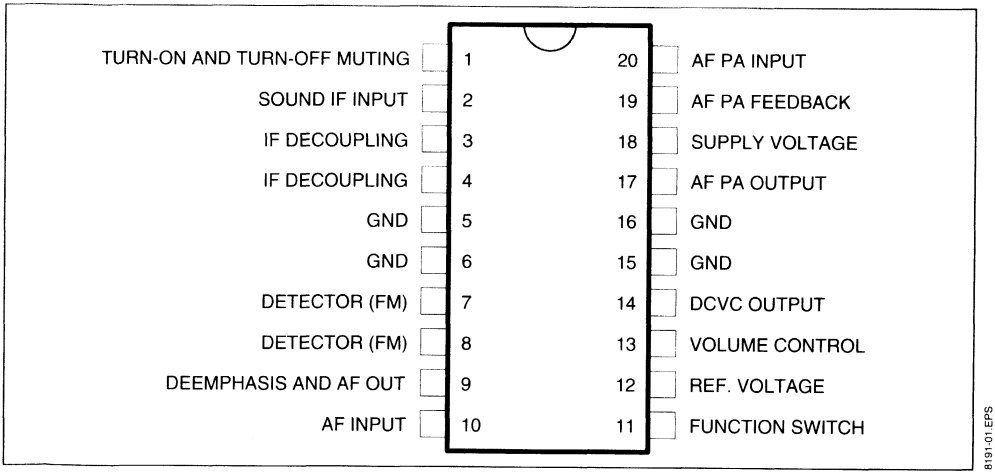
DIP20
(Plastic Package)

ORDER CODE : TDA8191

DESCRIPTION

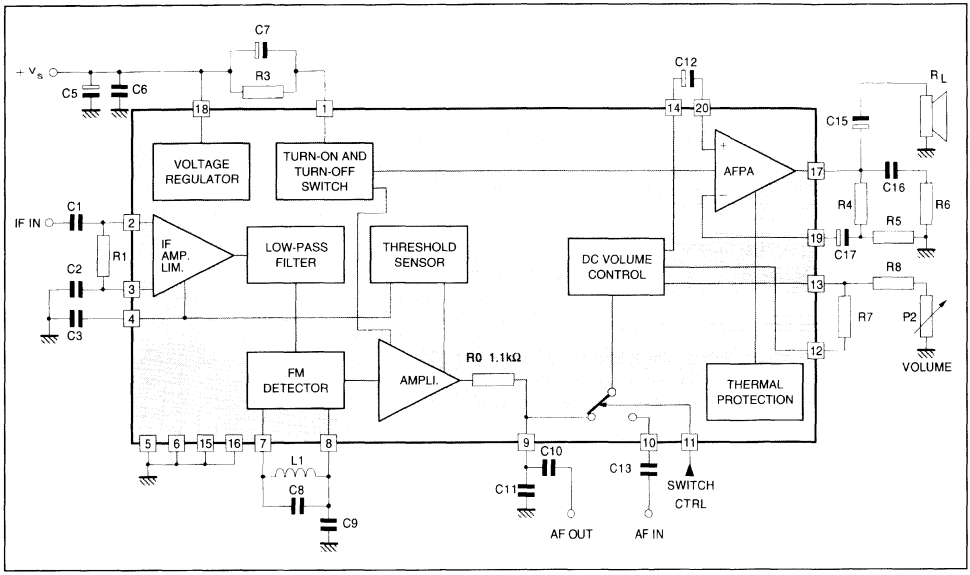
The TDA8191 is a monolithic integrated circuit that includes all the functions needed for a complete TV sound channel. The TDA8191 is assembled in a 20 pin dual in line power package.

PIN CONNECTION



8191-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 18)	28	V
V_I	Voltage at Pin 1	± V_S	
V_I	Input Voltage (pin 2)	1	V_{PP}
I_O	Output Peak Current (repetitive)	1.5	A
I_O	Output Peak Current (non repetitive)	2	A
P_{tot}	Total Power Dissipation : at Tpins = 90°C at Tamb = 70°C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

8191-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}pins)}$	Junction-pins Thermal Resistance	Max	14	°C/W
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Max	80	°C/W

8191-02.TBL

ELECTRICAL CHARACTERISTICS

(Refer to fig. 1 ; V_S = 24V, R_L = 16Ω, Pin 11 floating, Δf = ±50kHz, V_i = 1mV, f_o = 5.5MHz, f_m = 1kHz, T_{amb} = 25°C unless otherwise specified)

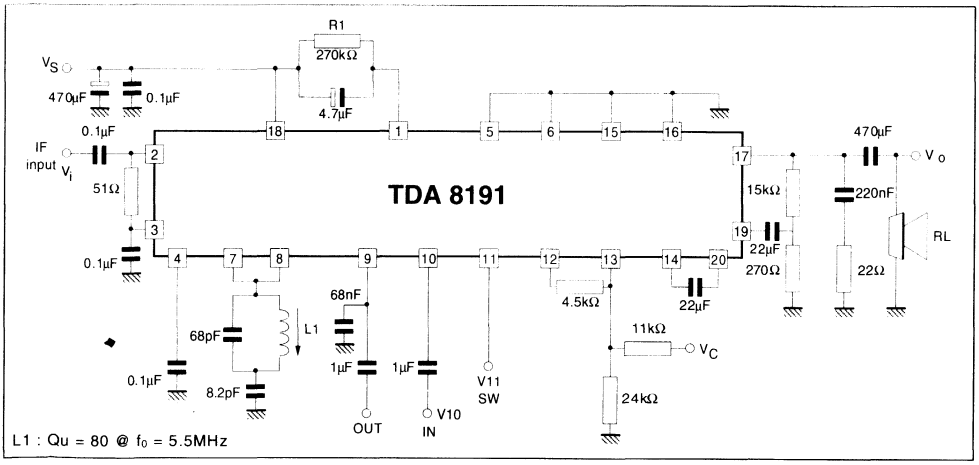
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (Pin 18)	Vc = 4.5V	10.8	24	27	V
V_O	Quiescent Output Voltage (Pin 17)	Vc = 4.5V	11	12	13	V
V_1	Pin 1 DC Voltage	Vc = 4.5V		5.3		V
I_D	Quiescent Drain Current	Vc = 4.5V		35		mA
V_I	Input Limiting Voltage at Pin 2 (– 3dB)	Vo = $4V_{RMS}$		50	100	µV

8191-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
(Refer to fig. 1 ; V_S = 24V, R_L = 16Ω, Pin 11 floating, Δf = ±50kHz, V_i = 1mV, f_o = 5.5MHz, f_m = 1kHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_9	Recovered Audio Voltage (pin 9)	V_C = 4.5V, Δf = ± 15kHz	200		400	mV_{RMS}
R_9	Deemphasis Resistance	f = 20Hz to 20kHz	500	700	1000	Ω
AMR	Amplitude Modul. Rejection	m = 0.3, V_O = $4V_{RMS}$	45	60		dB
R_I	Input Resistance (pin 2)	Δf = 0		30		kΩ
C_I	Input Capacitance (pin 2)	Δf = 0, V_C =4.5V		6		pF
V_{12}	DCVC Reference Voltage		5.6		6.2	V
Kv	Volume Attenuation	V_C = 0.5V ; Fig. 2 V_C = 4.5V ; Fig. 2	 80		1.0	dB dB
$\frac{\Delta K_V}{\Delta T_j}$	Volume Attenuation Thermal Drift	T_j = 300 to 380°K Fig. 3		– 0.05	– 0.1	dB/°C
P_O	Output Power (d = 10%)		3.5	4		W
SVR	Supply Voltage Rej. (Pin 17) (Pin 9)	 V_C = 4.5V f_{ripple} = 100Hz	 20 50	 26 60		 dB dB
V_{11}	Function Switch. - Television Broadc. Reproduction		 0		 2	 V
				or Pin 11 Floating		
	- Peritelevision Reproduction		8		12	V
R_{11}	Input Resistance		10			kΩ
V_{10}	Input Voltage (d ≤ 2%)	V_O = $4V_{RMS}$; V_{11} = 12V		0.5	2.0	V_{RMS}
R_{10}	Input Resistance	f = 20Hz to 20kHz	10			kΩ
CT	Crosstalk between Pins 9, 10		60			dB
$\frac{S+N}{N}$	Signal to Noise Ratio	Δf = 0 ; V_O = $4V_{RMS}$	60	70		dB
d	Distortion (P_O = 250mV)				2	%
Δf	Deviation Sens.	V_C = 0.5V ; V_O = $4V_{RMS}$		± 4	± 10	kHz

Figure 1 : Test Circuit



TYPICAL APPLICATION

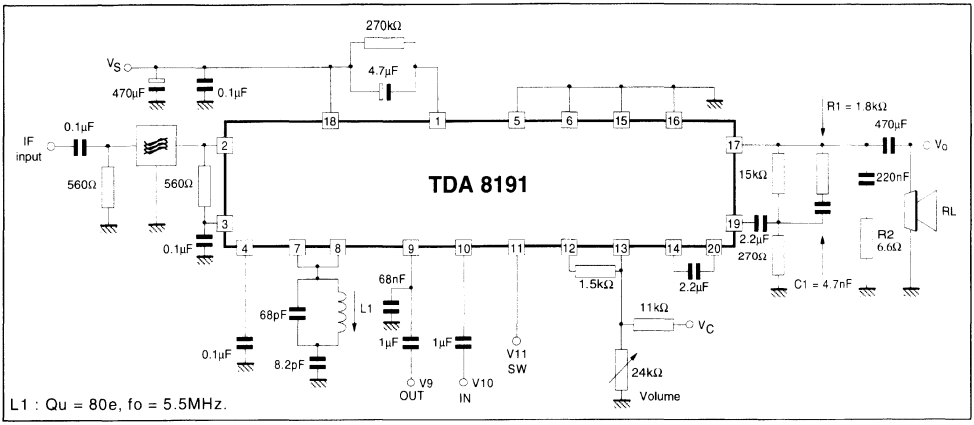


Figure 2 : Volume Attenuation versus DC Volume Control Voltage

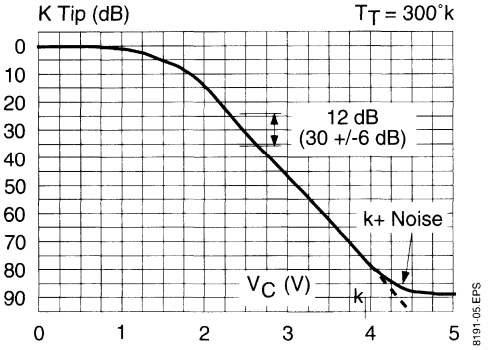


Figure 3 : Volume Attenuation Thermal Drift

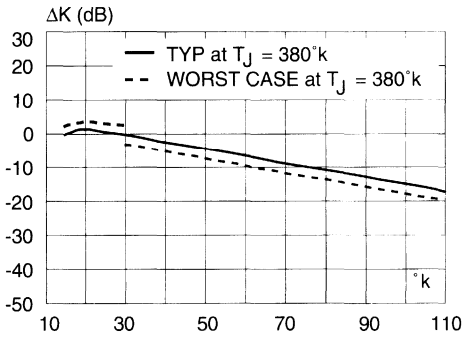


Figure 4 : Relative Audio Output Voltage and Output Noise versus Input Signa

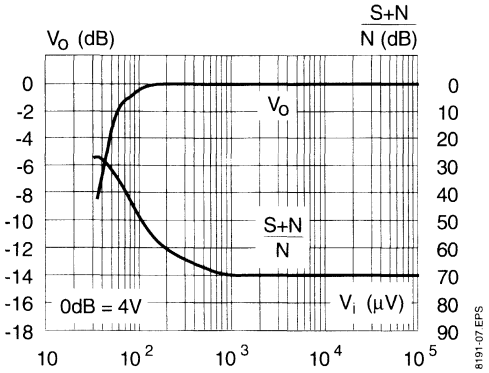


Figure 5 : Distortion versus Output Power

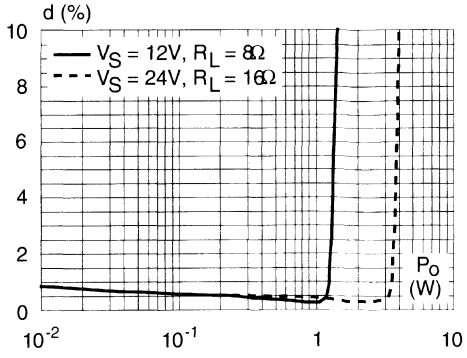


Figure 6 : Audio Amplifier Frequency Response

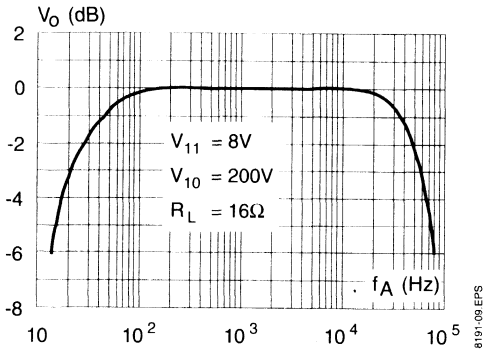


Figure 7 : Output Power versus Supply Voltage

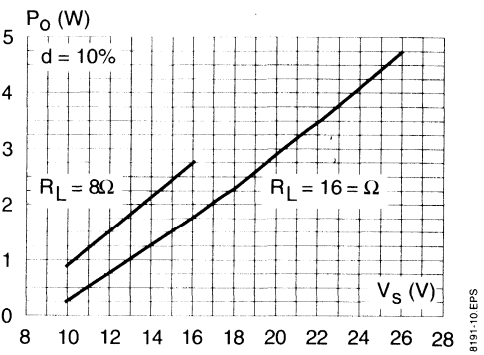


Figure 8 : Power Dissipation versus Supply Voltage (sine wave operation)

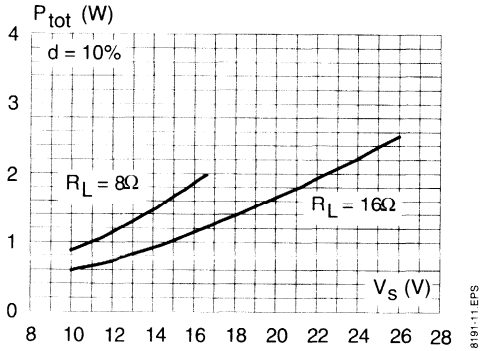


Figure 9 : Power Dissipation and Efficiency versus Output Power

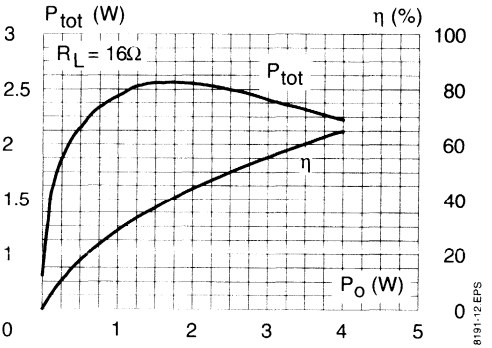
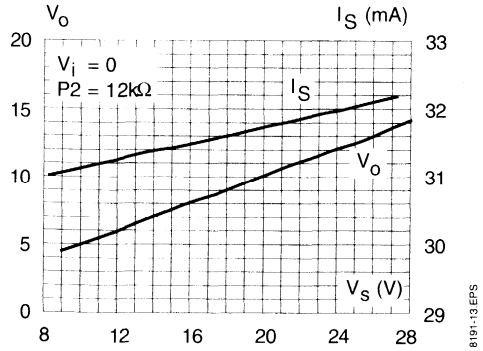


Figure 10 : Quiescent Drain and Quiescent Output Voltage versus Supply Voltage

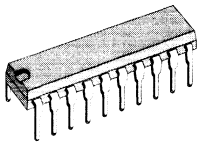


SGS-THOMSON MICROELECTRONICS

TDA8192

MULTISTANDARD AM AND FM SOUND IF CIRCUIT FOR TV

- A 2-STAGE GAIN CONTROLLED AMPLIFIER, PROVIDING COMPLETE IF GAIN ; (AM SECTION)
- A PEAK DETECTOR AND INTEGRATION WHICH PROVIDES AGC-VOLTAGE ; (AM SECTION)
- A 6-STAGE LIMITING AMPLIFIER FOLLOWED BY A SYNCHRONOUS DEMODULATOR AND DEEMPHASIS NETWORK ; (FM SECTION)
- AN AUDIO PREAMPLIFIER
- A CIRCUIT PROVIDING AM/FM SWITCHING AND MUTE FACILITIES
- AN EXTERNAL AUDIO INPUT CIRCUIT WITH SWITCHING FACILITIES TO DELIVER EITHER THE DEMODULATED IF, OR THE EXTERNAL AUDIO SIGNAL AT THE OUTPUT FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN50 049
- A DC CONTROLLED VOLUME CIRCUIT



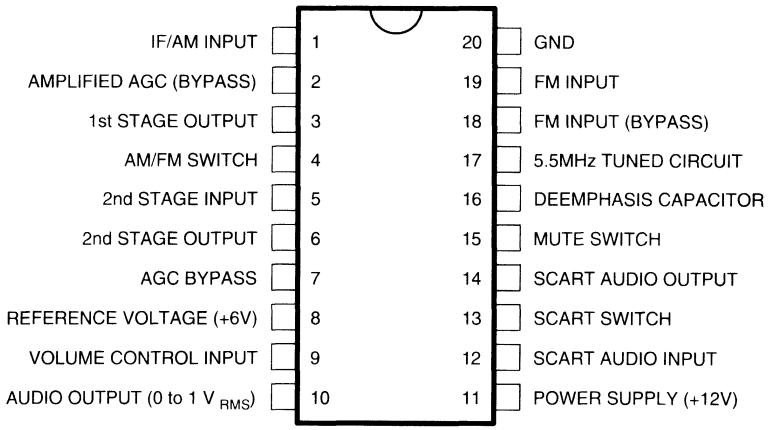
DIP20
(Plastic Package)

ORDER CODE : TDA8192

DESCRIPTION

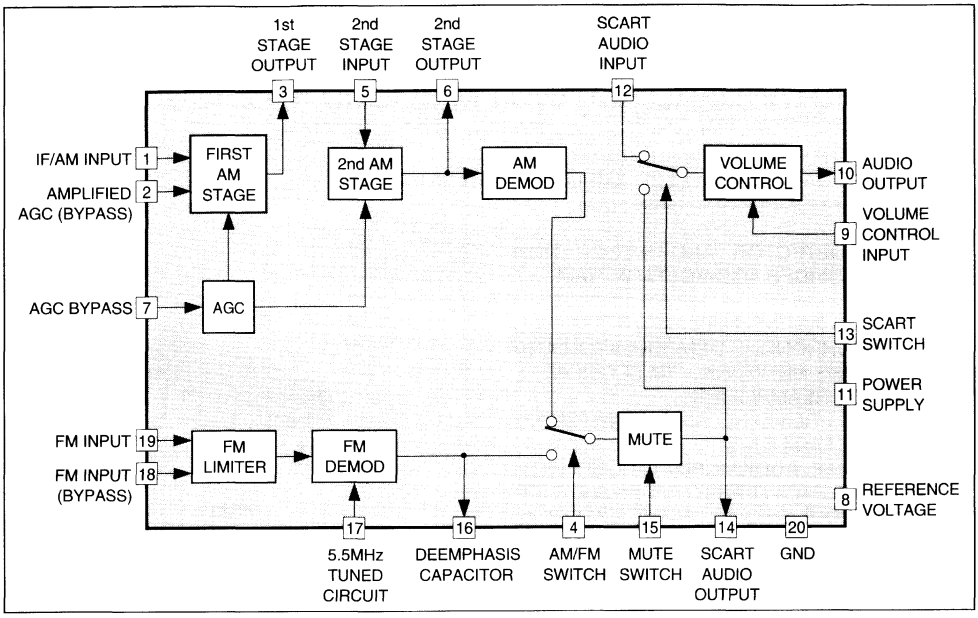
The demodulated IF signal is always available at a low impedance output.

PIN CONNECTIONS



8192-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70°C$	800	mW
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 150	°C

8192-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

8192-02.TBL

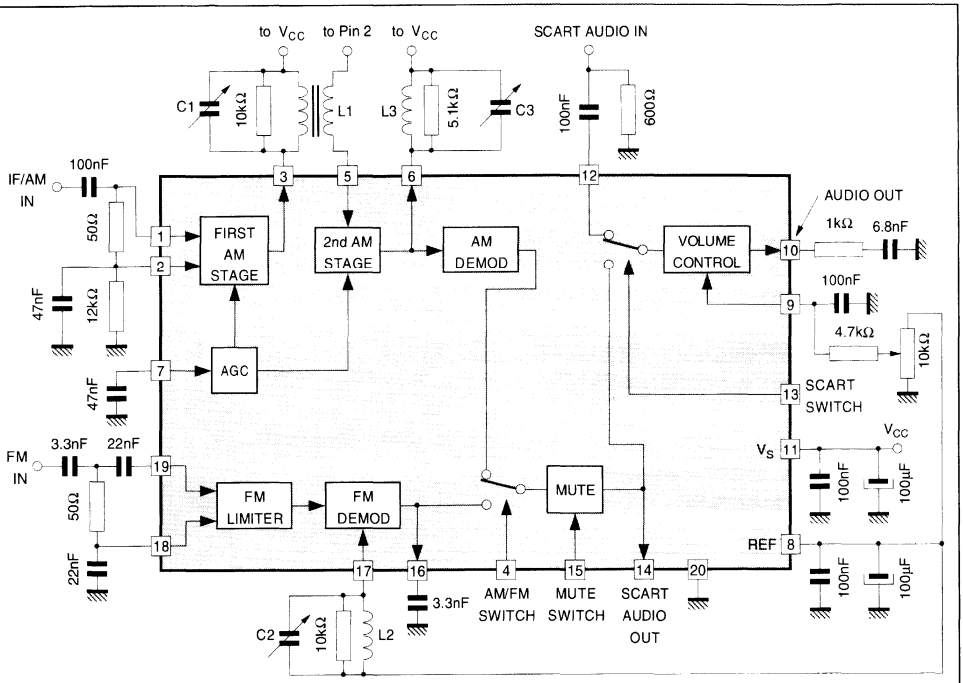
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		10.8	12	13.2	V
I_d	Supply Current	V_i = 0 AM FM		30 30		mA mA
AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1kHz unless otherwise specified)						
V_i	Input Sensitivity	S/N = 26dB		35		µV
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 0.1mV m = 0.3 V_i = 1mV V_i = 10mV	 50	36 50 56		dB
V_i	AGC Range	ΔV_{OUT} = – 1 to + 1dB		66		dB
V_o	Recovered Audio Signal		0.6	1	1.5	V_{RMS}
d	Distortion (1)				3	%
d	Distortion (2)				3	%
R_i	Input Resistance between Pins 1 and 2	m = 0	2			kΩ
C_i	Input Capacitance between Pins 1 and 2	m = 0		18		pF
FM SECTION (f_i = 5.5MHz, V_i = 1mV, Δf = ± 50KHz, f_m = 1kHz, unless otherwise specified) (continued)						
V_i	Input Limiting Voltage	– 3dB Limiting Point		30		µV
AMR	Amplitude Modulation	V_i = 30mV, m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 1mV	60			dB
d	Distortion (3)				1.5	%
d	Distortion (4)			2		%
V_o	Recovered Audio Signal		0.5	1	1.5	V_{RMS}
R_i	Input Resistance	Δf = 0	2			kΩ
C_i	Input Capacitance	Δf = 0		14		pF
C_T	Crosstalk AM/FM			70		dB
AM/FM AND MUTE SWITCHING						
	FM "on" (pin. 4)		2.5		V_S	V
	AM "on" (pin 4)		0		0.8	V
	Mute "on" (pin 15)		0		1	V
	Mute "off" (pin 15)		5		V_S	V
	Signal Attenuation for Mute "off"		70			dB
	Mute Switch Current				110	µA
	AM/FM Switch Current		50		250	µA
SCART SWITCHING						
	Mode Selection Voltage : TV Selected (pin. 13)		0		5	V
	Mode Selection Voltage : Scart Selected (pin 13)		8		12	V
	Scart Switch Input Resistance		10			kΩ
	Scart Audio Input Amplitude (pin 12)			0.5	2	V_{rms}
	Crosstalk Between Switched Inputs (TV scart)			80		dB
DC VOLUME CONTROL						
	Audio Output Impedance (pin 10)				1	kΩ
	Control Range			90		dB
	Output/input Gain for Maximum Gain Control			0		dB
	Gain Control Voltage		0.5		4.5	V
	Noise Level (DIN 45405)			25		μV_{rms}

8192-03.TBL

(1) 50% volume setting, V_i = 1mV
(2) 50% volume setting, V_i = 10mV
(3) V_i = 1mV, fm = 100 to 10.000Hz
(4) Vi = 1mV, ± 20KHz offset (detuning of phase shift filter).

TEST CIRCUIT



L1 = L2 : Qu = 95 at f_O = 39.2MHz with C_O = 100pF (TOKO HBKOCE-K5807 CF)
L3 : Qu = 80 at f_O = 5.5MHz with C_O = 68pF (TOKO BKAC-K1640 HM)

8192-03.EPS

SGS-THOMSON MICROELECTRONICS

TDA8120B

MULTISTANDARD VIDEO AND SOUND IF SYSTEM

- GAIN CONTROLLED IF AMPLIFIER
- VIF OPERATING FREQUENCY UP TO 50 MHz
- SYNCHRONOUS DETECTOR
- WHITE SPOT INVERTER
- VERY LOW DIFFERENTIAL ERROR
- VERY LOW PHASE ERROR
- INTERNAL AGC SWITCH (B/G - L)
- AGC TOP. SYNCH. FOR STANDARD B/G
- AGC TOP WHITE FOR STANDARD L
- QUASI SPLIT SOUND FOR STANDARD B/G
- SOUND DETECTOR FOR STANDARD L
- VIDEO MUTING FACILITY
- SEPARATED SOUND OUTPUT
- OPERATES WITHOUT EXTERNAL GATING PULSE

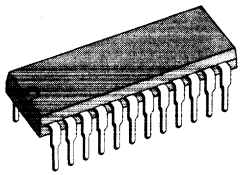
DESCRIPTION

The TDA8120B is a monolithic IC for TV video IF and Sound IF amplification and demodulation that can operate with all the TV standards.

The Video IF section can handle negative (B/G) or positive (L) modulated video signals by means of DC switching.

The Sound IF section acts as a Quasi Split Sound (QSS) subsystem in B/G transmission and allows a second Sound IF with high rejection of the video information.

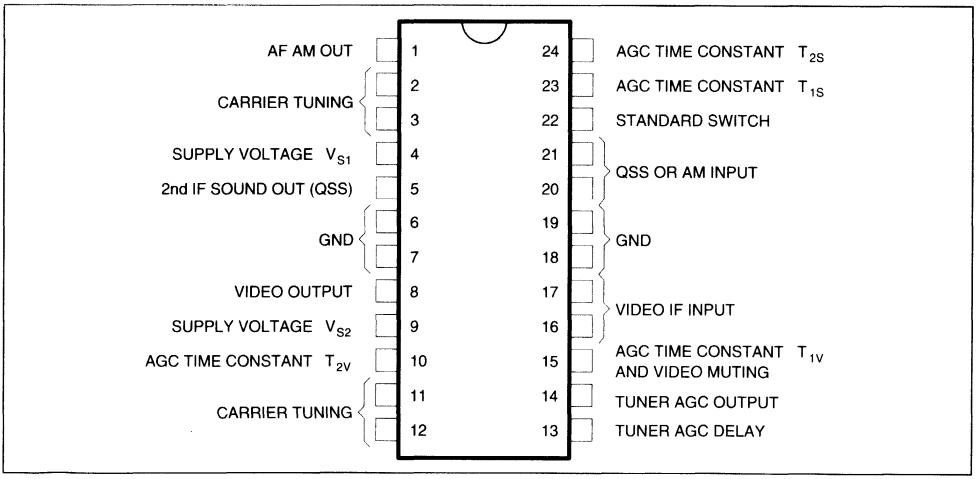
The DC switch can modify the Sound IF configuration to process AM modulated Sound signals (L). The TDA8120B is assembled in a 24 pin dual in line power package.



DIP24
(Plastic Package)

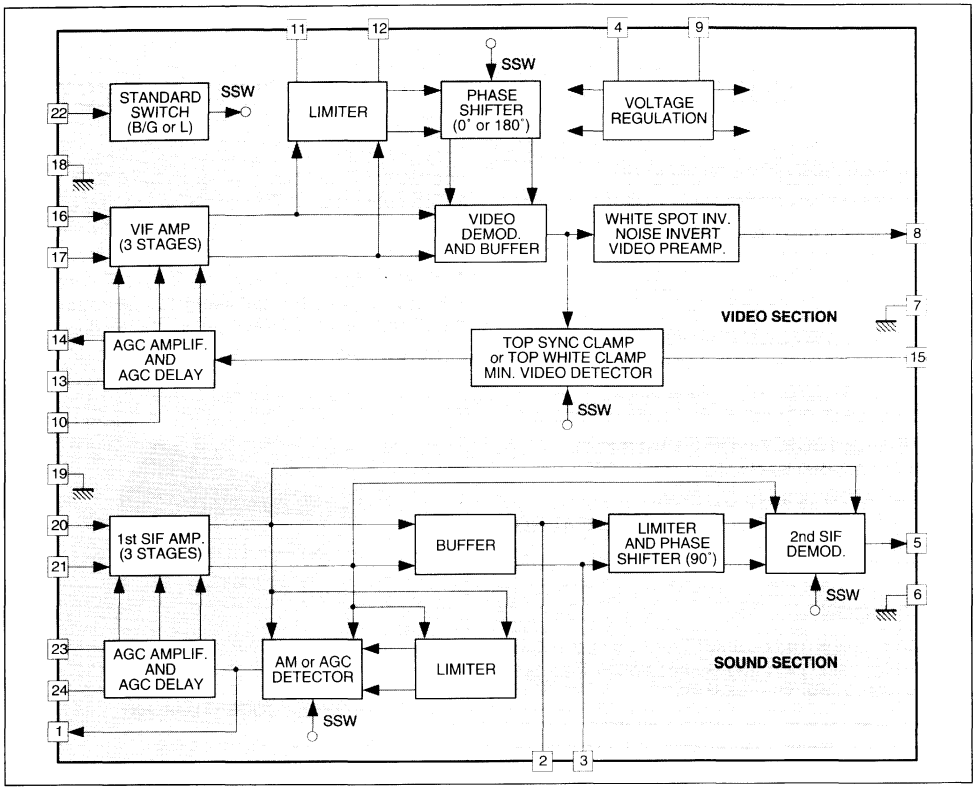
ORDER CODE : TDA8120B

PIN CONNECTIONS



8120B-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_4, V_9	Supply Voltage V_s	15	V
I_8, I_5, I_1	Video Out, QSS_{out}, AF AM Out, DC Output Current	10	mA
I_{22}, I_{15}	Pin 22 and Pin 15 Input Current	1	mA
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	2	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C
V_{14}	Voltage at Pin 14	V_s	

8120B-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance	Max	40	°C/W

8120B-02.TBL

ELECTRICAL CHARACTERISTICS (V_S = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDEO IF SECTION V_I = 10 mV_{RMS} (black field), F_O = 38.9MHz ; unless otherwise specified						
V_S	Supply Voltage (pin 4 and pin 9)		10.8	12	13.2	V
I_S	Supply Current	V_I= 0		120		mA
$V_{8\,H}$	Top White Level	V_I = 0, R_L = 1.5kΩ	5.5	6	6.5	V
$V_{8\,L}$	Top Synchronous Level		2.7	3	3.3	V
V_8	Video Output B/G	Modulation Depth D = 90%, R_L = 1.5kΩ	2.2	3	3.4	V_{pp}
V_8	Video Output L	R_L = 1.5kΩ, M = 100%	2.2	3	3.4	V_{pp}
ΔV_8	Video Output Variation between Standards B/G and L .	M = 100%		± 2		%
$-I_8$	Output Current	R_L = 1.5kΩ		4		mA
I_8	Input Current		2			mA
I_{14}	Tuner AGC Current Capability			4.5		mA
S/N	Signal to Noise Ratio	B = 5MHz, D = 90%	50			dB
ΔV_I	AGC Range	ΔV_8 = 1dB, D = 90%	60			dB
B	Bandwidth	ΔV_8 = − 3dB, D = 90%	7			MHz
V_{16-17}	Input Sensitivity for Full Output Signal	D = 90%		50		µV
V_8	Carrier Leakages	F_o = 38.9MHz F_o = 77.8MHz		20 50		mV mV
dG	Differential Gain	Subcarrier Modulated Staircase Video Signal, D = 90%			10	%
dφ	Differential Phase	Subcarrier Modulated Staircase Video Signal, D = 90%			10	degree
d_{IM}	Intermodulation Product 1.07MHz	Video Carrier Relative Level = 0dB Chroma Subcarrier Relative Level = − 3.2dB Sound Carrier Relative Level = − 20dB		50		dB
R_i	Input Resistance (between pin 16 and pin 17)			1.5		kΩ
C_i	Input Capacitance (between pin 16 and pin 17)			2		pF
QUASI SPLIT SOUND CHANNEL OR FRENCH SOUND CHANNEL (see notes 1 and 2)						
V_{20-21}	Input Sensitivity for Full Output Signal (between pin 20 and 21)	R Channel Missing		50		µV
ΔV_i	AGC Range	ΔV_5 = 1 dB R Channel Missing	60			dB
V_5	Output Voltage Standard B/G	R_L = 600Ω, AC Coupled, F_O = 5.5MHz		100		mV_{RMS}
I_5	Output Current			2.5		mA
Z_5	Small Signal Output Impedance (QSS)	F_O = 5.5MHz or F_O = 5.74MHz			50	kΩ
R_i	Input Resistance (between Pin 21 and Pin 20)			1.5		kΩ
C_i	Input Capacitance (between Pin 21 and Pin 20)			2		pF
S/N	Noise Ratio QSS (after SIF limitation and FM demodulation) F_O = 5.50MHz F_O = 5.74MHz	Channel R or Channel L Switched off F_m = 1kHz, Δf = ± 30kHz Carrier Modulated with Syncs. Pulses Only. CCIR 468-2 Recommendant	 60 58			dB
V_1	Output Voltage Standard L		0.58	0.7	1	V_{RMS}
I_1	Output Current			2.5		mA
Z_1	AF Output Impedance (L)				50	Ω
S/N	Noise Ratio AM Standard L	B_N = 20kHz	46			dB

8120B-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
QUASI SPLIT SOUND CHANNEL OR FRENCH SOUND CHANNEL (see notes 1 and 2)						
d	Distorsion				2	%
V_{22}	B/G Operation L Operation		2 0		5 0.8	V V
V_{15}	Video Muting		8		V_S	V

8120B-04.TBL

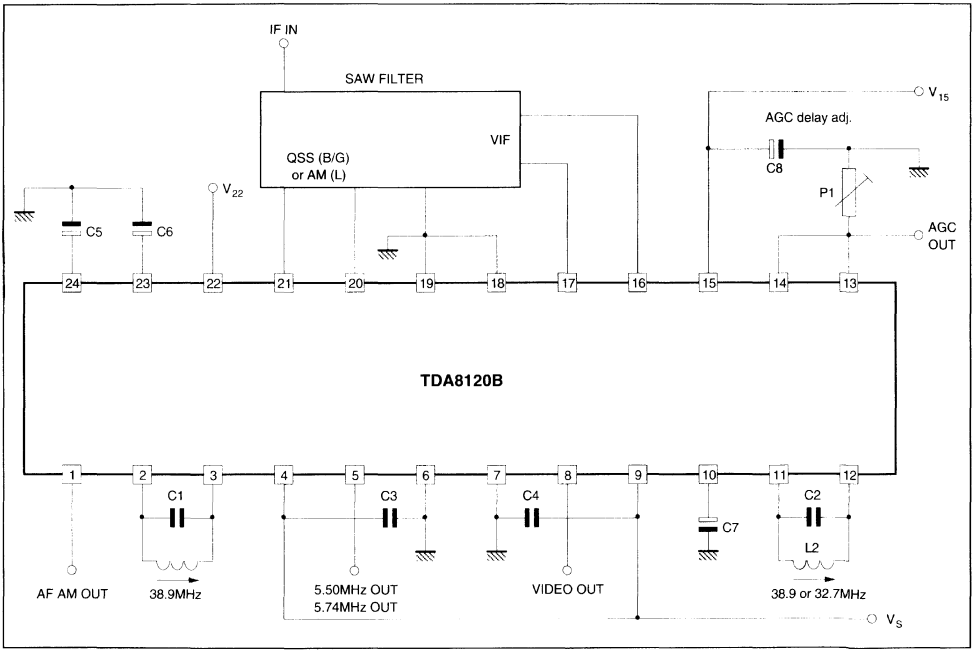
Notes : 1. QUASI SPLIT SOUND CHANNEL

$\Delta f = 0$ { Video carrier relative level = 0 dB f= 38.9 MHz
Sound carrier relative level = – 13 dB (mono or L) f = 33.4 MHz
Sound carrier relative level = – 20 dB (R) f= 33.16 MHz

V_I = 10 mV Video carrier modulated with syncs ; V_{22} = 2 V, unless otherwise specified.

2. FRENCH SOUND CHANNEL
V_I = 10 mV (Carrier level) ; f_o = 39.2 MHz ; F_m = 1 KHz ; m = 80 % ; V_{22} = 0.8 V, unless otherwise specified.

TEST CIRCUIT



8120B-03.EPS

CIRCUIT OPERATION

The TDA8120B (see block diagram) consists of a video section and a sound section. The integration of both sections on the same chip requires a high isolation at IF frequencies. This is achieved by physically separating the two sections, with separate power supplies and ground pins. In addition, special care has been taken in the choice of pad positions for the IF inputs and sound/video outputs.

The video section consists of three AC-coupled IF stages with more than 60 dB AGC range, flat amplitude/frequency response from 10 to 85 MHz and linearized phase slope from 30 to 50 MHz. Video carrier regeneration is performed by a tuned limiter. The carrier is then applied to the video demodulator through a special circuit which switches the carrier phase from 0 to 180° so that the video polarity can be maintained constant when the standard switches from B/G to L. A noise inverter and a white spot inverter are included to eliminate ultra-black and white pulses.

A top sync or a top white clamping circuit and a minimum DC video component detector are implemented by two double comparators the characteristics of which may be controlled by an external control input to adapt to the modulation type for each standard. The voltage at the output of the two comparators is memorized by an external capacitor and used to drive the AGC network, which allows an input regulation of the video carrier from less than 100 µV to 100 mV. A delayed control storage with current output for the turner AGC completes the video section.

The sound section consists of three IF stages with the same characteristics as the video IF stages and an identical network to control and set the gains of the three IF amplifiers. The output of the third IF stage feeds the AM/AGC detector and the QSS section.

The AM/AGC detector consists of a wideband limiter for AM sound regeneration or video carrier regeneration used to feed the synchronous multiplier and consequently to obtain the AM demodulated audio signal. In addition, a DC voltage proportional to the peak-to-peak value of the video carrier is produced. Two comparators complete the sound AGC loop.

The subsequent QSS section consists of a reference amplifier tuned to the video IF which buffers a wideband limiter to reject completely the video AM information without introducing incidental phase modulation (IPM).
Following the limiter there are a 90° phase shifter and a linear-to-logarithmic converter which drives a linear multiplier as a demodulator for the intercarrier 2nd sound IF. This quadrature multiplier rejects all video components transmitted in DSB that is low frequency components of the video signal.

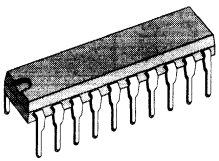
In addition to the sound and video sections, the TDA8120B includes a block for standard switching (B/G or L) controlled by a TTL-compatible input.

SGS-THOMSON MICROELECTRONICS

TDA8124

MULTISTANDARD VIDEO IF INTERFACE

- AUTOMATIC IDENTIFICATION OF PICTURE CARRIER MODULATION POLARITY
- VIDEO SIGNAL IDENTIFICATION (FOR SOUND MUTING)
- ANALOG AND DIGITAL A.F.C. FOR STOP TUNING FUNCTION
- PICTURE CARRIER DETECTION IN A RANGE OF 1MHz AROUND THE IF-PICTURE CARRIER VALUE



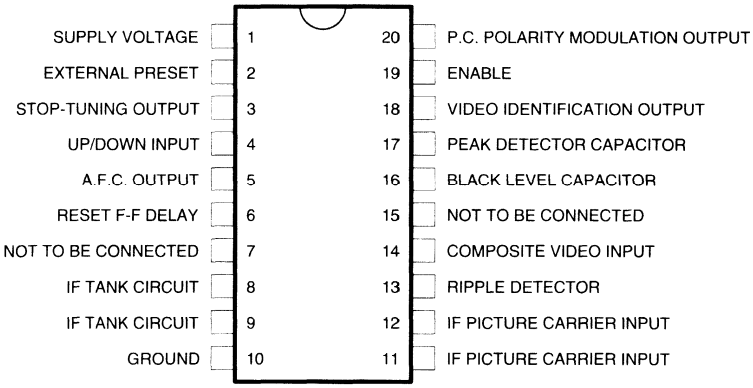
DIP20
(Plastic Package)

ORDER CODE : TDA8124

DESCRIPTION

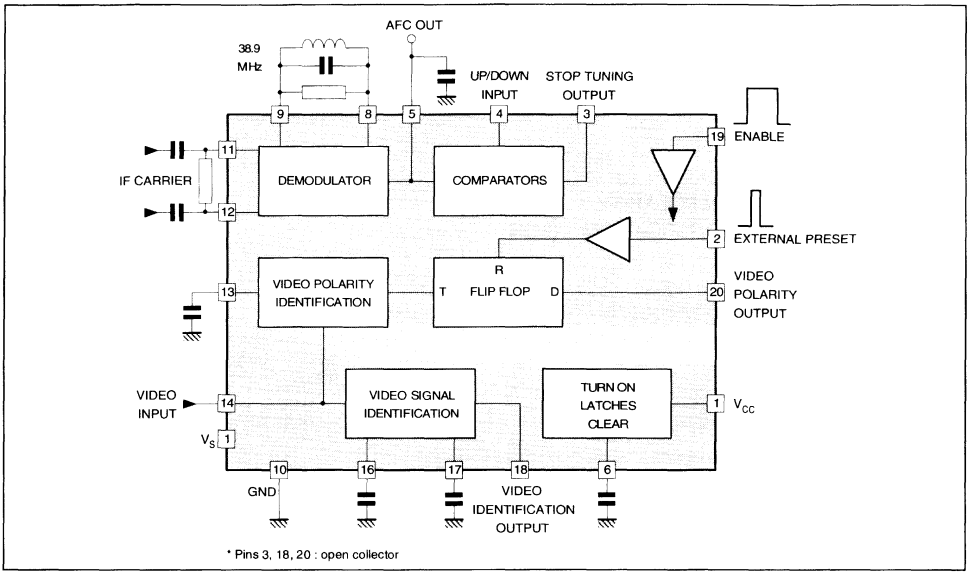
The TDA8124 has been developed in order to permit automatic standard switching and tuning when coupled with a multistandard VIDEO IF IC (for example TDA8120). It contains an A.F.C. synchronous demodulator and an A.F.C. comparator, a video polarity identification circuit with logic and a video signal identification system.

PIN CONNECTIONS



8124-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 1)	15	V
T_{oper}	Operating Ambient Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	- 20 to + 150	°C

8124-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	80	°C/W
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	Max.	14	°C/W

8124-02.TBL

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C, V_{CC} = 12V (unless otherwise specified)

- Positive video input signal V_i = $3V_{PP}$ with top sync level = 3V
- Enable ≥ 2V on Pin 19

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1		14	24	32	mA
	Video Input Top Sync Level	14	• B/G standard : M = 100%, D = 90% • L/E standard : M = 100%, R ≤ 6%		3		V
	Video Input Top White Level	14	• B/G standard : M = 100%, D = 90% • L/E standard : M = 100%, R ≤ 6%		6		V
	Composite Video Input Voltage	14		1.5	3	3.3	V_{PP}
	Ripple Voltage accross the 5.6nF External Capacitor	13	C13 = 5.6nF		400		mV

8124-03.TBL

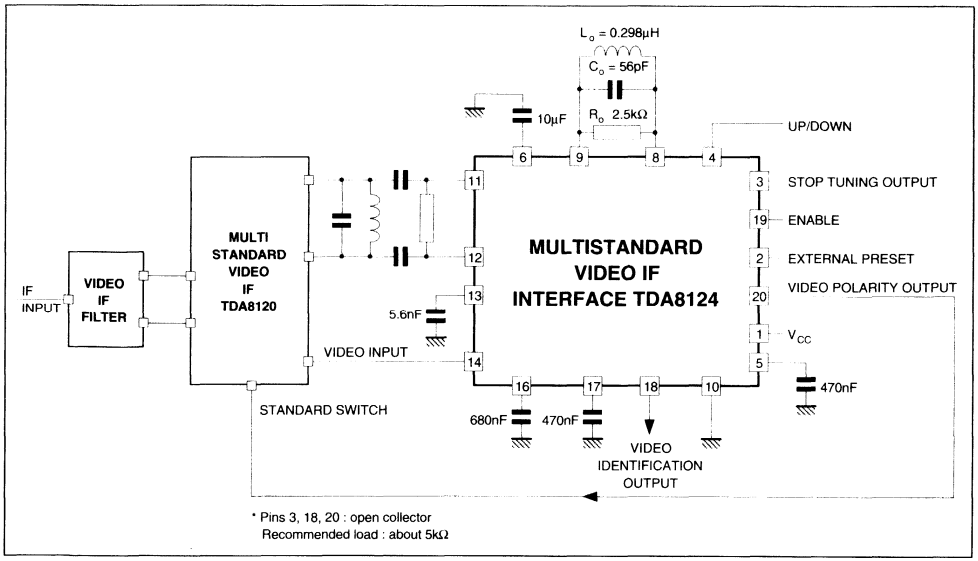
ELECTRICAL CHARACTERISTICS (continued)

T_{AMB} = 25°C, V_{CC} = 12V (unless otherwise specified)
- Positive video input signal V_i = 3V_{PP} with top sync level = 3V
- Enable ≥ 2V

Symbol	Parameter	Pins	Test Conditions	Min.	Typ.	Max.	Unit
	Peak Detector Threshold Voltage	17			4.5		V
	Video Identification Current Capability	18				10	mA
	Minimum Sync Amplitude for Video Identification	14		450			mV_{PP}
	External Preset up/down and Enable Switch Voltages	2, 4 19		0 2		0.8 V_{CC}	V V
	External Preset, up/down, Enable Pins Input Impedance	2, 4 19		35	50		kΩ
	Video Polarity Out Voltage	20	Enable ≥ 2V, P.C. IF = 38.9MHz • L/E (positive modulation) • B/G (negative modulation)		 V_{CC}	0.5	 V V
	Video Identification Out Voltage	18	• no video signal • with video signal		V_{CC}	 0.5	V V
	IF Picture Carrier Input Voltage	11, 12	P.C. IF = 38.9MHz	50			mV_{PP}
	A.F.C. Output Slope	5	Q_{LC} = 80, C_O = 56pF, $L_O \cong 0.298\mu H$, R_O = 2.5kΩ	0.5		0.85	V 100kHz
	V_{11-12} DC Voltage	11, 12			3.8		V
	V8-9 DC Voltage	8, 9			3.65		V
	Stop/Tuning Output Voltage	3	• No picture carrier or 39.4MHz < IF < 38.4MHz • With picture carrier $IF_{PC} \geq 38.9MHz$ $IF_{PC} \leq 39.4MHz$		0 V_S		V V
	Stop/Tuning Output Bandwidth	3		1.1	1.3	1.5	MHz

8124-04.TBL

TYPICAL APPLICATION (with TDA8120)



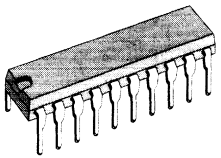
8124-03.EPS

SGS-THOMSON MICROELECTRONICS

TDA8213

VIDEO & SOUND IF SYSTEM

- VERY LOW CURRENT ABSORPTION
- 3 STAGE IF GAIN CONTROLLED AMPLIFIER
- SYNCHRONOUS VIDEO DEMODULATOR
- WHITE SPOT AND NOISE INVERTER
- AGC CIRCUIT WITH NOISE GATING
- TUNER AGC OUTPUT FOR PNP TUNERS
- FM DETECTOR
- AF AMPLIFIER WITH DC VOLUME CONTROL
- AFC
- 2 V_{PP} ON VIDEO OUTPUT



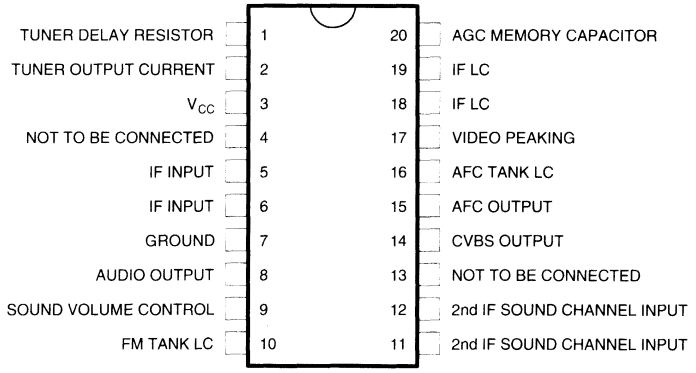
DIP20
(Plastic Package)

ORDER CODE : TDA8213

DESCRIPTION

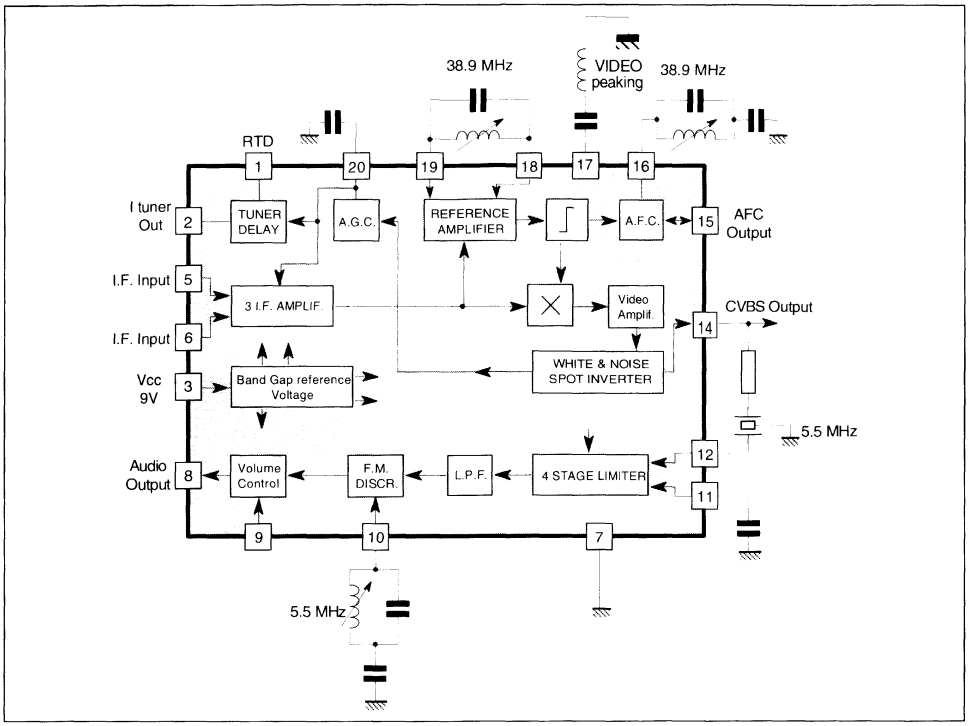
The TDA8213 is a monolithic integrated circuit in DIP20 package for colour and black & white television receivers using PNP tuners. It is intended to operate with a negatively modulated vision carrier and frequency modulated sound carrier. Used with TDA8214/15 (H/V deflection circuit) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications.

PIN CONNECTIONS



8213-01.EPS

BLOCK DIAGRAM



8213-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply voltage	13.5	V
V_X	Tuner AGC voltage	V_S	V
P	Power dissipation at T_{AMB} = 70°C	880	mW
T_{STG}	Storage temperature range	- 40, + 150	°C

8213-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-a)}$	Junction-ambient thermal resistance	Max.	80	°C/W

8213-02.TBL

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV$_{RMS}$ top sync, D = 90%, Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV$_{RMS}$, f_m = 1kHz, Audio BW = 20kHz, $\Delta f = \pm$ 25kHz, Volume attenuation = 0dB, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY						
	Supply voltage		8	9	12.8	V
	Supply current		14	20	28	mA

8213-03.TBL

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV_{RMS} top sync, D = 90%, Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV_{RMS}, f_m = 1kHz, Audio BW = 20kHz, Δf = ± 25kHz, Volume attenuation = 0dB, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IF AMPLIFIER						
	AGC range		58	64	67	dB
	IF - sensitivity (RMS)	Video out -3dB		70		µV
	R input differential	Guaranteed by process	1	1.5	2	kΩ
	C input Stray				2	pF
DEMODULATED VIDEO OUTPUT						
	S/N video (BW = 5MHz)	IF inp. = 10mV_{RMS} , 20 $\log_{10} \frac{(WH - BL)}{N_{RMS}}$	49	55		dB
	Intermodulation 1.07MHz	AGC open loop, Picture carrier = 0dB, Chrominance carrier = -3.2dB, Sound carrier = -20dB		50		dB
	Detected video output peak to peak (positive)		1.8	2	2.4	V
	Top synchro output level	-3dB, see Figures 1 and 2		1.9		V
	Video Bandwidth with output filter			7		MHz
	Differential phase			3	7	Degree
	Differential gain			3	7	%
	White noise clamp	Referred to the video output see Figure 6		4.5		V
	White noise insertion			3.2		V
	Video output current capability		1.2	2	2.6	mA
	Residual output carrier (RMS)	At 38.9MHz At 77.8MHz			10 20	mV mV
AFC						
	AFC slope	With R_{Load} = 200kΩ, see Figure 3	25	40	60	mV/kHz
AGC CIRCUIT						
	Maximum I charge		550	900	1200	µA
	Maximum I discharge		14	20	26	µA
	I_{CH} / I_{DISCH} Ratio			45		-
TUNER AGC						
	Sinked Current	Suitable for Mosfet-NCH	1.15	2	2.6	mA
	Slope	RTD = 0 ÷ 10kΩ			600	µA/dB
DEMODULATED AUDIO OUTPUT						
	Detected output audio signal (RMS)		120	270	350	mV
	Total harmonic distorsion			0.5	2	%
	Amplitude modulation rejection	m = 30%	40	53		dB
	2nd IF sound sensitivity -3dB FM detected audio signal (RMS)			200		µV
	$\frac{S+N}{N}$	Δf = ± 25kHz for signal Δf= 0 after deemphasis (BW = 20kHz)I	50	60		dB
	Thermal drift of volume			0.05		$\frac{dB}{°C}$
	Input resistance limiter		400	560	720	Ω
	Volume Control versus V_9	See Figure 4 V_9 = 4.5V V_9 = 2.5V V_9 = 0.9V	12 65	0 18 74	24	dB dB dB

8213-04.TBL

TEST CIRCUIT

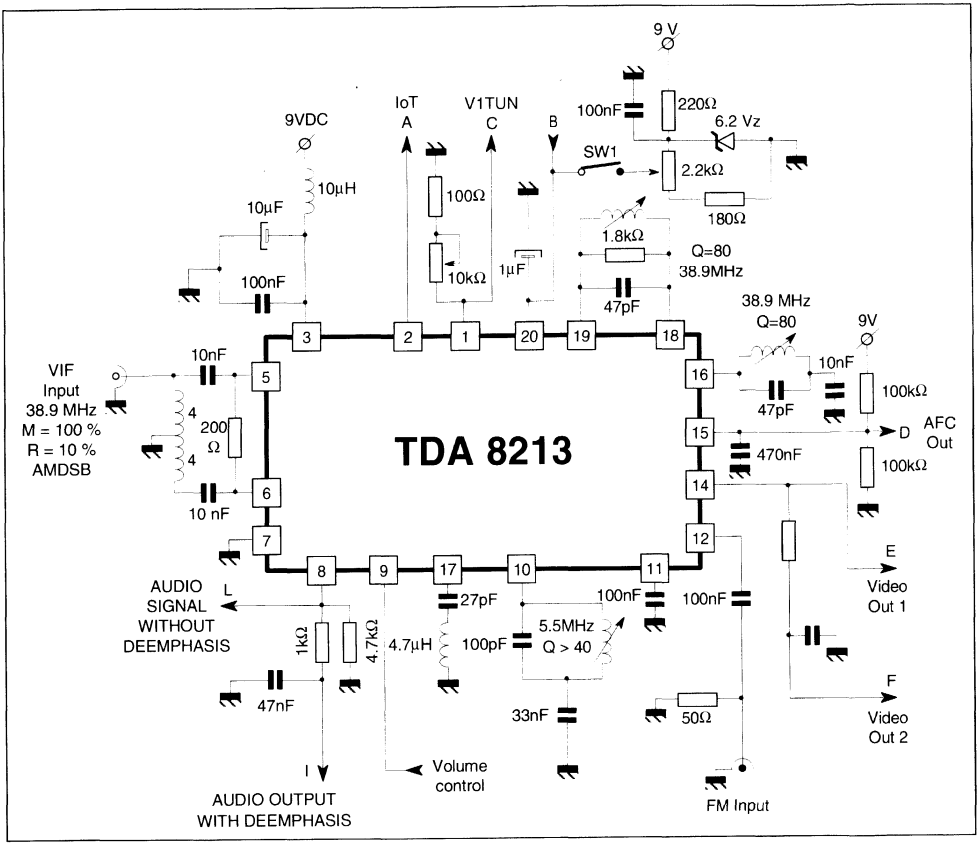


Figure 1 : Output Signal Bandwidth without Video peaking

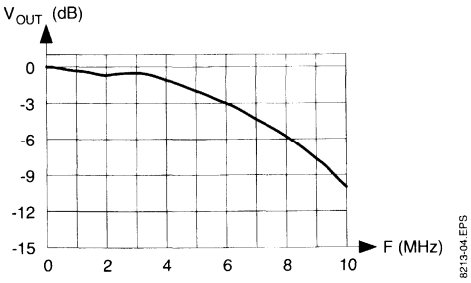


Figure 2 : Output Signal Bandwidth with Video peaking

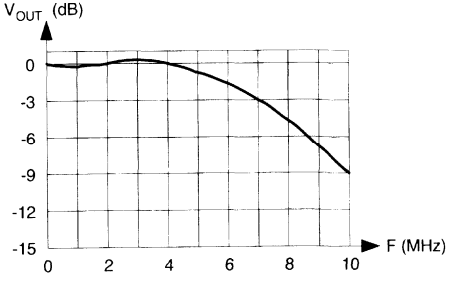


Figure 3 : AFC Voltage versus Input Frequency

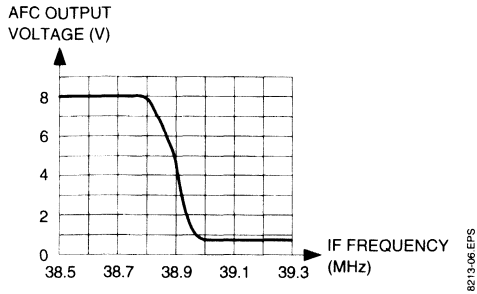


Figure 4 : Volume Control Attenuation versus Voltage in Pin 9

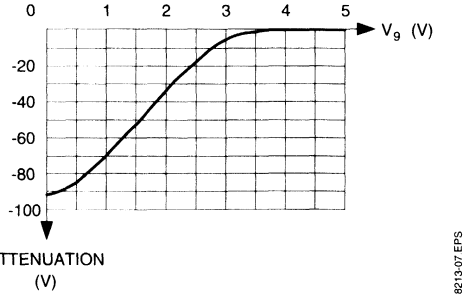


Figure 5 : Typical Connection from µP to TDA8213 for Remote Volume Control (Pin 9)

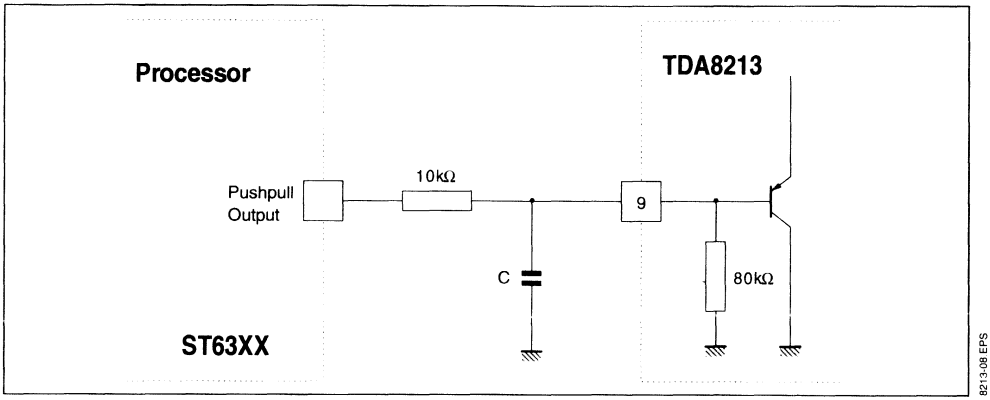


Figure 6 : Black and White Noise Inverter

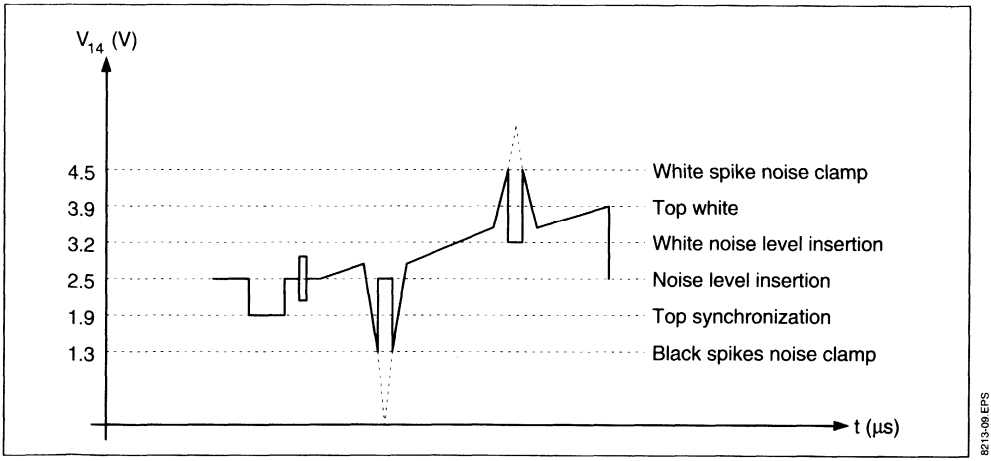
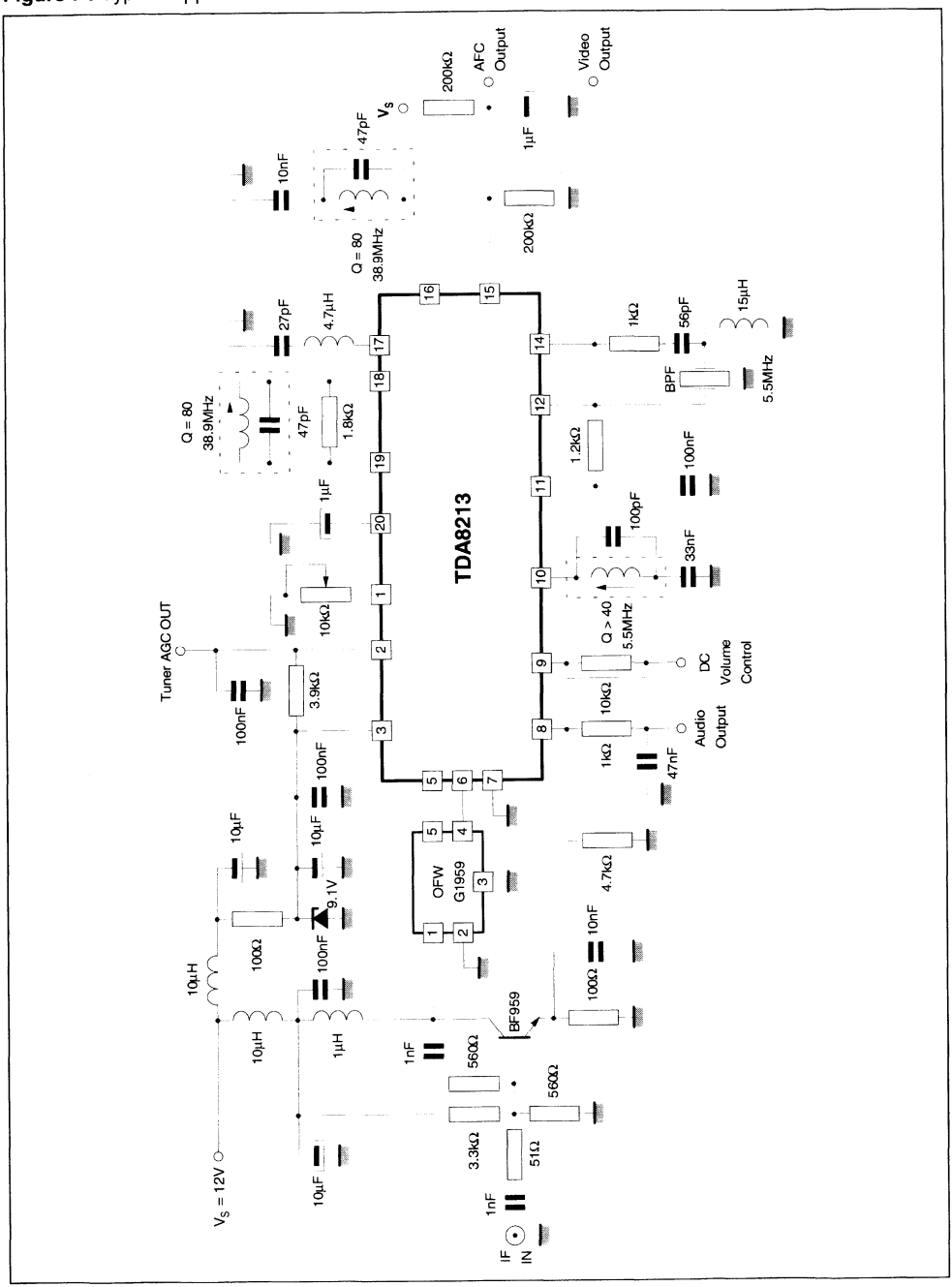


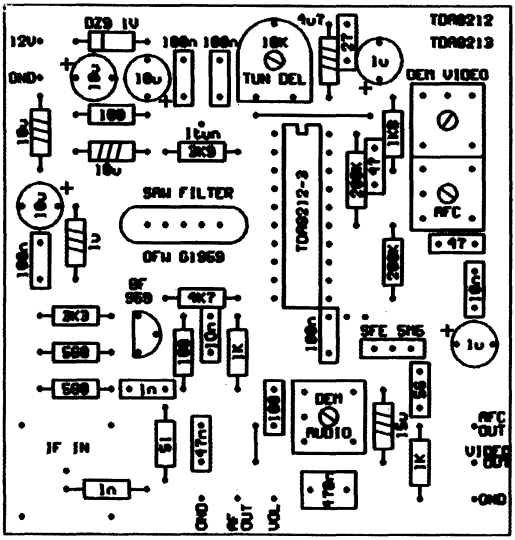
Figure 7 : Typical Application

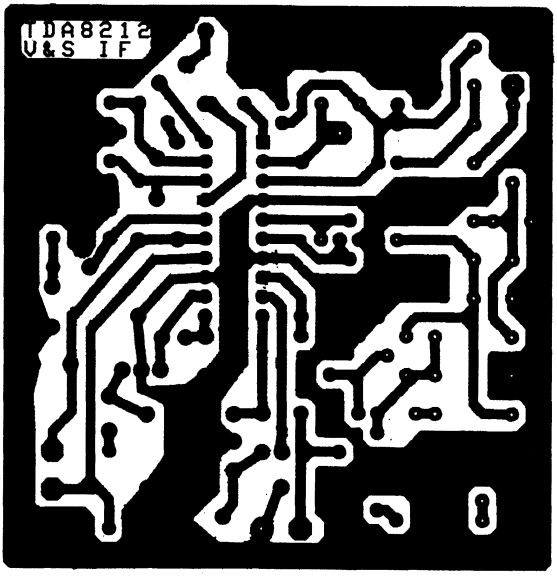


8213-10.EPS

SGS-THOMSON MICROELECTRONICS

Figure 8 : PC Board and Components Lay-out of the Circuit of Figure 7 (1 : 1 scale)





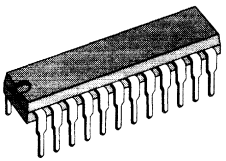
8213-11A.TIF/8213-11B.TIF

SGS-THOMSON MICROELECTRONICS

TDA8222

VIDEO & SOUND IF SYSTEM WITH VIDEO AND SOUND SWITCHES

- 3 STAGE IF GAIN CONTROLLED AMPLIFIER
- SYNCHRONOUS VIDEO DEMODULATOR
- TOP SYNC AGC CIRCUIT
- WHITE AND BLACK NOISE INVERTER
- TUNER AGC OUTPUT FOR PNP TUNERS (suitable also for MOSFET tuners)
- ANALOG AFC
- FM DETECTOR
- AUDIO AND VIDEO SWITCHES COMPATIBLE WITH SCART EUROPEAN NORM
- DC VOLUME CONTROL
- MUTE FUNCTION



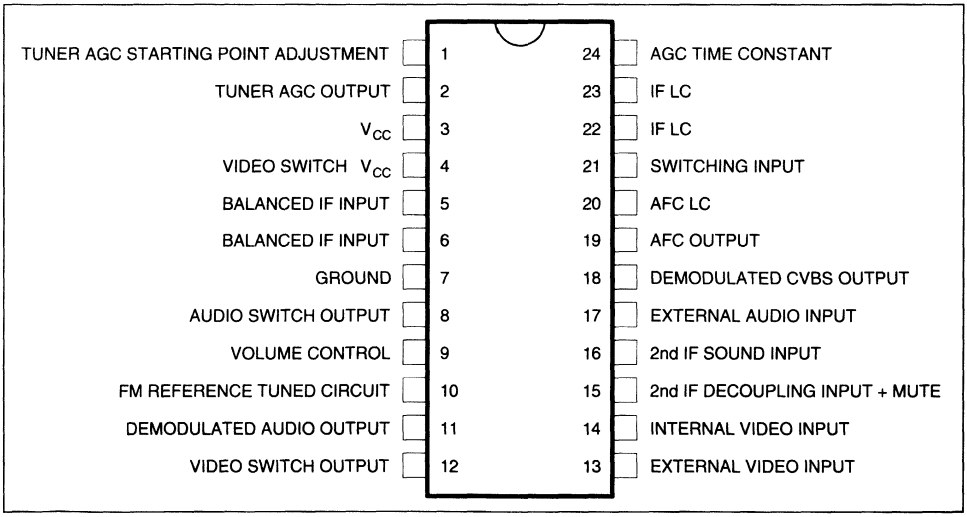
SHRINK DIP24
(Plastic Package)

ORDER CODE : TDA8222

DESCRIPTION

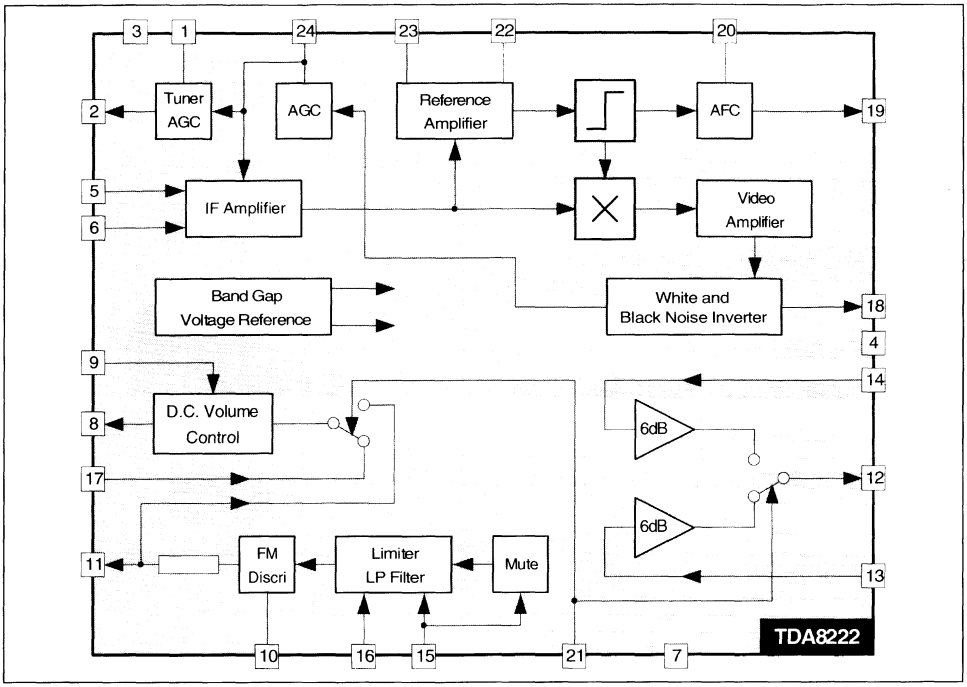
The TDA8222 is a video and sound IF circuit in Shrink DIP24 package for color and black and white TV sets. It is intended to operate with a negatively modulated vision carrier and frequency modulated sound carrier. It incorporates video and audio switches compatible with SCART european norm.

PIN CONNECTIONS



8222-01.EPS

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The IC consists of the following parts (see block diagram):

- Three stages gain controlled wide band amplifier
- Quasi-synchronous demodulator
- Video amplifier with white and black noise inverter
- AGC circuit which operates on top sync level
- Analog AFC circuit
- FM discriminator
- Mute function
- Video and audio switches
- DC volume control

IF Amplifier

It consists of three cascaded AC coupled differential gain stages. The gain of each amplifier is controlled by the AGC voltage. The global AGC range is more than 60dB. Thanks to the internal AC coupling no DC feedback is required.

Demodulation

It is a quasi-synchronous type with passive carrier regeneration done by an external tuned circuit, and a limiter amplifier.

Video Amplifier

The video amplifier provides a $2V_{PP}$ video signal to the output with a good phase and amplitude frequency response.

White and Black Noise Inverter

A fixed 3.2V level is inserted when a white spot above 4.5V (measured on the video output Pin 18) happens, this prevents from very noisy signal on the screen.

A fixed 2.5V level is inserted when a black spot below 1.3V happens, this to avoid synchronization on parasitic signals.

AGC Circuit

The AGC detector operates on top sync level, an external capacitor on Pin 24 controls the time constant.

The voltage on this capacitor is converted into a current to control the amplifier stage.

Tuner AGC

It sinks a current to control the gain of the tuner RF amplifier. Its starting point is adjusted by an external potentiometer (Pin 1).

AFC Circuit

It is a FM demodulator stage which delivers on Pin 19 a current proportional to the frequency difference between the IF input signal and the reference IF frequency of the external LC on Pin 20. This current is converted into a voltage by means of a resistor network.

FM Demodulation

It consists of a three stage limiter amplifier in order to reject the amplitude modulation and a quadrature demodulator. The deemphasis filter is built with an internal resistor and an external capacitor on Pin 11.

Mute Function

It is an internal switch to cut-off the internal audio signal. It acts when a level below 2.1V is applied on Pin 15. When no mute, the Pin 15 must be driven with a high DC impedance.

Video and Audio Switches

They are both controlled by the Pin 21 voltage.

Internal sources or external sources can be sent to the outputs (Pin 12 for video and Pin 8 for audio). The internal signals are selected by a control level below 2.5V on Pin 21, the external ones by a control level above 5V.

The gain of the video switch is 6dB for both internal and external signals.

The gain of the audio switch is 0dB for the maximum volume.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	13.5	V
V_X	Tuner AGC Voltage	V_{CC}	V
T_{stg}	Storage Temperature	-40, +150	°C
T_{oper}	Operating Temperature	0, +70	°C

8222-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	75	°C/W

8222-02.TBL

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV$_{RMS}$ top sync, D = 90%, Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV$_{RMS}$, f_m = 1kHz, Audio BW = 20kHz, $\Delta f = \pm$ 25kHz, Volume attenuation = 0dB, R_{load} on Pin 12 = 1kΩ, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Voltage Operating Range		8.1	9	12.6	V
I_{CC}	Supply Current	I(3) + I(4), V_{CC} = 9V	24	38	52	mA
IF AMPLIFIER						
	Input Sensitivity	Refer to test circuit		70		µV
R_{22-23}	Differential Input Resistance			1.5		kΩ
C_{22-23}	Differential Input Capacitance			2		pF
G_R	Gain Control Range			64		dB
DEMODULATED VIDEO OUTPUT (Pin 18)						
V_{A18}	Amplitude	Top sync to white	1.8	2.1	2.4	V_{PP}
V_{S18}	Top Sync Level	without output filter	1.6	1.9	2.2	V
BW	Bandwidth	See Figure 1	5	7		MHz

8222-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV$_{RMS}$ top sync, D = 90%, Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV$_{RMS}$, f_m = 1kHz, Audio BW = 20kHz, $\Delta f = \pm$ 25kHz, Volume attenuation = 0dB, R_{load} on Pin 12 = 1kΩ, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DEMODULATED VIDEO OUTPUT (Pin 18) (continued)						
D_G	Differential Gain	IF input = 5mV$_{RMS}$ top sync		3	7	%
D_P	Differential Phase			3	7	Degree
V_{18}	Residual Carrier Signal (RMS value)			1	10	mV
V_{18}	Residual 2nd Harmonic (RMS value)			2	20	mV
I_{18}	Internal Bias of Emitter Follower		3	5		mA
S/N	Signal to Noise Ratio	Note 1		55		dB
	Intermodulation 1.07MHz	Note 2		50		dB
V_{WTH}	White Noise Threshold Voltage	See Figure 5		4.5		V
V_{WIL}	White Noise Insertion Level	See Figure 5		3.2		V
V_{BTH}	Black Noise Threshold Voltage			1.3		V
V_{BIL}	Black Noise Insertion Level			2.5		V
AGC CIRCUIT						
I_{24C}	Charging Current		550	900	1200	µA
I_{24D}	Discharge Current		12	20	26	µA
C/D	Charging / Discharging Ratio			45		
TUNER AGC						
I_2	Sinked Current		1.2	1.9	2.6	mA
S_2	Current Slope	See FIgure 4		300		µA/dB
AFC						
	AFC Slope	See Figure 2, refer to test circuit		20		mV/kHz
FM SOUND DEMODULATION						
V_{16S}	Input Sensitivity	-3dB FM detected signal		60		µV
AMR	Amplitude Modulation Rejection	Note 3	40	53		dB
R_{16}	Limiter Input Resistance			1.2		kΩ
AUDIO OUTPUT (PIn 11)						
V_{11}	Detected Audio Output Signal			500		mV$_{RMS}$
THD	Total Harmonic Distortion			0.2	1	%
$\frac{S}{N}$	Signal to Noise Ratio	Note 4		68		dB
R_{11}	Internal Deemphasis Resistor		700	1000	1400	Ω
VOLUME CONTROL						
$V_{C\ range}$	Control Range	See Figure 3		80		dB

8222-04.TBL

Notes : 1. $\frac{S}{N} = 20 \text{ Log}_{10} \frac{V_{OUT} \text{ black to white}}{V_{N\ (RMS)}}$ at BW = 5MHz

2. Video carrier relative level = 0dB, Chroma subcarrier relative level = -3.2dB, Sound carrier relative level = -20dB.

3. AMR = $20 \text{ Log} \frac{V_{11}\ (mV_{RMS})}{V_{AM}\ (mV_{RMS})}$ (dB) where V_{AM} = output amplitude in AM for f_m = 1kHz and m = 30%

4. $\frac{S}{N} = 20 \text{ Log} \frac{V_{11}\ (mV_{RMS})}{V_N\ (mV_{RMS})}$ (dB)

ELECTRICAL CHARACTERISTICS (continued)
(T_{amb} = 25°C, V_{CC} = 9V, IF input = 10mV_{RMS} top sync, D = 90%, Video BW = 5MHz, Sound carrier input : 5.5MHz, 10mV_{RMS}, f_m = 1kHz, Audio BW = 20kHz, $\Delta f = \pm$ 25kHz, Volume attenuation = 0dB, R_{load} on Pin 12 = 1kΩ, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO SWITCH						
R_{17}	Input Resistance		40	65		kΩ
C_{Rtk}	Crosstalk		70	80		dB
EXTHD	THD on External Signal	V_{IN} = 2V_{RMS}, Attenuation = 0dB		0.05	0.3	%
VIDEO SWITCH						
$V_{DC\ 13\text{-}14}$	DC Input Level	No signal	1.6	1.9	2.2	V
$V_{S\ 13\text{-}14}$	Top Sync Clamp Level			1.8		V
V_{12}	DC Output Level	No signal	0.7	1.0	1.3	V
$V_{S\ 12}$	Top Sync Clamp Level			0.85		V
	Crosstalk			55		dB
$G_{13\text{-}14\ ,\ 12}$	Gain from inputs to output	V_{IN} = 1V_{PP}	5.5	6	6.5	dB
	Output Swing		4.5			V
$I_{13\text{-}14}$	Input Current	$V_{13\text{-}14}$ = $V_{DC\ 13\text{-}14}$ + 1.5V		1	5	µA
VBW	Bandwidth	V_{IN} = 1V_{PP}		15		MHz
SWITCHING INPUT						
$V_{21\ ext}$	External Input Selection Level		5			V
$V_{21\ int}$	Internal Input Selection Level				2.5	
I_{21}	Sourced Current		0		10	µA
MUTE						
V_{15}	Threshold Voltage			2.1		V
V_{15}	DC Level when mute disabled	High impedance controling circuit		2.8		V

f222-05.TBL

TEST CIRCUIT

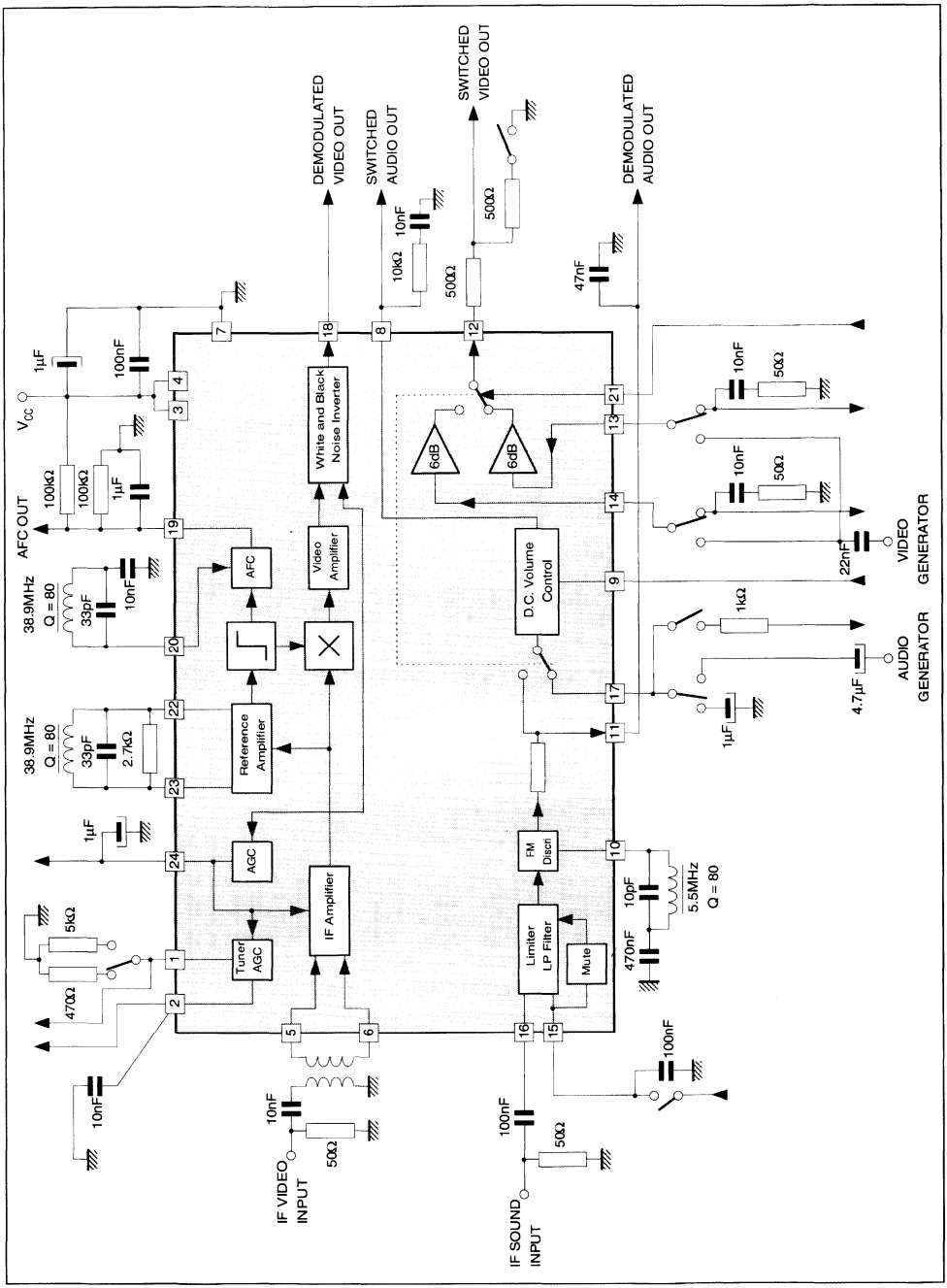


Figure 1 : Output Signal Bandwidth on Pin 18

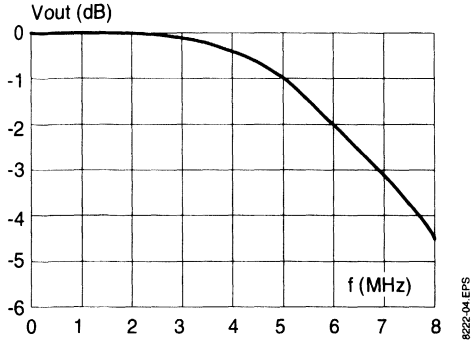


Figure 2 : AFC Voltage versus Input Frequency on Pin 19

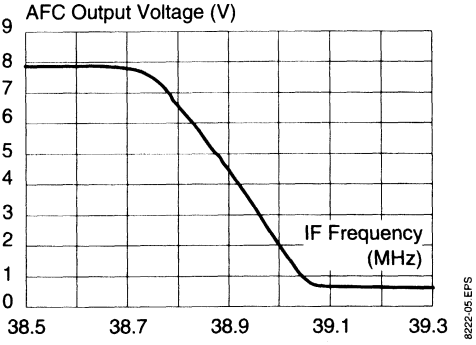


Figure 3 : Volume Control Attenuation versus Voltage on Pin 9

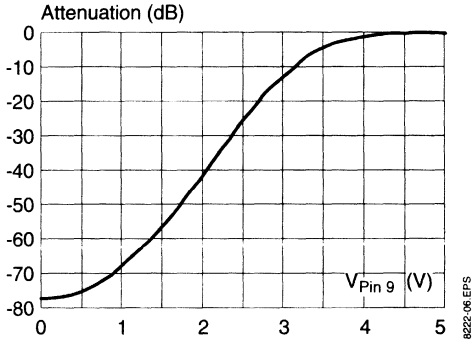


Figure 4 : Tuner AGC Output Current on Pin 2

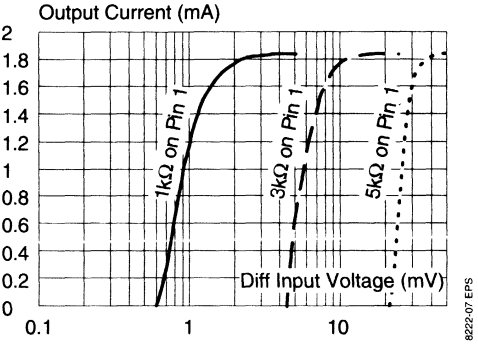
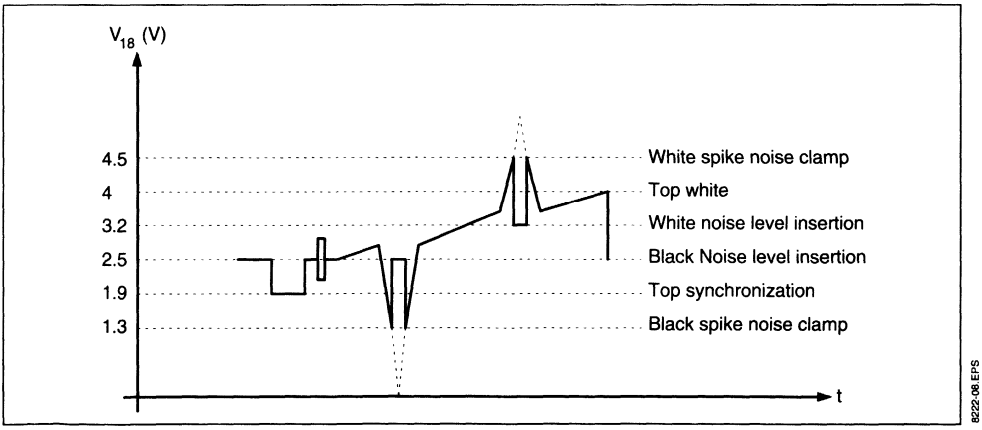
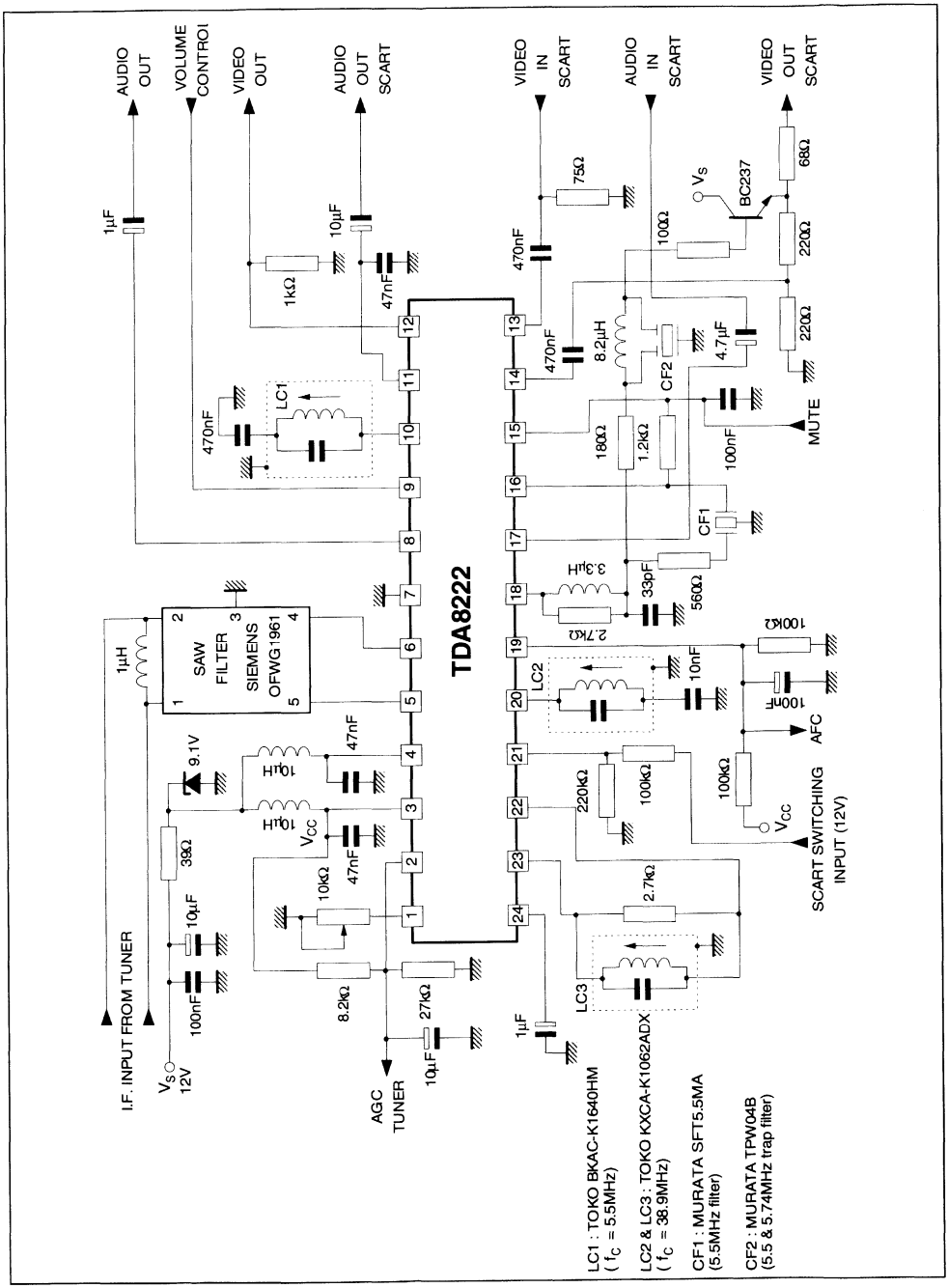


Figure 5 : Black and White Noise Inverter



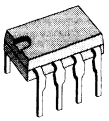
TYPICAL APPLICATION (for B/G standard)



AUDIO, VIDEO and SOUND SWITCHES

AUDIO SWITCH AND DC VOLUME CONTROL FOR TV

- TWO AUDIO INPUTS WITH SWITCHING FACILITIES FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN 50049
- DC VOLUME CONTROL



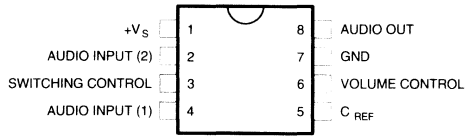
DIP8
(Plastic Package)

ORDER CODE : TDA8196

DESCRIPTION

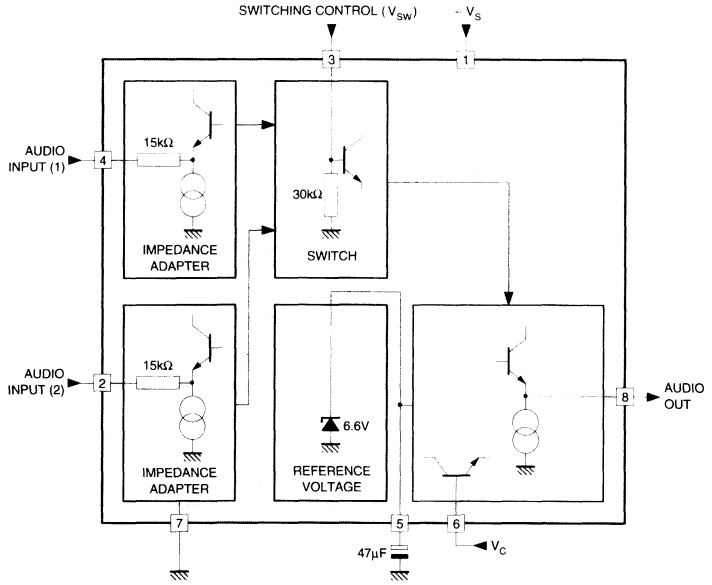
The TDA8196 is a monolithic integrated circuit in DIP8 package intended for TV applications.

PIN CONNECTION (top view)



8196-01.EPS

BLOCK DIAGRAM



8196-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 1)	16	V
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 125	°C
T_{amb}	Operating Ambient Temperature	0 to 70	°C

8196-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

8196-02.TBL

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1	V_i = 0, V_C = 0.5V		12		mA
V_R	Reference Voltage	5			6.6		V
V_{SW}	Switching Voltage Audio Input 1 Audio Input 2	3		 0 8		 5 12	 V V
R_{SW}	Switching Input Resistance	3	V_{SW} = 12V	20	30		kΩ
C_{SW}	Switching Input Capacitance	3				10	pF
C_t	Crosstalk between Switched Inputs		Selective Volmeter (B_W = 8Hz), see Fig.1	70	90		dB
V_i	Audio Input Amplitude (1 or 2)	4 2			0.5	2	V_{RMS}
R_i	Audio Input Resistance (1 or 2)	4 2		 10	 13		 kΩ
K_{min}	Output / Input Gain for Max Vol				0		dB
R_O	Audio Output Resistance	8			0.2	1	kΩ
K_V	Attenuation Range		Selective Volmeter (B_W = 8Hz), see Fig.2	70	90		dB
V_C	Control Voltage Range $K_V = K_{MAX}$ (Vol. min) $K_V = K_{MIN}$ (Vol. max)	6			0.5 4.5		V V
THD	Distortion	8	V_i = 2 V_{RMS} @ V_C = 4.5V		0.4	1	%
En	Output Noise Level	8	DIN45405 V_C = 0.5V Weighted		40		μV_{RMS}
En	Output Noise Level	8	DIN45405 V_C = 4.5V Weighted		120		μV_{RMS}
$\frac{K_V}{\Delta T_a}$	Vol. Attenuation Thermal Drift		T_{amb} = 0 to 70°C K_V = 30dB, see Fig.3		0.04		dB/°C
SVR	Supply Voltage Rejection	8	V_C = 0.5V, f = 100Hz V_{ripple} = 1V_{PP} Selective Volmeter (B_W = 8Hz), see Fig.4 and 5		38		dB
V_O	Output DC Shift	8	V_C = 0.5 + 4.5V, V_i = 2 V_{RMS}		0.25		V

8196-03.TBL

TEST CIRCUIT

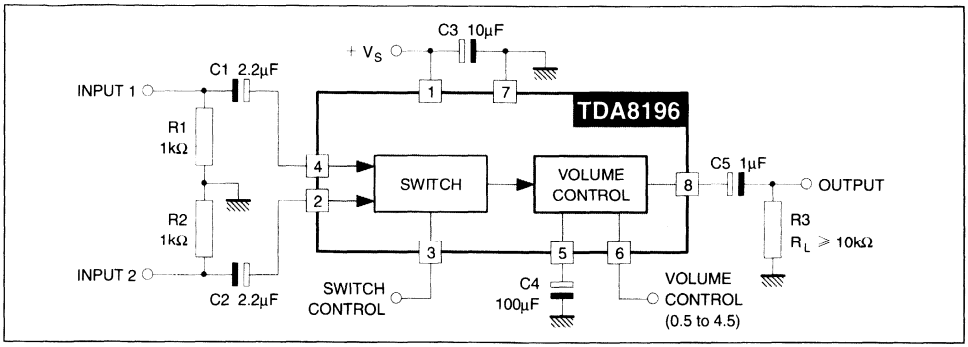
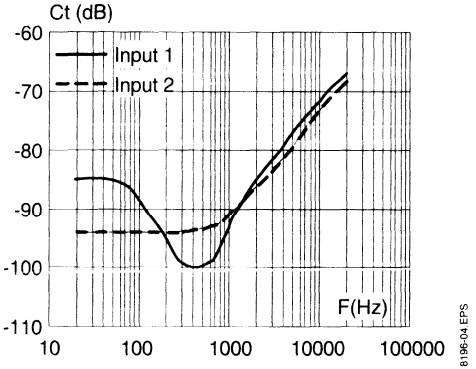


Figure 1 : TDA8196 Crosstalk

Figure 2 : Output Attenuation versus DC Volume Control Voltage



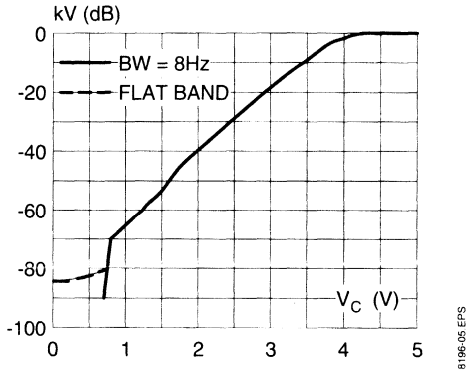
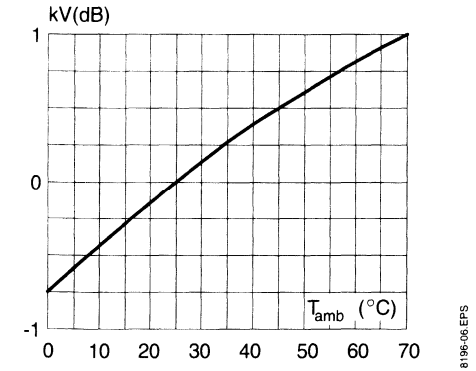


Figure 3 : K_V Drift vs. T_{amb} Variation

Figure 4 : SVR vs. Ripple Frequency



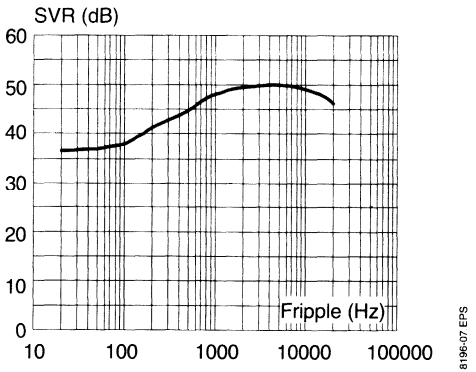
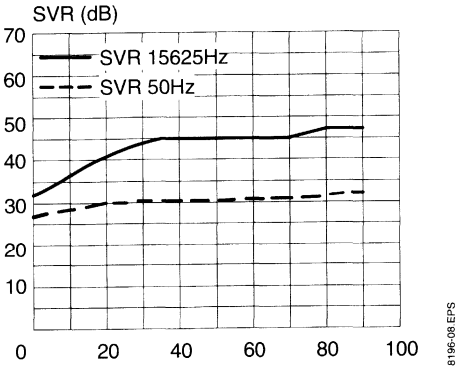
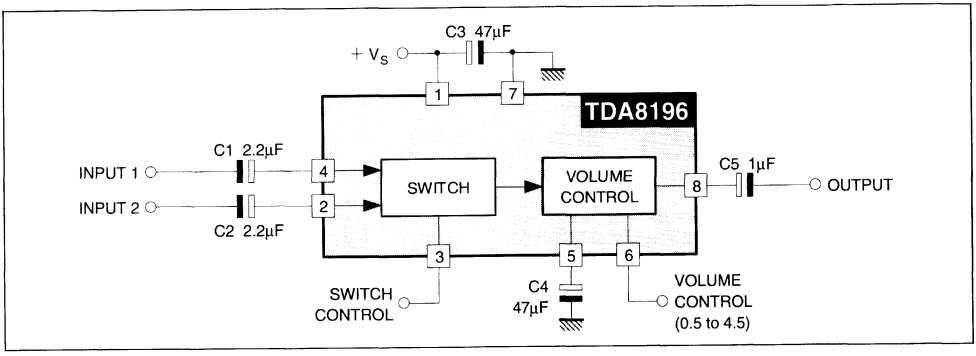


Figure 5 : SVR vs. Volume Attenuation



APPLICATION CIRCUIT

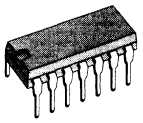


SGS-THOMSON MICROELECTRONICS

TDA8198

DOUBLE AUDIO SWITCH AND DC VOLUME CONTROL FOR TV

- A DOUBLE TWO-INPUT CIRCUITS WITH SWITCHING FACILITIES
- A DOUBLE DC VOLUME CONTROL
- 12dB MAXIMUM GAIN
- 90dB SIGNAL DYNAMIC RANGE



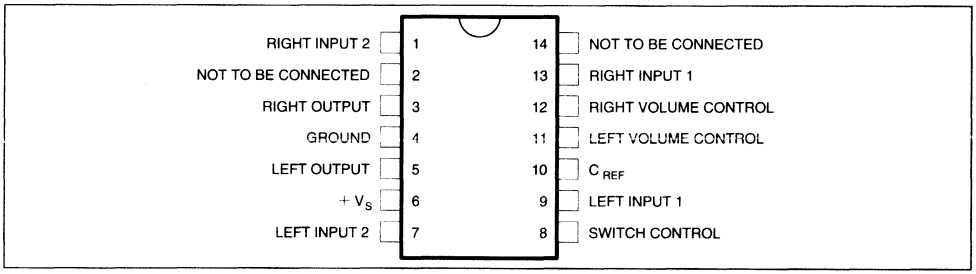
DIP14
(Plastic Package)

ORDER CODE : TDA8198

DESCRIPTION

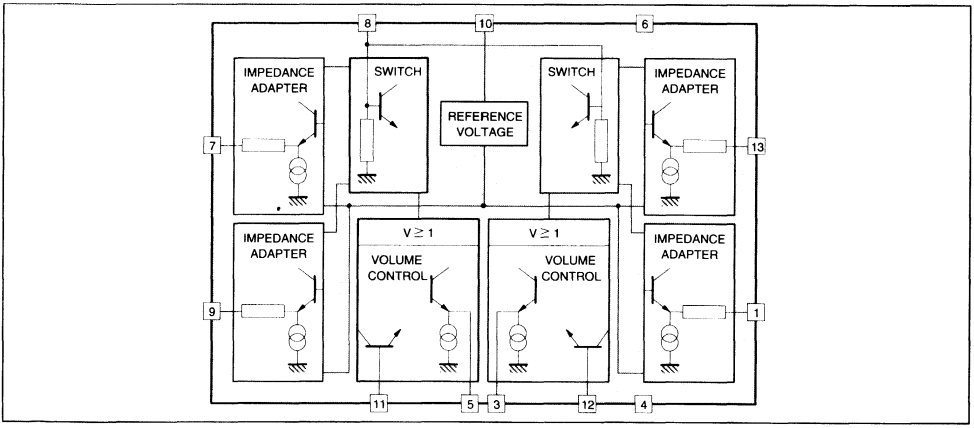
The TDA8198 is a monolithic integrated circuit in DIP14 package intented for TV applications which provides Audio switching facilities between two double inputs including DC volume control.

PIN CONNECTIONS



8198-01.EPS

BLOCK DIAGRAM



8198-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{STG}	Storage Temperature	-55, +125	°C
T_{OP}	Operating Ambient Temperature	0, +70	°C

8198-01.TBL

ELECTRICAL CHARACTERISTICS

Measured according to the following conditions, unless otherwise specified : $T_{AMB} = 25°C$, $V_S = +12V$.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range	10.8	12	13.2	V
I_S	Supply Current ($V_{IN} = 0$, $V_C = 0.5V$)		24	32	mA
V_R	Reference Voltage		6.9		V
V_M	Mode Selection Voltage Audio 1 Audio 2	 9.5		 5 V_S	V
R_{SW}	Switching Input Resistance	15	30		kΩ
V_I	Audio Input Amplitude		0.125	0.3	V_{RMS}
Δk	DC Volume Control Range @ $V_I = 0.3V_{RMS}$	70	90		dB
k_{MIN}	Output/Input Gain for Maximum Volume ($V_C = 5V$)		12		dB
dK	Gain Difference between Channels at $V_C = 5V$		0		dB
V_C	Voltage Control Range $k = k_{MAX}$ (volume minimum) $k = k_{MIN}$ (volume maximum)	 5		 0.5	V
THD1	Distortion for $V_I = 0.25V_{RMS}$ at Maximum Volume		0.3	1	%
THD2	Distortion for $V_O = 1.2V_{RMS}$			5	%
C_T	Crosstalk between Switched Inputs		80		dB
C_C	Crosstalk between Channels 1 & 2		70		dB
R_I	Audio Input Resistance		22		kΩ
R_O	Audio Output Resistance		10	300	Ω
	Output Noise Level @ $V_C = 5V$ (weighted) (curve : DIN45 405)		300		μV_{RMS}
I - V_C	Volume Control Input Current (Pins 11 and 12) at $V_C = 5V$		-12		μA
	Volume thermal stability ($k = 30dB$, $0 < T_{AMB} < 60°C$)		0.04		dB/°C

8198-02.TBL

Figure 1 : Gain versus Volume Control

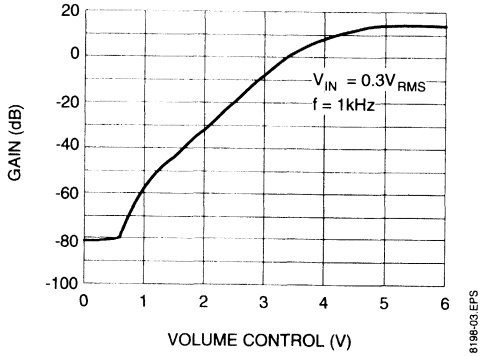


Figure 2 : Distortion versus Volume Control

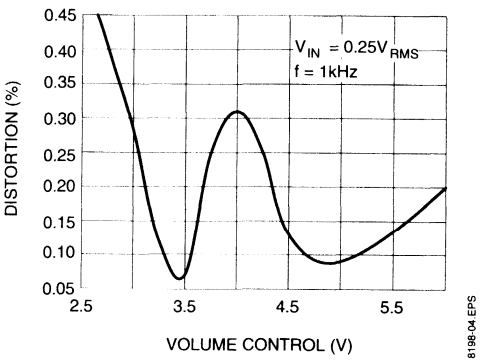


Figure 3 : Distortion versus Voltage Input

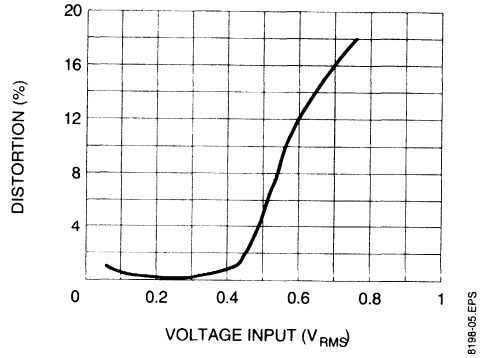


Figure 4 : Supply Voltage Rejection

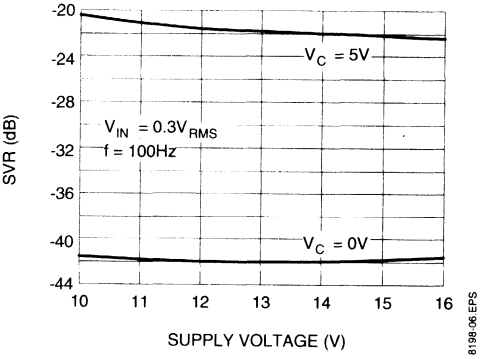


Figure 5 : Volume Control Current versus Voltage (pins 11 - 12)

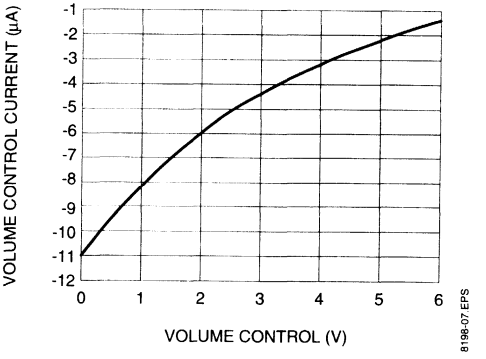
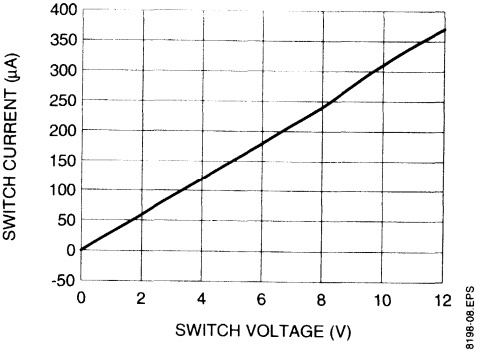
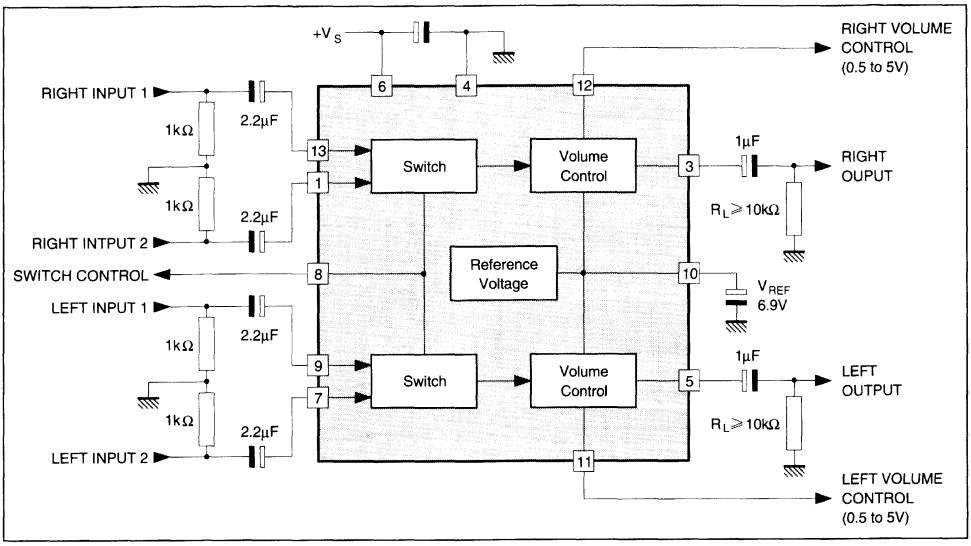


Figure 6 : Switch Current versus Voltage (pin 8)

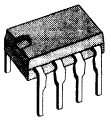


APPLICATION DIAGRAM



STEREO AMPLIFIER AND DC VOLUME CONTROL FOR TV

- STEREO CIRCUIT
- DC VOLUME CONTROL
- 12dB MAXIMUM GAIN



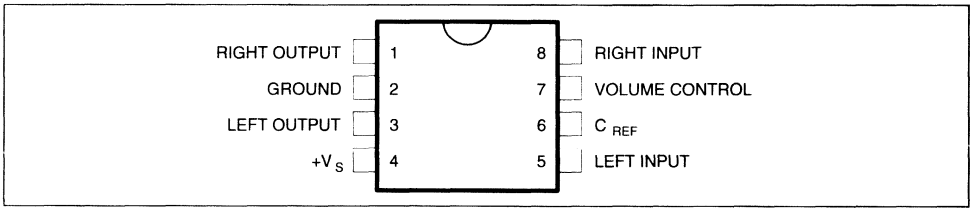
DIP8
(Plastic Package)

ORDER CODE : TDA8199

DESCRIPTION

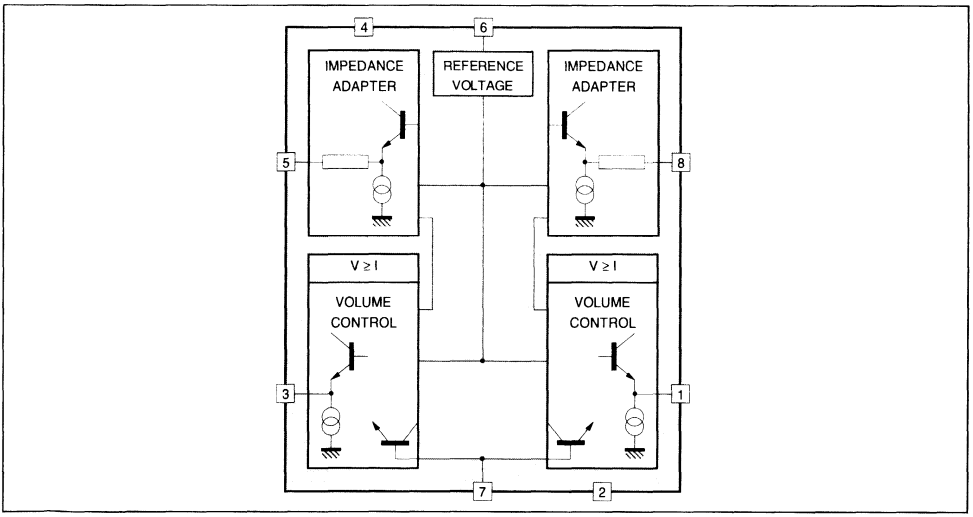
The TDA8199 is a monolithic integrated circuit in DIP8 package intented for TV applications.

PIN CONNECTIONS



8199-01.EPS

BLOCK DIAGRAM



8199-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{stg}	Storage Temperature	- 55, + 125	°C
T_{oper}	Operating Ambient Temperature	0, + 70	°C

8199-01.TBL

ELECTRICAL CHARACTERISTICS

Measured according to the following conditions : T_{amb} = 25°C, V_S = +12V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	10.8	12	13.2	V
I_S	Supply Current (V_{IN} = 0, V_C = 0.5V)		21	28	mA
V_{REF}	Reference Voltage		6.9		V
V_i	Audio Input Amplitude		0.125	0.5	V_{RMS}
THD1	Distortion for V_I = 0.25 V_{RMS} at Max. Volume		0.35	1	%
THD2	Distortion for V_O = 2 V_{RMS}			5	%
ΔK	DC Volume Control Range at V_I = 0.5 V_{RMS}	70	90		dB
Kmin	Output/Input Gain for Max. Volume (V_C = 5V)		12		dB
dK	Gain Difference between Channels at V_C = 5V		0		dB
C_C	Crosstalk between Channels (R_L > 10kΩ and F = 1kHz)		70		dB
R_I	Audio Input Resistance		22		kΩ
R_O	Audio Output Resistance		0.3	1	kΩ
	Output Noise Level at VC = 5V (weighted curve : DIN45405)		300		μV_{RMS}
	Volume Control Input Current (Pin 7) at V_C = 0V		- 25		μA
	Volume Thermal Stability (K = 30dB, 0 < T_{amb} < 60°C)		0.04		dB/°C

8199-02.TBL

Figure 1 : Gain versus Volume Control

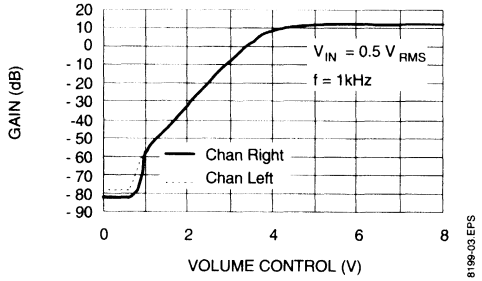


Figure 2 : Distortion versus Volume Control

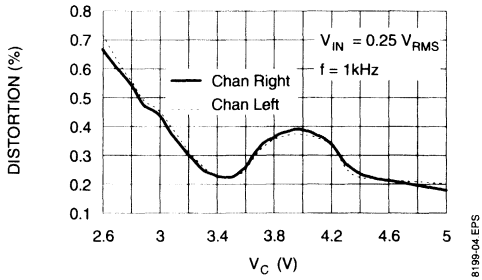


Figure 3 : Distortion Rate versus Voltage Input

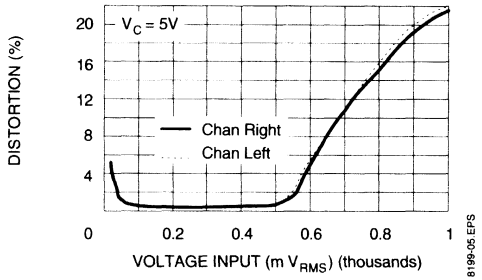
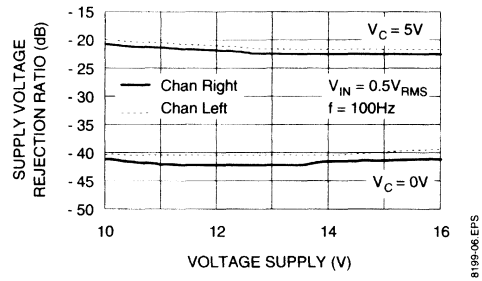
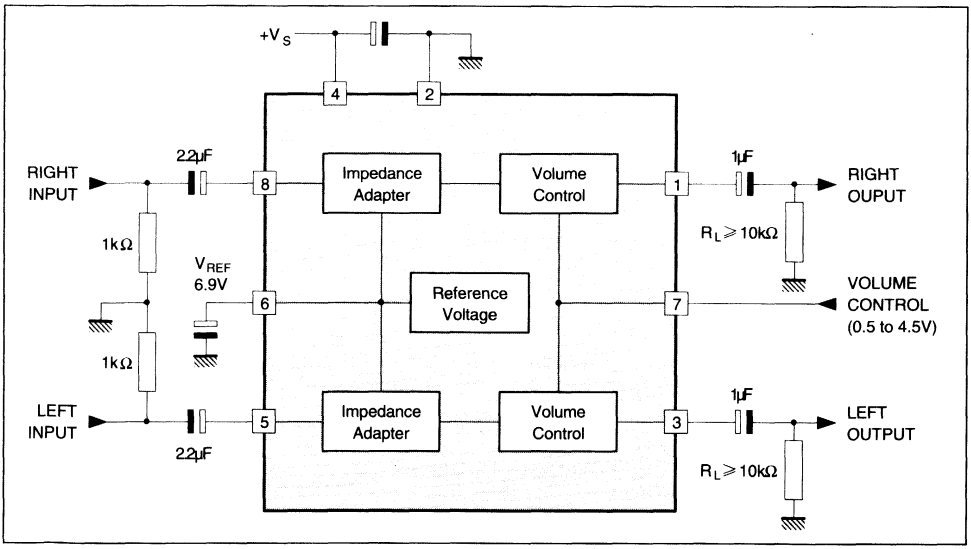


Figure 4 : Supply Voltage Rejection



APPLICATION DIAGRAM

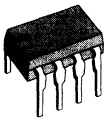


SGS-THOMSON MICROELECTRONICS

TEA2014A

VIDEO SWITCH

- 1 VIDEO OUTPUT 75 Ω- 1 V_{PP} NOT SWITCHED
- 1 SWITCHED VIDEO OUTPUT 2 V_{PP}
- VIDEO CROSSTALK : 50 dB TYPICAL
- SHORT CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- CLAMPED VIDEO INPUTS



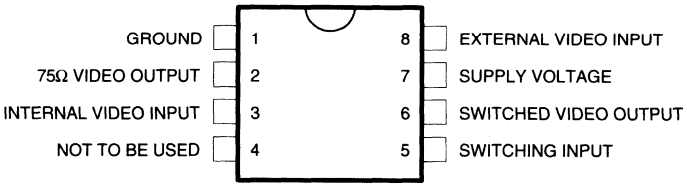
DIP8
(Plastic package)

ORDER CODE : TEA2014A

DESCRIPTION

This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA2014A is supplied in a DIP8.

PIN CONNECTIONS



2014A-01.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{oper}	Operating Temperature with Load > 150 Ω on PIN 2 with Load = 75 Ω on PIN 2	 0, + 100 0, + 70	°C
T_j	Junction Temperature	– 40, + 150	°C
T_{stg}	Storage Temperature	– 40, + 150	°C
–	Minimum DC Load Resistor PIN 6 Minimum DC Load Resistor PIN 2	600 75	Ω Ω

2014A-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Typ.	90	°C/W

2014A-02.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, V_{CC} = 9 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	8	–	14	V
I_{CC}	Supply Current (no load on Pin 2 and Pin 6)	–	–	20	mA
I_{CC}	Supply Current (with 75 Ω Pin 2.1, with 600 Ω between Pin 6.1)	–	45	–	mA
P_{tot}	Total Power Dissipation with Load	–	400	–	mW
INPUTS (pin 8 and pin 3)					
–	Internal Video Input Swing from Picture IF (positive Video)	–	–	4.5	Vpp
–	Internal Video Input Impedance (positive video)	50	–	–	kΩ
–	Internal Video Input Bias Current (positive video)	6	25	40	µA
–	External Video Input Swing (positive video)	–	–	2	Vpp
–	External Video Input Impedance (positive video)	50	–	–	kΩ
SWITCHED OUTPUT (pin 6) - R_{LOAD} = 600 Ω					
–	Video Output Swing	4	–	–	Vpp
–	Video Output Dynamic Impedance	–	–	25	Ω
–	Video DC Output Voltage (sync. pulse level note 1)	1.7	2	2.4	V
–	Video Bandwith Pin 6 – from Internal Input Pin 3 (– 1 dB)	6	–	–	MHz
–	Video Bandwith Pin 6 – from External Input Pin 8 (– 3 dB)	6	–	–	MHz
–	Output Gain Pin 6 – Pin 8	+ 5	+ 6	+ 7	dB
–	Output Gain Pin 6 – Pin 3	– 1	– 0.5	0	dB
EXTERNAL OUTPUT (pin 2) - R_{LOAD} = 75 Ω					
–	Video Output Swing	2.2	–	–	Vpp
–	Video Output Dynamic Impedance	–	10	–	Ω
–	Video DC Output Voltage (sync. pulse level , note)	1.7	2	2.4	V
–	Video Bandwidth (– 1dB)	6	–	–	MHz
–	Video Output Gain (pin 2 – pin 3)	– 1.8	– 1	– 0.4	dB
SWITCHING INPUT (pin 5)					
–	Switching Input Unactive Low Level or Unconnected Pin (TV receiving)	0	–	3	V
–	Switching Input Active Level (ext. receiving)	7	–	V_{CC}	V
–	Switching Input Impedance	10	–	–	kΩ

2014A-03.TBL

Note : Use a video signal with a synchro pulse in order to make the clamp work in a correct way. (75Ω to the ground and 10µF in series).

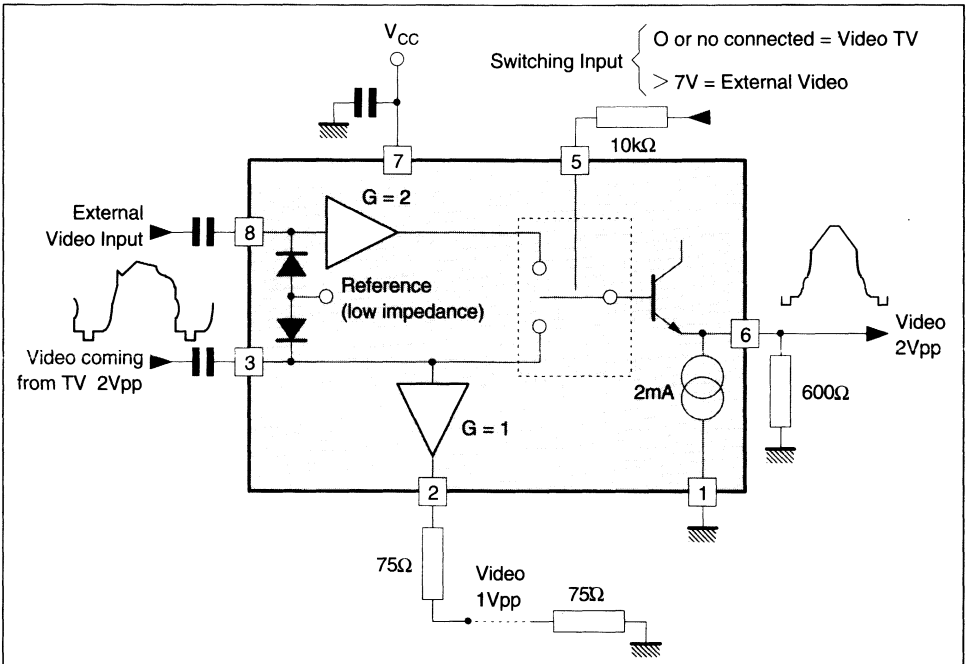
ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = + 25 °C, V_{CC} = 9 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
OTHER DYNAMIC FEATURES					
–	Video rejection Between Two Inputs 1MHz 1kHz	 – – 50	 – 50 –	 – –	 dB dB
–	Linearity Distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma – Chroma (test line 331)	 – – –	 2 2 5	 – – –	 % % %
–	Supply Voltage Rejection (1 kHz)	40	50	–	dB

2014A-04.TBL

TYPICAL APPLICATION



We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage higher than 9 V.

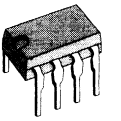
2014A-02.EPS

SGS-THOMSON MICROELECTRONICS

TEA2114

VIDEO SWITCH

- 2 VIDEO OUTPUTS WITH 150Ω LOAD DRIVE CAPABILITY
- DYNAMIC OUTPUT AMPLITUDE 4 V_{PP} ON EACH OUTPUT
- BANDWIDTH 18MHz TYP
- CLAMPED VIDEO INPUTS
- FULL PROTECTION AGAINST ESD



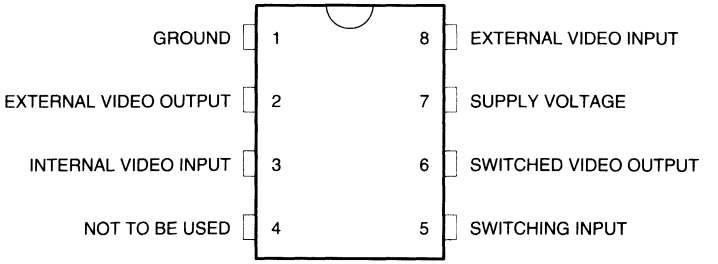
DIP8
(Plastic Package)

ORDER CODE : TEA2114

DESCRIPTION

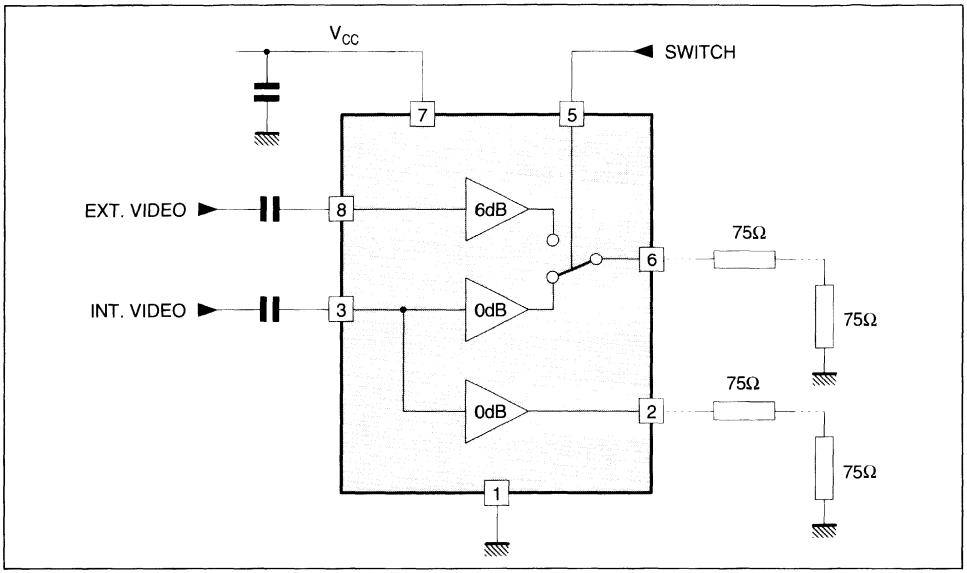
This integrated circuit provides general video switches. It is particularly intended for switching between the peri TV plug and video section of the sets. Its electrical performances make it suitable for wide bandwidth applications (Teletext, D2MAC).

PIN CONNECTIONS



2114-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14	V
T_j	Junction Temperature	- 40, + 150	°C
T_{stg}	Storage Temperature	- 40, + 150	°C

2114-01.TBL

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 8V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.5		13.2	V
I_{CC}	Supply Current (no load Pin 2 and Pin 6)		10	15	mA
I_{CC}	Supply Current (with load 150Ω on Pin 2 and Pin 6, no video on inputs)		25		mA

INPUTS (Pin 3 and Pin 8)

	Video Input Swing Pin3 Pin8		4 2		V_{PP} V_{PP}
V_{DCIN}	DC Level Input	1.6	1.9	2.2	V
I_{IN}	Input Bias Current (V_{DC} = V_{DCIN} + 1.5 V_{DC})		2	5	µA

2114-02.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25°C$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SWITCHED OUTPUT (Pin 6) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1.1	1.4	V
	Video Gain Pin 6 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal Pin 6 versus Pin 8, measured at 100kHz, 1 V_{PP} input signal	-0.8 5.5	-0.3 6	0.2 6.5	dB dB
	Video Bandwidth Pin 6 versus Pin 3, 1V_{PP} input signal Pin 6 versus Pin 8, 1V_{PP} input signal	18 12	27 18		MHz MHz
	Output Impedance (measured Pin 6)		1		Ω
EXTERNAL OUTPUT (Pin 2) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1.1	1.4	V
	Video Gain (Pin 2 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal)	-0.8	-0.3	0.2	dB
	Video Bandwidth (Pin 2 versus Pin 3, 1V_{PP} input signal)	18	27		MHz
	Output Impedance (measured Pin 2)		1		Ω
SWITCHING INPUT (Pin 5)					
	Output Current Selection Pin ($V_5 = 0V$)			10	µA
	Threshold Voltage	2.5	3.7	5	V
	Max DC Level			V_{CC}	V
OTHER DYNAMIC FEATURES ($R_{LOAD} = 150\Omega$ on Pin 2 and Pin 6)					
	Crosstalk (between any input, measured at 5MHz)		- 50		dB

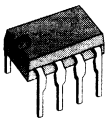
2114-03.TBL

SGS-THOMSON MICROELECTRONICS

TEA2124

VIDEO SWITCH

- 2 VIDEO OUTPUTS WITH 150Ω LOAD DRIVE CAPABILITY
- DYNAMIC OUTPUT AMPLITUDE 4 V_{PP} ON EACH OUTPUT
- BANDWIDTH 18MHz TYP
- CLAMPED VIDEO INPUTS
- FULL PROTECTION AGAINST ESD



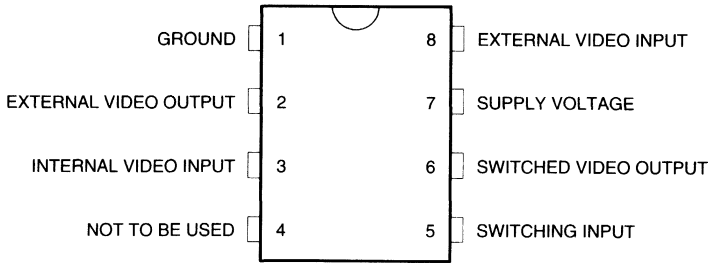
DIP8
(Plastic Package)

ORDER CODE : TEA2124

DESCRIPTION

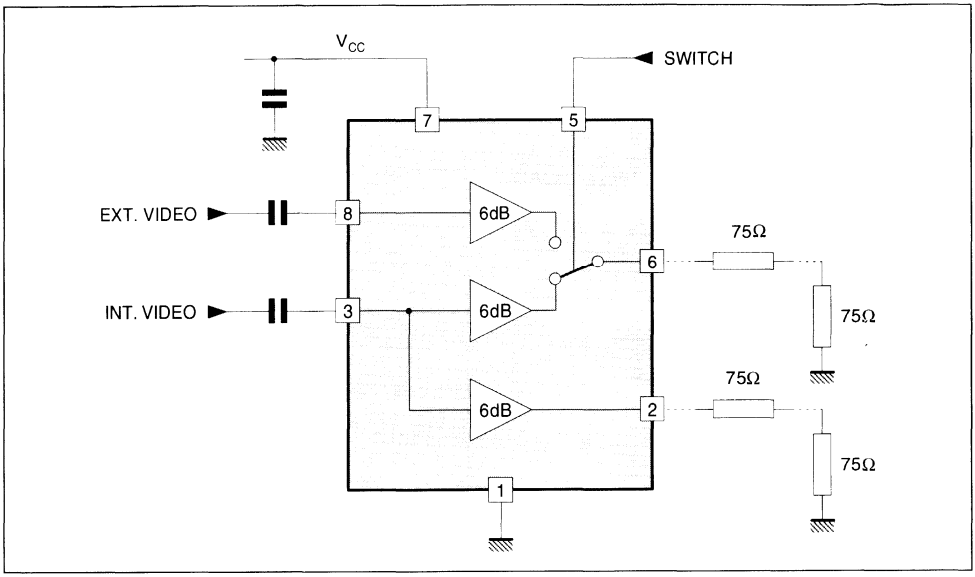
This integrated circuit provides general video switches. It is particularly intended for switching between the peri TV plug and video section of the sets. Its electrical performances make it suitable for wide bandwidth applications (Teletext, D2MAC).

PIN CONNECTIONS



2124-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14	V
T_j	Junction Temperature	- 40, + 150	°C
T_{stg}	Storage Temperature	- 40, + 150	°C

2124-01.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.5		13.2	V
I_{CC}	Supply Current (no load Pin 2 and Pin 6)		10	15	mA
I_{CC}	Supply Current (with load 150Ω on Pin 2 and Pin 6, no video on inputs)		25		mA
INPUTS (Pin 3 and Pin 8)					
	Video Input Swing		2		V_{PP}
V_{DCIN}	DC Level Input	1.6	1.9	2.2	V
I_{IN}	Input Bias Current ($V_{DC} = V_{DCIN} + 1.5\ V_{DC}$)		1	5	µA

2124-02.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_{CC} = 8V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SWITCHED OUTPUT (Pin 6) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1	1.3	V
	Video Gain (Pin 6 versus Pin 3 or Pin 8, measured at 100kHz, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (Pin 6 versus Pin 3 or Pin 8, 1V_{PP} input signal)	12	18		MHz
	Output Impedance (measured Pin 6)		1		Ω
EXTERNAL OUTPUT (Pin 2) ($R_{LOAD} = 150\Omega$)					
	Video Output Swing	3	4		V_{PP}
	DC Level Output	0.7	1	1.3	V
	Video Gain (Pin 2 versus Pin 3, measured at 100kHz, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (Pin 2 versus Pin 3, 1V_{PP} input signal)	12	18		MHz
	Output Impedance (measured Pin 2)		1		Ω
SWITCHING INPUT (Pin 5)					
	Output Current Selection Pin ($V_5 = 0V$)			10	µA
	Threshold Voltage	2.5	3.7	5	V
	Max DC Level			V_{CC}	V
OTHER DYNAMIC FEATURES					
	Crosstalk (between any input, measured at 5MHz) $R_{LOAD} = 150\Omega$ on Pins 2 and 6 $R_{LOAD} = 1k\Omega$ on Pins 2 and 6		 - 50 -55		 dB dB

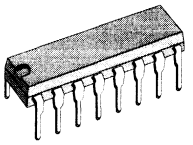
2124-03.TBL

SGS-THOMSON MICROELECTRONICS

TEA5114A

RGB SWITCHING CIRCUIT

- 25 MHz BANDWIDTH
- CROSSTALK : 55 dB
- SHORT CIRCUIT TO GROUND OR V_{CC} PROTECTED
- ANTI SATURATION GAIN CHANGING
- VIDEO SWITCHING



DIP16
(Plastic Package)

ORDER CODE : TEA5114A

DESCRIPTION

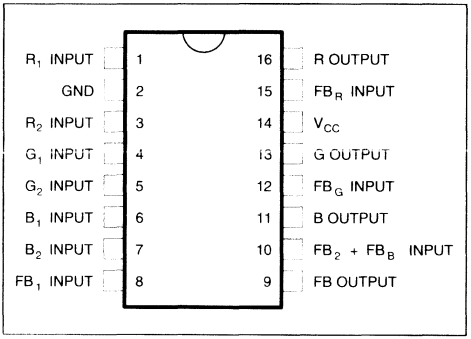
This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

An AC output signal higher than 2 Vpp makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

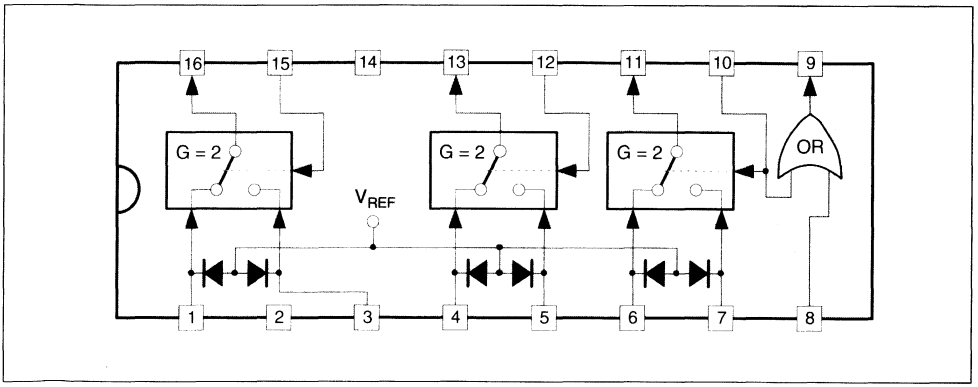
Fast blanking output is a logicial OR between FB1 (Pin 8) and FB2 (Pin 10).

PIN CONNECTIONS



5114A-01.EPS

BLOCK DIAGRAM



5114A-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		18	V
T_j	Junction Temperature		- 40 to 150	°C
T_{stg}	Storage Temperature		- 40 to 150	°C
Z_L	Minimum Load Resistor on Each Output	V_{CC} = 12 V V_{CC} = 10 V	300 150	Ω Ω
T_{amb}	Operating Ambient Temperature		0 to 70	°C

THERMAL DATA

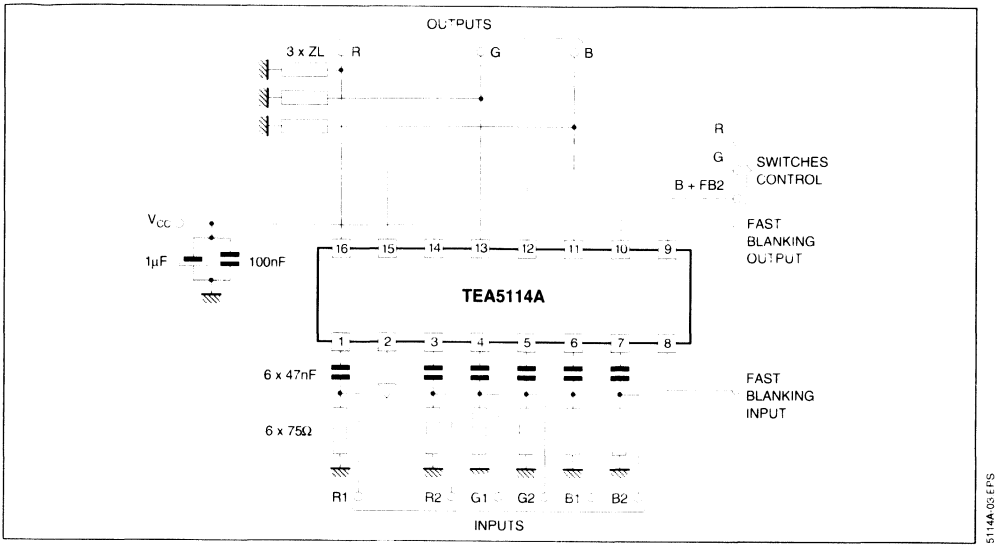
Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

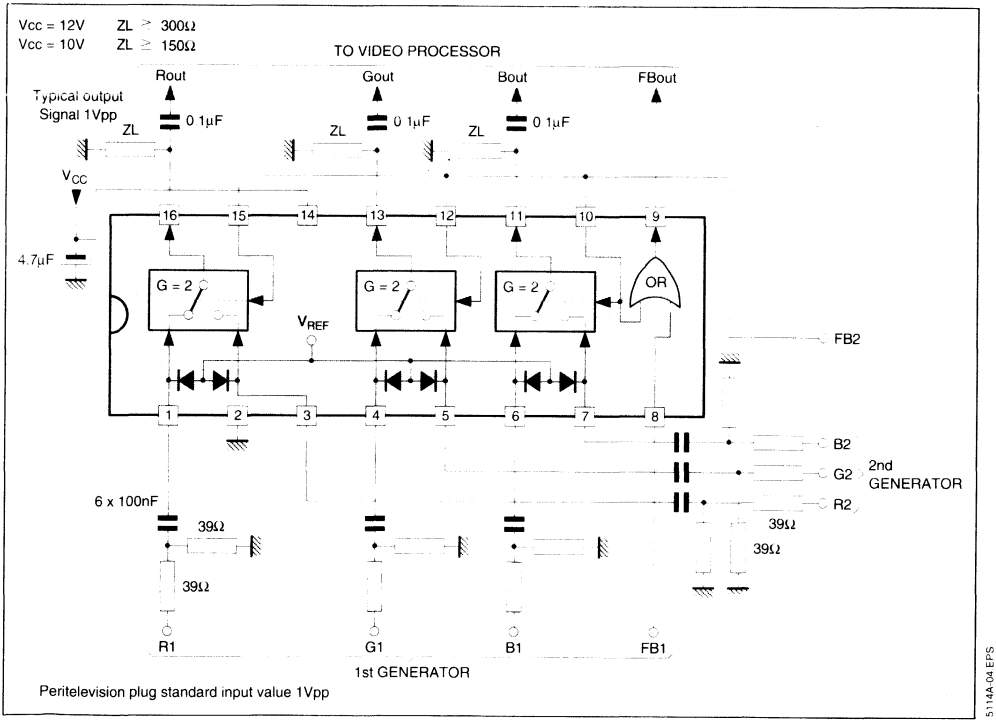
T_{amb} = 25 °C, V_{CC} = 12 V, Z_L (RGB) = 300 Ω
V_{CC} = 10 V, Z_L (RGB) = 150 Ω (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	9	12	13.2	V
I_{CC}	Supply Current without Load V_{CC} = 12 V	20	30	40	mA
V_{ON}	Black Level Output Voltage (on pins 11, 13, 16 square wave output signal 1 kHz - 1 Vpp) T_j = 25 °C (5mV/°C typical variation)	1.8	2.5	2.9	V
G_{RGB}	Gain of Each Channel Pins 11, 13, 16 F = 1 MHz, V_{in} = 0.5 V_{pp}	5	5.5	6	dB
B_{RGB}	Bandwidth (- 3 dB) V_O = 1 V_{pp}	18	22		MHz
V_{GC}	Threshold Output Voltage for Gain Changing (- 0.5 dB)	2			V_{pp}
V_R	Video Rejection between Two Inputs R, G or B F = 1 MHz Sinus V_O = 1 V_{pp}	50	55		dB
Z_{IRGB}	Input Impedance on Pins 1, 3, 4, 5, 6, 7 V_O = 1 V_{pp}	10			kΩ
Z_{ORGB}	R, G, B Output Impedance on Pins 11, 13, 16			15	Ω
T_{FB}	FB rising and falling time on pin 9 1 Vpp Input Voltage Pins 8, 10		20		ns
V_{IHFB}	FB High Level Input Voltage on Pins 8, 10, 12, 15	1		4	V
V_{ILFB}	FB Low Level Input Voltage on Pins 8, 10, 12, 15	0		0.4	V
Z_{IFB}	Input Impedance on Pins 8, 10, 12, 15	0.7	1	1.3	kΩ
V_{OHFB}	High Level FB Output Voltage (pin 9) Input 1 V on Pins 8, 10	0.8	1	1.2	V
V_{OLFB}	Low Level FB Output (pin 9) Input 0 V on Pins 8, 10			0.3	V
Z_{OFB}	FB Output Impedance Pin 9 High Level			30	Ω
T_{dFBRGB}	Delay Time between FB Inputs and R, G, B Switching		20		ns

TEST DIAGRAM



TYPICAL R, G, B SWITCHING APPLICATION

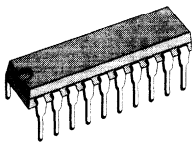


SGS-THOMSON MICROELECTRONICS

TEA5115

5 CHANNELS VIDEO SWITCH

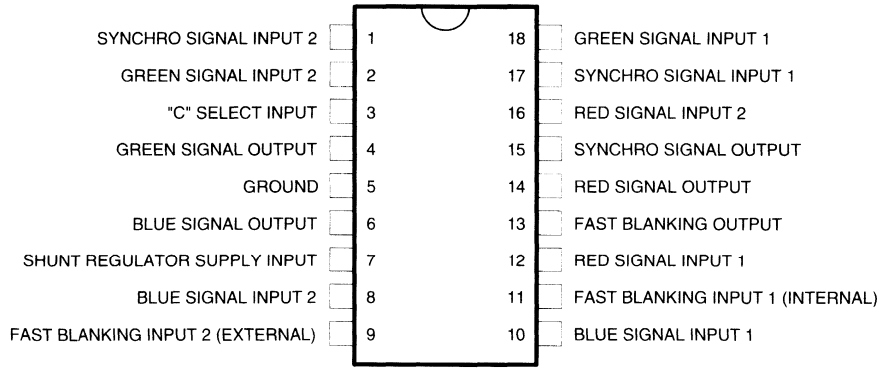
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- INDEPENDANT VIDEO OR SYNCHRONIZING SIGNAL SELECTION
- SIMULTANEOUS SWITCHING OF R, G, B AND FB SIGNALS BY FB1 INPUT (internal)



DIP18
(Plastic Package)

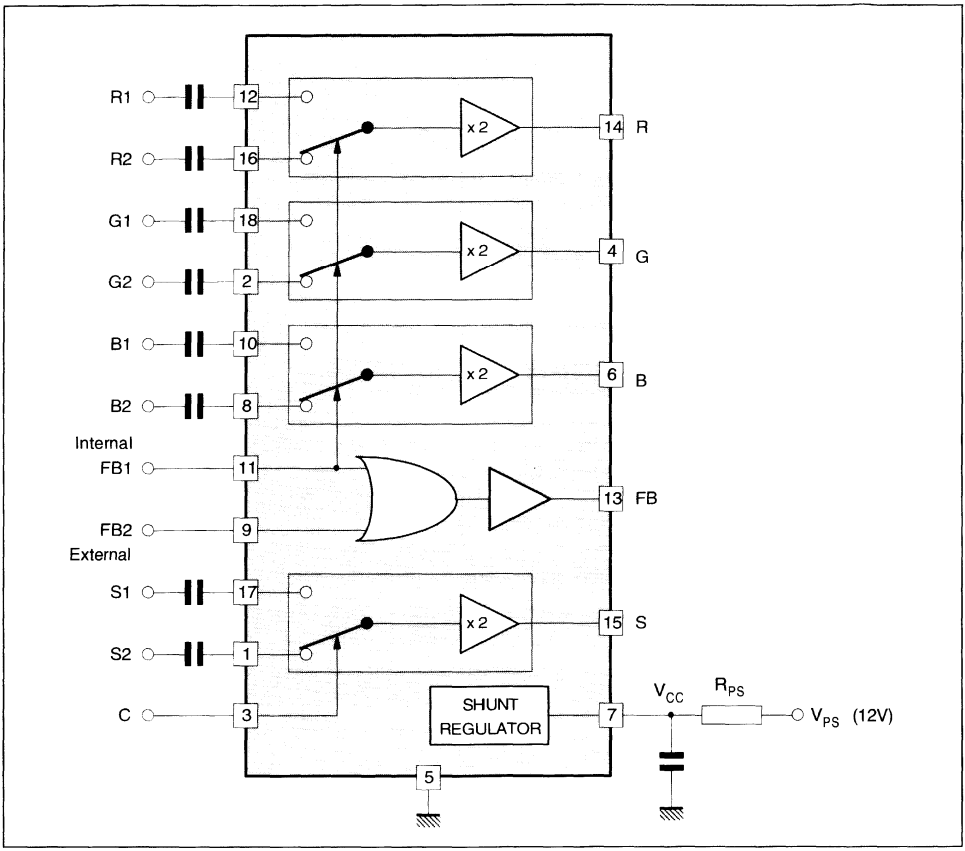
ORDER CODE : TEA5115

PIN CONNECTIONS



5115-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	− 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	− 40 to + 150	°C
T_{stg}	Storage Temperature	− 40 to + 150	°C

5115-01.TBL

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

5115-02.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω
(sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator	I_{CC} = 120 mA	6.3	6.7	7.2	V
		I_{CC} = 90 mA	6.2		7.3	V
		I_{CC} = 150 mA	6.2		7.3	V
R, G, B Switches (pins 4, 6, 14) (Time Measurement Conditions : Δ inputs RGB = 0.7 V_{pp} ; FB input pulse amplitude = 2 V)						
V_C	DC Output Voltage (no input voltage)	$T_{junction}$ = 25 °C		0.9	1.25	V
		$T_{junction}$ stabilized		1.2		
V_{AC}	Max Output Swing Voltage		2	4.0		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})		20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; f = 1MHz)		5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; f = 1 MHz)			0.1	0.5	dB
	Input Swing			0.7 V ± 3dB		
z_{ic}	DC Input Impedance			10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; f = 1MHz) with R_{load} = 300 Ω			10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; f = 1 MHz).		45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; f = 1 MHz).		40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.			10		ns
t_{sr1}	Switching rise time between FB1 input signal and R, G, B output signal.			60	110	ns
t_{sf1}	Switching fall time between FB1 input signal and R, G, B output signal.			10	40	ns
t_{sr2}	Switching rise time between FB2 input signal and R, G, B output signal.			10		ns
t_{sf2}	Switching fall time between FB2 input signal and R, G, B output signal.			10		ns
t_{d11}	R1, G1, B1 Decay Time			30		ns
t_{d12}				60		ns
t_{d21}	R2, G2, B2 Decay Time			45		ns
t_{d22}				40		ns
Fast Blanking Switch (pin 13) (time measurement conditions : FB input pulse amplitude = 2 V)						
V_{IL}	Low Level Input Voltage FB1 and FB2		- 0.5		0.45	V
V_{IH}	High Level Input Voltage FB2 External		1		V_{CC}+0.5	V
V_{IH}	High Level Input Voltage FB1 Internal		1.2		V_{CC}+0.5	V
V_{OL}	Low Level Output Voltage				0.6	V
V_{OH}	High Level Output Voltage	$T_{junction}$ = 25°C	1.4	1.7	3.5	V
		$T_{junction}$ stabilized	1.5	1.9		V
	Input Current (without load)			1.5		µA
	Dynamic Output Impedance : with R_{load} = 300 Ω			10		Ω
t_{FB1r}	Switching rise time between FB1 input and FB output.			120	160	ns
t_{FB1f}	Switching fall time between FB1 input and FB output.			25	60	ns
t_{FB2r}	Switching rise time between FB2 input and FB output.			70		ns
t_{FB2f}	Switching fall time between FB2 input and FB output.			35		ns
d_{tr}	Delay Between RGB Output Signal and FB Output Signal (rise time)			50	100	ns
d_{tf}	Delay Between RGB Output Signal and FB Output Signal (fall time)			20	40	ns

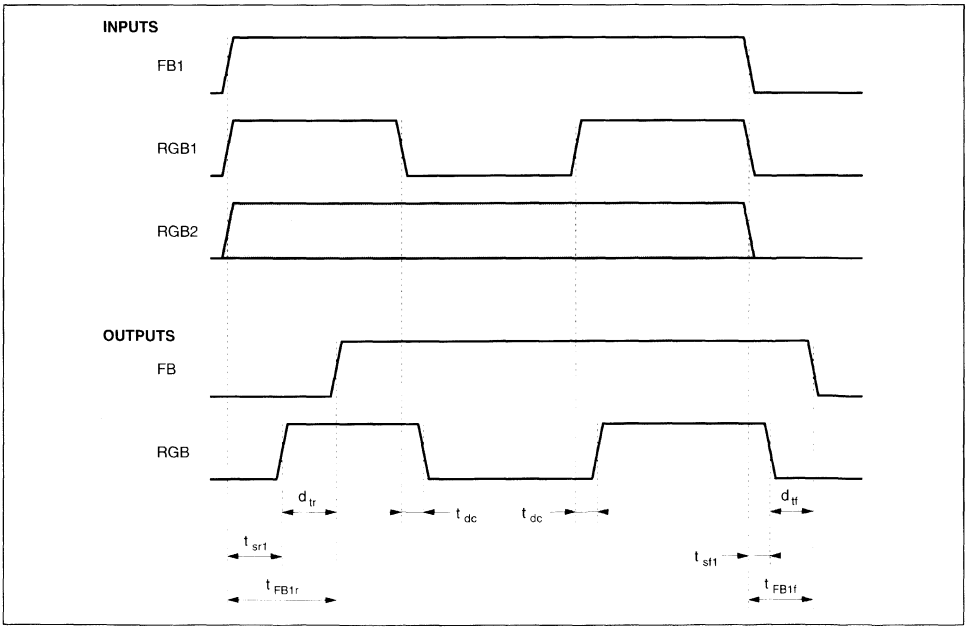
5-115-03 TBL

ELECTRICAL CHARACTERISTICS (continued)
T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω
(sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Video (or synchro) **Signal Switch** (pin 15)					
V_S	DC Output Voltage (no input voltage)				
	$T_{junction}$ = 25°C		0.9	1.25	V
	$T_{junction}$ stabilized		1.2		V
	Max Output Swing Voltage	2.6			V_{pp}
	DC Input Impedance		10		kΩ
	Dynamic Output Impedance (input voltage $1V_{pp}$; f = 1MHz) with R_{load} = 300 Ω		10		Ω
	Gain (input voltage 1 V_{pp} ; f = 1MHz)	5.5	6	6.5	dB
	Bandwidth (– 3 dB) (input voltage 1 V_{pp})	15	20		MHz
	Input Swing		1V ± 3 dB		
t_{cr}	Switching rise time between C input signal and S output signal (C pulse amplitude 3 V).		30		ns
t_{cf}	Switching fall time between C input signal and S output signal (C pulse amplitude 3 V).		10		ns
t_{dc}	Delay Time Between S Input and S Output (Δ input 0.7 V_{pp})		10		ns
Select Input "C" (pin 3)					
V_{IL}	Low Level Input Voltage	– 0.5		1	V
V_{IH}	High Level Input Voltage	2		V_{CC}+0.5	V
I_{IL}	Low Level Input Current (V_{IL} = 1 V)	– 0.6		– 0.1	mA
I_{IH}	High Level Input Current (V_{IH} = 3 V)			0.5	mA

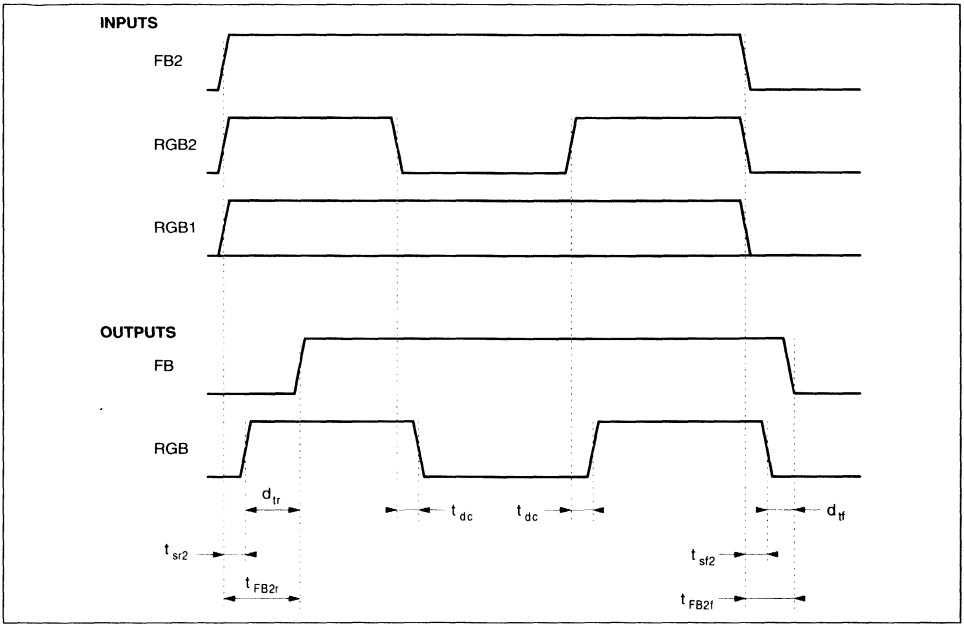
5115-04.TBL

FB2 = 0

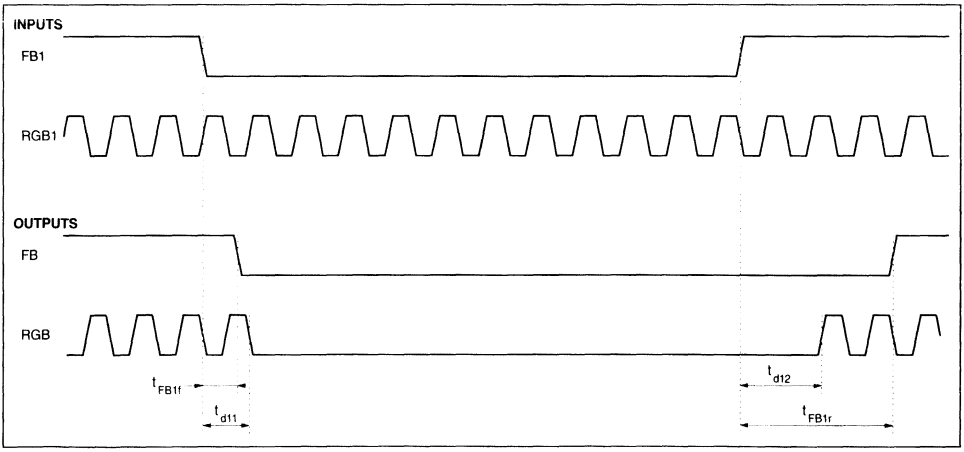


5115-03.EPS

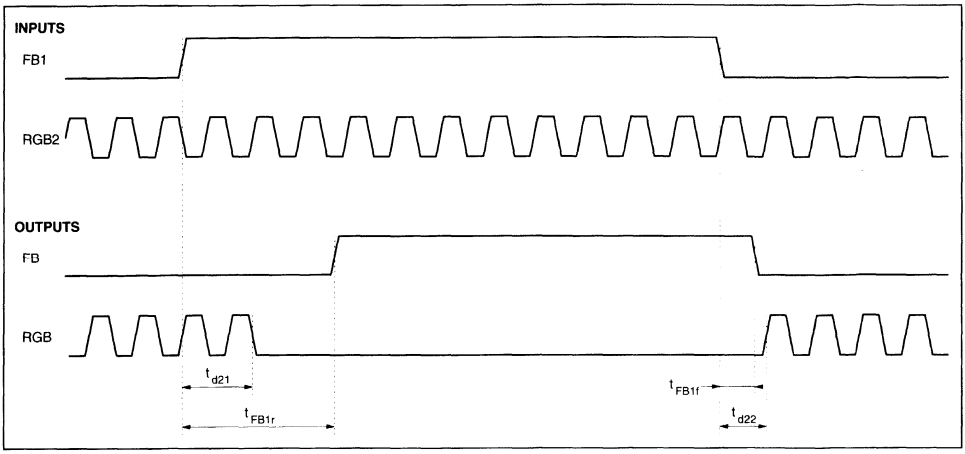
FB1 = 0

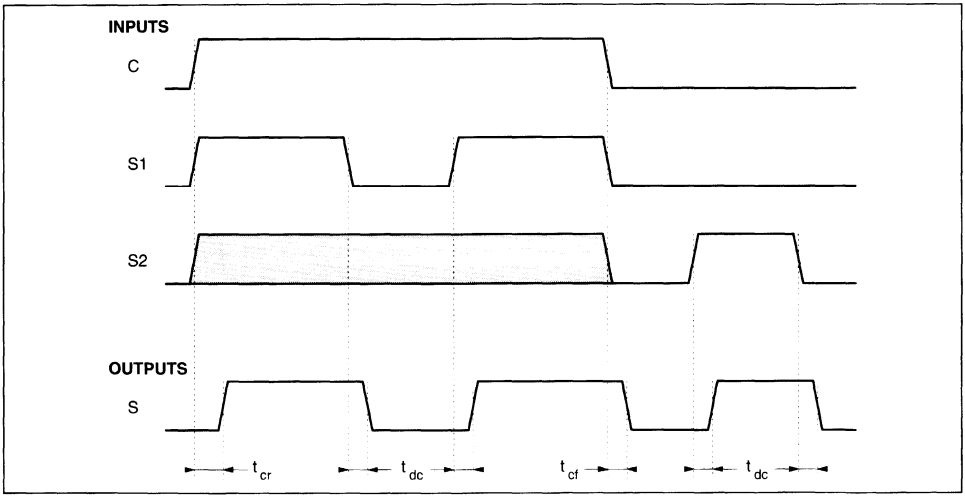


RGB2 = 0, FB2 = 0

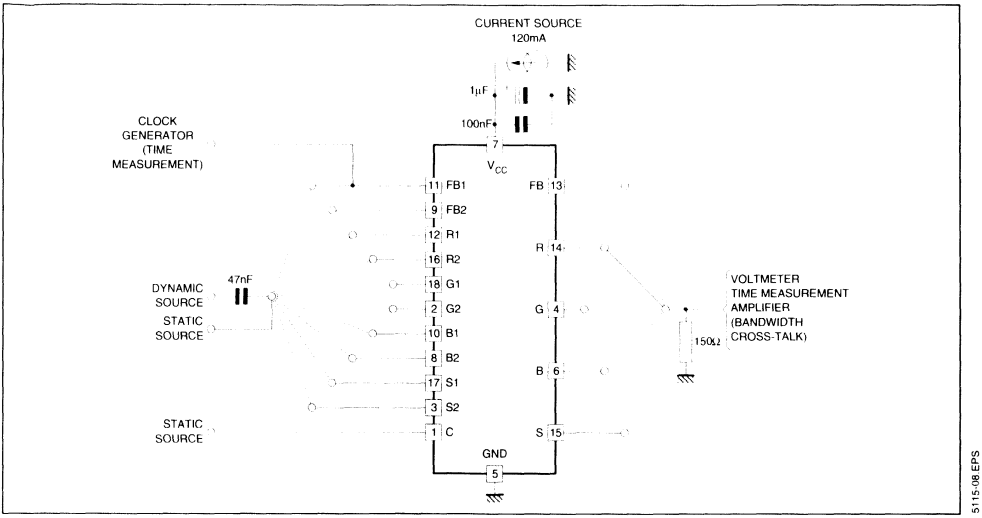


RGB1 = 0, FB2 = 0


INPUTS
FB1
RGB2
OUTPUTS
FB
RGB
t_{d21}
t_{FB1r}
t_{FB1f}
t_{d22}
5115-06.EPS

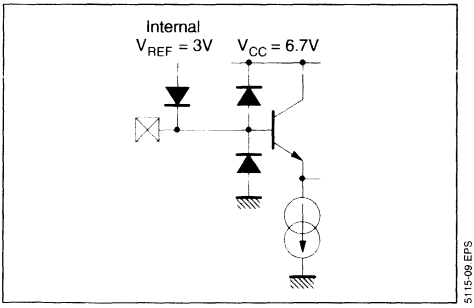

INPUTS
C
S1
S2
OUTPUTS
S
t_{cr}
t_{dc}
t_{cf}
t_{dc}
5115-07.EPS

TEST CIRCUIT

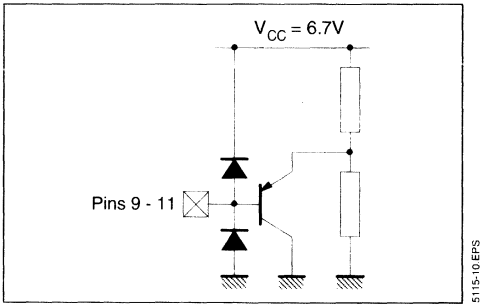


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

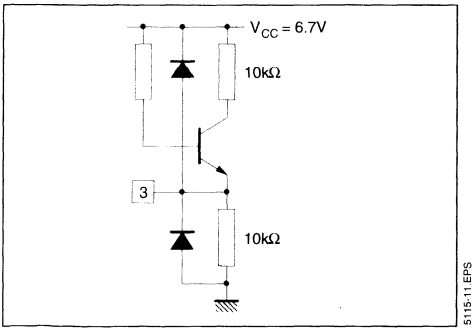
R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



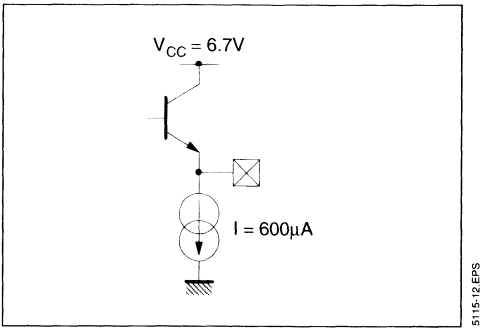
FB inputs (pins 9, 11)



C input (pin 3)

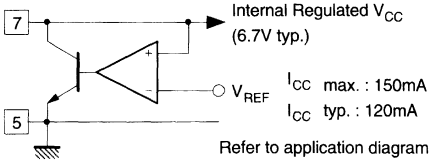


All Outputs (pins 4, 6, 13, 14, 15)



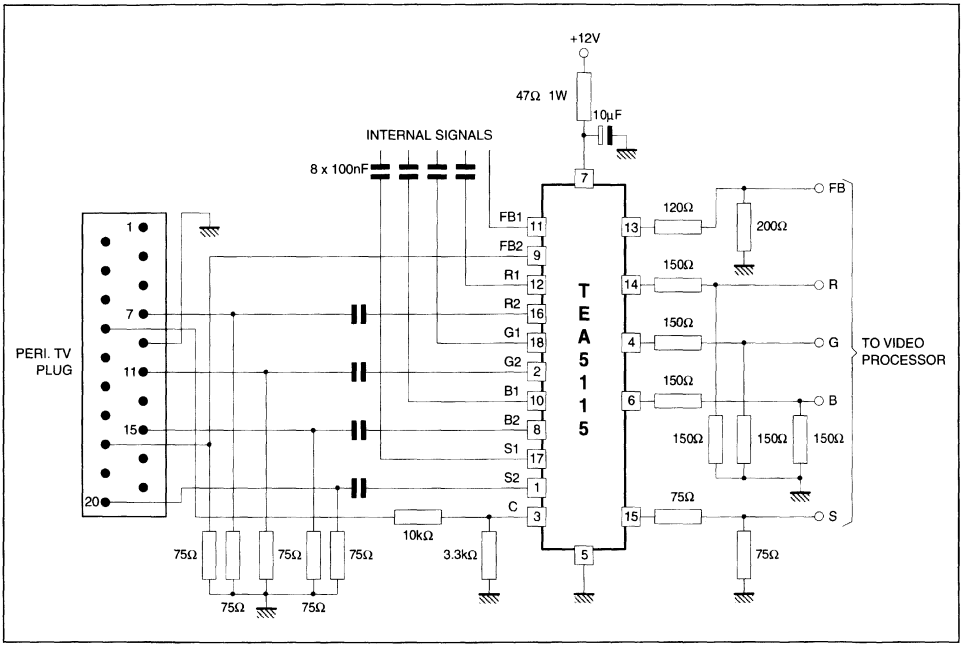
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

I_{CC} Supply (shunt transistor regulation system) (Pin 7)



5115-13.EPS

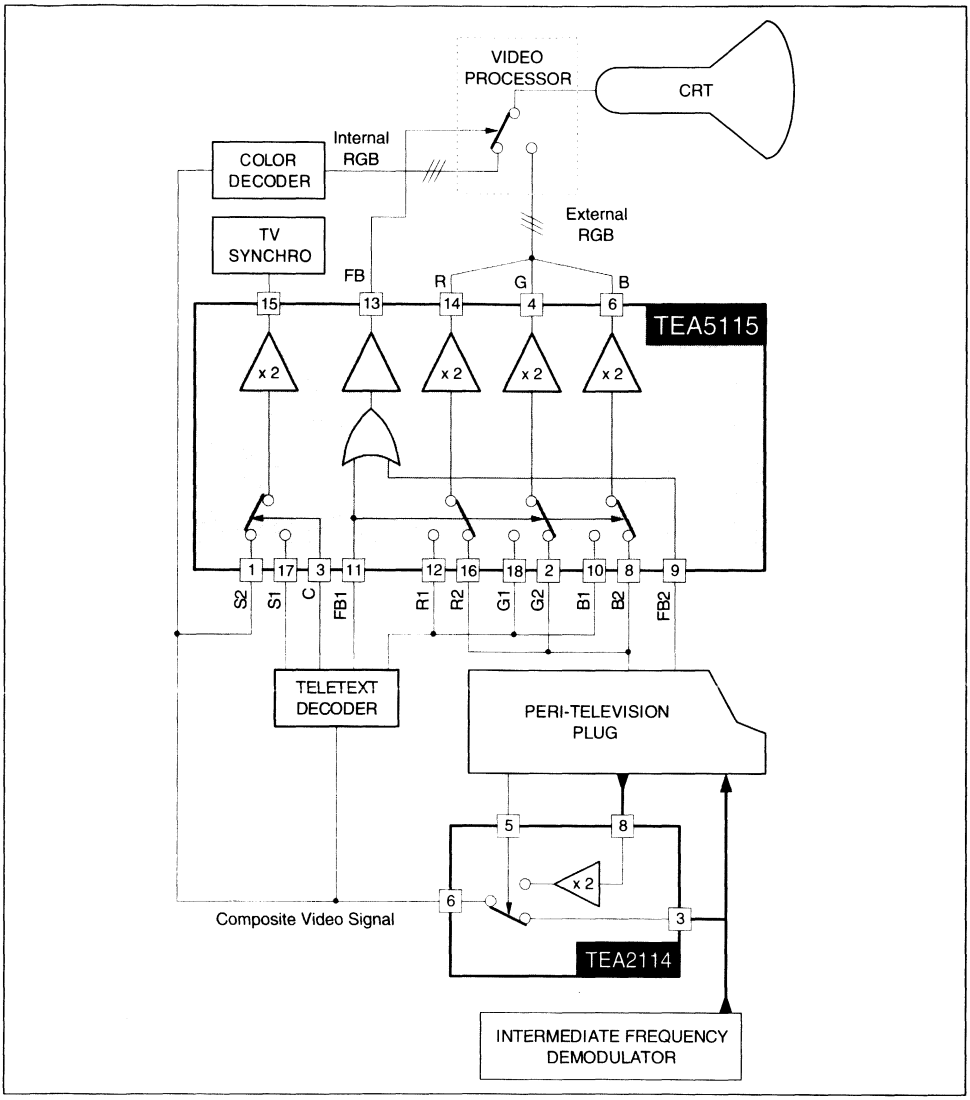
TYPICAL APPLICATION DIAGRAM



5115-14.EPS

- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

TELETEXT SWITCHING APPLICATION WITH TEA5115 AND TEA2114

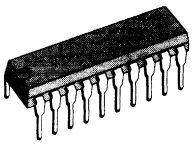


SGS-THOMSON MICROELECTRONICS

TEA5116

5 CHANNELS VIDEO SWITCH

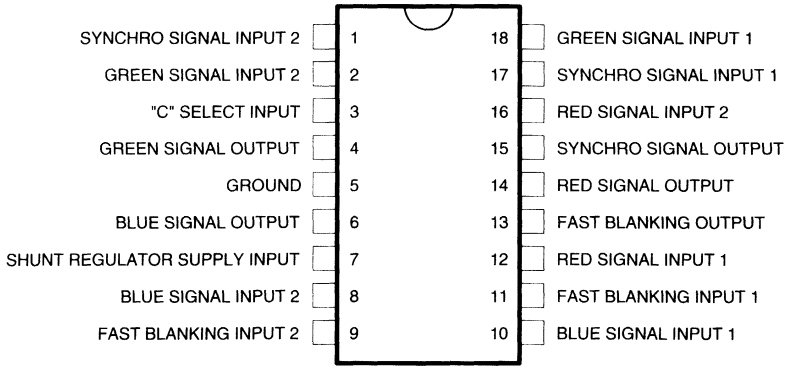
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- THE FIVE CHANNELS ARE SIMULTANEOUSLY SWITCHED BY ONLY ONE SELECT INPUT



DIP18
(Plastic Package)

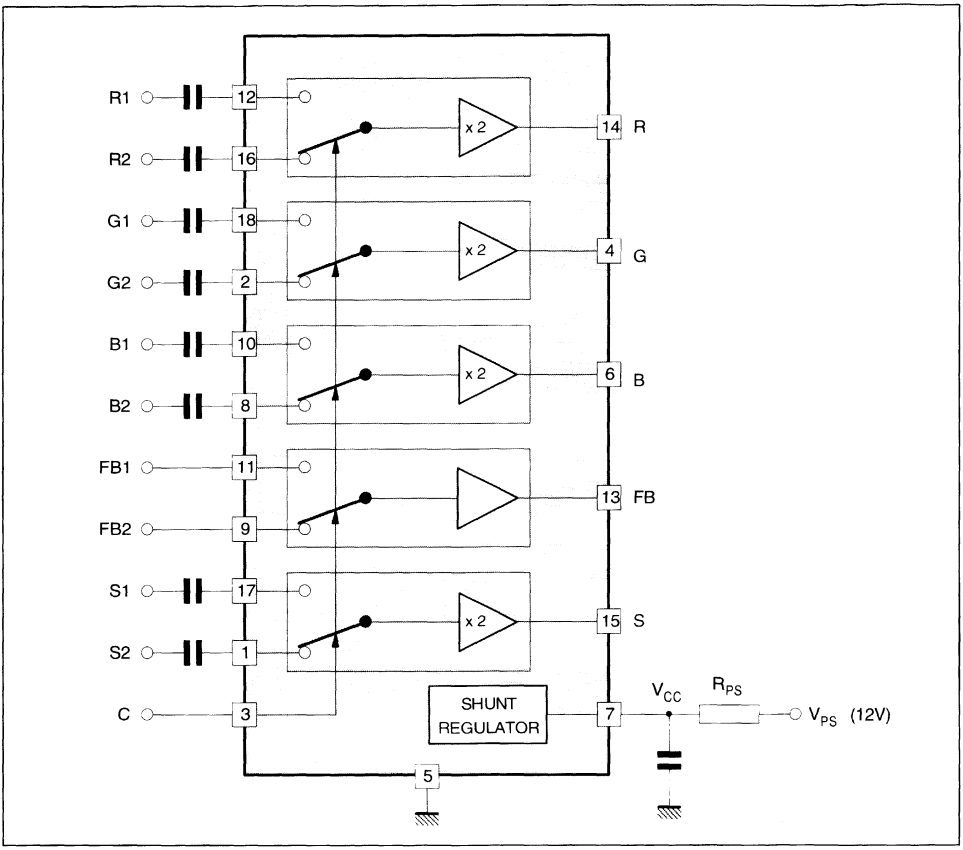
ORDER CODE : TEA5116

PIN CONNECTIONS



5116-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	− 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0, 70	°C
T_j	Junction Temperature	− 40, + 150	°C
T_{stg}	Storage Temperature	− 40, + 150	°C

5116-01.TBL

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

5116-02.TBL

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω
(sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator	I_{CC} = 120 mA I_{CC} = 90 mA I_{CC} = 150 mA	6.3 6.2 6.2	6.7	7.2 7.3 7.3	V V V

R, G, B Switches (pins 4, 6, 14) (Time Measurement Conditions : Δ inputs RGB = 0.7 V_{pp} ; C pulse amplitude = 3 V)

V_C	DC Output Voltage (no input voltage)	$T_{junction}$ = 25 °C $T_{junction}$ stabilized		0.9 1.2	1.25	V
V_{AC}	Max Output Swing Voltage		2	4		V_{pp}
B	Bandwidth (– 3dB) (input voltage 0.7V_{pp})		20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7V_{pp} ; f = 1MHz)		5.5	6	6.5	dB
A_{dc}	Gain Difference between any two R, G, B Channels (input voltage 0.7V_{pp} ; f = 1MHz)			0.1	0.5	dB
	Input Swing			0.7 V ± 3dB		
z_{ic}	DC Input Impedance			10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; f = 1MHz) with R_{load} = 300Ω			10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7V_{pp} ; f = 1MHz).		45	55		dB
	Crosstalk between any outputs (input voltage 0.7V_{pp} ; f = 1MHz)		40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.			10		ns
t_{sr1}	Switching Rise Time between FB1 Input Signal and R, G, B Output Signal (input signal on RGB1)			45		ns
t_{sf1}	Switching Fall Time between FB1 input Signal and R, G, B Output Signal (input signal on RGB1)			25		ns
t_{sr2}	Switching Rise Time between FB2 Input Signal and R, G, B Output Signal (input signal on RGB2)			55		ns
t_{sf2}	Switching Fall Time between FB2 Input Signal and R, G, B Output Signal (input signal on RGB2)			25		ns

Fast Blanking Switch (pin 13)
(time measurement conditions : FB input pulse amplitude = 2 V, C pulse amplitude = 3V))

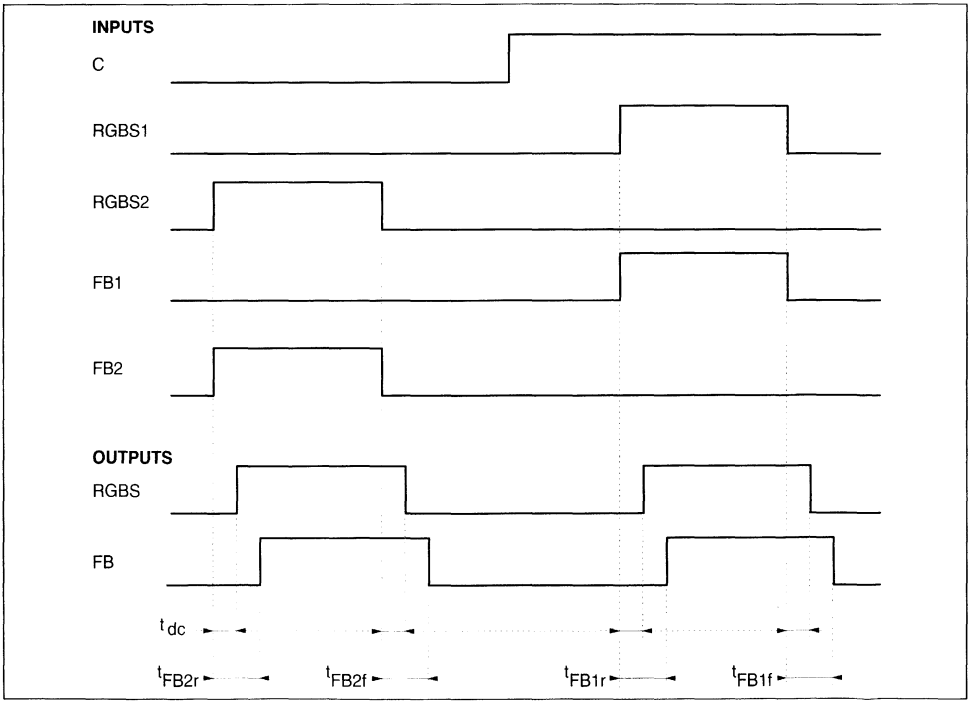
V_{IL} V_{IH} V_{OL} V_{OH}	Low Level Input Voltage High Level Input Voltage Low Level Output Voltage High Level Output Voltage	 $T_{junction}$ = 25°C $T_{junction}$ stabilized	- 0.5 1 1.4 1.5	 1.7 1.9	0.4 V_{CC}+0.5 V_{CC}+0.5 3.5	V V V V V
	Dynamic Output Impedance : with R_{load} = 300Ω			10		Ω
t_{FB1r}	Delay Rise Time between FB1 Input and FB Output			60	110	ns
t_{FB1f}	Delay Fall Time between FB1 Input and FB Output			40	60	ns
t_{FB2r}	Delay Rise Time between FB2 Input and FB Output			60		ns
t_{FB2f}	Delay Fall Time between FB2 input and FB Output			40		ns
t_{SFB1r}	Switching Rise Time between C Input and FB Output (input signal on FB1 input)			75		ns
t_{SFB1f}	Switching Fall Time between C Input and FB Output (input signal on FB1 input)			50		ns
t_{SFB2r}	Switching Rise Time between C Input and FB Output (input signal on FB2 input)			85		ns
t_{SFB2f}	Switching Fall Time between C Input and FB Output (input signal on FB2 input)			50		ns

5116-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

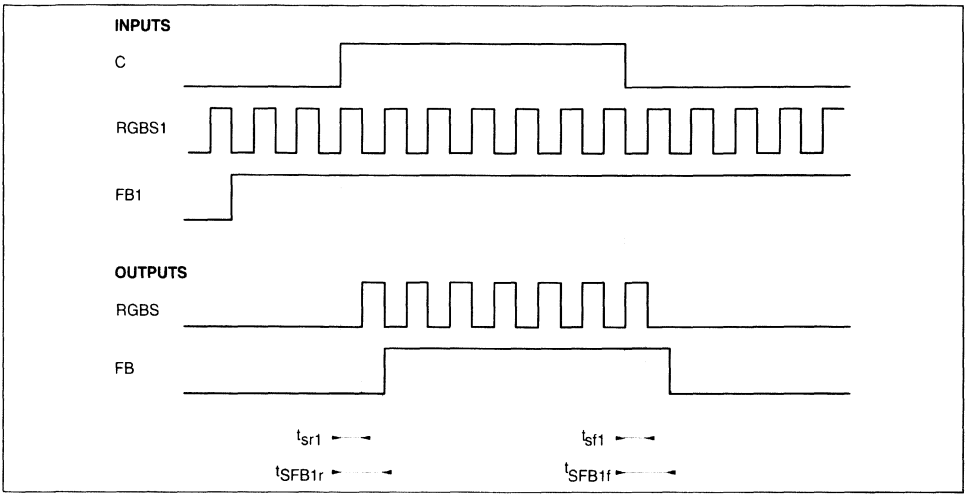
Symbol	Parameter	Min.	Typ.	Max.	Unit
Video (or synchro) **Signal Switch** (pin 15) - time measurement conditions : (C pulse amplitude = 3V)					
V_S	DC Output Voltage (no input voltage)				
	$T_{junction}$ = 25°C		0.9	1.25	V
	$T_{junction}$ stabilized		1.2		V
V_{as}	Max Output Swing Voltage	2.6			V_{pp}
Z_{ic}	DC Input Impedance		10		kΩ
Z_{cc}	Dynamic Output Impedance (input voltage $1V_{pp}$; f = 1MHz) with R_{load} = 300 Ω		10		Ω
A_V	Gain (input voltage 1 V_{pp} ; f = 1MHz)	5.5	6	6.5	dB
B	Bandwidth (– 3 dB) (input voltage 1 V_{pp})	15	20		MHz
	Input Swing		1V ± 3 dB		
t_{dc}	Delay Time between S Input and S Output (Δ input : $0.7V_{PP}$)		10		ns
t_{sr1}	Switching rise time between C input signal and S output signal (input signal on S1)		45		ns
t_{sf1}	Switching fall time between C input signal and S output signal (input signal on S1)		25		ns
t_{sr2}	Switching Rise time between C input signal and S output signal (input signal on S2)		55		
t_{sf2}	Switching fall time between C input signal and S output signal (input signal on S2)		25		
Select Input "C" (pin 3)					
V_{IL}	Low Level Input Voltage	– 0.5		1	V
V_{IH}	High Level Input Voltage	2		V_{CC}+0.5	V
I_{IL}	Low Level Input Current (V_{IL} = 1 V)	– 0.6		– 0.1	mA
I_{IH}	High Level Input Current (V_{IH} = 3 V)			0.5	mA

5116-04.TBL

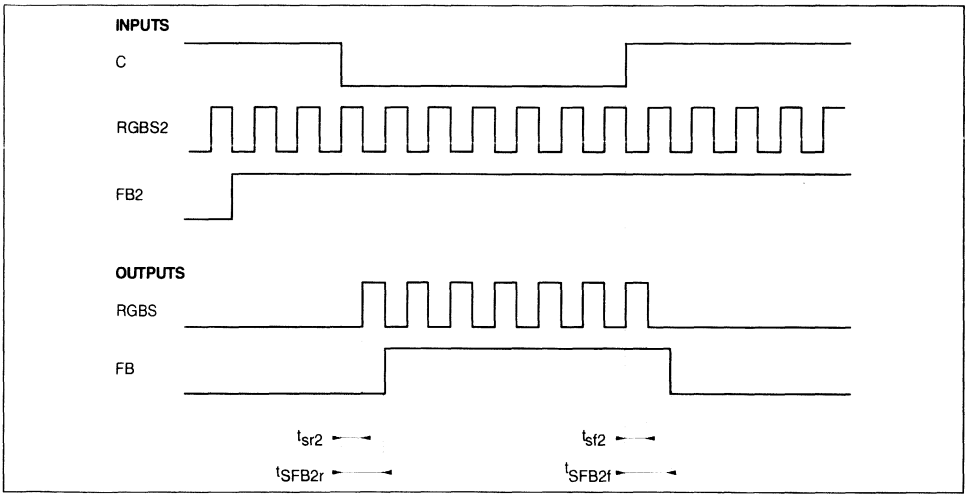


5116-03.EPS

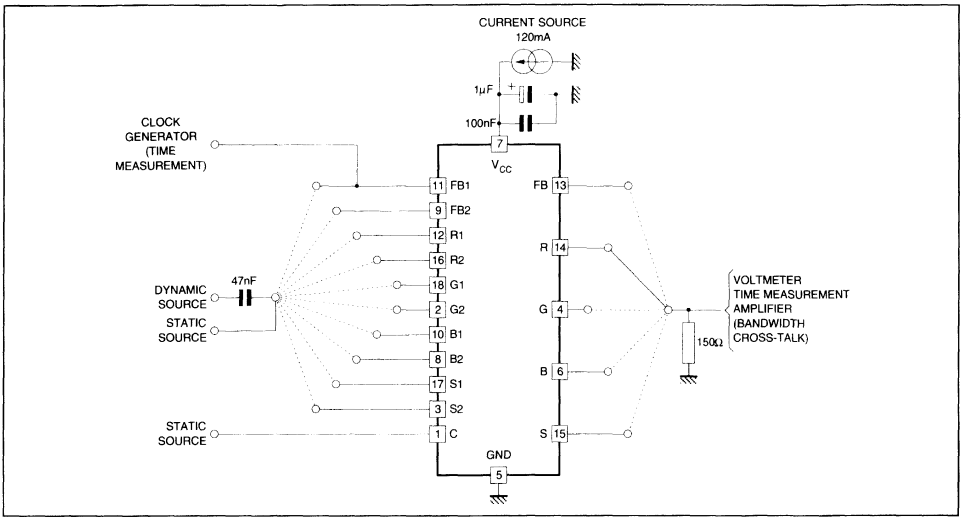
RGBS2 = 0, FB2 = 0



RGBS1 = 0, FB1 = 0

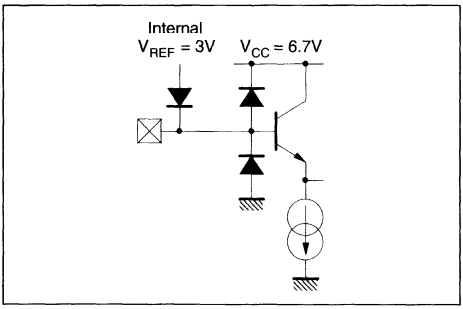


TEST CIRCUIT

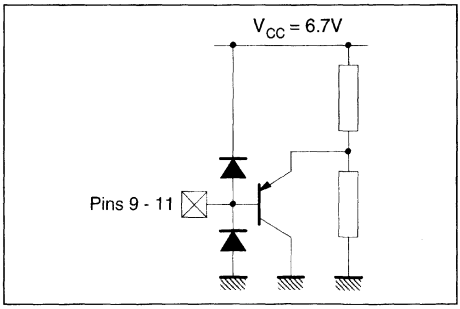


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

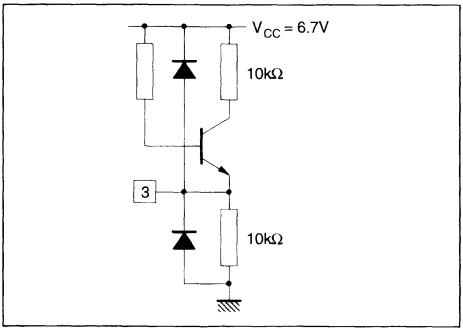
R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



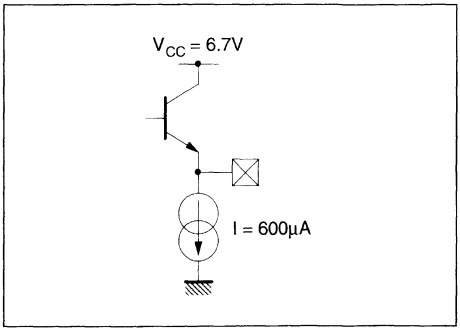
FB inputs (pins 9, 11)



C input (pin 3)

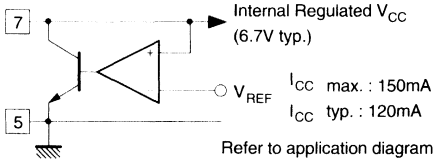


All Outputs (pins 4, 6, 13, 14, 15)



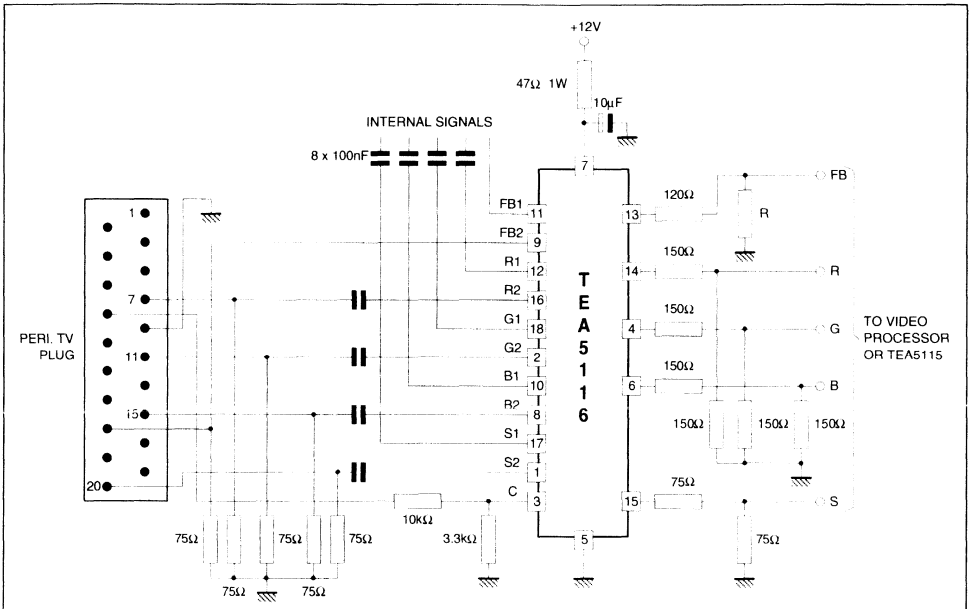
INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS (continued)

I_{CC} Supply (shunt transistor regulation system) (Pin 7)



5116-11.EPS

TYPICAL APPLICATION DIAGRAM



R values
1) towards TEA5115 : R = 300Ω
2) towards video processor : R = 200Ω

5116-12.EPS

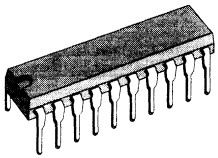
- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

SGS-THOMSON MICROELECTRONICS

TEA6415B

BUS-CONTROLLED VIDEO MATRIX SWITCH

- 15MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6415B (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7 VOLTAGE)
- 8 INPUTS (CVBS, RGB, MAC, CHROMA...)
- 6 OUTPUTS
- POSSIBILITY OF MAC OR CHROMA SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 50dB CROSSTALK AT 5 MHz
- FULLY ESD PROTECTED



DIP20
(Plastic Package)

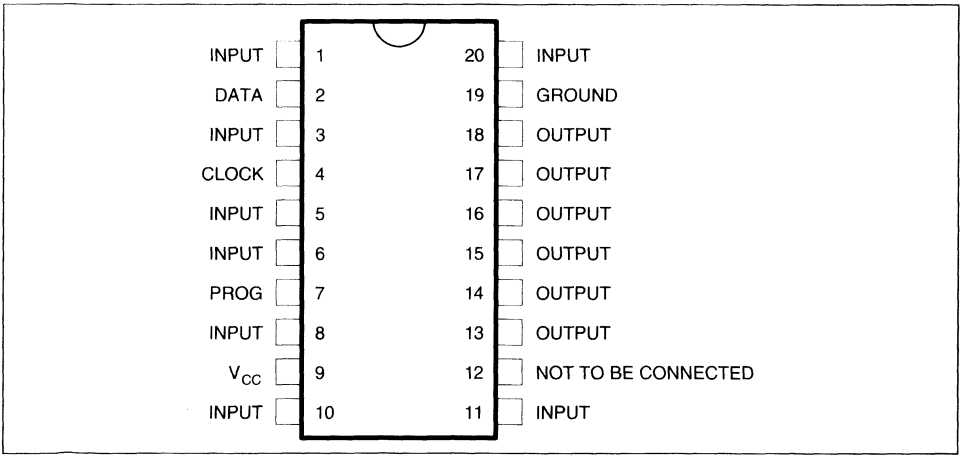
ORDER CODE : TEA6415B

DESCRIPTION

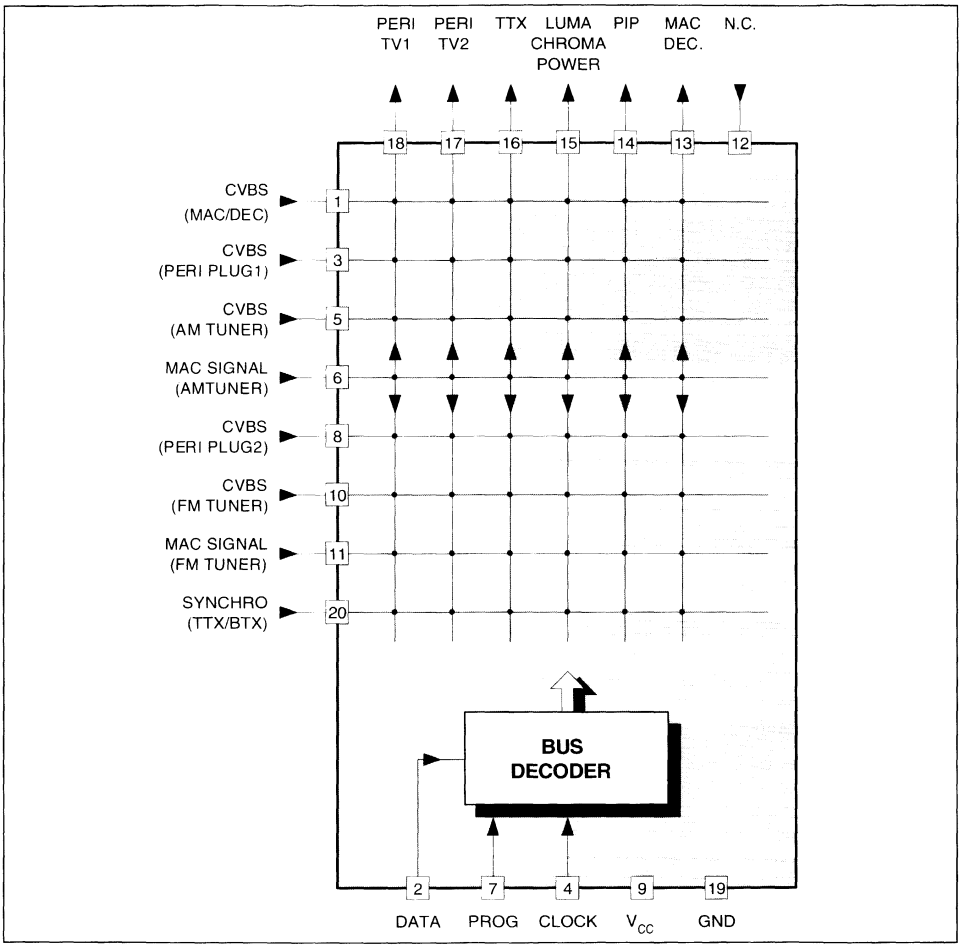
The main function of the TEA6415B is to switch 8 video input sources on the 6 outputs.

Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (pin 9)	13	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-20 to +150	°C

6415B-01.TBL

THERMAL DATA

Symbol	Parameter	Min.	Typ.
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80	°C/W

6415B-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (pin 9)	8	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC}=10V)	20	30	40	mA
INPUTS					
	Maximum Signal Amplitude (CVBS signal)	2			V_{PP}
	Input Current (per output connected, input voltage = $5V_{DC}$) (this current is X6 when all outputs are connected on the input)		1	3	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70°C)		5	100	mV
OUTPUTS (V_{IN} = $1V_{PP}$ for all dynamic tests) Pins 13 - 14 - 15 - 16 - 17 - 18					
	Dynamic	4.5	5.5		V_{PP}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth ● -1dB attenuation ● -3dB attenuation	7	 10 15		 MHz MHz
	Crosstalk (f = 5MHz)		-50		dB
	DC level	2.4	2.7	3	V
I^2C BUS INPUT : DATA, CLOCK, PROG (Pins 2 - 4 - 7)					
	Threshold Voltage	1.5	2	3	V

64156-03.TBL

GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

It is possible to have the same input connected to several outputs.

The starting configuration upon power on (power supply : 0 to 10V) is undetermined.

In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

BUS SELECTIONS (I^2C-BUS)

2nd byte of transmission

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	Pin 18	Output is selected by address bits
00100	XXX	Pin 14	
00010	XXX	Pin 16	
00110	---	Not used	
00001	XXX	Pin 17	
00101	XXX	Pin 13	
00011	XXX	Pin 15	
00111	---	Not used	
		Selected Input	
00XXX	000	Pin 5	Input is selected by data bits
00XXX	100	Pin 8	
00XXX	010	Pin 3	
00XXX	110	Pin 20	
00XXX	001	Pin 6	
00XXX	101	Pin 10	
00XXX	011	Pin 1	
00XXX	111	Pin 11	

6415B-04.TBL

Example :00100 101 connects pin 10 (input) to pin 14 (output) (equals 25 in hexadecimal)

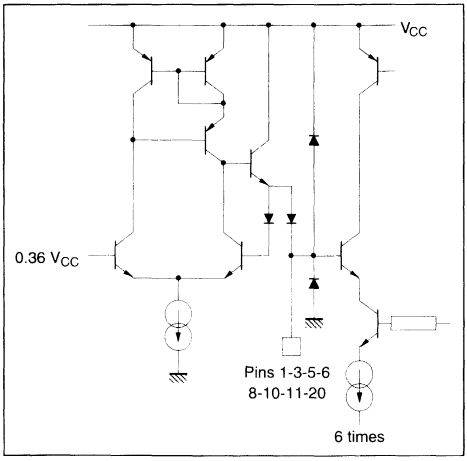
Adress byte (1st byte of transmission)

86	1000	0110	When pin PROG is connected to ground
06	0000	0110	When pin PROG is connected to V_{CC}

6415B-05.TBL

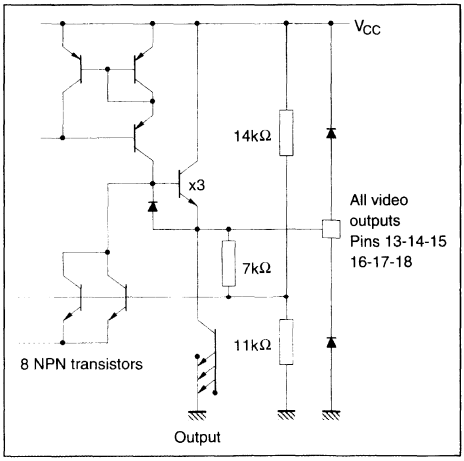
IN / OUT PIN CONFIGURATION

Figure 1 : Input Configuration



6415B-03.EPS

Figure 2 : Output Configuration



6415B-04.EPS

SGS-THOMSON MICROELECTRONICS

IN / OUT PIN CONFIGURATION (continued)

Figure 3 : Bus I/O Configuration

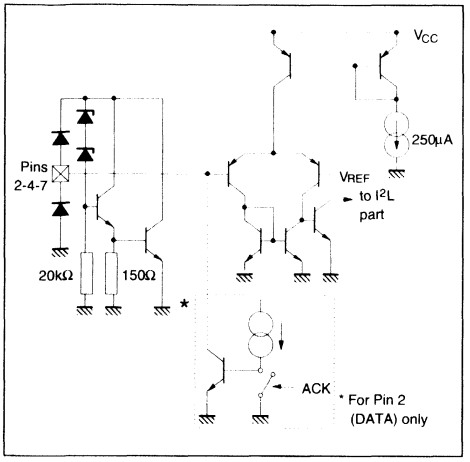
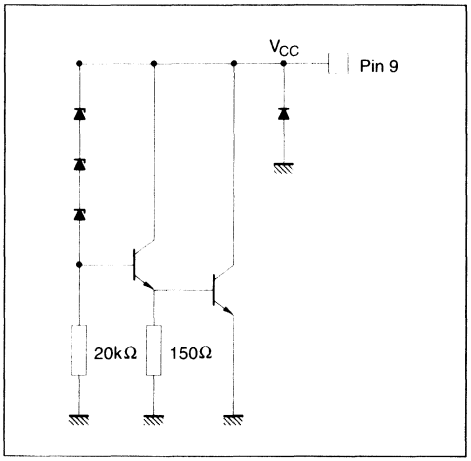


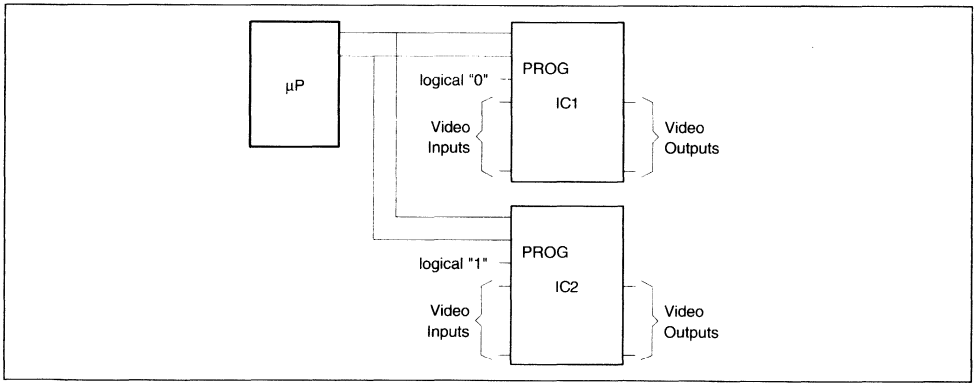
Figure 4 : V_{CC} Pin Configuration



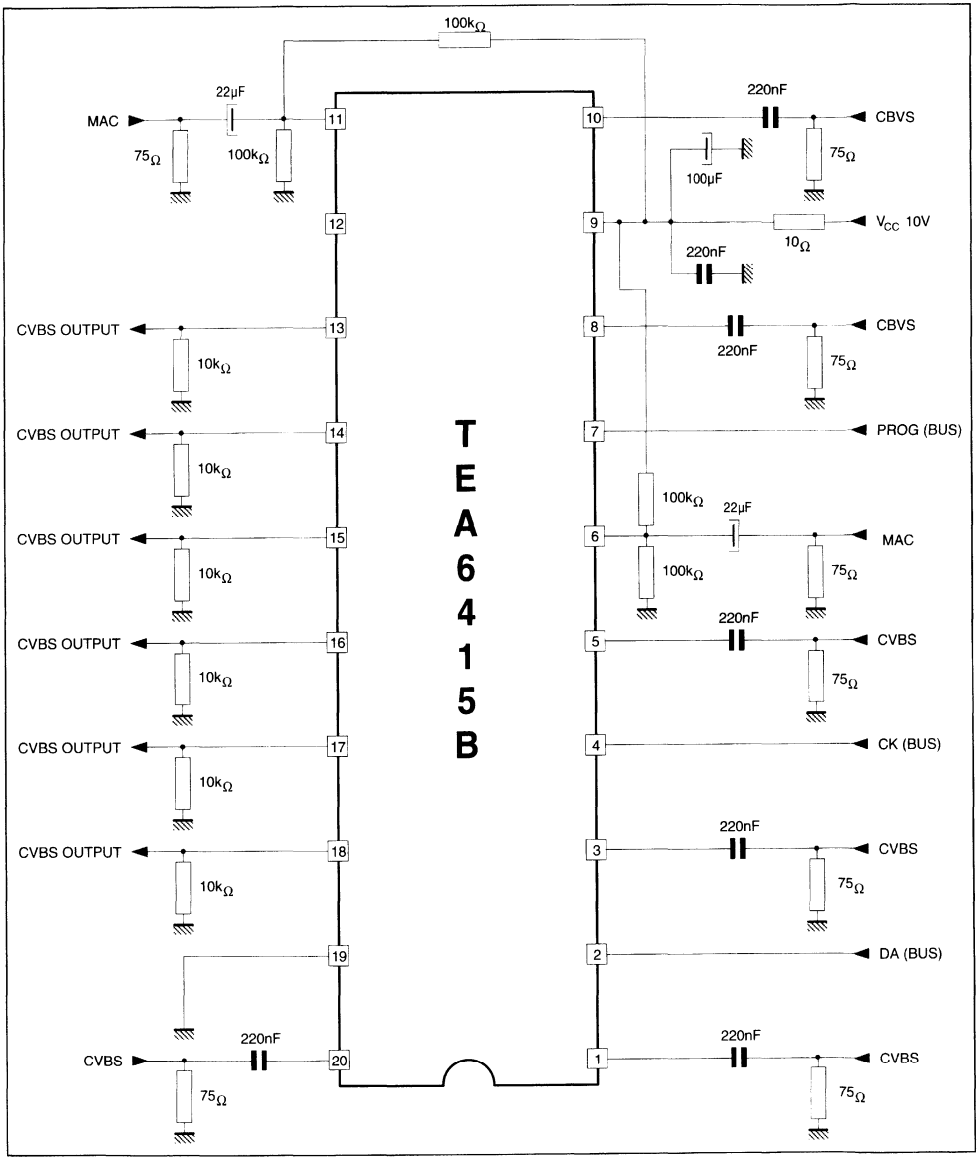
USE WITH AN OTHER TEA6415B

The programmation input (PROG) permits to operate with two TEA6415B in parallel and to select them independantly through the I^2C-BUS without modifying the adress byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.

Figure 5



TYPICAL APPLICATION

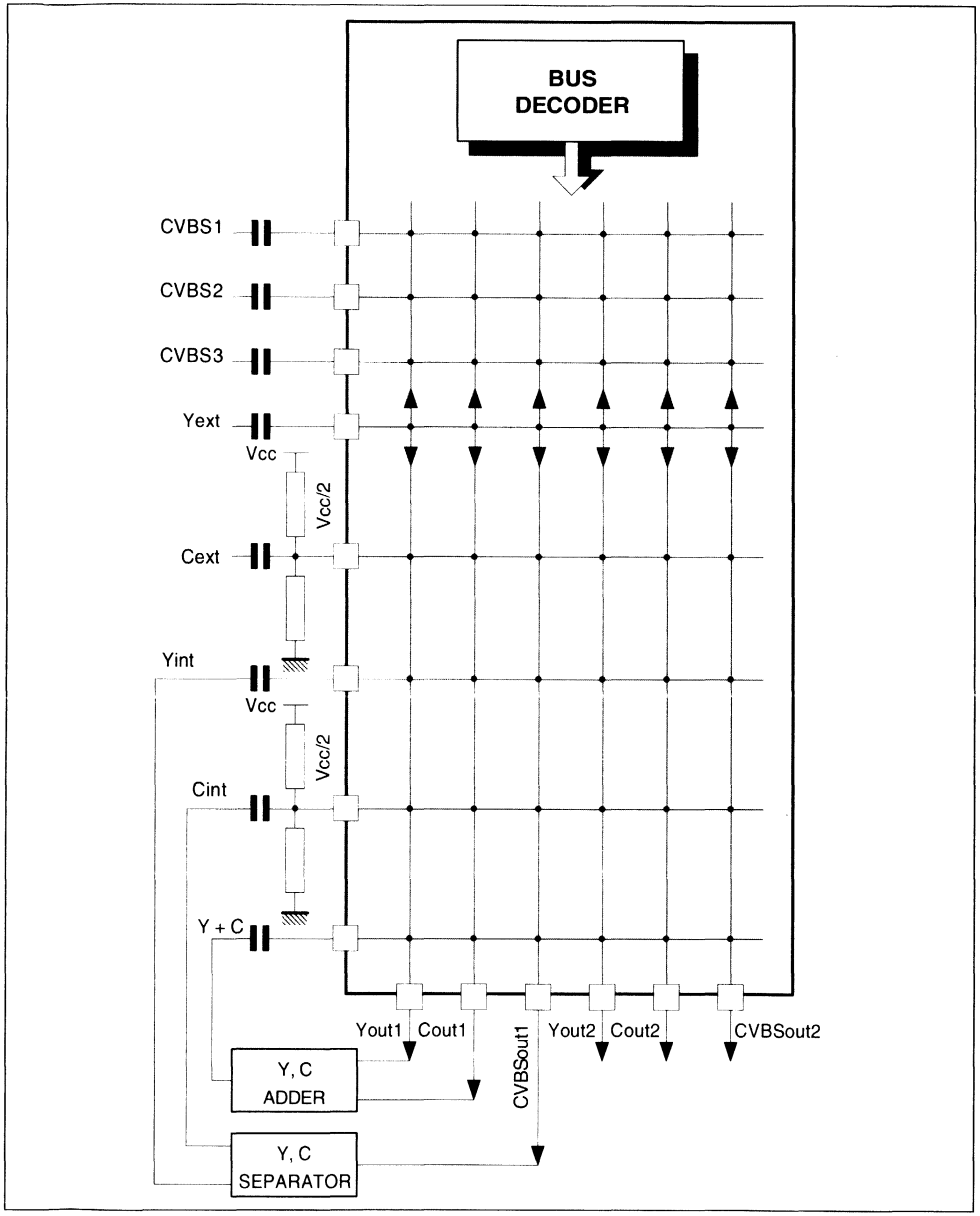


CROSSTALK IMPROVEMENT

1 - When any input is not used, it must be bypassed to ground through a 220nF capacitor.

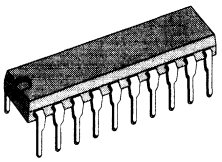
2 - An important improvement can be achieved considering the input crosstalk by means of the application (see technical note).

OTHER APPLICATION DIAGRAM EXAMPLE



BUS-CONTROLLED VIDEO MATRIX SWITCH

- 15MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6416 (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7 VOLTAGE)
- 8 INPUTS (CVBS, RGB, MAC, CHROMA...)
- 6 OUTPUTS
- EACH INPUT INTERNALLY BIASED@ $V_{CC}/2$ BY RESISTOR NETWORK
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 50dB CROSSTALK AT 5MHz
- FULLY ESD PROTECTED



DIP20
(Plastic Package)

ORDER CODE : TEA6416

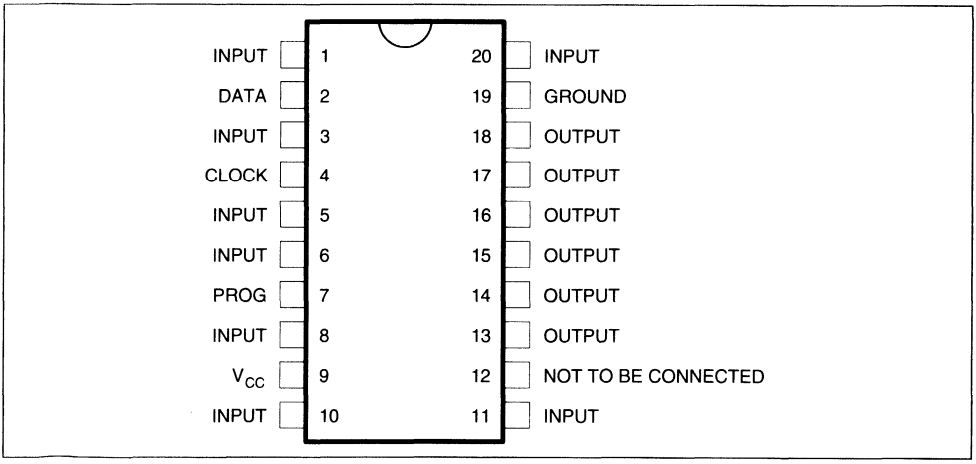
DESCRIPTION

The main function of the TEA6416 is to switch 8 video input sources on the 6 outputs.

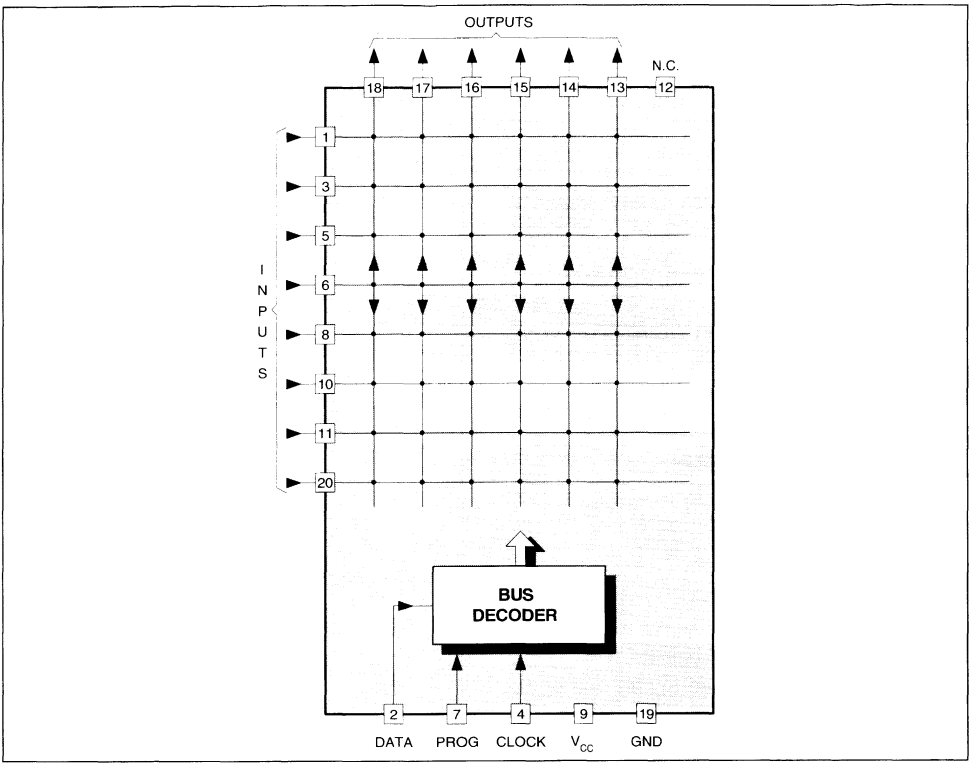
Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.

All the switching possibilities are controlled through the I^2C Bus.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (pin 9)	13	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-20 to +150	°C

6416-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80	°C/W

6416-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (pin 9)	8	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC}=10V)	20	30	40	mA

6416-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25°C$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
INPUTS					
	Maximum Signal Amplitude (CVBS signal)	2	2.5		V_{PP}
	Input Resistance	30	45		kΩ
	DC Level (1 input linked with 1 output)	4.75	5	5.25	V
	DC Level Shift (temperature from 0 to 70°C)		5	100	mV
OUTPUTS (V_{IN} = 1V_{PP} for all dynamic tests) Pins 13 - 14 - 15 - 16 - 17 - 18					
	Dynamic	4.5	5.5		V_{PP}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth ● -1dB attenuation	7	10		MHz
	● -3dB attenuation		15		MHz
	Crosstalk (f = 5MHz)		-50		dB
	DC level (1 input linked with 1 output)	5.2	5.7	6.2	V
I^2C BUS INPUT : DATA, CLOCK, PROG (Pins 2 - 4 - 7)					
	Threshold Voltage	1.5		2	

6416-04.TBL

GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.

Each output can be switched on only one of each input. Each input is connected to $V_{CC}/2$ through a resistive network (no clamp on sync. bottom).

Each nominal gain between any input and output is 6.5dB. All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

It is possible to have the same input connected to several outputs.

The starting configuration upon power on (power supply : 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

BUS SELECTIONS (I^2C-BUS) - 2nd byte of transmission

ADDRESS - MSB	**DATA** - LSB	**Selected Output**	
00000	XXX	pin 18	Output is selected by address bits
00100	XXX	pin 14	
00010	XXX	pin 16	
00110	- - -	Not used	
00001	XXX	pin 17	
00101	XXX	pin13	
00011	XXX	pin 15	
00111	- - -	Not used	
		Selected Input	
00XXX	000	pin 5	Input is selected by data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

6416-05.TBL

Example : 00100 101 connects pin 10 (input) to pin 14 (output)- (equals 25 in hexadecimal)

Adress byte (1st byte of transmission)

86	1000	0110	When pin PROG is connected to ground
06	0000	0110	When pin PROG is connected to V_{CC}

6416-06.TBL

IN / OUT PIN CONFIGURATION

Figure 1 : Input Configuration

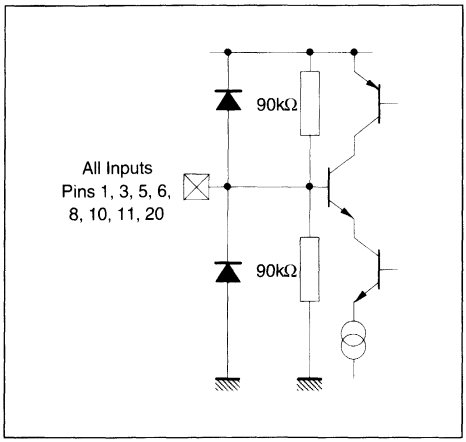


Figure 2 : Output Configuration

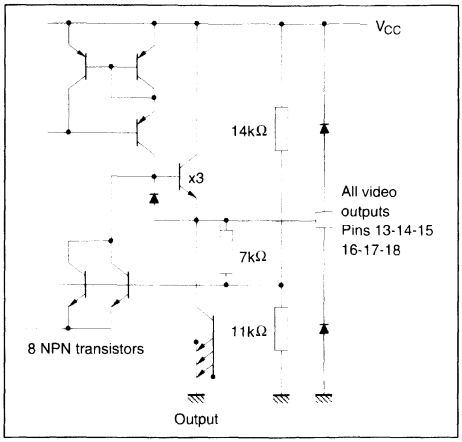


Figure 3 : Bus I/O Configuration

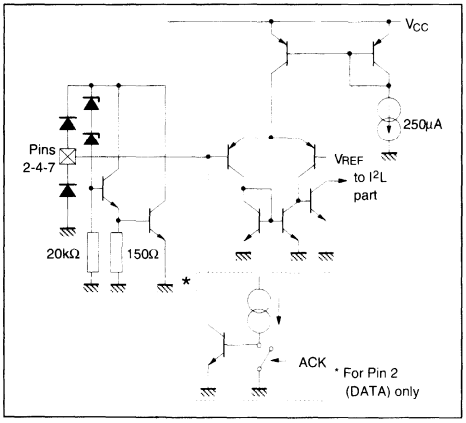
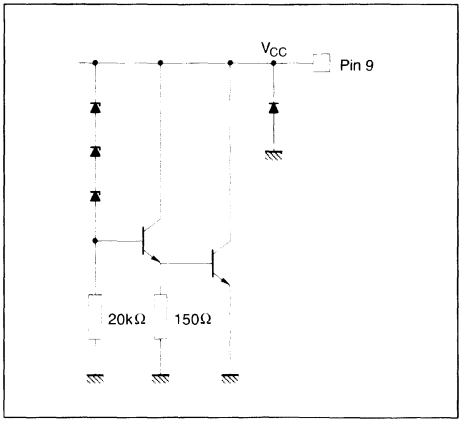
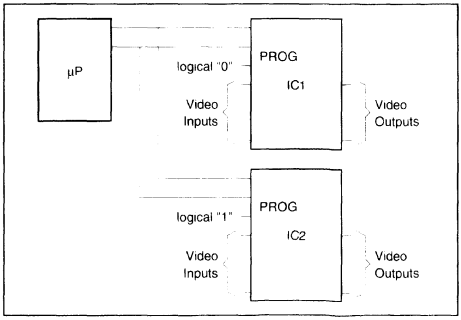


Figure 4 : V_{CC} Pin Configuration

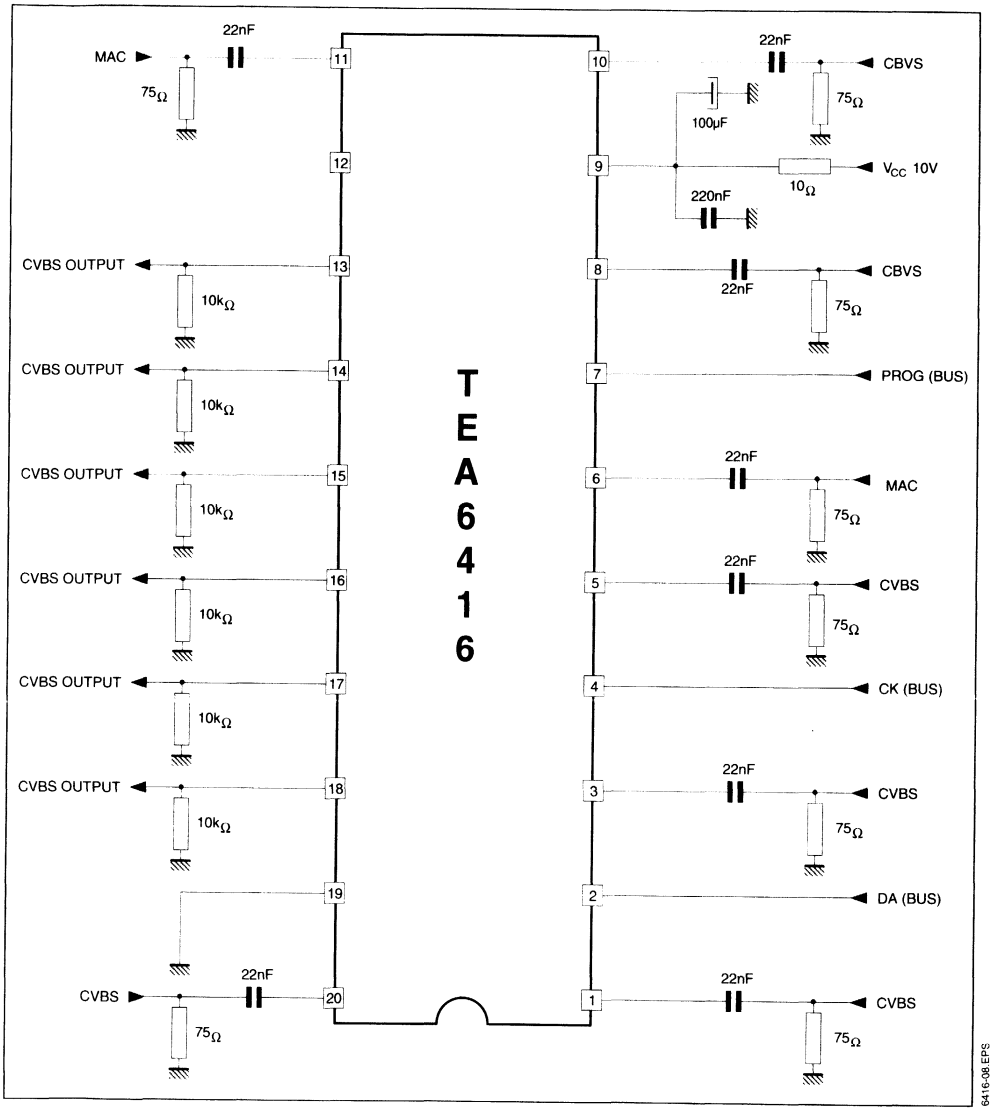


USE WITH AN OTHER TEA6416

The programmation input (PROG) permits to operate with two TEA6416 in parallel and to select them independantly through the I^2C-BUS without modifying the adress byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.



TYPICAL APPLICATION



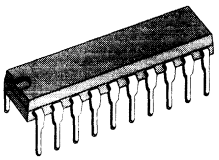
CROSSTALK IMPROVEMENT

1 - When any input is not used, it must be bypassed to ground through a 22nF capacitor.

2 - An important improvement can be achieved considering the input crosstalk by means of the application (see technical note).

BUS-CONTROLLED VIDEO MATRIX SWITCH

- 15MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6417 (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7 VOLTAGE)
- 8 INPUTS (CVBS, RGB, MAC, CHROMA...)
- 6 OUTPUTS
- POSSIBILITY OF MAC OR CHROMA SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 60dB CROSSTALK AT 3.58MHz
- FULLY ESD PROTECTED



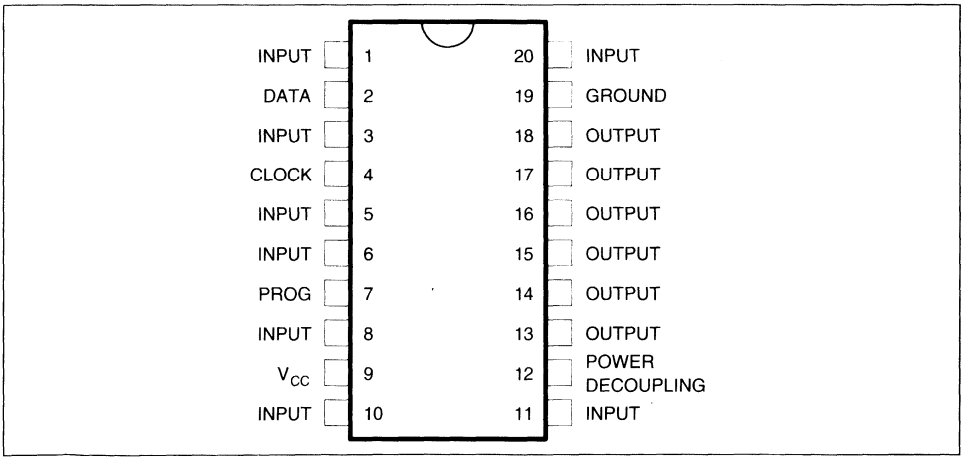
DIP20
(Plastic Package)

ORDER CODE : TEA6417

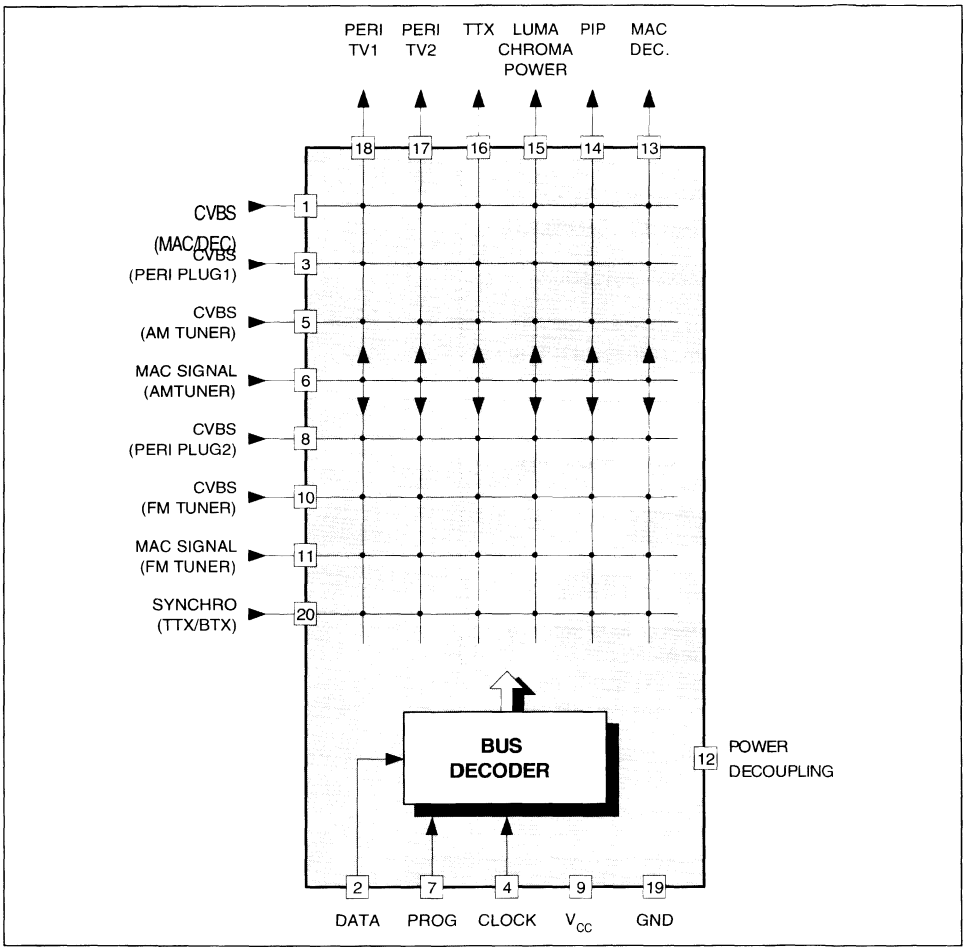
DESCRIPTION

The main function of the TEA6417 is to switch 8 video input sources on the 6 outputs.
Each output can be switched to only one of the inputs whereas but any same input may be connected to several outputs.
All the switching possibilities are controlled through the I^2C Bus.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (Pin 9)	13	V
T_A	Operating Ambient Temperature Range	0 to +70	°C
T_{stg}	Storage Temperature Range	-20 to +150	°C

6417-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	80	°C/W

6417-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25^oC$, $V_{CC} = 10V$, $R_{LOAD} = 10k\Omega$, $C_{LOAD} = 3pF$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (Pin 9)	8	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC}=10V)	20	30	40	mA
INPUTS					
	Maximum Signal Amplitude (CVBS signal)	2			V_{PP}
	Input Current (per output connected, input voltage = $5V_{DC}$) (this current is X6 when all outputs are connected on the input)		1	3	µA
	DC Level	2.8	3.1	3.4	V
OUTPUTS (V_{IN} = $1V_{PP}$ for all dynamic tests) Pins 13 - 14 - 15 - 16 - 17 - 18					
	Dynamic	4	4.8		V_{PP}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth -1dB attenuation -3dB attenuation	7	 10 15		 MHz MHz
	Crosstalk f = 3.58MHz f = 5MHz		 -60 -55	 -50	 dB dB
	DC level	3.3	3.6	3.9	V
I^2C BUS INPUT : DATA, CLOCK, PROG (Pins 2 - 4 - 7)					
	Threshold Voltage	1.5	2	3	V

6417-03.TBL

GENERAL DESCRIPTION

The main function of the IC is to switch 8 video input sources on 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge. 5 V_{DC} on the input.Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

It is possible to have the same input connected to several outputs.

The starting configuration upon power on (power supply : 0 to 10V) is undetermined.

In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

BUS SELECTIONS (I^2C-BUS)

2 nd byte of transmission

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	pin 18	Output is selected by address bits
00100	XXX	pin 14	
00010	XXX	pin 16	
00110	- - -	Not used	
00001	XXX	pin 17	
00101	XXX	pin13	
00011	XXX	pin 15	
00111	- - -	Not used	
		Selected Input	
00XXX	000	pin 5	Input is selected by data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

6417-04.TBL

Example :00100 101 connects pin 10 (input) to pin 14 (output) (equals 25 in hexadecimal)

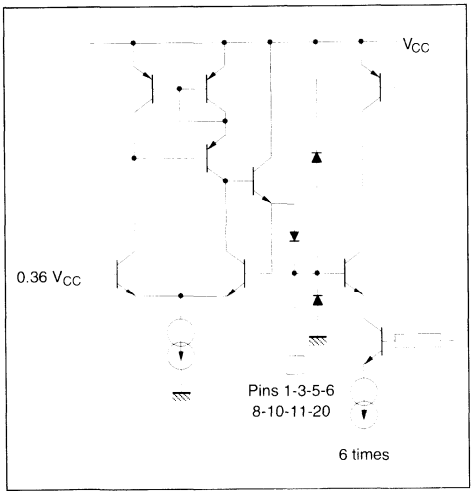
Adress byte (1st byte of transmission)

96	1001	0110	When pin PROG is connected to ground
92	1001	0010	When pin PROG is connected to V_{CC}

6417-05.TBL

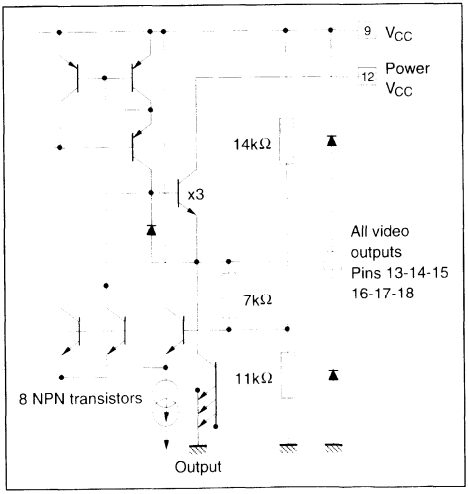
IN / OUT PIN CONFIGURATION

Figure 1 : Input Configuration



6417-03.EPS

Figure 2 : Output Configuration



6417-04.EPS

IN / OUT PIN CONFIGURATION (continued)

Figure 3 : Bus I/O Configuration

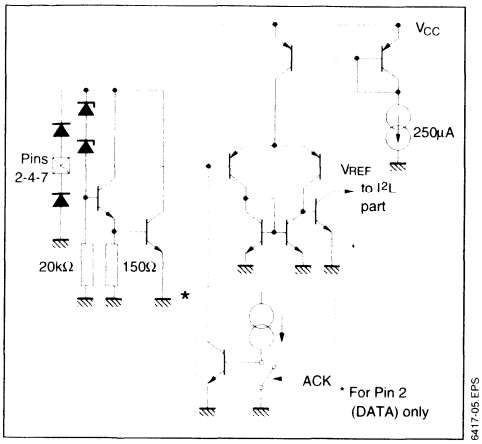
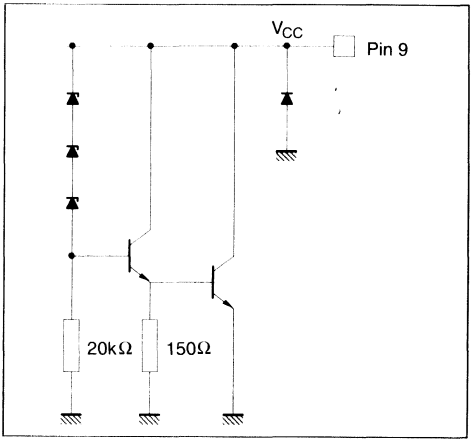


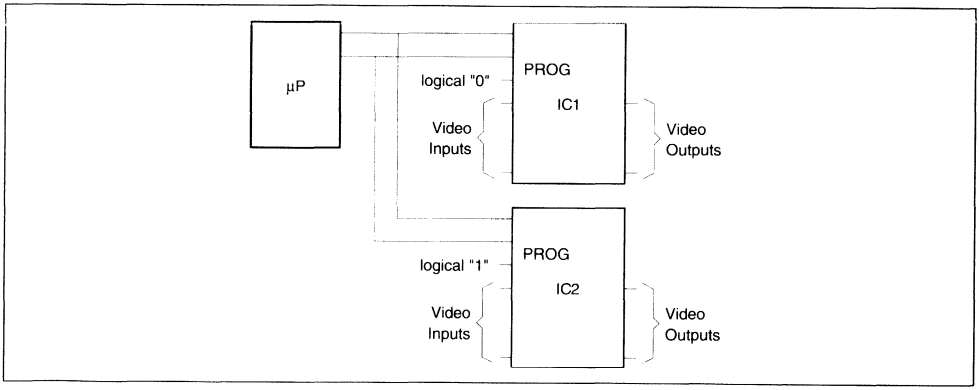
Figure 4 : V_{CC} Pin Configuration



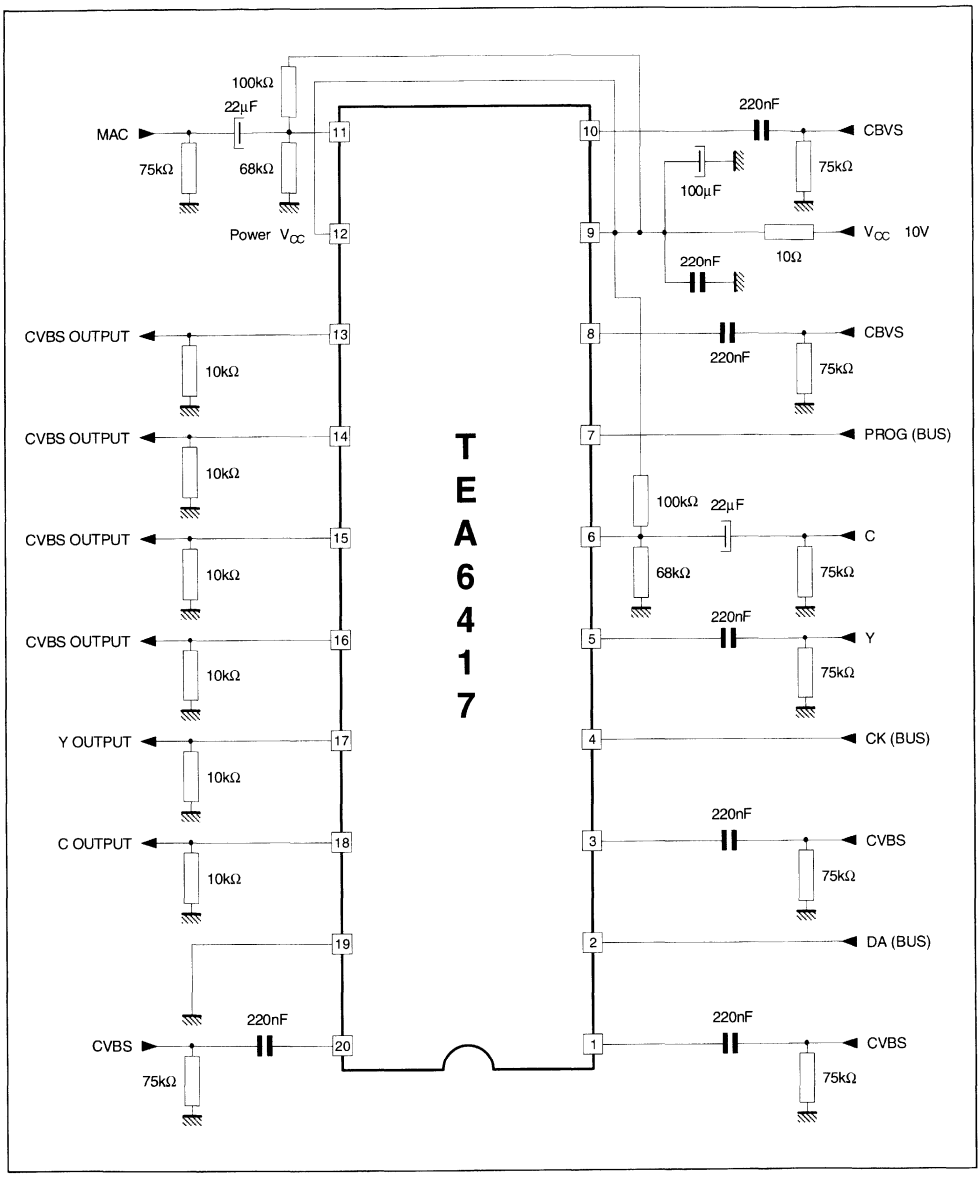
USE WITH AN OTHER TEA6417

The programmation input (PROG) permits to operate with two TEA6417 in parallel and to select them independantly through the I^2C-BUS without modifying the adress byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.

Figure 5



TYPICAL APPLICATION



CROSSTALK IMPROVEMENT

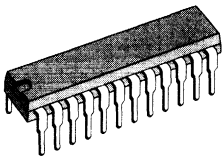
When any input is not used, it must be bypassed to ground through a 220nF capacitor.

SGS-THOMSON MICROELECTRONICS

TEA6420

BUS-CONTROLLED AUDIO MATRIX

- 5 STEREO INPUTS
- 4 STEREO OUPUTS
- GAIN CONTROL 0/2/4/6DB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE
- VERY LOW DISTORSION



SHRINK 24
(plastic package)

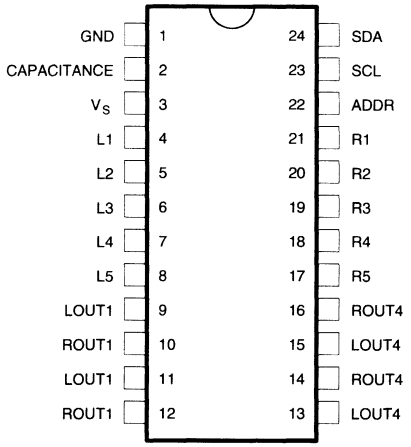
ORDER CODE : TEA6420

DESCRIPTION

The TEA6420 switches 5 stereo audio on 4 stereo outputs.

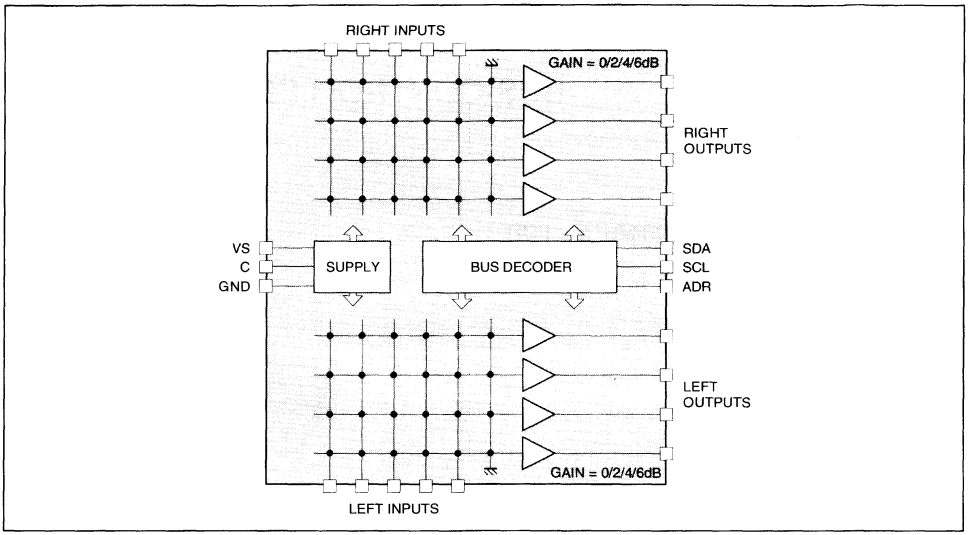
All the switching possibities are changed through the I^2C BUS.

PIN CONNECTIONS



6420-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	10.2	V
Toper	Operating ambient temperature	0, + 70	°C
Tstg.	Storage Temperature	- 20, + 150	°C

6420-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction - ambient thermal resistance	75	°C/W

6420-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	9	10.2	V
I_S	Supply Current			5	8	mA
SVR	Ripple Rejection	$V_{IN} = 500mV_{RMS}$, BW = 20 - 20kHz	70	80		dB
MATRIX						
V_{IN}	Input DC Level		4.5	5	5.5	V
R_I	Input Resistance		30	50	100	kΩ
C_S	Channel Separation	$V_{IN} = 2V_{RMS}$ Gain = 0dB f = 1kHz Gain = 6dB	80 70	90 82		dB dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level		4.5	5	5.5	V
R_{OUT}	Output Resistance			70	200	Ω

6420-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUTPUT BUFFER (continued)						
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		µV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G_{min}	Min. Gain		-1	0	+ 1	dB
G_{max}	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			kΩ
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage (pin 24)		4			V
I_I	Input Current		- 10		10	µA
V_O	Output Voltage	I_O = 3mA ; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note	40	50		kΩ

6420-04.TBL

Note : R_{pu} is an internal pull-up resistor connected between the address programming pin ADDR and the internal positive supply voltage. Leaving ADDR disconnected or "floating" allows it to become logic 1. Connecting ADDR externally to the GND pin forces it to logic 0.

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

6420-05.TBL

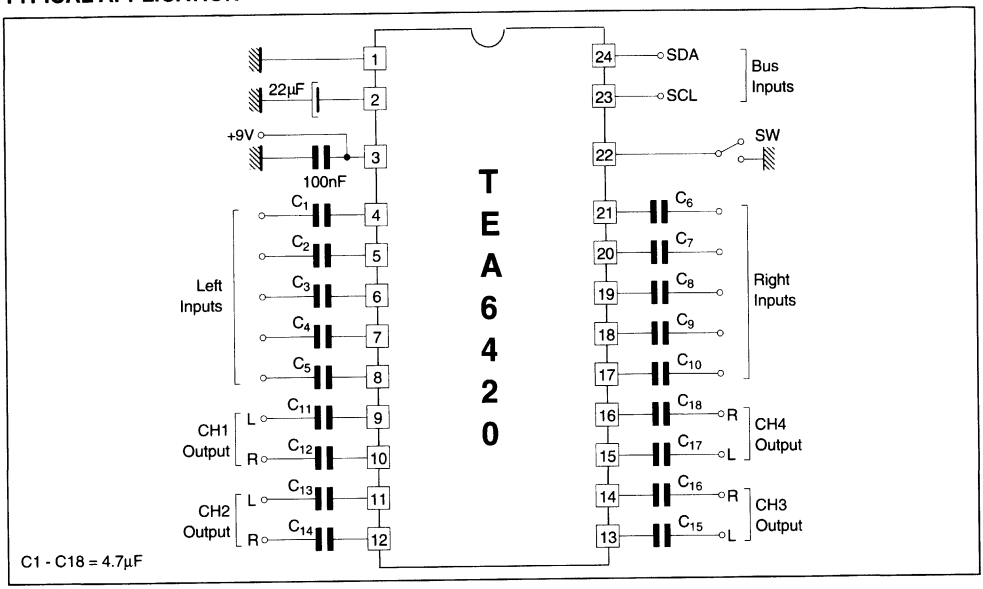
2. Data bytes

Output select								
X	0	0	G_1	G_0	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3
	1	1						Output 4
Input select								
X	Q_1	Q0	G_1	G_0	0	0	0	Input 0
					0	0	1	Input 1
					0	1	0	Input 2
					0	1	1	Input 3
					1	0	0	Input 4
					1	0	1	Mute
Gain select								
X	Q_1	Q0	0	0	I_2	I_1	I_0	Gain = 6 dB
			0	1				Gain = 4 dB
			1	0				Gain = 2 dB
			1	1				Gain = 0 dB

6420-06.TBL

X = don't care
MSB is transmitted first
Example : 0 10 01 100 connects outputs 3 with input 4 at a gain of 4dB
The following are selected after power-on reset : input 4 selected for all outputs ; gain = 0dB.

TYPICAL APPLICATION

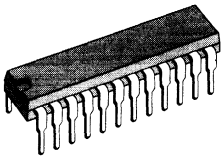


SGS-THOMSON MICROELECTRONICS

TEA6422

BUS-CONTROLLED AUDIO MATRIX

- 6 STEREO INPUTS
- 3 STEREO OUPUTS
- GAIN CONTROL 0dB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERRENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE
- VERY LOW DISTORSION
- FULLY ESD PROTECTED



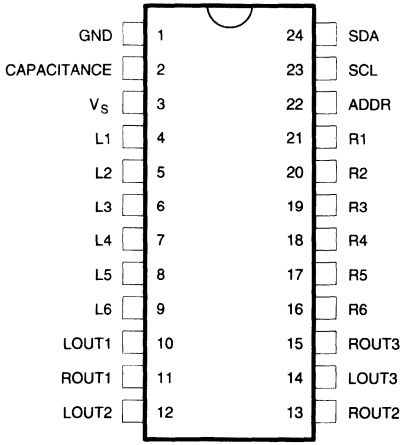
SHRINK 24
(plastic package)

ORDER CODE : TEA6422

DESCRIPTION

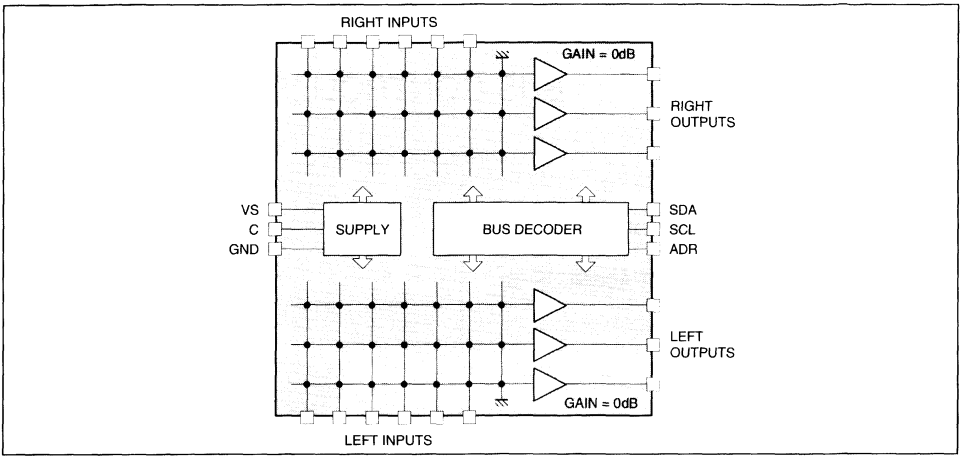
The TEA6422 switches 6 stereo audio on 3 stereo outputs.
All the switching possibities are changed through the I^2C BUS.

PIN CONNECTIONS



6422-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	13.5	V
T_{oper}	Operating ambient temperature	0, + 70	°C
T_{stg}	Storage Temperature	- 20, + 150	°C

6422-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction - ambient thermal resistance	75	°C/W

6422-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	9	12	V
I_S	Supply Current			3	8	mA
SVR	Ripple Rejection	$V_{IN} = 500mV_{RMS}$, f = 20Hz to 20kHz	70	80		dB
MATRIX						
V_{IN}	Input DC Level			4.5		V
R_I	Input Resistance		30	50	100	kΩ
C_S	Channel Separation	$V_{IN} = 2V_{RMS}$, f = 1kHz	70	90		dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level		4.2	4.5	4.8	V
R_{OUT}	Output Resistance			50	100	Ω
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		μV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			kΩ

6422-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^oC$, $V_S = 9V$, $R_L = 10k\Omega$, $R_G = 600\Omega$, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IN}	Input High Voltage (pin 24)		4			V
I_I	Input Current		- 10		10	µA
V_O	Output Voltage	I_O = 3mA ; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note		50		kΩ

6422-04 TBL

Note : R_{pu} is an internal pull-up resistor connected between the address programming pin ADDR and the internal positive supply voltage. Leaving ADDR disconnected or "floating" allows it to become logic 1. Connecting ADDR externally to the GND pin forces it to logic 0.

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

6422-05 TBL

2. Data bytes

Output select								
X	0 0 1	0 1 0	X	X	I_2	I_1	I_0	Output 1 Output 2 Output 3
Input select								
X	Q_1	Q0	X	X	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 0	Input 1 Input 2 Input 3 Input 4 Input 5 Input 6 Mute

6422-06 TBL

X = don't care - MSB is transmitted first
Example : 0 10 XX 100 connects outputs 3 with input 5.
The following are selected after power-on reset all outputs are in mute mode.

Figure 1 : Distorsion Level versus Input Voltage

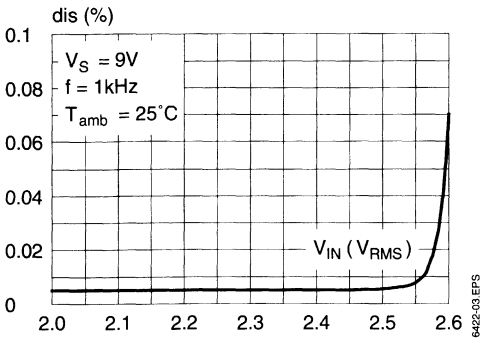


Figure 2 : Clipping Level versus Supply Voltage

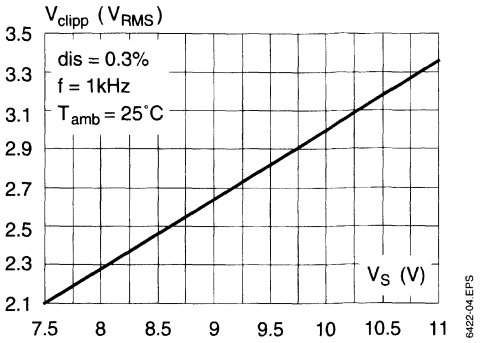
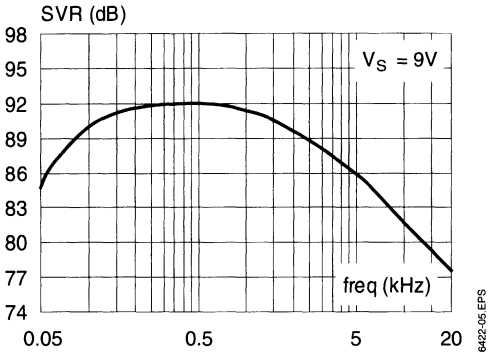
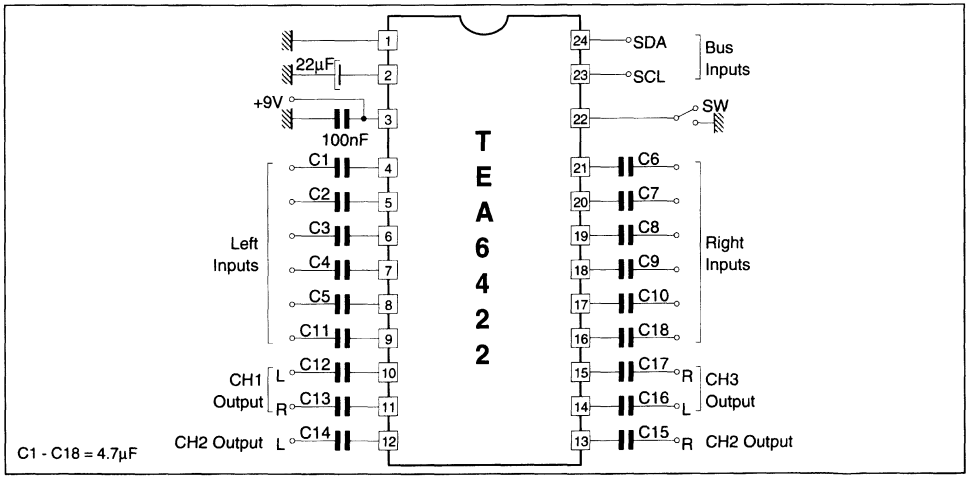


Figure 3 : Supply Voltage Rejection versus frequency (V_{IN} = 500mV_{RMS})



TYPICAL APPLICATION



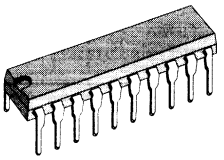
SGS-THOMSON MICROELECTRONICS

TEA6425

VIDEO CELLULAR MATRIX

ADVANCE DATA

- 6 VIDEO INPUTS - 8 VIDEO OUTPUTS
- 2 INTERNAL SELECTABLE YC ADDERS
- 15MHz BANDWIDTH @ -3dB
- SELECTABLE 0.5/6.5dB GAIN FOR EACH OUTPUT
- HIGH IMPEDANCE SWITCH FOR EACH OUTPUT (3-state operation)
- PROGRAMMABLE CLAMP MODE ON EACH INPUT (sync bottom or average value)
- -60dB CROSSTALK @ 5MHz
- 4 SUB-ADDRESS CAPABILITY
- I^2C BUS CONTROL



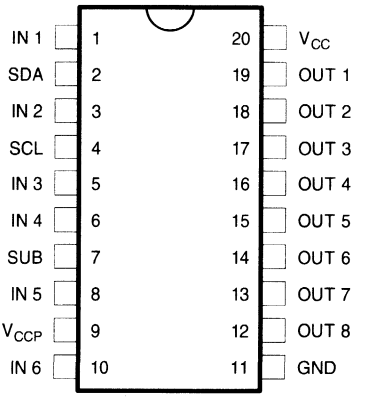
DIP20
(Plastic Package)

ORDER CODE : TEA6425

DESCRIPTION

This device is intended for switching between video and chroma signals such as CVBS, SVHS, base-band CVBS, MAC. Each input clamp mode, each output gain, all switching are controlled through the I^2C bus. The 8 outputs can be set separately in high impedance state, to enable parallel DC connection of several devices (up to 4).

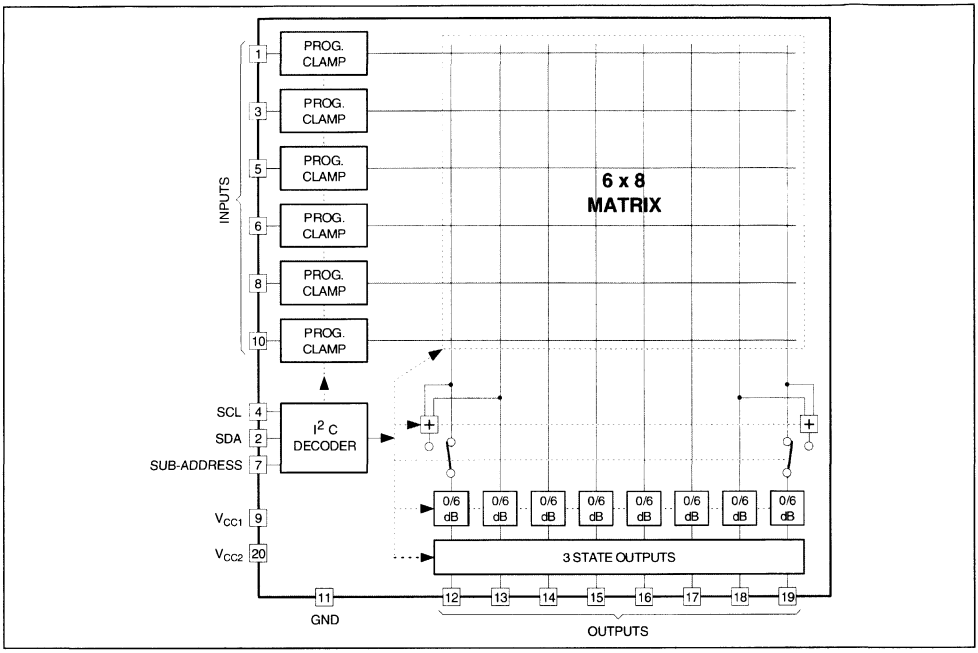
PIN CONNECTIONS



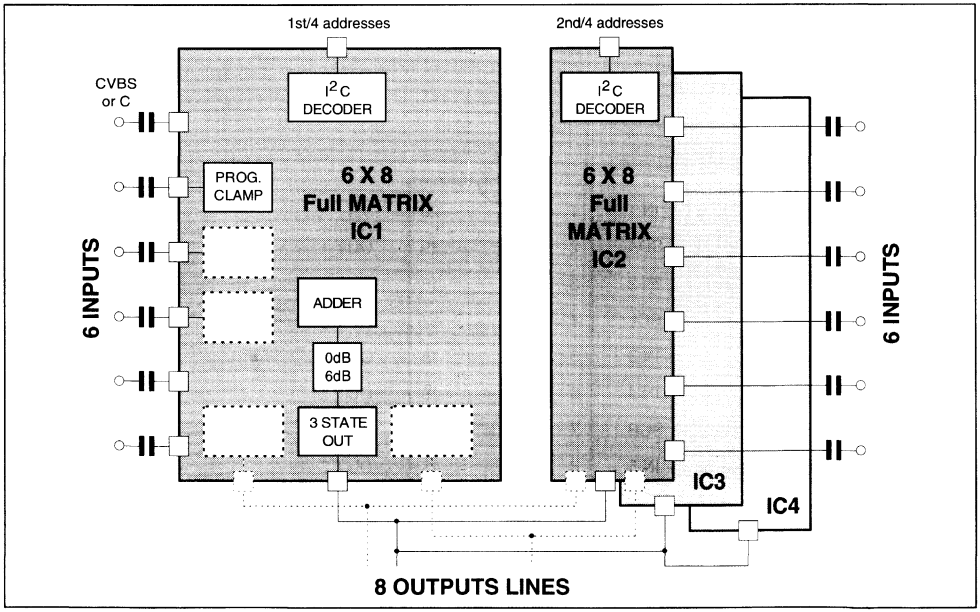
6425-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



CELLULAR MATRICE CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
V_I	Voltage at Pin i to GND	0, V_{CC}	V
T_{oper}	Operating Ambient Temperature	0, + 70	°C
T_{stg}	Storage Temperature	-20, + 150	°C

6425-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Min.	80	°C/W

6425-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, V_{IN} = 1V, Gain = 6.5dB, C_{load} = 20pF, R_{load} = 4.7kΩ ; Gain condition, clamp and 3-state are controlled by I^2C bus, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply Voltage		7.2	8	8.8	V
I_{CC}	Supply Current			30		mA
RR	Supply Voltage Rejection	f = 1kHz	TBD			dB
VIDEO INPUTS (clamping at bottom sync level)						
V_{IN}	Max. Signal Amplitude	Clamp Active	2			V_{PP}
V_{clamp}	Clamp Level	Clamp Active		2		V
V_{DC}	Input DC Level	Clamp Inactive		3		V
I_{IN}	Leakage Current			1	5	µA
I_{clamp}	Clamp Current	V_{clamp} = -200mV		0.9		mA
VIDEO OUTPUTS						
R_{OUT}	Output Resistance			15	50	Ω
Z_{HI}	Output "off" Impedance	no load	TBD			kΩ
C_{HI}	C_{OUT} in 3-state	no load		3		pF
G1	Voltage Gain	f = 100kHz	0	0.5	1	dB
G2	Voltage Gain	f = 100kHz	6	6.5	7	dB
V_{sync}	Top Level Sync (Y or CVBS)		1.15	1.3	3	V
V_{bias}	Output Mean Level (chroma)	G = 6.5dB	3	3.4		V
	Isolation "off" State	f = 5MHz	-60			dB
	Crosstalk Attenuation between Channels	f = 5MHz	-55			dB
B	Bandwidth	C_{load} = 20pF, G = 6.5dB at ± 0.5dB at ± 1dB at - 3dB		 5 10 21		MHz

6425-03.TBL

FUNCTIONAL DESCRIPTION

This device is controlled via a bidirectional I^2C bus, 4 addresses can be selected by a 4-level detector on Pin 7, thus enabling parallel connection of 4 devices.

Via the I^2C bus :

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 0.5 and 6.5dB.
- Each of the 6 inputs can be connected to the 8 outputs.
- Each output can individually be set in a high impedance state.

Two internal SVHS mixers will add the selected Y and C inputs. Two dedicated outputs will have the option to select this added signal also.

I²C BUS SELECTION

I²C Bus Slave Address

Address	A6	A5	A4	A3	A2	A1	A0	R/W
Value	1	0	0	1	0	A1	A0	0

Sub-address I²C

Symbol	Parameter	Conditions		Pin 7 Voltage (typ.)	Unit
Vsub	Slave address HEXA	Sub-address (see note)			
		A1	A0		
1	90	0	0	GND	V
2	96	1	1	V_{CC}	V
3	94	1	0	1/3	V_{CC}
4	92	0	1	2/3	V_{CC}

Note : The first 3 levels are defined by connecting the sub-address pin to the appropriate level. Sub-address 4 will be selected when this pin is left open.

1th Data Byte

	b7	b6	b5	b4	b3	b2	b1	b0	Selected Output
	a2	a1	a0	*	*	*	*	I	
Output Select	0	0	0	*	*	*	*	0	OUT1
	0	0	1	*	*	*	*	0	OUT2
	0	1	0	*	*	*	*	0	OUT3
	0	1	1	*	*	*	*	0	OUT4
	1	0	0	*	*	*	*	0	OUT5
	1	0	1	*	*	*	*	0	OUT6
	1	1	0	*	*	*	*	0	OUT7
	1	1	1	*	*	*	*	0	OUT8

2nd Data Byte

	b7	b6	b5	b4	b3	b2	b1	b0	Action
	a2	a1	a0	*	*	*	*	I	
Input Select	0	0	0	*	*	*	*	1	IN1
	0	0	1	*	*	*	*	1	IN2
	0	1	0	*	*	*	*	1	IN3
	0	1	1	*	*	*	*	1	IN4
	1	0	0	*	*	*	*	1	IN5
	1	0	1	*	*	*	*	1	IN6
Clamp	*	*	*	0	*	*	*	1	Free
	*	*	*	1	*	*	*	1	Clamped
Gain	*	*	*	*	0	*	*	1	0.5dB
	*	*	*	*	1	*	*	1	6.5dB
Mixer	*	*	*	*	*	0	*	1	Disabled
	*	*	*	*	*	1	*	1	Enabled
Tri-state	*	*	*	*	*	*	0	1	Low impedance
	*	*	*	*	*	*	1	1	Tri-state

Power On Reset

When active : outputs in 3-state, inputs are clamped.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
		Decr. V_{CC}			4.2	V
	End of Reset	Incr. V_{CC}	4.5			V

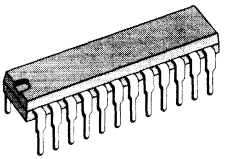
SGS-THOMSON MICROELECTRONICS

TEA6430

AUDIO CELLULAR MATRIX

ADVANCE DATA

- 5 STEREO INPUTS - 4 STEREO OUTPUTS
- 3-STATE OPERATION FOR EACH OUTPUT
- GAIN OUTPUT CONTROL 0dB/2/4/6dB/MUTE FOR EACH
- VERY LOW NOISE AND DISTORTION
- I^2C BUS CONTROL
- 4 SUB-ADDRESS FACILITY
- 90dB CROSSTALK BETWEEN ANY INPUT AND OUTPUT



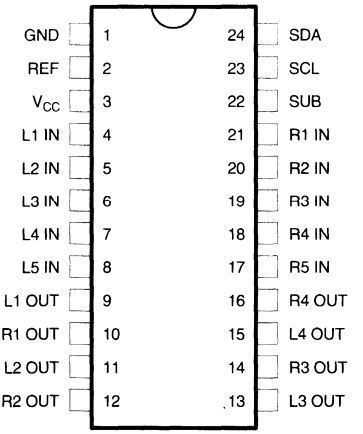
SHRINK 24
(Plastic Package)

ORDER CODE : TEA6430

DESCRIPTION

The TEA6430 switches 5 stereo inputs on 4 stereo outputs, providing the customer with high quality sound (low noise, low distortion). The 4 stereo outputs can be set separately in high impedance state, to enable parallel connection of several devices (up to 4). All functions are controlled through the I^2C bus.

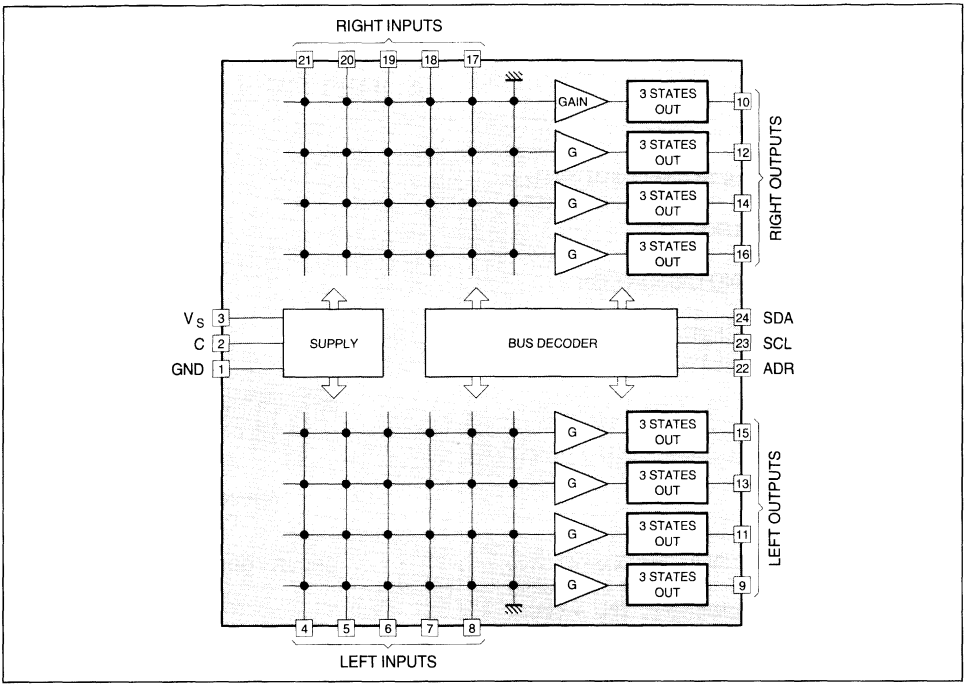
PIN CONNECTIONS



6430-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



The output loads have to be larger than 2kΩ (typical 10kΩ) and 1500pF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
V_I	Voltage at Pin i to GND	0, V_{CC}	V
T_{oper}	Operating Ambient Temperature	0, + 70	°C
T_{stg}	Storage Temperature	-20, + 150	°C

6430-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	75	°C/W

6430-02.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, R_L = 10kΩ, R_G = 600Ω, f = 1kHz, V_{IN} = 0.5V_{RMS} ; 3-state is controlled by I^2C bus, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply Voltage		7.2	8	8.8	V
I_{CC}	Supply Current			7		mA
RR	Ripple Rejection	V_{IN} = 0.5V_{RMS}, f = 1kHz	70			dB

6430-03.TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 8V, T_{amb} = 25°C, R_L = 10kΩ, R_G = 600Ω, f = 1kHz, V_{IN} = 0.5V_{RMS} ; 3-state is controlled by I^2C bus, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO INPUTS						
V_{IN}	Max. Signal Amplitude		2			V_{RMS}
V_{DC}	Input DC Level			$V_{CC}/2$		V
R_I	Input Resistance		30	50		kΩ
AUDIO OUTPUTS						
R_{OUT}	Output Resistance			60	100	Ω
Z_{HI}	Output "off" Impedance	f = 20kHz, output disabled	50			kΩ
V_{OFF}	DC Offset Change	Switching between inputs, see note 1		0.1	5	mV
V_{OUT}	Output DC Level			$V_{CC}/2$		V
V_N	Output Noise Voltage	B = 20-20kHz, flat, see note 2			5	μV
G	Gain	B = 20-20kHz, R_L = 2kΩ	-0.5	0	+0.5	dB
	Isolation "off" State	f = 1kHz, output disabled	85			dB
THD	Distortion	V_{IN} = 1V_{RMS}, f = 1kHz		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3%	2	2.3		V_{RMS}
C_S	L, R Channel Separation	f = 1kHz	-85			dB
	Crosstalk Audio Channels	f = 1kHz, see note 3	-85	-100		dB

6430-04.TBL

Notes : 1. DC offset change is less than maximum limit, in all configurations (one or several devices in parallel), provided that the reference Pins (P2) are all connected together.
2. Flat filter according to CCIR-468-4, B = 20Hz-20kHz
3. Measured from any selected output which contains no signal to a set of other outputs.

I^2C BUS SELECTION

I^2C Bus Slave Address

Address	A6	A5	A4	A3	A2	A1	A0	R/W
Value	1	0	0	1	1	A1	A0	0

Sub-address I^2C

Symbol	Parameter	Conditions		Pin 22 Voltage (typ.)	Unit
Vsub	Slave address HEXA	Sub-address (see note)			
		A1	A0		
1	98	0	0	GND	V
2	9E	1	1	V_{CC}	V
3	9C	1	0	1/3	V_{CC}
4	9A	0	1	2/3	V_{CC}

Note : The first 3 levels are defined by connecting the sub-address pin to the appropriate level. Sub-address 4 will be selected when this pin is left open.

Data Byte

	b7	b6	b5	b4	b3	b2	b1	b0	Action
	T	01	00	G1	G0	I2	I1	I0	
Input Select	*	*	*	*	*	0	0	0	IN1
	*	*	*	*	*	0	0	1	IN2
	*	*	*	*	*	0	1	0	IN3
	*	*	*	*	*	0	1	1	IN4
	*	*	*	*	*	1	0	0	IN5
	*	*	*	*	*	1	0	1	Mute
Output Select	*	0	0	*	*	*	*	*	OUT1
	*	0	1	*	*	*	*	*	OUT2
	*	1	0	*	*	*	*	*	OUT3
	*	1	1	*	*	*	*	*	OUT4
Gain	*	*	*	0	0	*	*	*	6dB
	*	*	*	0	1	*	*	*	4dB
	*	*	*	1	0	*	*	*	2dB
	*	*	*	1	1	*	*	*	0dB
Tri-state	0	*	*	*	*	*	*	*	Low impedance
	1	*	*	*	*	*	*	*	Tri-state

Example : 00111100 enables L(R)2 out and connect it with a gain of 0dB to L(R)5 in.

Power On Reset

When active : outputs in 3-state. All outputs are disabled and L(R)5 is selected to drive all outputs. Gain = 0dB.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
		Decr. V_{CC}			4.2	V
	End of Reset	Incr. V_{CC}	4.5			V

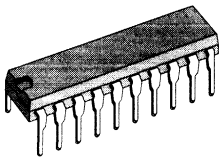
REMOTE CONTROL

SGS-THOMSON MICROELECTRONICS

M3004AB1

REMOTE CONTROL TRANSMITTER

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



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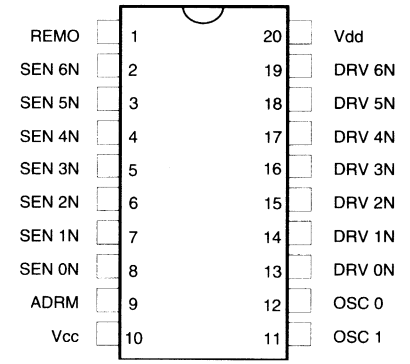
PIN CONNECTIONS



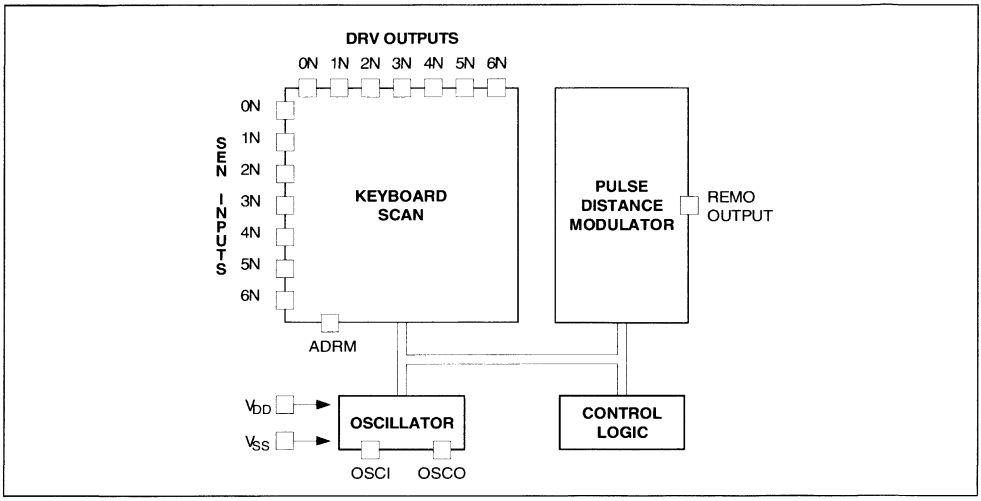
3004-01.EPS

DESCRIPTION

The M3004AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)
The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT
(OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple keystroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key.protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

3004-01.TBL

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

3004-02.TBL

Table 2 : Pulse Train Separation (t_b)

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

3004-03.TBL

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

3004-04.TBL

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1	**			8 to 15
*	SEN2N	0	1	0	**			16 to 23
*	SEN3N	0	1	1	**			24 to 31
*	SEN4N	1	0	0	**			32 to 39
*	SEN5N	1	0	1	**			40 to 47
*	SEN6N	1	1	0	**			48 to 55
*	SEN5N and SEN6N	1	1	1	**			56 to 63

3004-05.TBL

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5/SEN6N.
** The C, B and A codes are identical to SEN0N as given above.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

3004-06.TBL

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C		4		12	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload	V_{DD} = 6V V_{DD} = 9V		0.8 1.5	1.5 3	mA mA
		• Inactive (stand-by mode)	V_{DD} = 6V V_{DD} = 9V			2 2	µA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)		350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N							
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V				0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V		0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V V_{DD} = 11V, V_I = 0V		25 75		250 750	µA µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = VDD				1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N							
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA V_{DD} = 11V, I_O = 1mA				0.3 0.5	V V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V				10	µA

3004-07.TBL

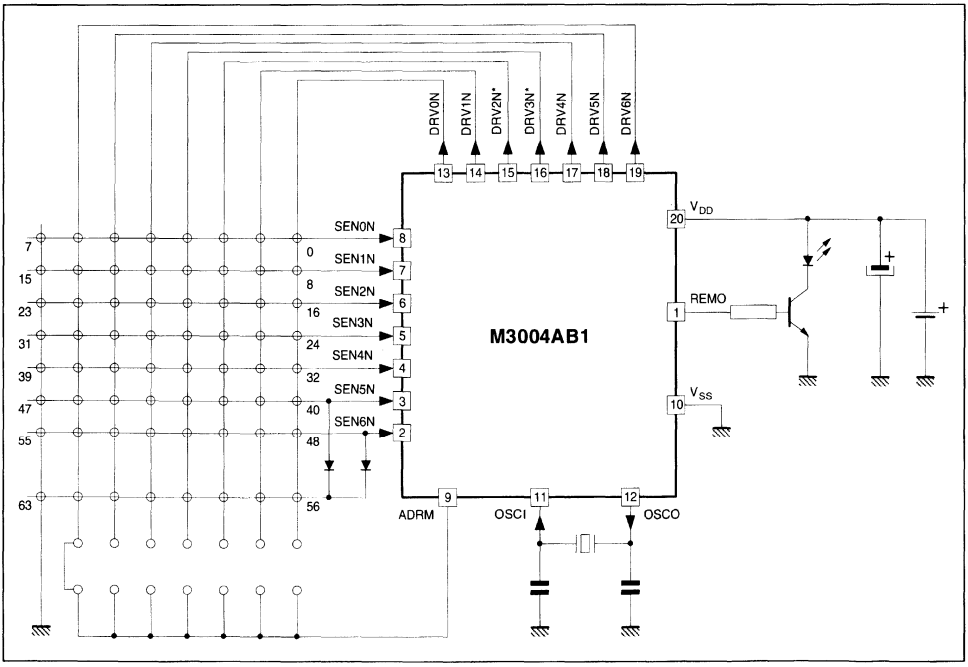
ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

3004-08.TBL

Figure 1 : Typical Application



3004-03.EPS

Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated)

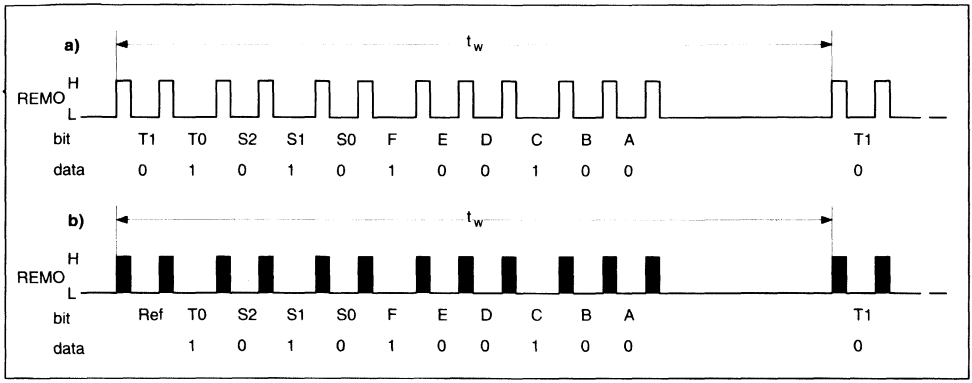


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$)}

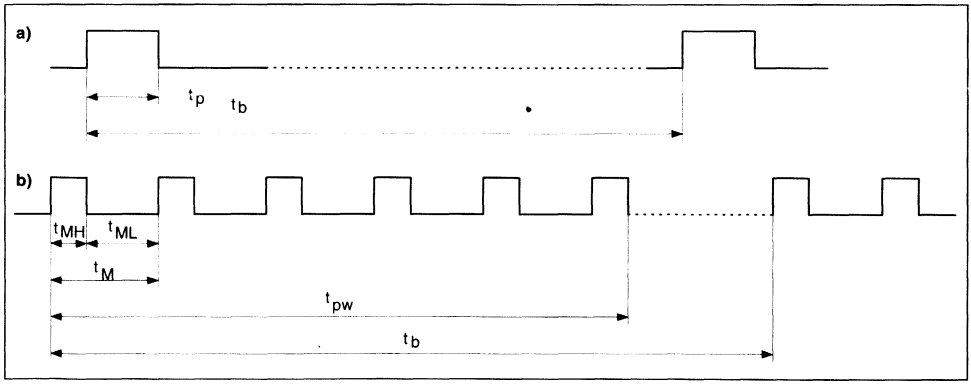


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O

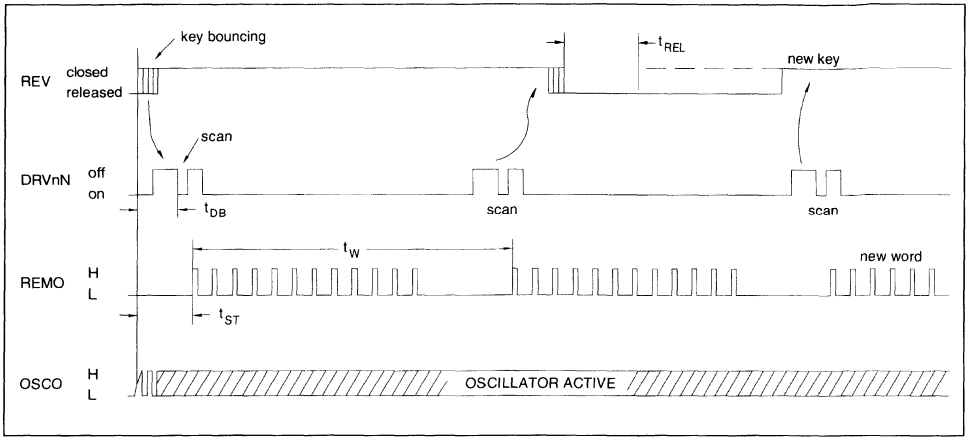
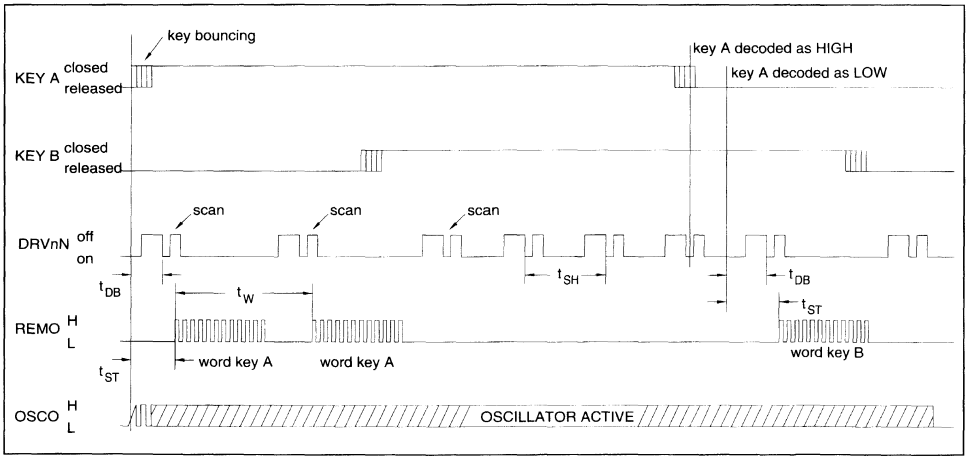


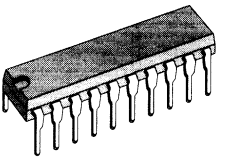
Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O



M3004LAB1
M3004LD

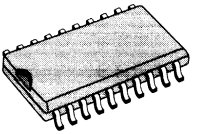
REMOTE CONTROL TRANSMITTER

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

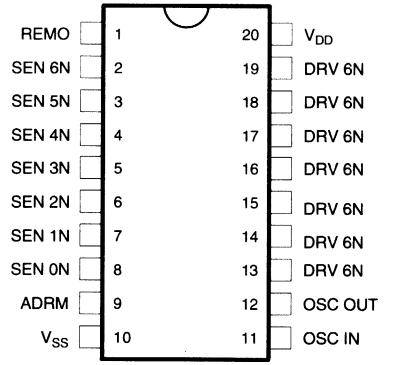
ORDER CODE : M3004LAB1



SO20
(Plastic Package)

ORDER CODE : M3004LD

PIN CONNECTIONS

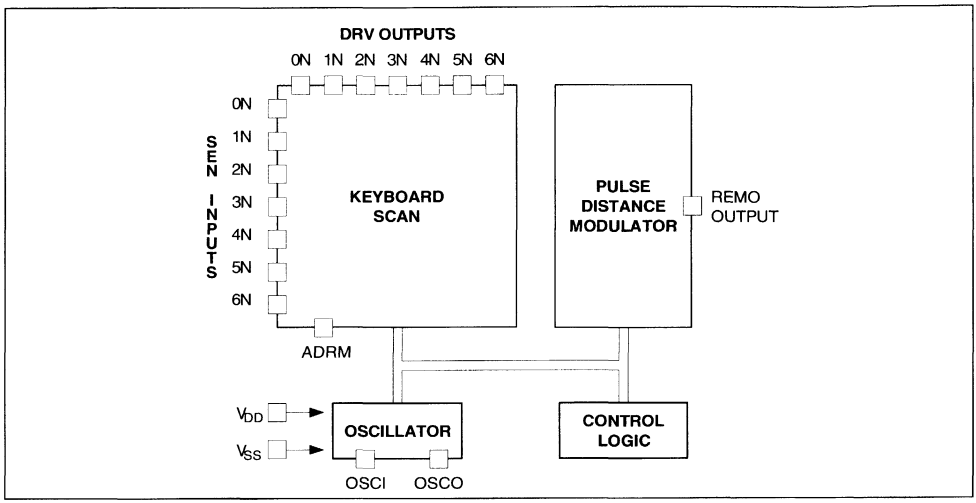


DESCRIPTION

The M3004LAB1/M3004LD transmitter IC are designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004LAB1/M3004LD generate the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)
The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT
(OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple keystroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

3004L-01.TBL

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period Low
t_{MH}	4 x t_{OSC}	Modulation Period High
t_W	55296 x t_{OSC}	Word Distance
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance

3004L-02.TBL

The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ration is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b)

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

3004L-03.TBL

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

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O= connected to ADRM
blank= not connected to ADRM
X = don't care

Table 4 : Key Codes

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		*		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

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* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 125	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

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ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz V_{DD} = 3V REMO,Output unload V_{DD} = 6V • Inactive (stand-by mode) V_{DD} = 6V		0.25 1.0	0.5 2 2	mA mA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V	10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA V_{DD} = 6.5V, I_O = 2.5mA			0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V			10	µA

3004L-07.TBL

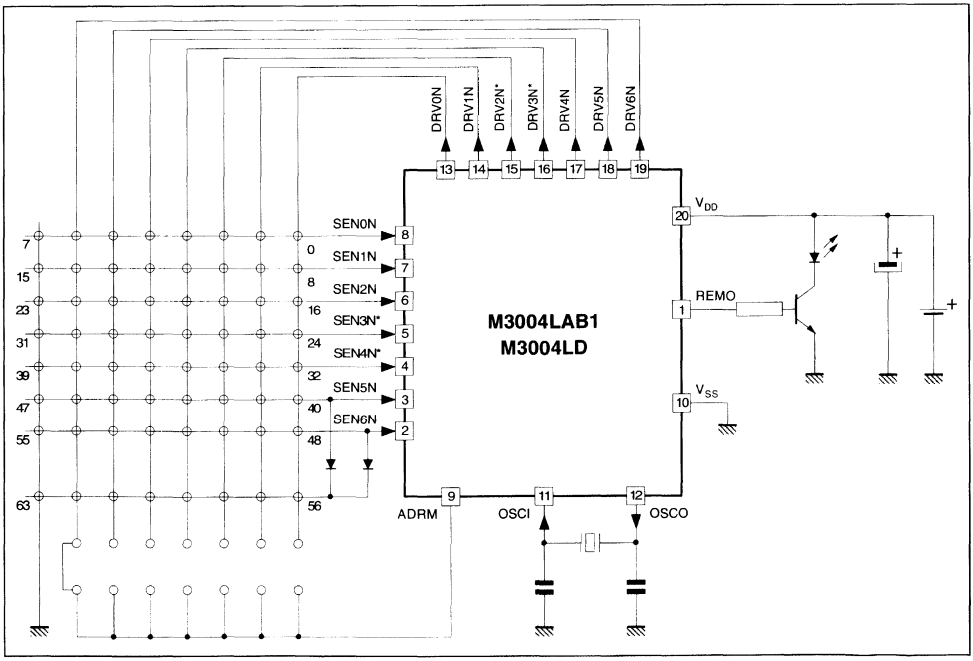
ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

3004L-08.TBL

Figure 1 : Typical Application



3004L-03.EPS

Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated)

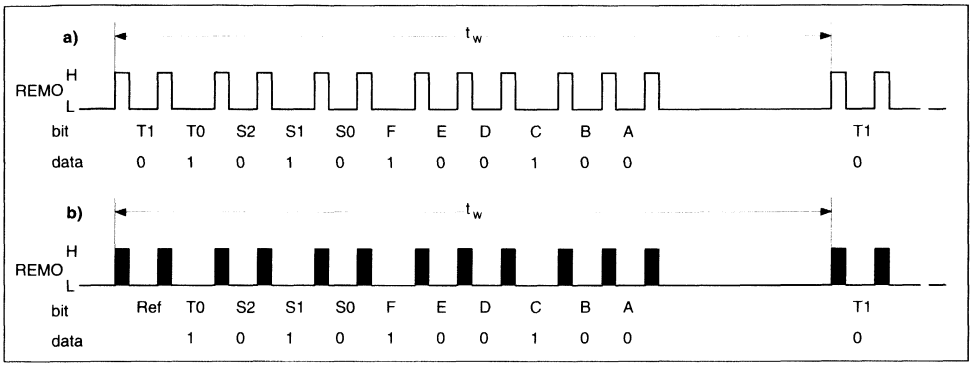


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse [$t_{PW} = (5 \times t_M) + t_{MH}$]

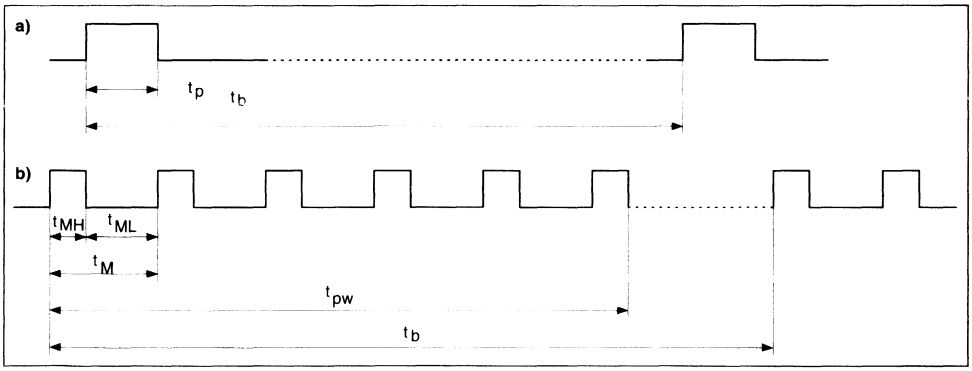


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O

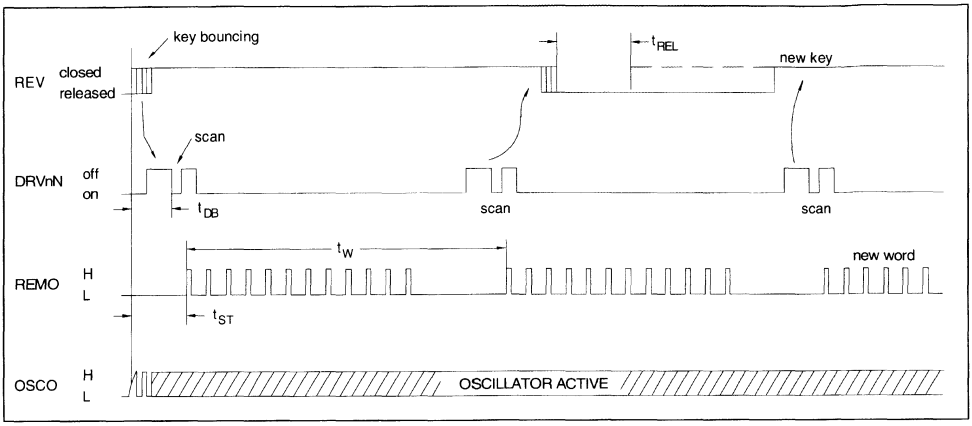
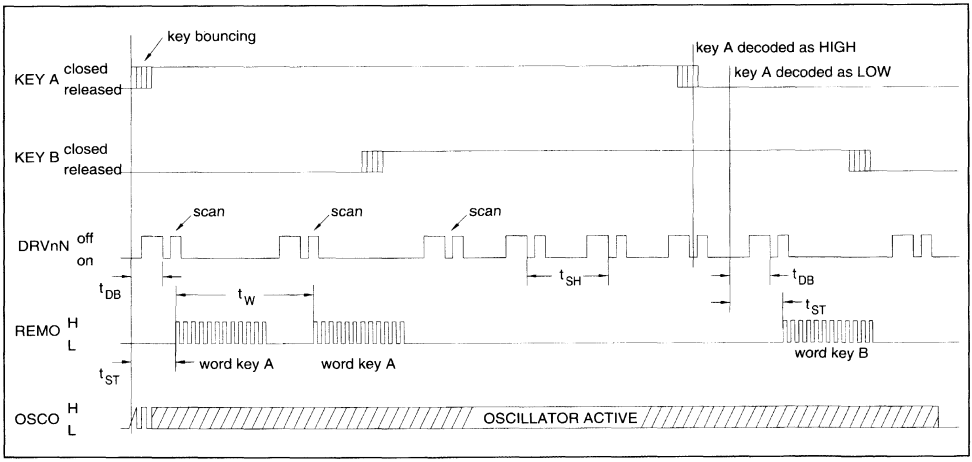


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O

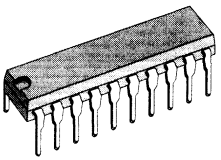


SGS-THOMSON MICROELECTRONICS

M3005AB1

REMOTE CONTROL TRANSMITTER

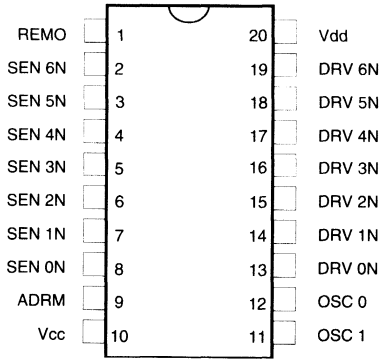
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 11V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

ORDER CODE : M3005AB1

PIN CONNECTIONS



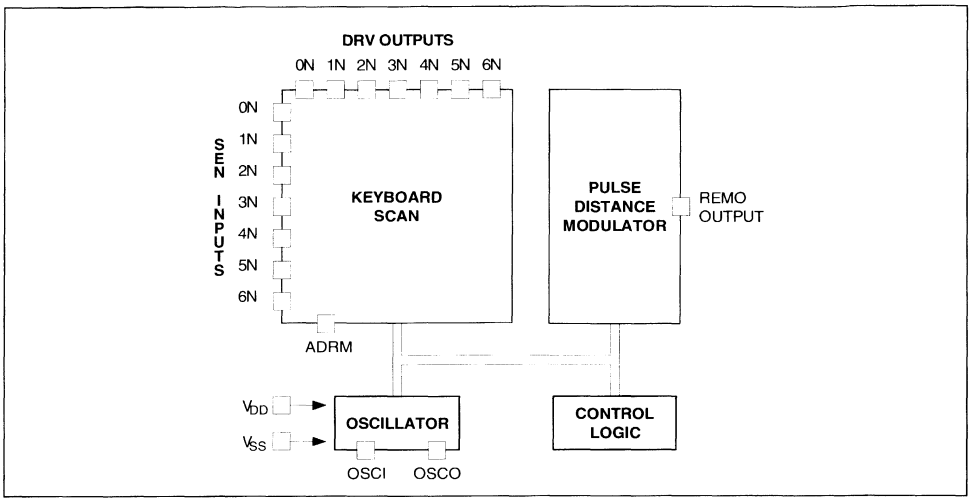
3005-01.EPS

DESCRIPTION

The M3005AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3005AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



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ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

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(OSCI and OSCO)

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The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple keystroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

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Flashed	2.53	8.8	-	121
Modulated	2.53	-	t_{OSC}	121

3005-01 TBL

	Flash Mode	Carrier Mode	
f_{OSC}	455kHz	600kHz	
t_P	4 x t_{OSC}		Flashed Pulse Width
t_M		t_{OSC}	Modulation Period
			Number of Modulation Pulses
T_O	1152 x t_{OSC}	1536 x tOSC	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	73728 x tOSC	Word Distance

3005-02 TBL

The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples. the correct divider ration is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b)

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O

3005-03 TBL

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The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

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O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes

Matrix Drive	Matrix Sense	Code F	E	D	C	B	A	Matrix Position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		**		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

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* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5/SEN6N.
** The C. B and A codes are identical to SEN0N as given above.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 12	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

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ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C		4		11	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz	V_{DD} = 6V		0.8	1.5	mA
		REMO,Output unload	V_{DD} = 9V		1.5	3	mA
		• Inactive (stand-by mode)	V_{DD} = 6V			2	µA
			V_{DD} = 9V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 4 to 11V (cer resonator)		350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N							
V_{IL}	Input Voltage Low	V_{DD} = 4 to 11V				0.2 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 4 to 11V		0.8 x V_{DD}			V
- I_I	Input Current	V_{DD} = 4V, V_I = 0V		25		250	µA
		V_{DD} = 11V, V_I = 0V		75		750	µA
I_I	Input Leakage Current	V_{DD} = 11V, V_I = V_{DD}				1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N							
V_{OL}	Output Voltage "ON"	V_{DD} = 4V, I_O = 0.1mA				0.3	V
		V_{DD} = 11V, I_O = 1mA				0.5	V
I_O	Output Current "OFF"	V_{DD} = 11V, V_O = 11V				10	µA

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ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.2 x V_{DD}	V
V_{IH}	Input Voltage High		0.8 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 4V V_{DD} = 11V	 25 75		 250 750	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 6V, V_{OH} = 3V V_{DD} = 9V, V_{OH} = 6V	80 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 6V, V_{OL} = 0.2V V_{DD} = 9V, V_{OL} = 0.1V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 6V, OSC1 at V_{DD}	0.8		2.7	µA
V_{OH}	Output Voltage high	V_{DD} = 6V, - I_{OL} = 0.1mA			V_{DD} - 0.6	V
V_{OL}	Output Voltage Low	V_{DD} = 6V, I_{OH} = 0.1mA			0.6	V

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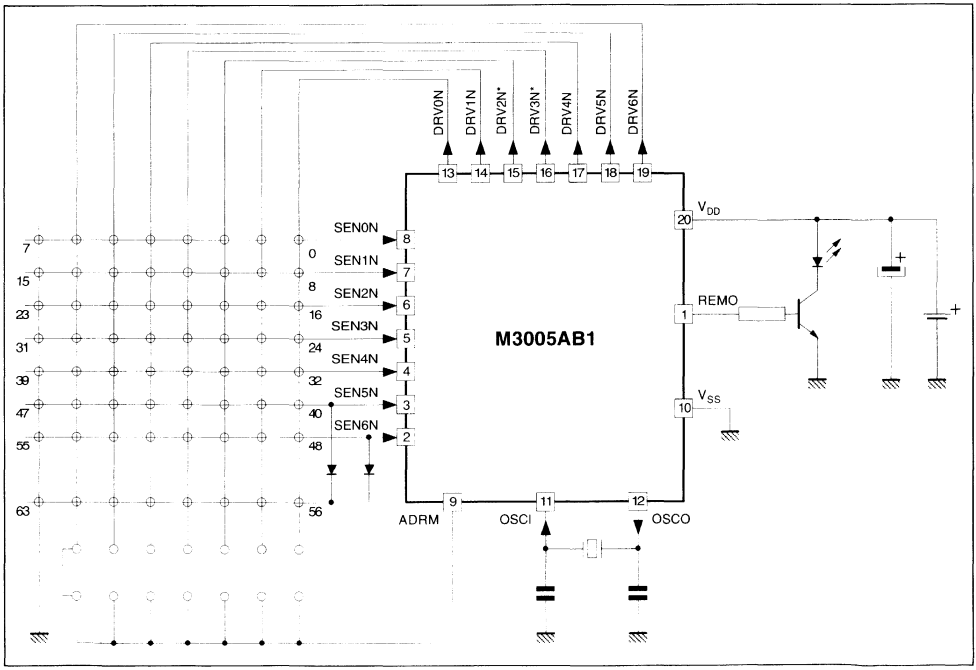
Figure 1 : Typical Application



3005-03.EPS

Figure 2 : Data Format of REMO Output

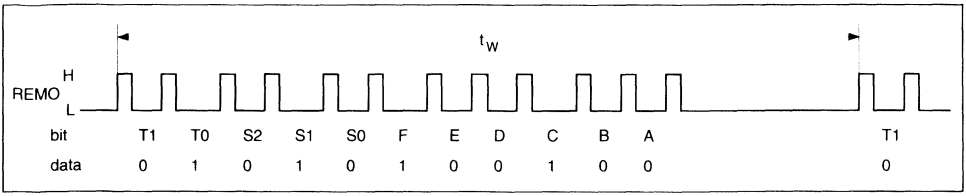


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

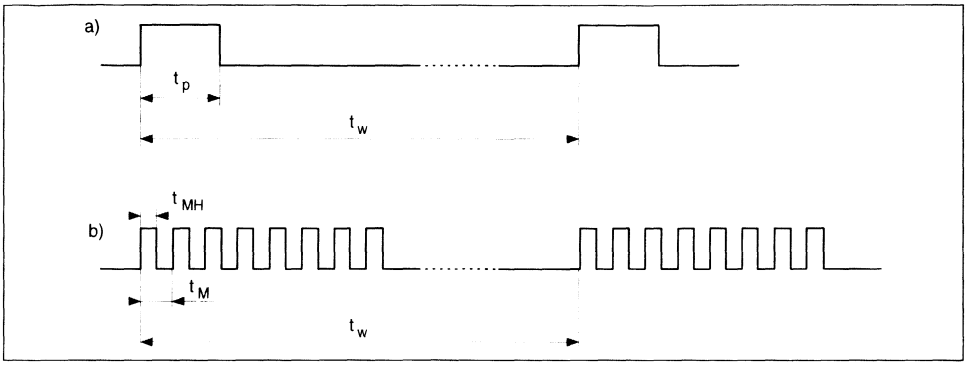


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O

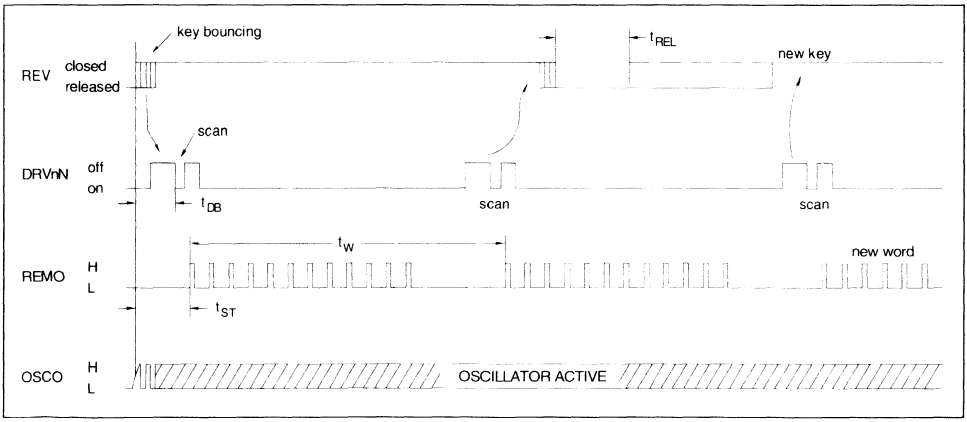
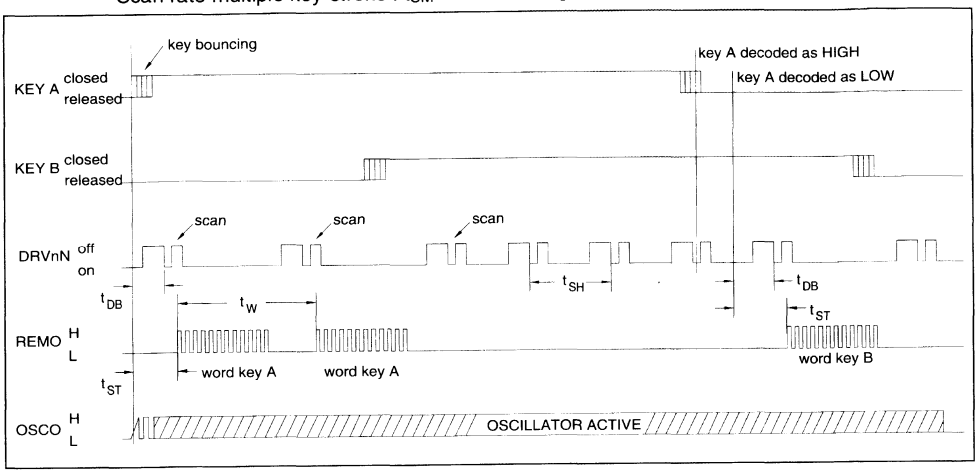


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O

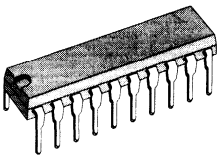


SGS-THOMSON MICROELECTRONICS

M3005LAB1
M3005LD

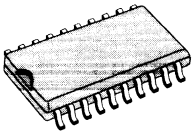
REMOTE CONTROL TRANSMITTER

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V (– I_{OH} = 80mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)



DIP20
(Plastic Package)

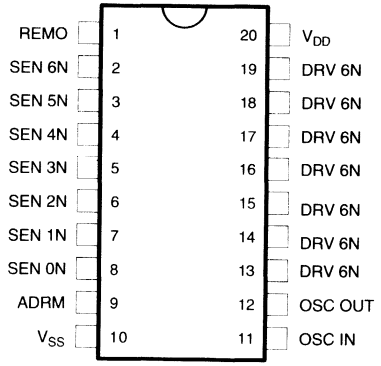
ORDER CODE : M3005LAB1



SO20
(Plastic Package)

ORDER CODE : M3005LD

PIN CONNECTIONS



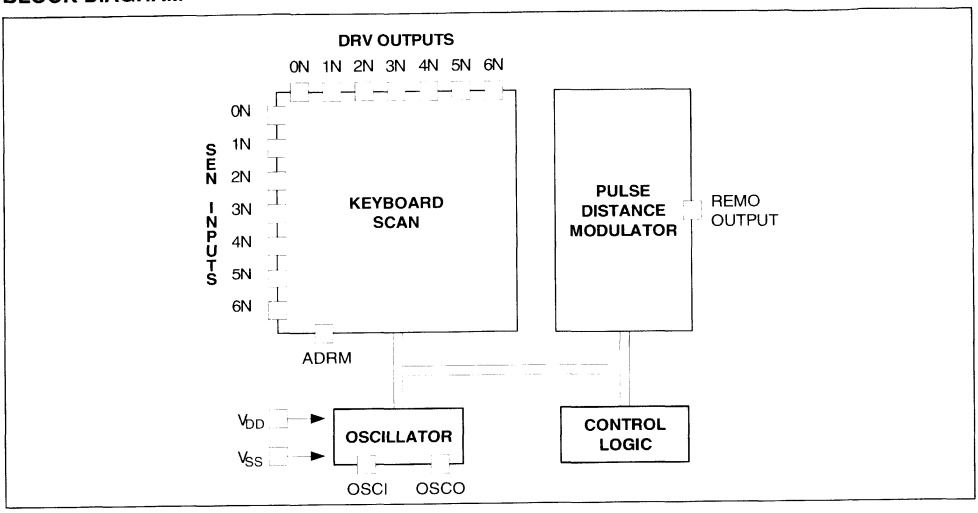
3005L-01.EPS

DESCRIPTION

The M3005LAB1/M3005LD transmitter IC are designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3005LAB1/M3005LD generate the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N)
The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function is an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1ms, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT / OUTPUT
(OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively.

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple keystroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_W (ms)
Flashed	2.53	8.8	-	121
Modulated	2.53	-	tosc	121

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	Flash Mode	Carrier Mode	
fosc	455kHz	600kHz	
t_P	4 x tosc		Flashed Pulse Width
t_M	12 x tosc	tOSC	Modulation Period
N		8*	Number of Modulation Pulses
T_O	1152 x tosc	1536 x tOSC	Basic Unit of Pulse Distance
t_W	55296 x tosc	73728 x tOSC	Word Distance

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The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ration is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b)

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O

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Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

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O= connected to ADRM
blank= not connected to ADRM
X = don't care

Table 4 : Key Codes

Matrix Drive	Matrix Sense	Code F	E	D	C	B	A	Matrix Position
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
V_{SS}	SEN0N	0	0	0	1	1	1	7
*	SEN1N	0	0	1		**		8 to 15
*	SEN2N	0	1	0		**		16 to 23
*	SEN3N	0	1	1		**		24 to 31
*	SEN4N	1	0	0		**		32 to 39
*	SEN5N	1	0	1		**		40 to 47
*	SEN6N	1	1	0		*		48 to 55
*	SEN5N and SEN6N	1	1	1		**		56 to 63

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* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5/SEN6N.

** The C, B and A codes are identical to SEN0N as given above.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
+ I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

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ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C		2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz REMO,Output unload	V_{DD} = 3V V_{DD} = 6V		0.25 1.0	0.5 2	mA mA
		• Inactive (stand-by mode)	V_{DD} = 6V			2	µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)		350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N							
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V				0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V		0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V		10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}				1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N							
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.25mA V_{DD} = 6.5V, I_O = 2.5mA				0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 11V				10	µA

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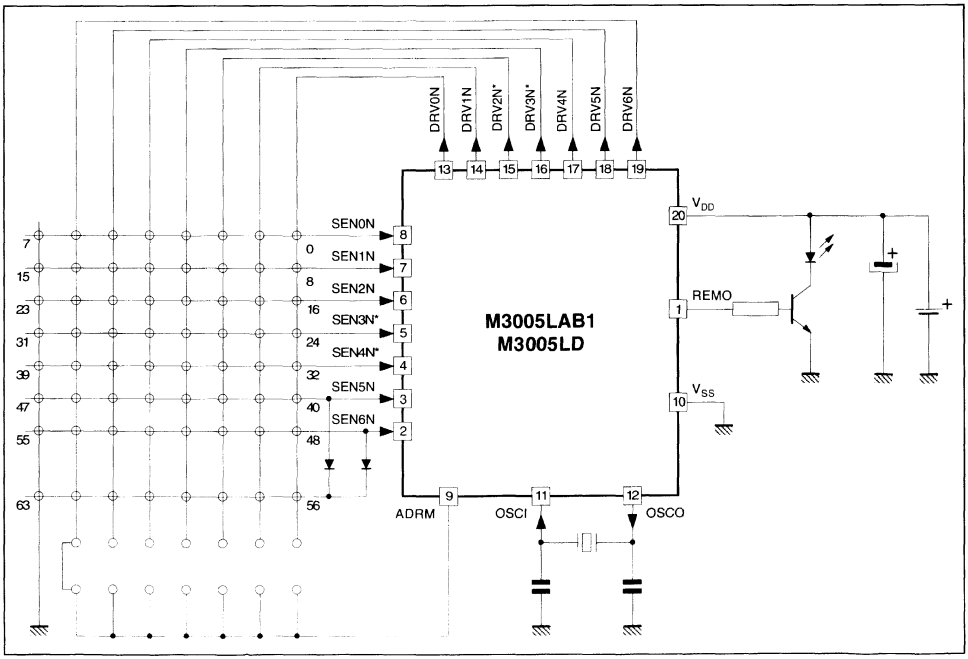
ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
- I_{OH}	Output Current High	V_{DD} = 2V, V_{OH} = 0.8V V_{DD} = 6.5V, V_{OH} = 5V	60 80			mA mA
I_{OL}	Output Current Low	V_{DD} = 2V, V_{OL} = 0.4V V_{DD} = 6.5V, V_{OL} = 0.4V			0.6 0.6	mA mA
t_{MH}/t_{OSC}	Pulse Duty Cycle	During Carrier Mode	0.4	0.5	0.6	
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = 2V V_{DD} = 6.5V, OSC1 at V_{DD}	 5		5 7	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

3005L-08.TBL

Figure 1 : Typical Application



3005L-03.EPS

Figure 2 : Data Format of REMO Output

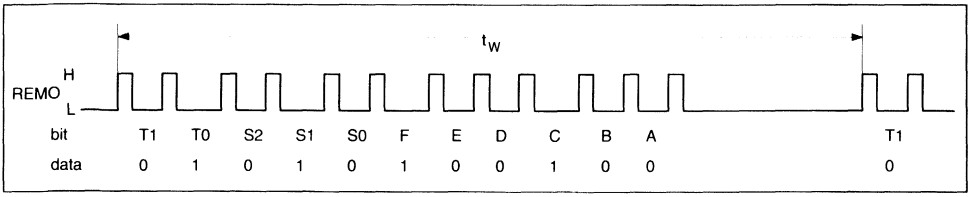


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse

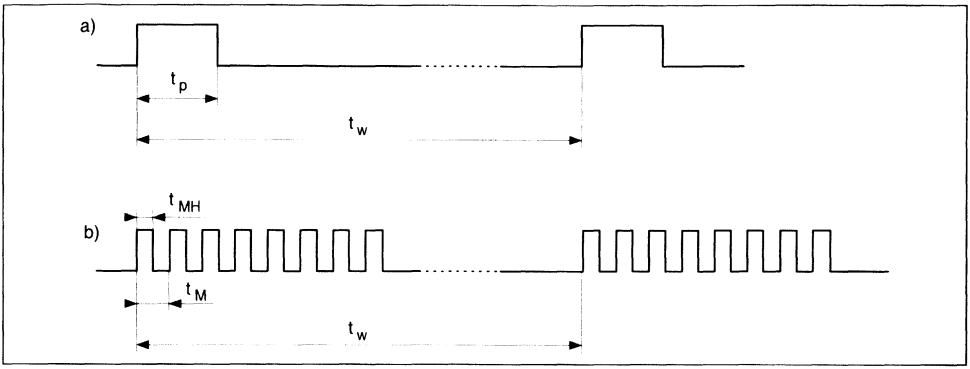


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O

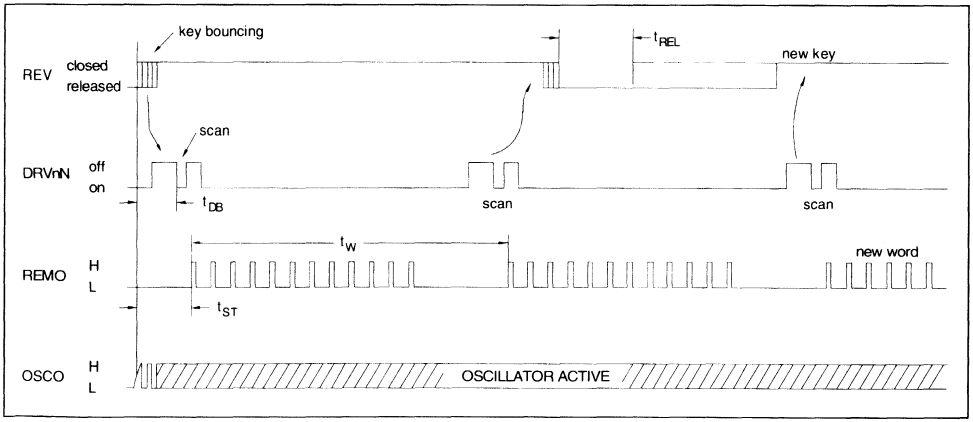
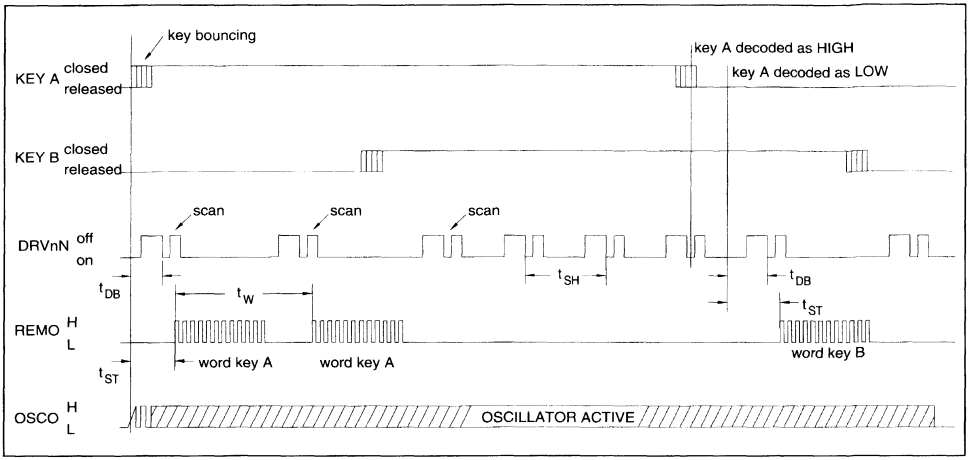


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O

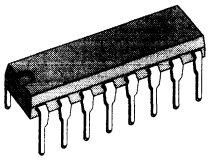


SGS-THOMSON MICROELECTRONICS

M3006LAB1

REMOTE CONTROL TRANSMITTER

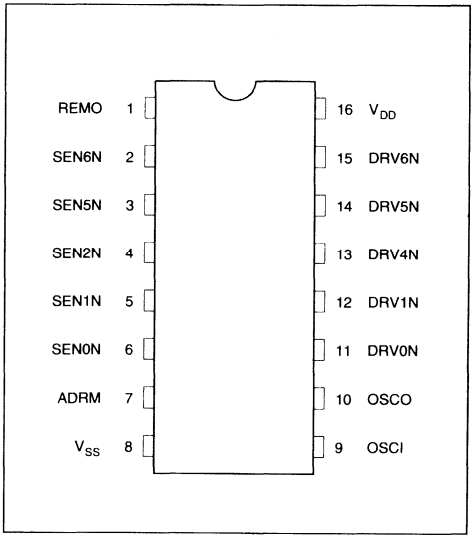
- FLASHED OR MODULATED TRANSMISSION
- 5 SUB-SYSTEM ADDRESSES
- UP TO 36 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 120mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2µA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 16-LEAD PLASTIC DIL



DIP16
(Plastic Package)

ORDER CODE : M3006LAB1

PIN CONNECTIONS



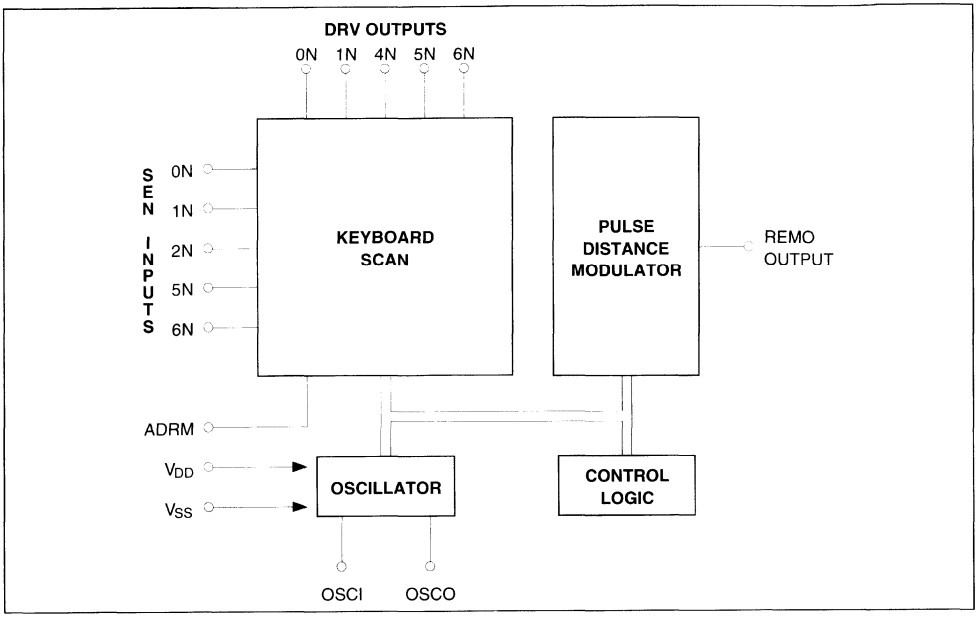
3006L-01.EPS

DESCRIPTION

The M3006LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 180 commands which are divided into 5 sub-system groups with 36 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3006LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).
The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 5 driver outputs and 5 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 5 sense inputs (SEN0N to SEN6N) enable the generation of 30 command codes. With 2 external diodes all 36 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRVON to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of five sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode, only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnN with the highest number (n) defines the sub-system address, e.g. if drivers DRV1N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV4N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 5. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT
(OSCI and OSCO)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple keystroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 5, 11, 17, 23, 29 and 35) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 30 to 35).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1 : Pulse Train Timing

Mode	T_O (ms)	t_P (µs)	t_M (µs)	t_{ML} (µs)	t_{MH} (µs)	t_W (ms)
Flashed	2.53	8.8	-	-	-	121
Modulated	2.53	-	26.4	17.6	8.8	121

3006L-01.TBL

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	Word Distance

3006L-02.TBL

Table 2 : Pulse Train Separation (t_b)

Code	t_b
Logic "0"	2 x T_O
Logic "1"	3 x T_O
Toggle Bit Time	2 x T_O or 3 x T_O
Reference Time	3 x T_O

3006L-03.TBL

Table 3 : Transmission Mode and Sub-system Adress Selection.
The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N To DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Adress				Driver DRVnN for n =				
	#	S2	S1	S0	0	1	4	5	6
FLASHED	0	1	1	1					
	1	0	0	0	O				
	2	0	0	1	X	O			
	5	1	0	0	X	X	O		
	6	1	0	1	X	X	X	O	
MODULATED	0	1	1	1					O
	1	0	0	0	O				O
	2	0	0	1	X	O			O
	5	1	0	0	X	X	O		O
	6	1	0	1	X	X	X	O	O

3006L-04.TBL

O = connected to ADRM
blank = not connected to ADRM
X = don't care

Table 4 : Key Codes

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV4N	SEN0N	0	0	0	1	0	0	2
DRV5N	SEN0N	0	0	0	1	0	1	3
DRV6N	SEN0N	0	0	0	1	1	0	4
V_{SS}	SEN0N	0	0	0	1	1	1	5
*	SEN1N	0	0	1	**			6 to 11
*	SEN4N	0	1	0	**			12 to 17
*	SEN5N	1	0	1	**			18 to 23
*	SEN6N	1	1	0	**			24 to 29
*	SEN5N and SEN6N	1	1	1	**			30 to 35

3006L-05.TBL

* The complete matrix drive as shown above for SEN0N is also applicable for the matrix sense inputs SEN1N to SEN6N and the combined SEN5/SEN6N.
** The C, B and A codes are identical to SEN0N as given above.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	- 0.3 to + 7	V
V_I	Input Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	- 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max. 10	mA
- I (REMO) M	Peak REMO Output Current during 10µs, Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_A = - 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	- 55 to + 150	°C
T_A	Operating Ambient Temperature Range	- 20 to + 70	°C

3006L-06.TBL

ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	T_A = 0 to + 70°C	2		6.5	V
I_{DD}	Supply Current	• Active f_{OSC} = 455kHz V_{DD} = 3V REMO,Output unload V_{DD} = 6V • Inactive (stand-by mode) V_{DD} = 6V		0.25 1.0	 4	mA mA µA
f_{OSC}	Oscill. Frequency	V_{DD} = 2 to 6.5V (cer resonator)	350		600	kHz
KEYBOARD MATRIX - Inputs SE0N to SEN6N						
V_{IL}	Input Voltage Low	V_{DD} = 2 to 6.5V			0.3 x V_{DD}	V
V_{IH}	Input Voltage High	V_{DD} = 2 to 6.5V	0.7 x V_{DD}			V
- I_I	Input Current	V_{DD} = 2V, V_I = 0V V_{DD} = 6.5V, V_I = 0V	10 100		100 600	µA µA
I_I	Input Leakage Current	V_{DD} = 6.5V, V_I = V_{DD}			1	µA
KEYBOARD MATRIX - Outputs DRV0N to DRV6N						
V_{OL}	Output Voltage "ON"	V_{DD} = 2V, I_O = 0.1mA V_{DD} = 6.5V, I_O = 1mA			0.3 0.6	V V
I_O	Output Current "OFF"	V_{DD} = 6.5V, V_O = 6.5V			10	µA

3006L-07.TBL

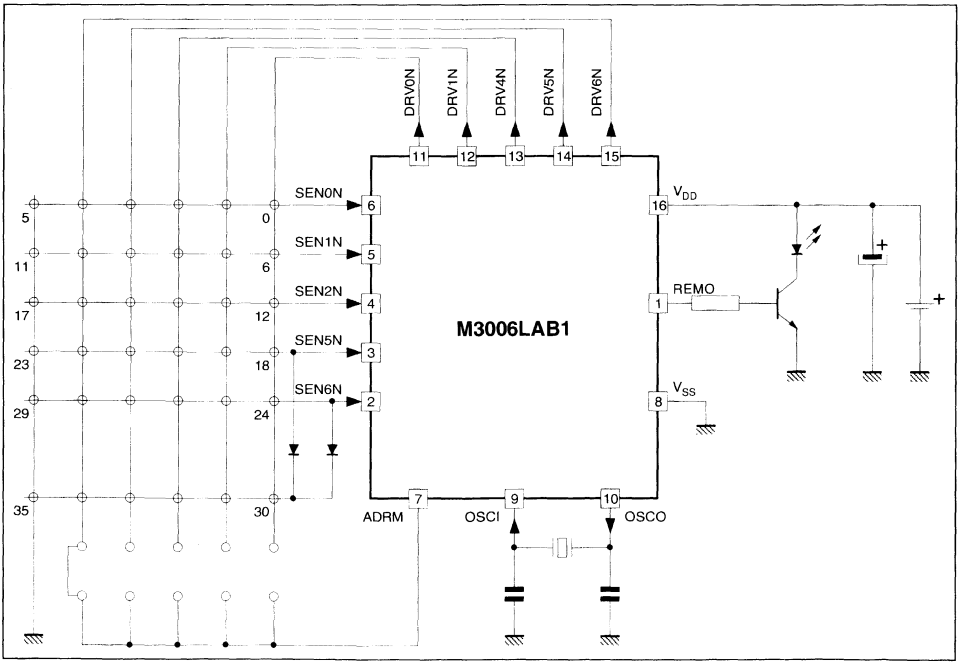
ELECTRICAL CHARACTERISTICS (continued)

V_{SS} = 0V, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CONTROL INPUT ADRM						
V_{IL}	Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Input Voltage High		0.7 x V_{DD}			V
I_{IL}	Input Current Low (switched P and N channel pull-up/pull down)	Pull-up Act. Oper. Condition, V_{IN} = V_{SS} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
I_{IH}	Input Current High (switched P and N channel pull-up/pull down)	Pull-down Act. Stand-by Cond., V_{IN} = V_{DD} V_{DD} = 2V V_{DD} = 6.5V	 10 100		 100 600	 µA µA
DATA OUTPUT REMO						
V_{OH}	Output Voltage High	V_{DD} = 2V, -I_{OH} = 60mA V_{DD} = 6.5V, -I_{OH} = 60mA	0.8 5.0			V V
V_{OL}	Output Voltage Low	V_{DD} = 2V, I_{OL} = 0.3mA V_{DD} = 6.5V, I_{OL} = 0.3mA			0.4 0.4	V V
t_{OH}	Pulse Length	V_{DD} = 6.5V, Oscill. Stopped			1	mS
OSCILLATOR						
I_I	Input Current	V_{DD} = V, OSC1 at V_{DD} V_{DD} = 6.5V, OSC1 at V_{DD}	 5.0		5.0 7.0	µA µA
V_{OH}	Output Voltage high	V_{DD} = 6.5V, - I_{OL} = 0.1mA	V_{DD} - 0.8			V
V_{OL}	Output Voltage Low	V_{DD} = 6.5V, I_{OH} = 0.1mA			0.7	V

3006L-08.TBL

Figure 1 : Typical Application



3006L-03.EPS

Figure 2 : Data Format of REMO Output; REF = Reference Time; T0 and T1 = Toggle bits; S0, S1 and S2 = System address; A, B, C, D, E and F = Command bits.
(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)
(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated)

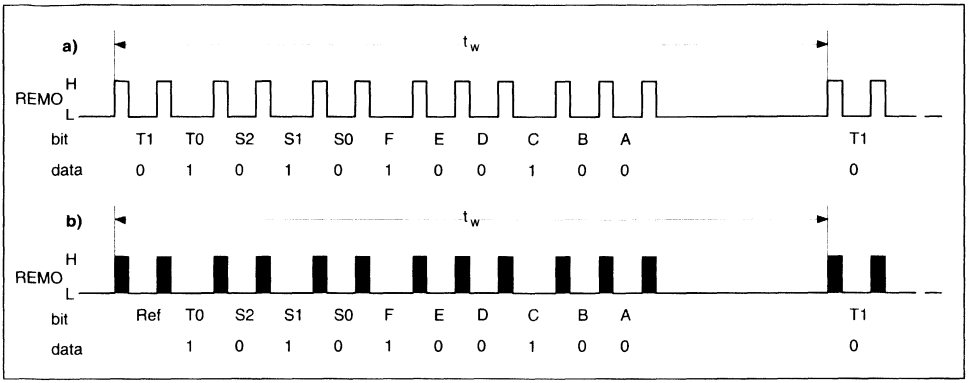


Figure 3 : REMO Output Waveform
(a) flashed pulse
(b) modulated pulse { $t_{PW} = (5 \times t_M) + t_{MH}$)}

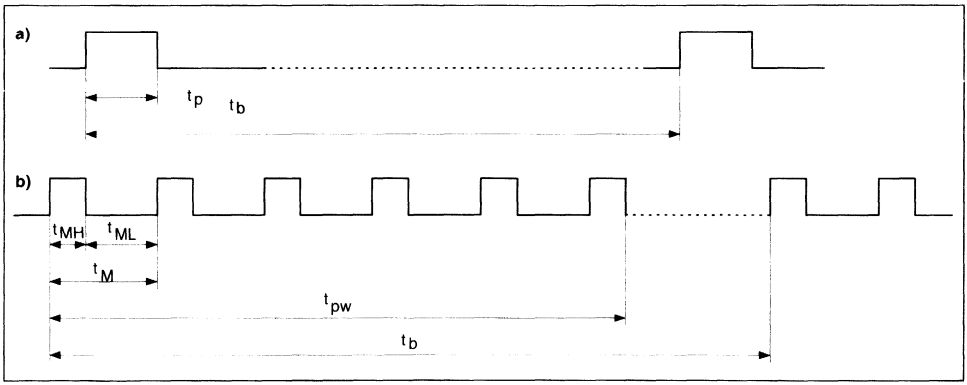


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O

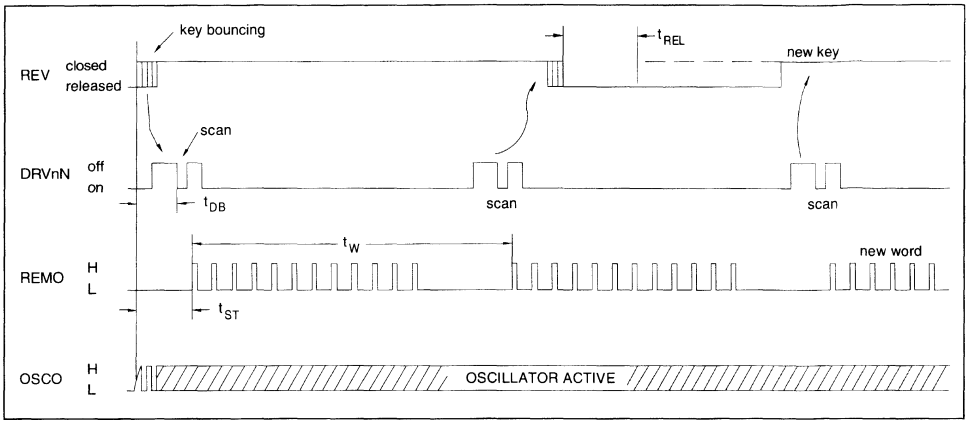
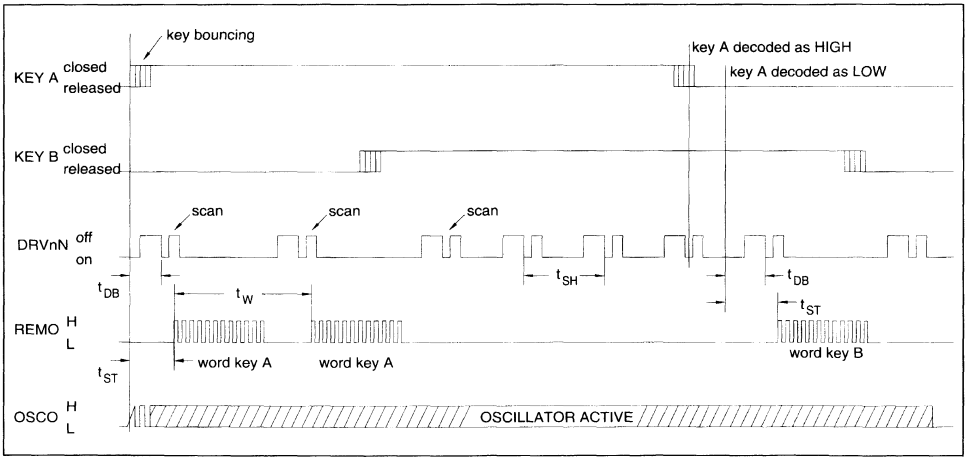


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O

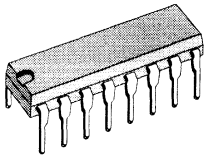


SGS-THOMSON MICROELECTRONICS

M145026
M145027 - M145028

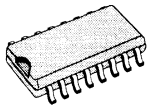
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS WIRE LESS TELEPHONES



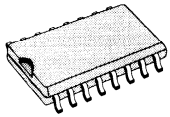
DIP16 (0.25")
(Plastic package)

ORDER CODES :
M145026B1
M145027B1
M145028 B1



SO16 Narrow (0.15")
(Plastic package)

ORDER CODE : M145026D



SO16 Large (0.3")
(Plastic package)

ORDER CODE : M145028D

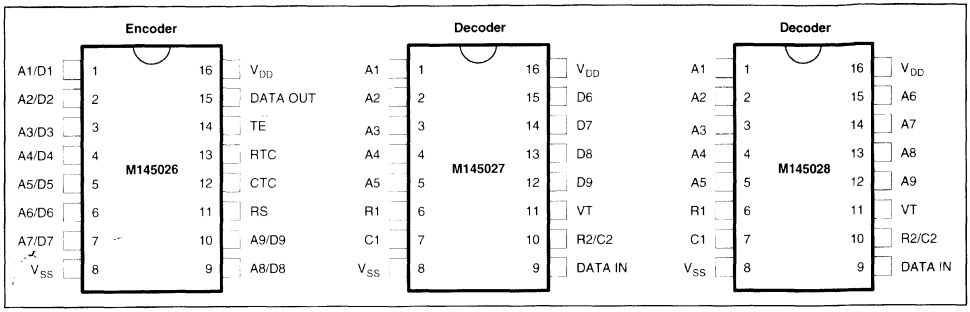
DESCRIPTION

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0,1, open) to allow 3^9 (19.683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145027 interprets the first five transmitted bits as address and the last four bits as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

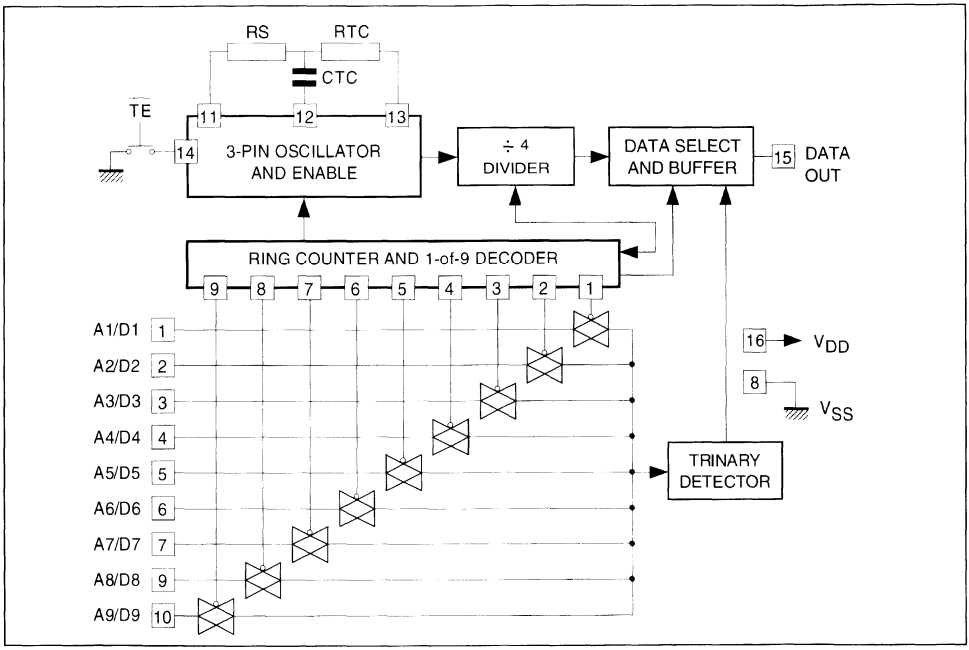
All the devices are available in 16 lead plastic package. The M145026 is available in SO16 plastic package (narrow) and the M145028 is available in SO16 plastic package (large).

PIN CONNECTIONS



BLOCK DIAGRAMS

Figure 1 : Encoder M145026



BLOCK DIAGRAMS (continued)

Figure 2 : Decoder M145027

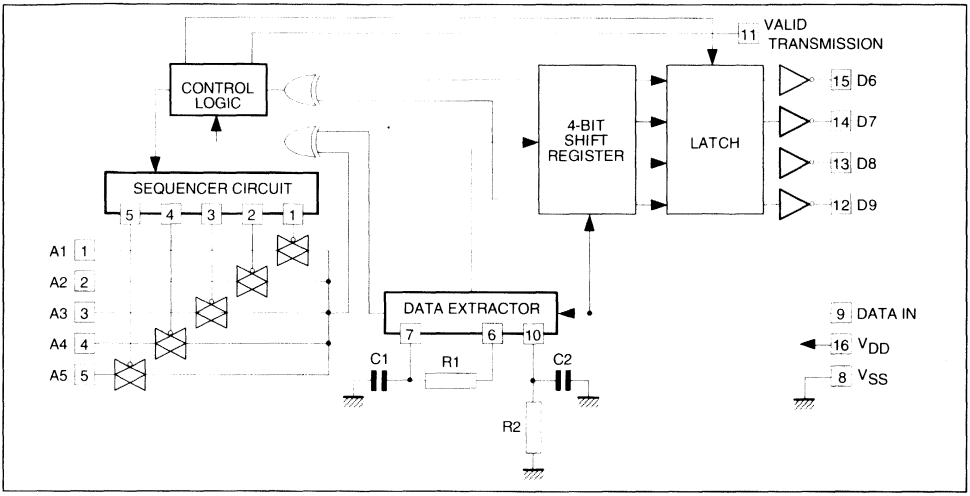
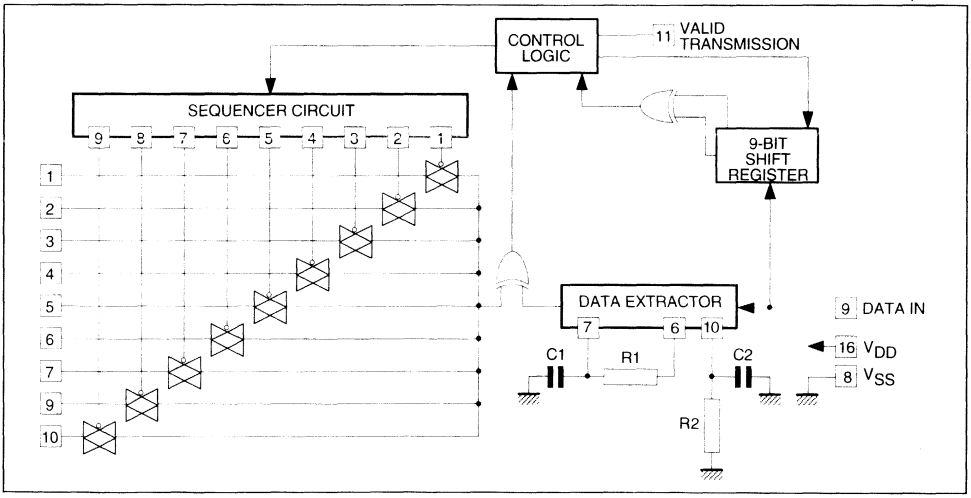


Figure 3 : Decoder M145028



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 18	V
V_I	Input Voltage, All Inputs	− 0.5 to V_{DD} + 0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	− 65, + 150	°C
T_{op}	Operating Temperature Range	− 40, + 85	°C

14502-01 TBL

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at thses or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS (C_L = 50pF, T_{amb} = 25°C)

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15		100 50 40	200 100 80	ns ns ns
t_{TLH} t_{THL}	Data in Rise and Fall Time (M145027 - M145028)	5 10 15			15 15 15	ms ms ms
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0		2 5 5	MHz MHz MHz
t_{WL}	Maximum Decoder Frequency (referenced to encoder clock) (see Figure 9)	5 10 15			240 410 450	kHz kHz kHz
	$\overline{TE}$ Pulse Width	5 10 15	65 30 20			ns ns ns
	System Propagation Delay ($\overline{TE}$ to valid transmission)			182		Clock Cycles
	Tolerance on Timing Components $\Delta RTC + \Delta CTC + \Delta R1 + \Delta C1$ $\Delta R2 + \Delta C2$				±25 ±25	% %

14502-02.TBL

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{DD} (V)	-40°C		25°C			+85°C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Level Voltage (V_I = V_{DD} or 0, "0" Level)	5 10 15		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH}	Output High Level Voltage (V_I = V_{DD} or 0, "1" Level)	5 10 15	4.95 9.95 14.95		4.95 9.95 14.95			4.95 9.95 14.95		V V V
V_{IL}	Input Low Level Voltage ("0" Level) V_O = 4.5 or 0.5V V_O = 0.9 or 1V V_O = 13.5 or 1.5V	 5 10 15		 1.5 3 4		 2.25 4.50 6.25	 1.5 3 4		 1.5 3 4	 V V V
V_{IH}	Input High Level Voltage ("1" Level) V_O = 4.5 or 0.5V V_O = 0.9 or 1V V_O = 13.5 or 1.5V	 5 10 15	 3.5 7 11		 3.5 7 11	 2.75 5.50 8.25		 3.5 7 11		 V V V
I_{OH}	Output Drive Source Current V_{OH} = 2.5V V_{OH} = 4.6V V_{OH} = 9.5V V_{OH} = 13.5V	 5 5 10 15	 -2.5 -0.52 -1.3 -3.6		 -2.1 -0.44 -1.1 -3	 -4.2 -0.88 -2.25 -8.8		 -1.7 -0.36 -0.9 -2.4		 mA mA mA mA
I_{OL}	Output Drive Sink Current V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V	 5 10 15	 0.52 1.3 3.6		 0.44 1.1 3	 0.88 2.25 8.8		 0.36 0.9 2.4		 mA mA mA
I_I	Input Current TE (M145026, pull up devide)	5 10 15			3 16 35	4 20 45	7 26 55			µA µA µA
I_I	Input Current RS (M145026) Data In (M145027 - M145028)	15		±0.3		±0.00001	±0.3		±1.0	µA
I_I	Input Current A1/D1-A9/D9 (M145026) A1-A5 (M145027) A1-A9 (M145028)	 5 10 15				 ±55 ±300 ±650	 ±80 ±340 ±725			 µA µA µA
C_I	Input Capacitance (V_I = 0)					5	7.5			pF

14502-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	V_{DD} (V)	-40°C		25°C			+85°C		Unit
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
C_I	Input Capacitance (V_I = 0)					5	7.5			pF
I_{DD}	Quiescent Current (M145026)	5				0.0050	0.10			µA
		10				0.0100	0.20			µA
		15				0.0150	0.30			µA
I_{DD}	Quiescent Current (M145027 - M145028)	5				30	50			µA
		10				60	100			µA
		15				90	150			µA
I_T	Total Supply Current (f_{CL} = 20kHz) (M145026)	5				100	200			µA
		10				200	400			µA
		15				300	600			µA
I_T	Total Supply Current (f_{CL} = 20kHz) (M145027 - M145028)	5				200	400			µA
		10				400	800			µA
		15				600	1200			µA

14502-04.TBL

OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0,1, open) allowing 3^9 = 19683 possible codes.The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).

Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.

The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. if this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.

Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.

Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only 2 x 3^8 = 13.122 different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the trans-

mitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words fo error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figures 7 and 8.

PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9. These inputs will be encoded and the data serially output form the encoder.

V_{SS}. The most negative supply (usually ground).

RS, CTC, RTC. These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$. This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

DATA OUT. This is the output of the encoder that will present the serially encoded signals.

V_{DD}. The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028). These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9 in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027). These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.

Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1. These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2. This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words. R2C2 = 77 x RTC x CTC.

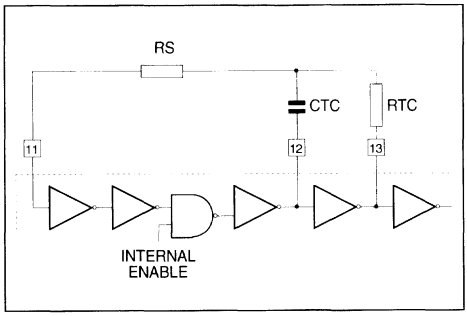
VALID TRANSMISSION, VT. This output will go high when the following conditions are satisfied:

1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}. The most positive supply.
V_{SS}. The most negative supply (usually ground).

Figure 4 : Encoder Oscillator Information



This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \approx \frac{1}{2.3 \cdot RTC \cdot CTC} \text{ (Hz) for 1 kHz} \leq f \leq 400 \text{ kHz}$$

where: CTC = CTC + C layout + 12 pF
RS ≈ 2 RTC
RS ≥ 20 k
RTC ≥ 10 k
400pF < CTC < µF

The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC.For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1Hz to over 1MHz.

Figure 5 : Encoder/Decoder Timing Diagram

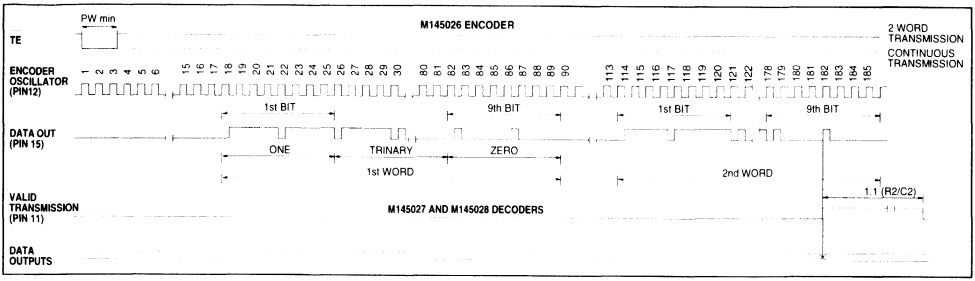
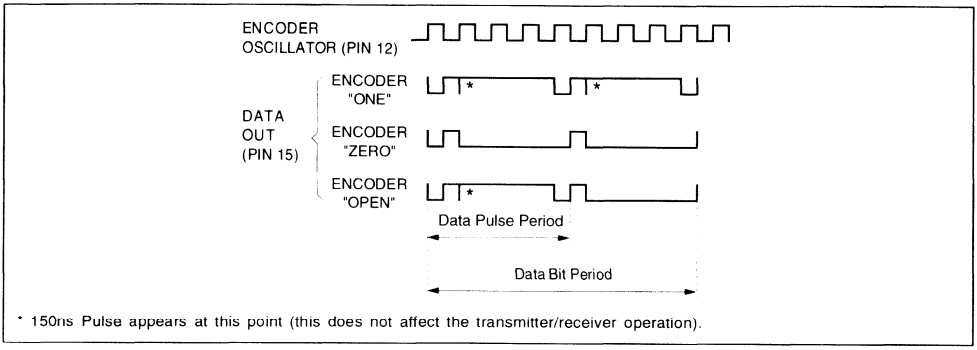


Figure 6 : Encoder Data Waveforms (M145026)



* 150ns Pulse appears at this point (this does not affect the transmitter/receiver operation).

Figure 7 : M145027 Flowchart

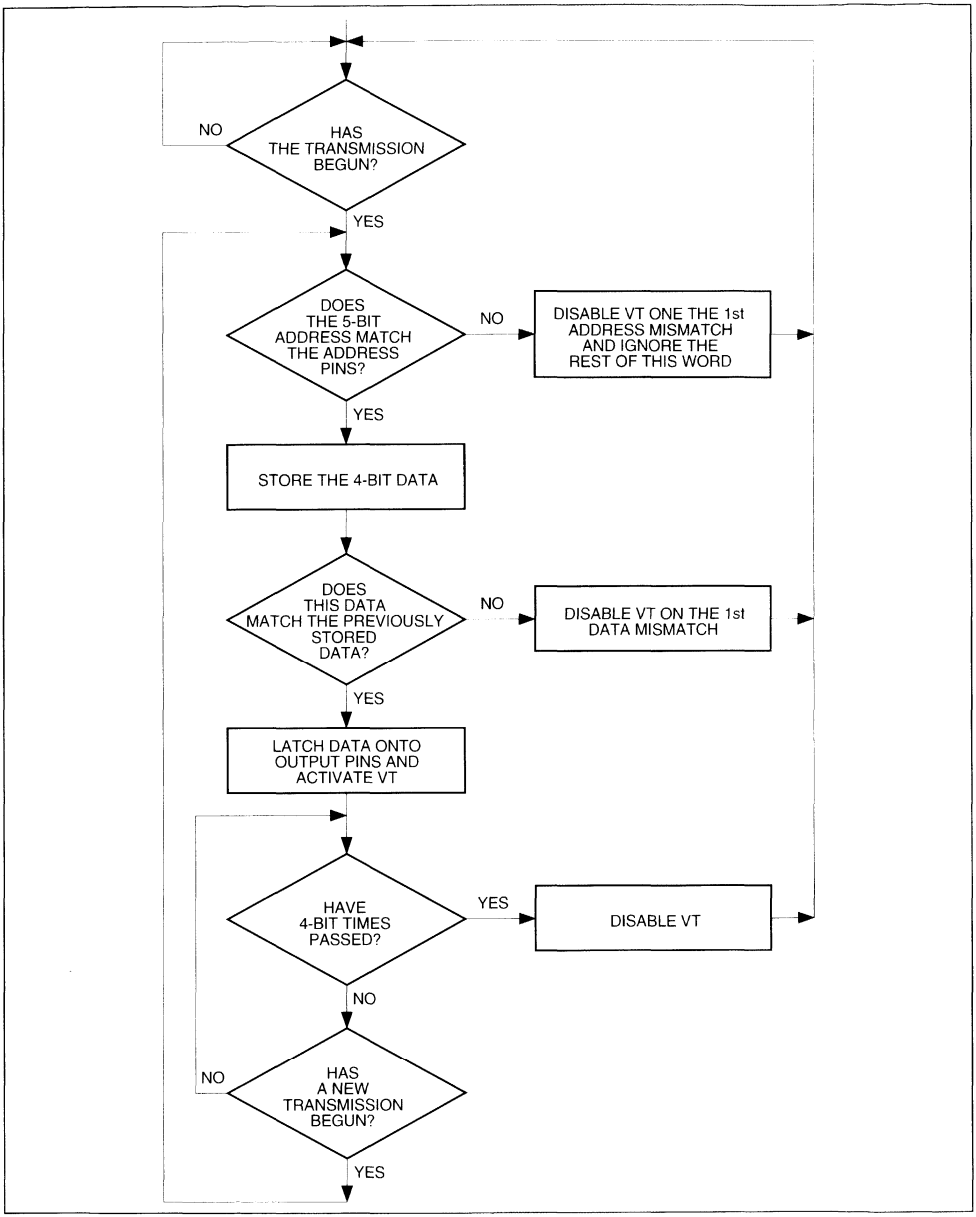


Figure 8 : M145028 Flowchart

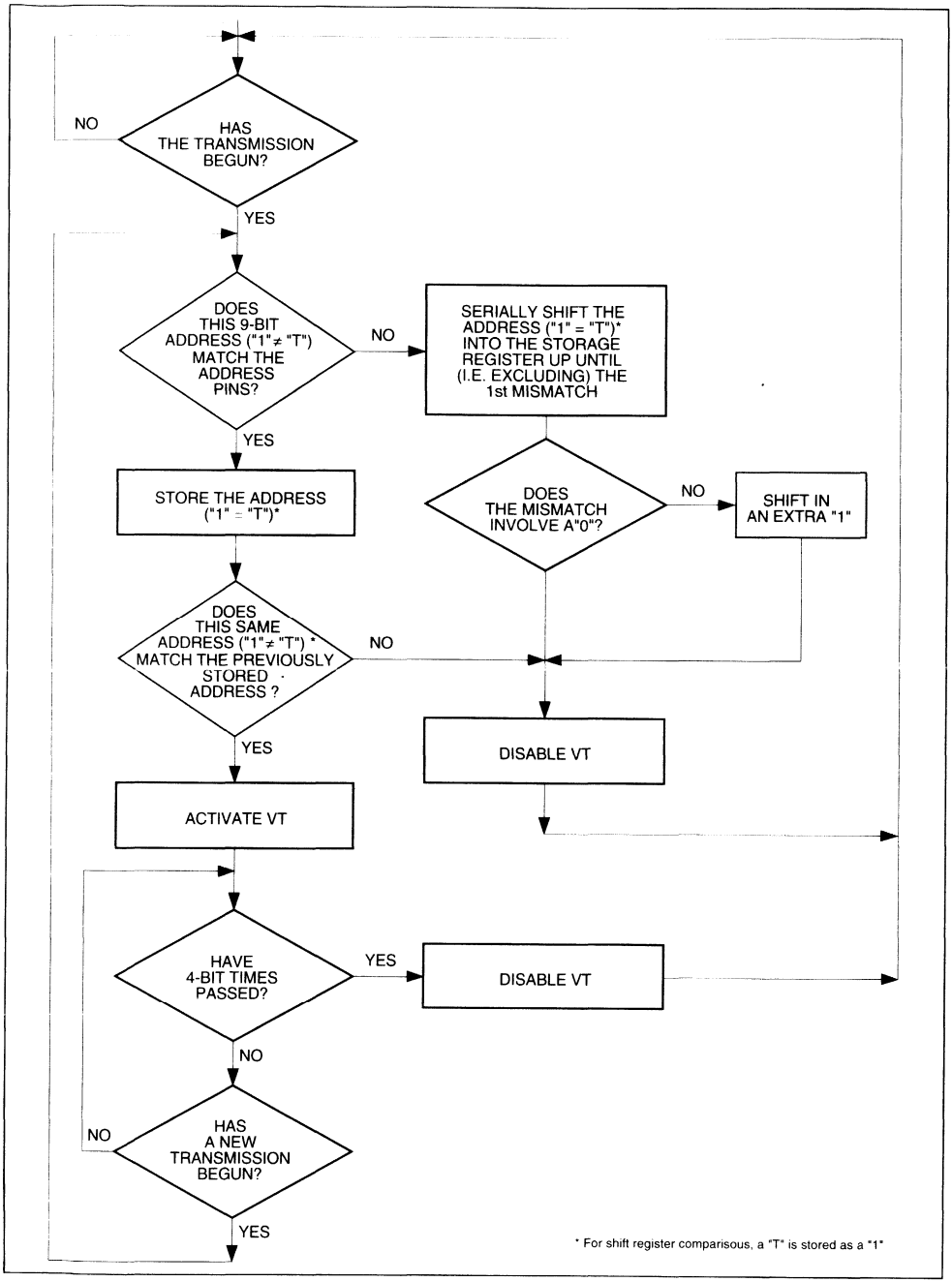


Figure 9 : M145027/M145028 (f_{max} vs. C_{layout})

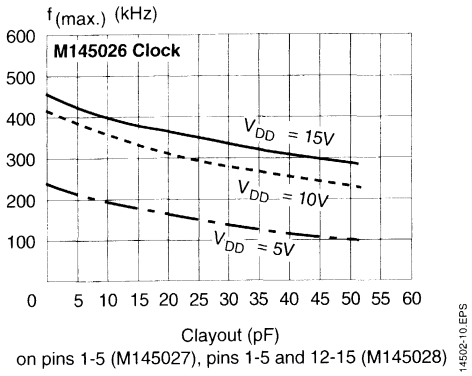
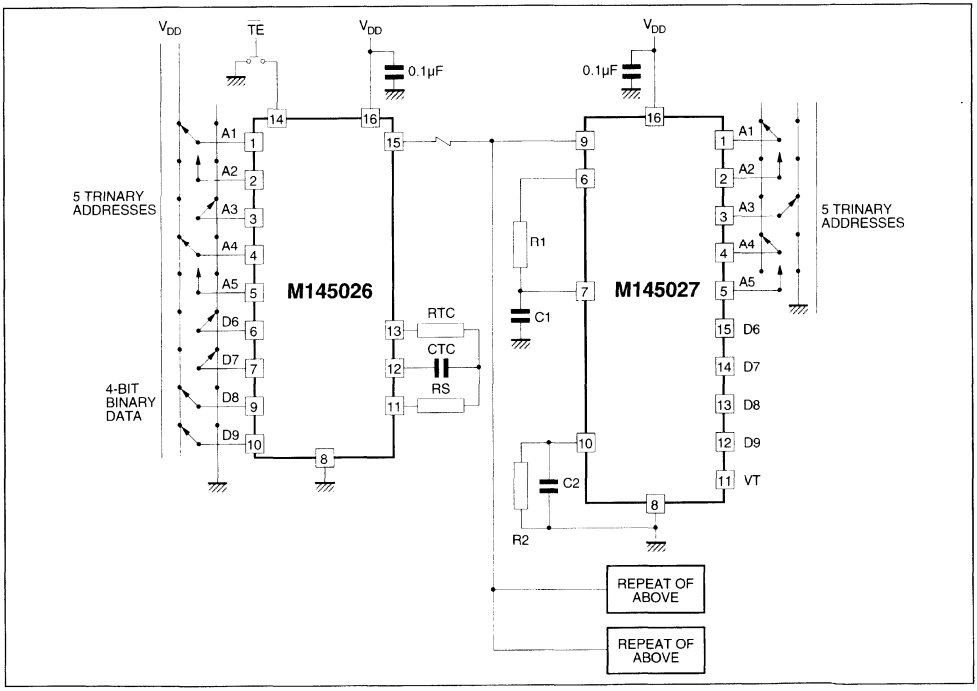


Figure 10 : Typical Application



Example R/C Values (all resistors and capacitors are ± 5 %) (CTC' = CTC + 20pF)

f_{OSC} (kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10k	120pF	20k	10k	470pF	100k	910pF
181	10k	240pF	20k	10k	910pF	100k	1800pF
88.7	10k	490pF	20k	10k	2000pF	100k	3900pF
42.6	10k	1020pF	20k	10k	3900pF	100k	7500pF
21.5	10k	2020pF	20k	10k	8200pF	100k	0.015µF
8.53	10k	5100pF	20k	10k	0.02µF	200k	0.02µF
1.71	50k	5100pF	100k	50k	0.02µF	200k	0.1µF

14502-05.TBL

AUDIO POWER AMPLIFIERS

SGS-THOMSON MICROELECTRONICS

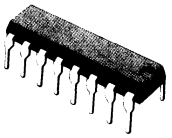
TDA1904

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

4W AUDIO AMPLIFIER

- HIGH OUTPUT CURRENT CAPABILITY (UP TO 2A)
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- SUPPLY VOLTAGE RANGE: 4V TO 20V

The TDA 1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in wide range of applications in portable radio and TV sets.



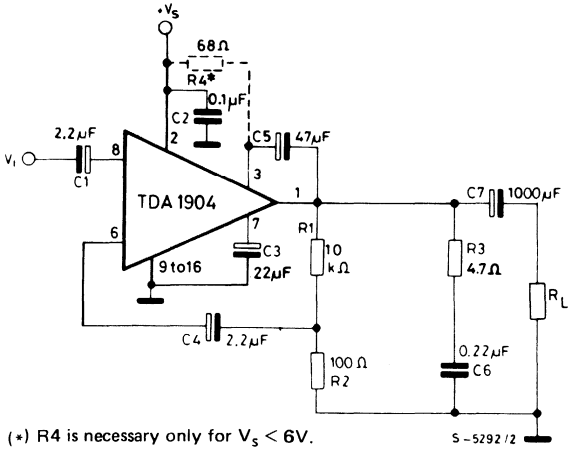
Powerdip
(8 + 8)

ORDERING NUMBER: TDA 1904

ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
I_O	Peak output current (non repetitive)	2.5	A
I_O	Peak output current (repetitive	2	A
P_{tot}	Total power dissipation at $T_{amb} = 80°C$	1	W
	at $T_{pins} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUIT



(*) R4 is necessary only for $V_S < 6V$.

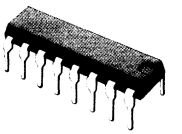
5W AUDIO AMPLIFIER WITH MUTING

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

The TDA1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).



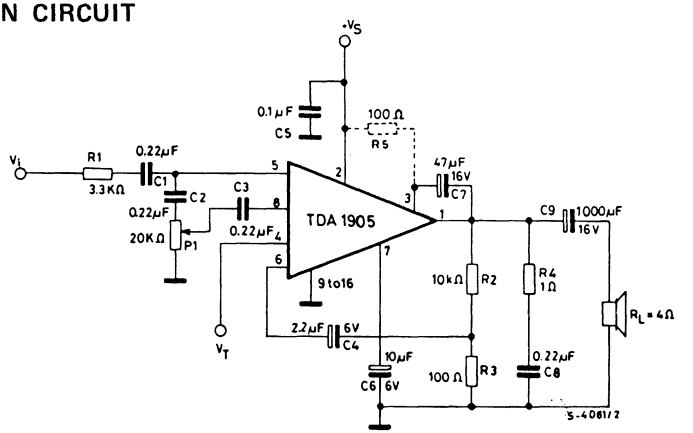
Powerdip
(8 + 8)

ORDERING NUMBER: TDA1905

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3	A
I_o	Output peak current (repetitive)	2.5	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{amb} = 80°C	1	W
	T_{case} = 60°C	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

APPLICATION CIRCUIT



12W AUDIO AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.

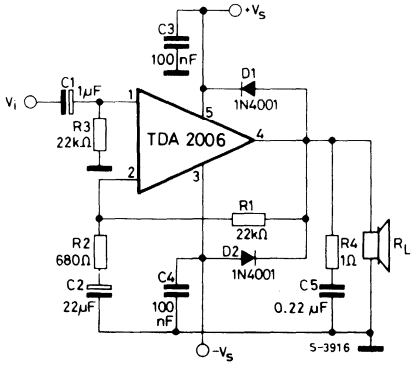
Pentawatt

ORDER CODE: TDA2006H
TDA2006V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 12	V
I_o	Output peak current (internally limited)	3	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUIT



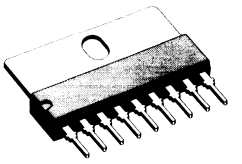
SGS-THOMSON MICROELECTRONICS

TDA2007A

6 + 6W SHORT-CIRCUIT PROTECTED STEREO AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- HIGH OUTPUT POWER
- HIGH CURRENT CAPABILITY
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION



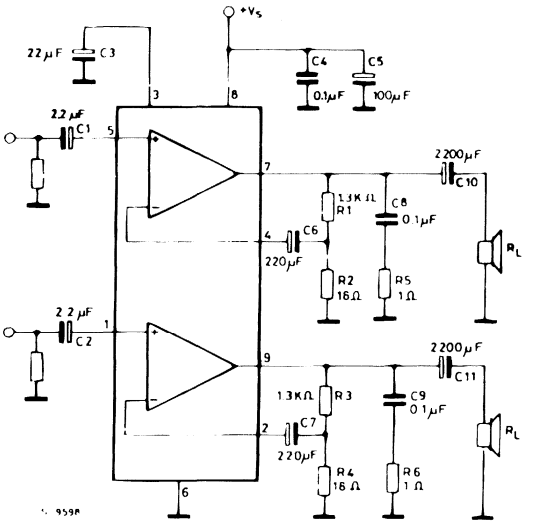
SIP. 9

ORDERING NUMBER : TDA2007A

DESCRIPTION

The TDA2007A is a class AB dual Audio power amplifier assembled in single in line 9 pins package, specially designed for stereo application in music centers TV receivers and portable radios.

STEREO TEST CIRCUIT



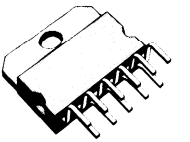
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

10+10W SHORT CIRCUIT PROTECTED STEREO AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

The TDA2009A is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 1%)
- High current capability (up to 3.5A)
- AC short circuit protection
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.



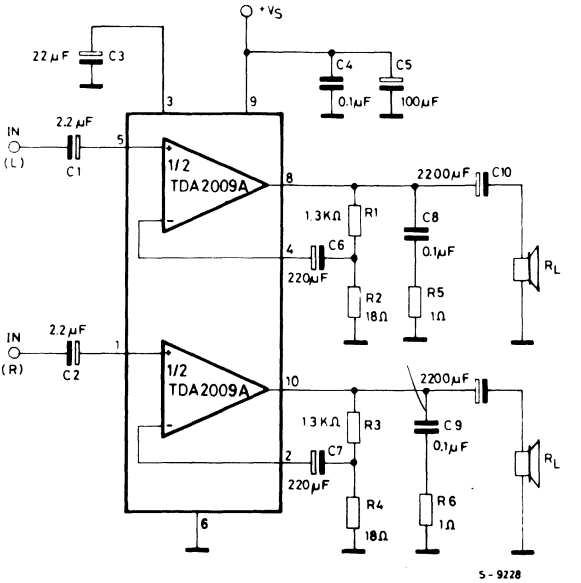
Multiwatt-11

ORDERING NUMBER: TDA2009A

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST CIRCUIT



14W Hi-Fi AUDIO AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

The TDA2030 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at 14V/4Ω; at ± 14V the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN45500). The TDA2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.

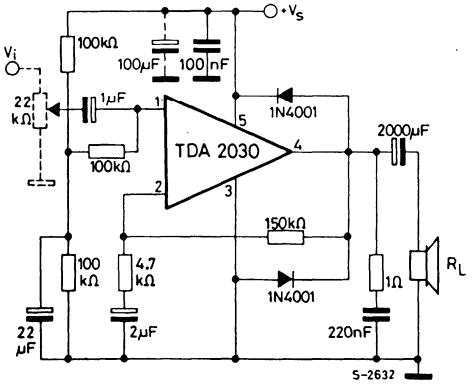
Pentawatt

ORDERING NUMBER: TDA2030H
TDA2030V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TYPICAL APPLICATION



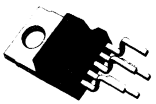
SGS-THOMSON MICROELECTRONICS

TDA2040

20W Hi-Fi AUDIO POWER AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

The TDA2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at $V_s = 32V/4\Omega$. The TDA2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.



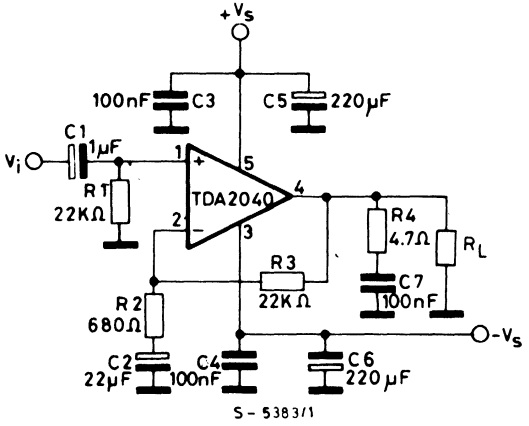
Pentawatt

ORDERING NUMBER: TDA2040V
TDA2040H

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	4	A
P_{tot}	Power dissipation at $T_{case} = 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

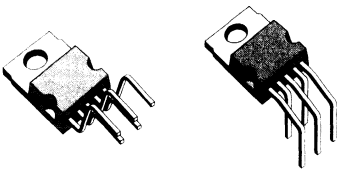
TEST CIRCUIT



32W Hi-Fi AUDIO POWER AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- HIGH OUTPUT POWER (50W MUSIC POWER IEC 268.3 RULES)
- HIGH OPERATING SUPPLY VOLTAGE (50V)
- SINGLE OR SPLIT SUPPLY OPERATIONS
- VERY LOW DISTORTION
- SHORT CIRCUIT PROTECTION (OUT TO GND)
- THERMAL SHUTDOWN



Pentawatt V **Pentawatt H**

ORDERING NUMBERS:
TDA2050V TDA2050H

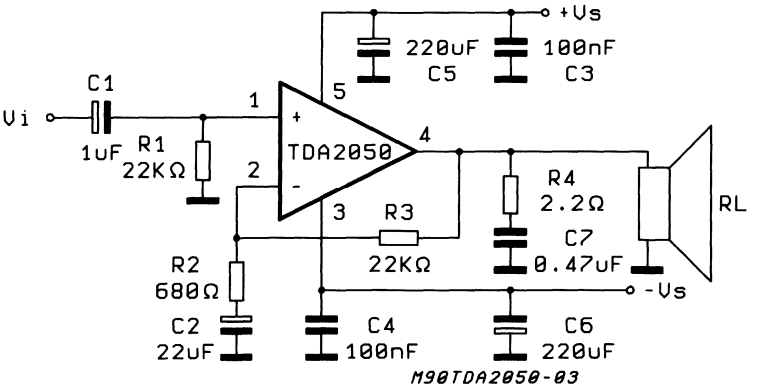
DESCRIPTION

The TDA 2050 is a monolithic integrated circuit in Pentawatt package, intended for use as an audio class AB audio amplifier. Thanks to its high power capability the TDA2050 is able to provide up to 35W true rms power into 4 ohm load @ THD = 10%, V_S = ±18V, f = 1KHz and up to 32W into 8ohm load @ THD = 10%, V_S = ±22V, f = 1KHz.

Moreover, the TDA 2050 delivers typically 50W music power into 4 ohm load over 1 sec at V_S= 22.5V, f = 1KHz.

The high power and very low harmonic and cross-over distortion (THD = 0.05% typ, @ V_S = ±22V, P_O = 0.1 to 15W, R_L=8ohm, f = 100Hz to 15KHz) make the device most suitable for both HiFi and high class TV sets.

TEST AND APPLICATION CIRCUIT



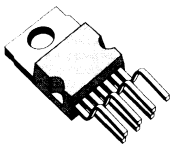
SGS-THOMSON MICROELECTRONICS

TDA2052

60W Hi-Fi AUDIO POWER AMPLIFIER WITH MUTE / STAND-BY

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- SUPPLY VOLTAGE RANGE UP TO ±25V
- SPLIT SUPPLY OPERATION
- HIGH OUTPUT POWER (UP TO 60W MUSIC POWER)
- LOW DISTORTION
- MUTE/STAND-BY FUNCTION
- NO SWITCH ON/OFF NOISE
- AC SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN



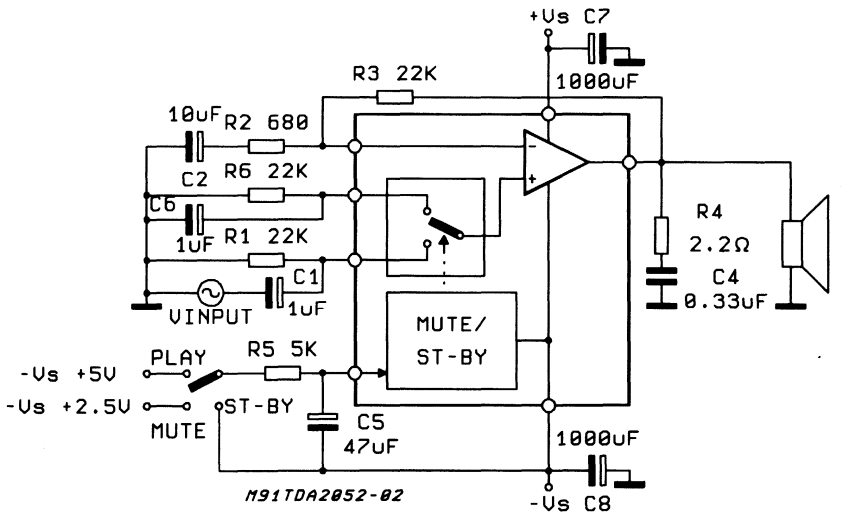
Heptawatt
ORDERING NUMBER: TDA2052

DESCRIPTION

The TDA2052 is a monolithic integrated circuit in Heptawatt package, intended for use as audio class AB amplifier in TV or Hi-Fi field application. Thanks to the wide voltage range and to the high out current capability it's able to supply the highest power into booth 4Ω and 8Ω loads even in presence of poor supply regulation.

The built in muting/Stand-by function simplifies the remote operations avoiding also switching on-off noises.

TEST AND APPLICATION CIRCUIT



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SGS-THOMSON MICROELECTRONICS

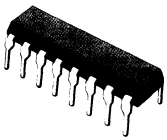
TDA2822

DUAL POWER AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- SUPPLY VOLTAGE DOWN TO 3V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA2822 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in portable radios and TV sets.



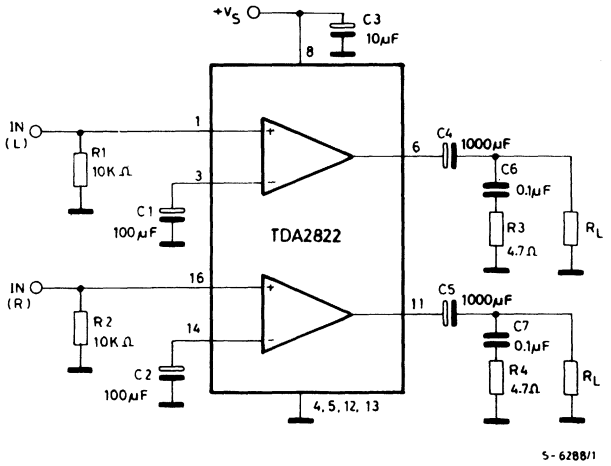
Powerdip Plastic (12+2+2)

ORDERING NUMBER: TDA2822

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	15	V
I_o	Output peak current	1.5	A
P_{tot}	Total power dissipation at T_{amb} = 50°C	1.25	W
	at T_{case} = 70°C	4	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TYPICAL APPLICATION CIRCUIT (STEREO)



SGS-THOMSON MICROELECTRONICS

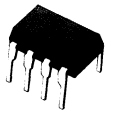
TDA7231/A

1.6W AUDIO AMPLIFIER

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- OPERATING VOLTAGE 1.8 TO 15V
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION
- SOFT CLIPPING

The TDA7231 is a monolithic integrated circuit in 4+4 lead minidip package. It is intended for use as class AB power amplifier with wide range of supply voltage in portable radios, cassette recorders and players, etc.



Powerdip (4 + 4)

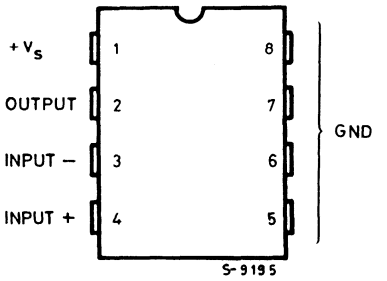
ORDERING NUMBER: TDA7231

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} = 50°C$	1.25	W
	at $T_{case} = 70°C$	4	W
I_o	Output peak current	1	A
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM

(Top view)

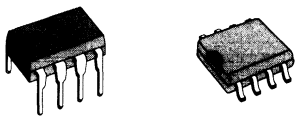


TDA7233
TDA7233D

1W AUDIO AMPLIFIER WITH MUTE

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION



Minidip **SO8**

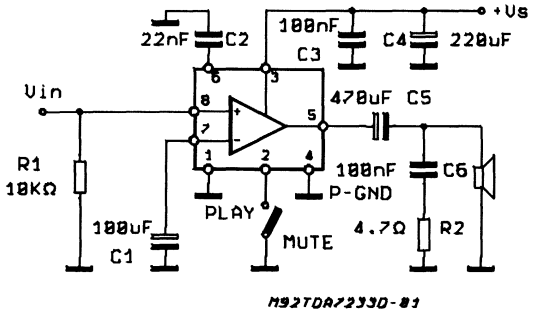
ORDERING NUMBERS:

TDA7233 TDA7233D

DESCRIPTION

The TDA7233/D is a monolithic integrated circuit in 8 pin Minidip or SO8 package, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable players, cordless telephones and Cellular Radios.

TEST AND APPLICATION CIRCUIT



M92TDA7233D-01

Note: Switch Open = Mute
Switch Closed = Play

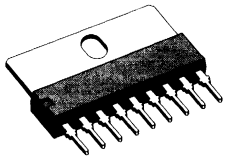
SGS-THOMSON MICROELECTRONICS

TDA7233S

1W AUDIO AMPLIFIER WITH MUTE

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- OPERATING VOLTAGE 1.8 TO 15V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION



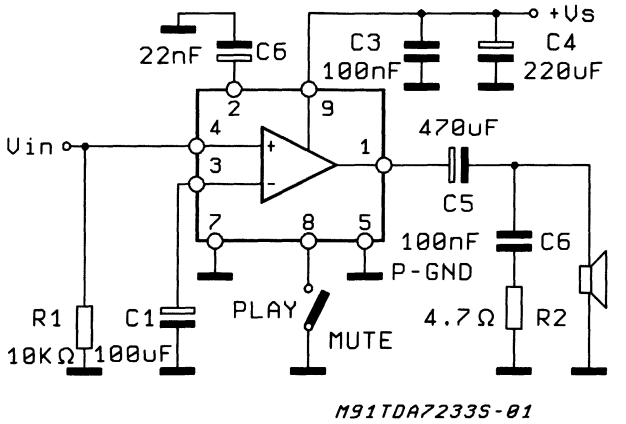
SIP9

ORDERING NUMBER: TDA7233S

DESCRIPTION

The TDA7233S is a monolithic integrated circuit in SIP 9, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable radios, cassette recorders and players.

TEST AND APPLICATION CIRCUIT



M91TDA7233S-01

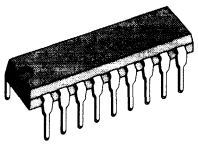
MUTE SWITCH	CONDITION
OPEN	MUTE
CLOSED	PLAY

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

5W AUDIO AMPLIFIER WITH MUTING AND STAND-BY

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- MUTING AND STAND-BY FUNCTIONS
- VOLTAGE RANGE UP TO 30V
- HIGH SUPPLY VOLTAGE REJECTION SVR TYP = 50dB (f = 100Hz)
- MUSIC POWER = 12W (R_L = 4Ω, d = 10%)
- PROTECTION AGAINST CHIP OVER TEMPERATURE



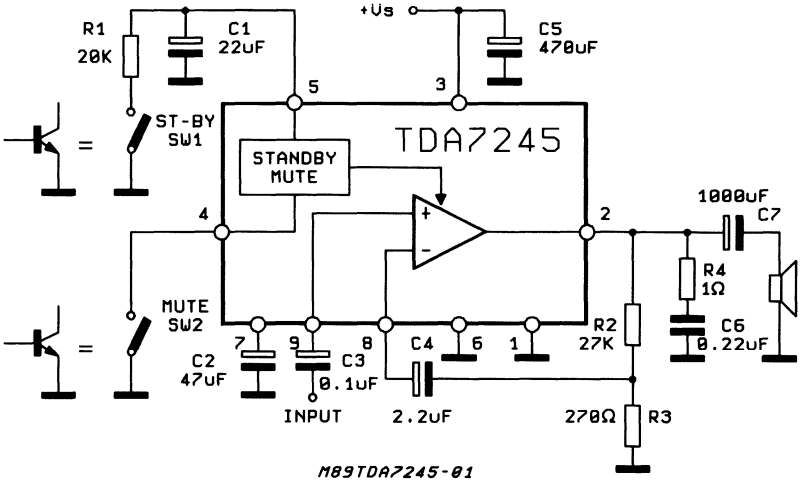
Powerdip 9+9

ORDERING NUMBER: TDA7245

DESCRIPTION

The TDA7245 is a monolithic integrated circuit in 9+9 POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.

Figure 1: Test and Application Circuit



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

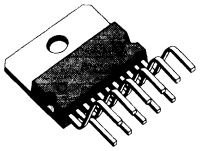
SGS-THOMSON MICROELECTRONICS

TDA7262

20+20W STEREO AMPLIFIER WITH STAND-BY

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- WIDE SUPPLY VOLTAGE RANGE
- HIGH OUTPUT POWER
  28+28W TYP. MUSIC POWER
  20+20W @ THD = 10%, R_L = 4Ω, V_S = 28V
- HIGH CURRENT CAPABILITY (UP TO 3.5A)
- STAND-BY FUNCTION
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

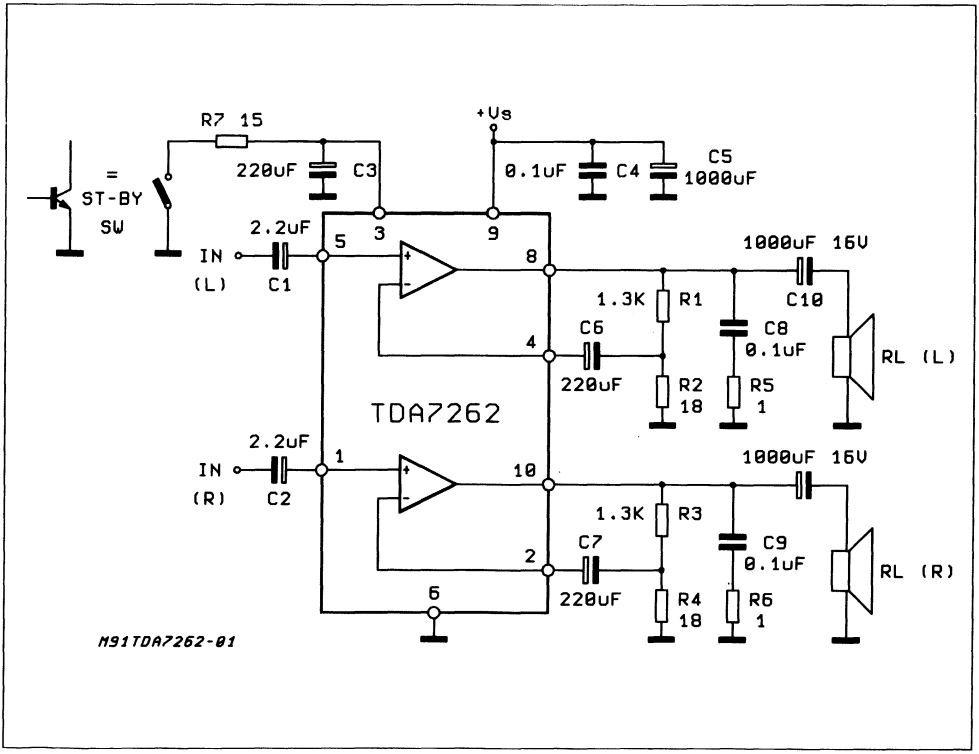


Multiwatt-11
ORDERING NUMBER: TDA7262

DESCRIPTION

The TDA7262 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt package, specially designed for high quality stereo application as Hi-Fi music centers and TV sets.

Figure 1: Stereo Application Circuit with Stand-By



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

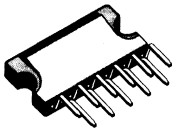
SGS-THOMSON MICROELECTRONICS

TDA7263

12 +12W STEREO AMPLIFIER WITH MUTING

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- WIDE SUPPLY VOLTAGE RANGE
- HIGH OUTPUT POWER
  12+12W @ V_S=28V, R_L = 8Ω, THD=10%
- MUTE FACILITY (POP FREE) WITH LOW CONSUMPTION
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION



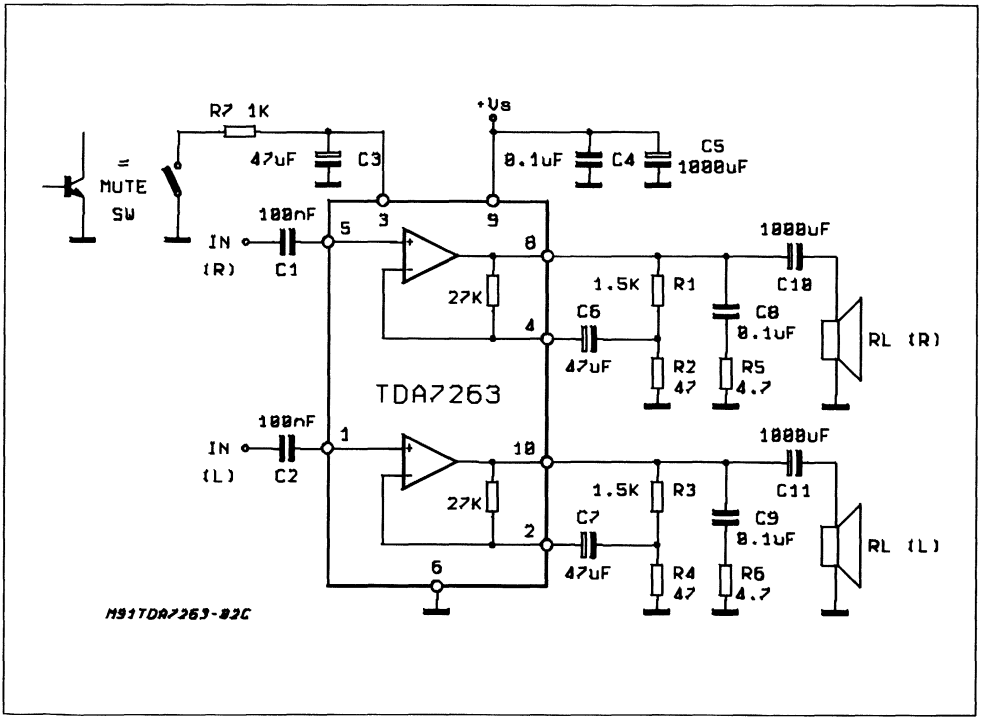
Clipwatt11

ORDERING NUMBER:TDA7263

DESCRIPTION

The TDA7263 is class AB dual audio power amplifier assembled in the new Clipwatt package, specially designed for high quality sound application as HI-FI music centers and stereo TV sets.

TEST AND APPLICATION CIRCUIT

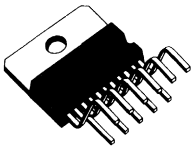


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

25 +25W STEREO AMPLIFIER WITH MUTE & ST-BY

For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

- WIDE SUPPLY VOLTAGE RANGE (UP TO ±25V ABS MAX.)
- SPLIT SUPPLY
- HIGH OUTPUT POWER
  25 + 25W @ THD =10%, R_L = 8Ω, V_S = ±20V
- NO POP AT TURN-ON/OFF
- MUTE (POP FREE)
- STAND-BY FEATURE (LOW I_q)
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION



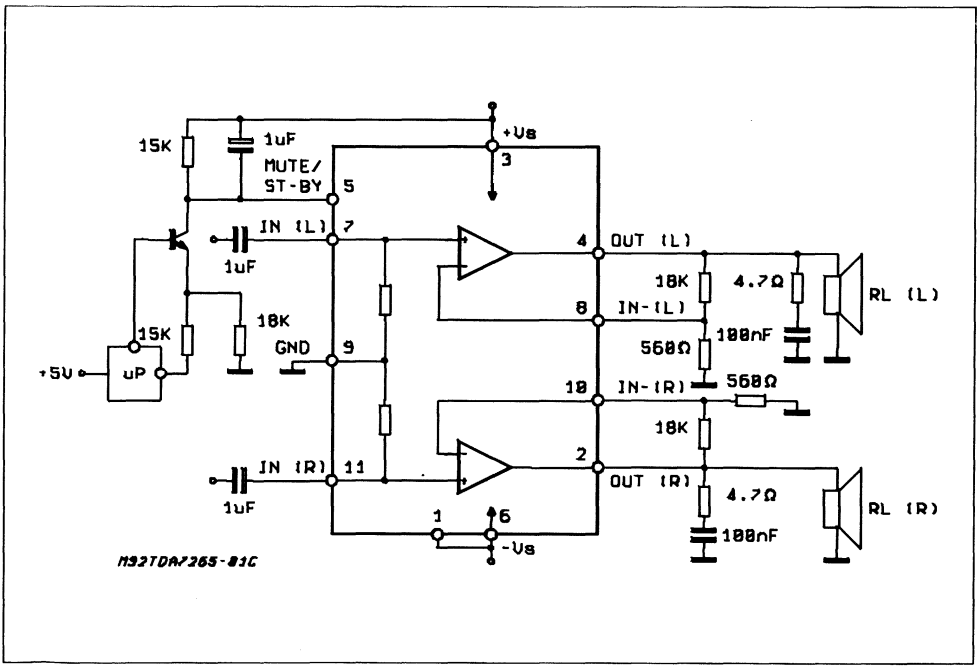
Multiwatt11

ORDERING NUMBER: TDA7265

DESCRIPTION

The TDA7265 is class AB dual Audio power amplifier assembled in the Multiwatt package, specially designed for high quality sound application as Hi-Fi music centers and stereo TV sets.

APPLICATION CIRCUIT (STEREO CONFIGURATION)

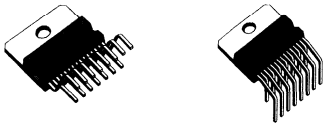


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

100V - 100W DMOS AUDIO AMPLIFIER WITH MUTE/ST-BY

- VERY HIGH OPERATING VOLTAGE RANGE (±40V)
- DMOS POWER STAGE
- HIGH OUTPUT POWER (UP TO 100W MUSIC POWER)
- MUTING/STAND-BY FUNCTIONS
- NO SWITCH ON/OFF NOISE
- NO BOUCHEROT CELLS
- VERY LOW DISTORTION
- VERY LOW NOISE
- SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



Multiwatt15V **Multiwatt15H**

ORDERING NUMBERS:

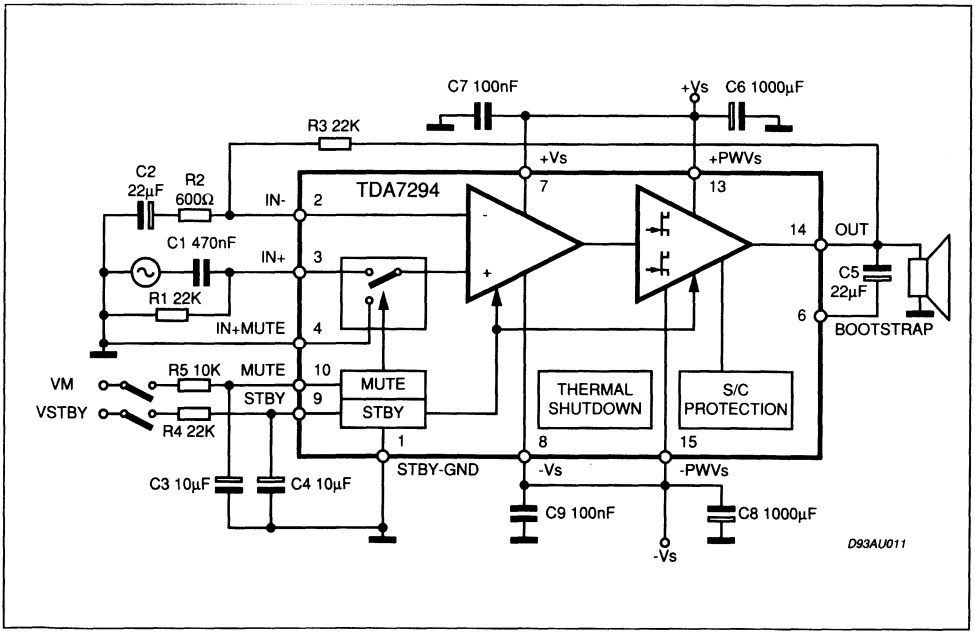
TDA7294V TDA7294H

DESCRIPTION

The TDA7294 is a monolithic integrated circuit in Multiwatt15 package, intended for use as audio class AB amplifier in Hi-Fi field applications (Home Stereo, self powered loudspeakers, Top-class TV). Thanks to the wide voltage range and to the high out current capability it is able to supply the highest power into both 4Ω and 8Ω loads even in presence of poor supply regulation, with high Supply Voltage Rejection.

The built in muting function with turn on delay simplifies the remote operation avoiding switching on-off noises.

Figure 1: Typical Application and Test Circuit



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

VIDEO RECORDER CIRCUITS

SGS-THOMSON MICROELECTRONICS

M8716B

CLOCK/CALENDAR WITH SERIAL I^2C BUS

- CLOCK/CALENDAR WITH SERIAL I^2C BUS
- 32kHZ QUARTZ TIMEBASE
- COUNTERS FOR SEC ; MIN ; HRS ; DAY ; MONTH OR SEC ; MIN ; HRS ; DAY OF WEEK
- EXTREMELY LOW POWER CONSUMPTION IN STANDBY OPERATION (Typ. 5µA)
- 8 PIN DIP PACKAGE
- INTEGRATED POWER FAIL DETECTION AND POWER-ON RESET
- PULSE OUTPUT FOR SECONDS
- CMOS PROCESS

DIP8
(Plastic Package)

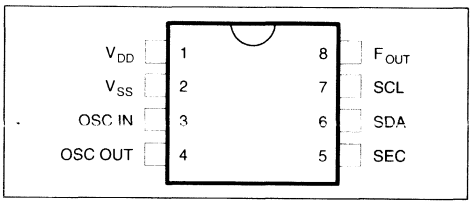
ORDER CODE : M8716AB1

DESCRIPTION

The integrated circuit M8716B contains a digital clock with a 32kHz quartz oscillator and a serial bus interface (I^2C Bus). The circuit is programmable to count seconds, minutes, hours, days and month or seconds, minutes, hours and day of the week.
This circuit is intended for use within a microcomputer system.

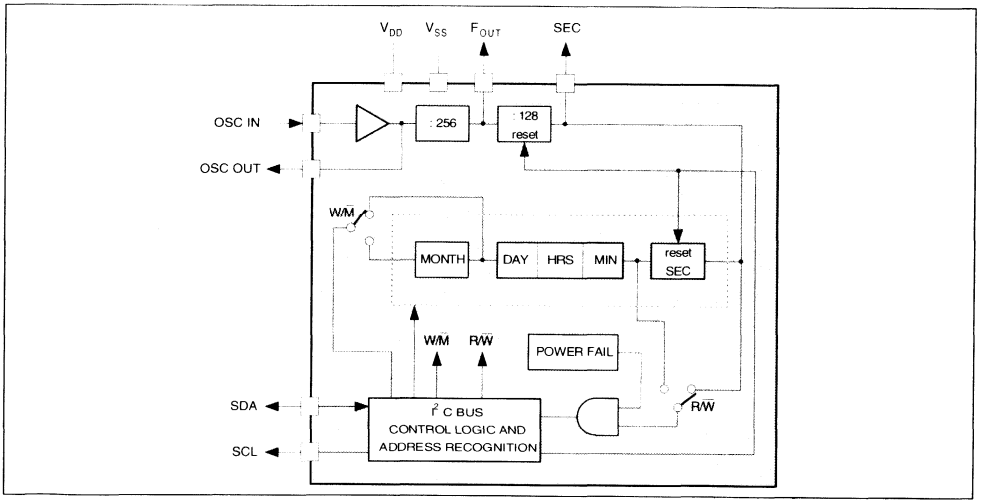
The M8716B is available in a 8 lead dual in-line plas-tic package.

PIN CONNECTIONS



8716B-01.EPS

BLOCK DIAGRAM



8716B-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}-V_{SS}	Supply Voltage	– 0.3 to + 10	V
V_I/V_O	Input Voltage, Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Total Package Power Dissipation	300	mW
T_{stg}	Storage Temperature	– 55, + 125	°C
T_A	Operating Temperature	0, + 70	°C

8716B-01 TBL

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C : V_{DD} = 5V ; F_{OSC} = 32.768kHz if not otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}	Supply Current				1	mA
V_{BAT}	Supply Voltage (standby operation)	No Data Transfer	2.0	2.4		V
I_{BAT}	Supply Current (standby operation)	Test Circuit, V_{BAT} = 2.4V		5	15	µA
I_{IN}	Input Current SDA ; SCL	V_{IN} = V_{DD} V_{IN} = V_{SS}			5 –5	µA µA
I_{OUT}	Output Current SDA	V_{OL} = 0.4V	4			mA
I_{OUT}	Output Current F_{OUT}, SEC	V_{OUT} = 1V V_{OUT} = 4V	0.1 -0.1			mA mA
C_{OUT}	Oscillator Output-capacitance		16	20	24	pF

8716B-02 TBL

GENERAL DESCRIPTION

The integrated circuit M8716B contains a digital clock counting seconds, minutes, hours, days and months or seconds, minutes, hours and days of the week as an option. A 32.768kHz quartz oscillator serves as time-base. This circuit is intended for use within a microcomputer system.

Writing (time setting) and reading of the counters is done via a serial interface (I^2C Bus). The microcomputer is used for controlling the data transfer and for generating the signals to drive a (7 segment) display. If a data transfer takes place between the M8716B and the microprocessor, a 5V supply voltage has to be provided. During standby the circuit is supplied by two NiCd-cells at a very low power consumption.

FUNCTIONAL DESCRIPTION

Dividers and Counters

The oscillator frequency of 32.768kHz is first divided by 256 and then again by 128. The resulting output frequency of 1Hz then serves as clock pulse for the time counters.

The content of the counters for sec, min, hr, day and month of sec, min, hr, and day of week can be read or modified (written) via the I^2C Bus interface. During a "write" cycle only the content of the counters starting from the minutes counter is modified : the seconds counter and the seconds divider block are reset to zero.

Selection between "calendar" operation (display of day and month) and "day of week" operation (display of day of week 1 to 7) is done as follows :

If the second bit in the first data byte is "1" during a "write" operation, the counters are set for the mode "day of week".

If this bit remains at "0" during a "write" operation the calendar mode is selected. In this case, carry of the "day" counter is performed automatically at positions 28, 30 or 31, depending on the month. In case of a leap year the day 29 (of February) can be set by a "write" operation.

In this case, carry takes place on 3-1 (March 1st).

I^2C Bus Interface General Description

Data transfer from the circuit M8716B to the microcomputer (reading) and vice versa (writing) takes place via the two lines SDA and SCL. Address and data are transmitted on SDA while at the same time clock pulses have to be provided on SCL for synchronization by the microcomputer.

I^2C Bus Interface Addressing (see Fig. 1, 2, 3)

A data transfer (reading or writing) is initiated by a start condition ("1" – > "0" transition on SDA while SCL remains at "1") and a subsequent address byte. By assigning a unique address to each circuit, several circuits may be connected to the I^2C Bus without interfering each other.

If the M8716B recognizes an address transmitted on the bus as its own address, the data transfer starts. The least significant bit of the address word controls the direction of data transfer (R/W-control). If it is set to "0", data is transferred from the microcomputer to the circuit, i.e. the content of the time counters is modified. If it is set to "1" the time information is read out by the microcomputer. A data transmission between the microprocessor and M8716B must always be completed otherwise the clock content may be lost. This means that the "master" can't use the possibility to stop the transmission after a certain byte by not sending the acknowledge bit.

Even 2f M8716B can work at the frequency four DC UP to 100kHz, it is tested at a frequency of 30kHz. If a carry of the time counter should take place during a data transfer, the carry will be stored and made after the data transfer. As only one carry can be stored, the whole data transfer must not take a time longer than one second.

Synchronization

For easy of synchronization with an external time reference in case of small deviations ($< \pm$ 30sec), only the address (with R/$\overline{W}$ = "0") has to be transmitted, followed immediately by a stop condition. No data is transmitted (see fig. 4). The second divider block (128Hz to 1Hz) and the seconds counter are reset. If the seconds counter was at position 30 ... 59, a carry to the minutes counter takes place in addition to the reset.

Figure 1 : Complete Timing for an Address/-read ; Resp. Address/-write Cycle

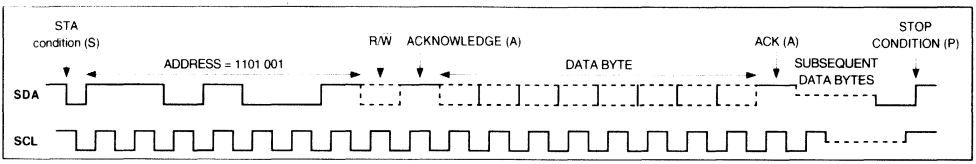


Figure 2a : Data Format for One Cycle Address/-read (with calendar)

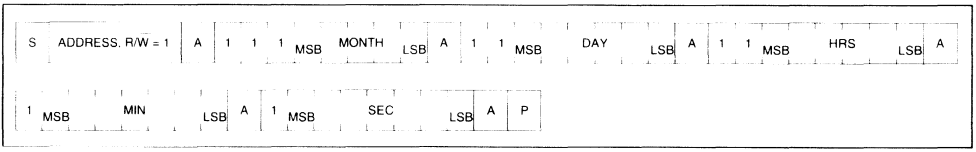


Figure 2b : Data Format for One Cycle Address/-write (with calendar)

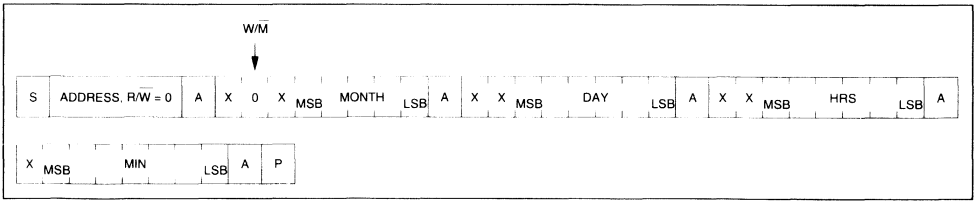


Figure 3a : Data Format for One Cycle Address/-read (with day of week indication)

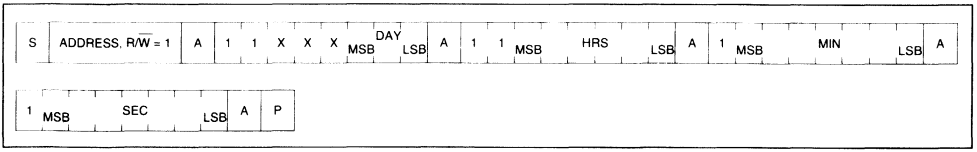
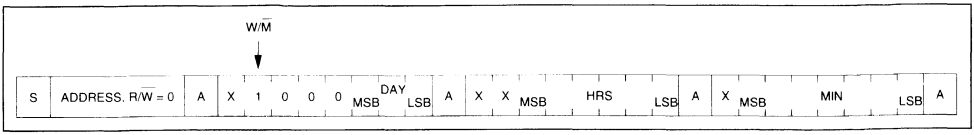
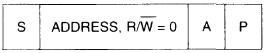


Figure 3b : Data Format for One Cycle Address/-write (with day of week indication)



8716B-07.EPS

Figure 4 : Data Format for Synchronization (deviation < 30sec)



8716B-08.EPS

Power Fail

In case of total power fail an internal register is set to "0". This register disables the data of the watch. So in a read cycle the µP recognizes "0" of the watch content. This is a unique situation appearing only in case of a power fail. The power fail register is automatically reset by the first "write" command.

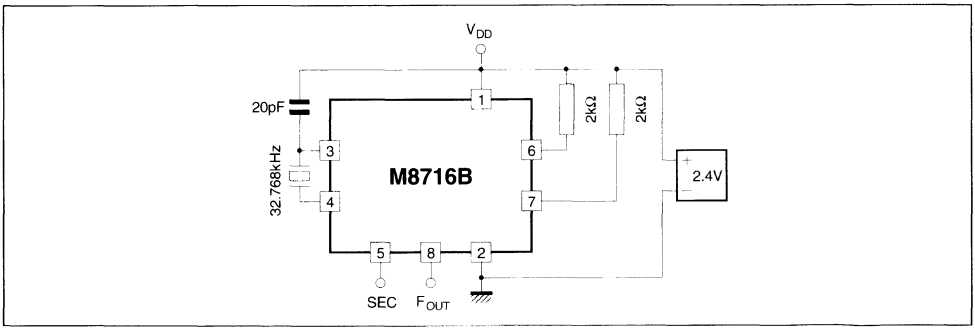
Pulse Outputs F_{OUT}, SEC

The output frequency of the first divider block (128Hz) is provided on the pin F_{OUT} and facilitates adjustment of the oscillator frequency without loading (and detuning) the oscillator.

The output SEC (1Hz) may be utilized for a blinking second indication.

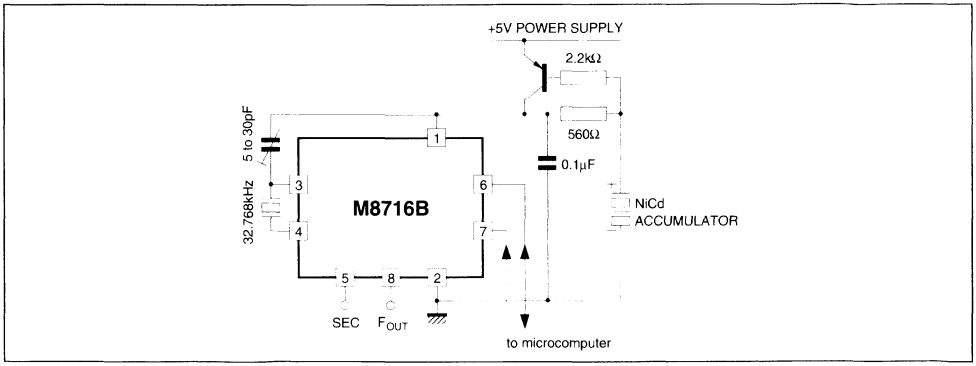
Both pins F_{OUT} and SEC can also be used as input during the functional test. A Low impedance (50 to 100Ω) external signal source which overrides the internal output buffer can drive the circuit at a frequency higher than the normal rate. This allows to reduce test time.

Figure 5 : Test Circuit



8716B-09.EPS

Figure 6 : Typical Application



8716B-10.EPS

SGS-THOMSON MICROELECTRONICS

STV5712

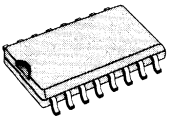
ADVANCED FM AUDIO PLAY-BACK AND RECORD AMPLIFIER FOR VCR

PLAY-BACK MODE

- LOW NOISE 68dB AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT
- MODE SELECTION BY LOGIC INPUT

RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- RECORD AMPLIFIER WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT
- 5V SUPPLY VOLTAGE



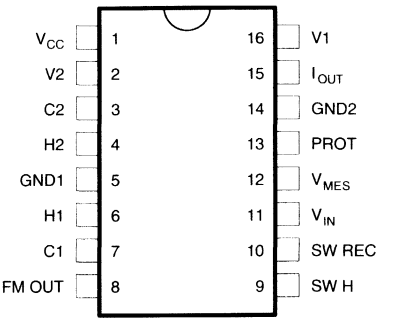
SO16J
(plastic micropackage)

ORDER CODE : STV5712

DESCRIPTION

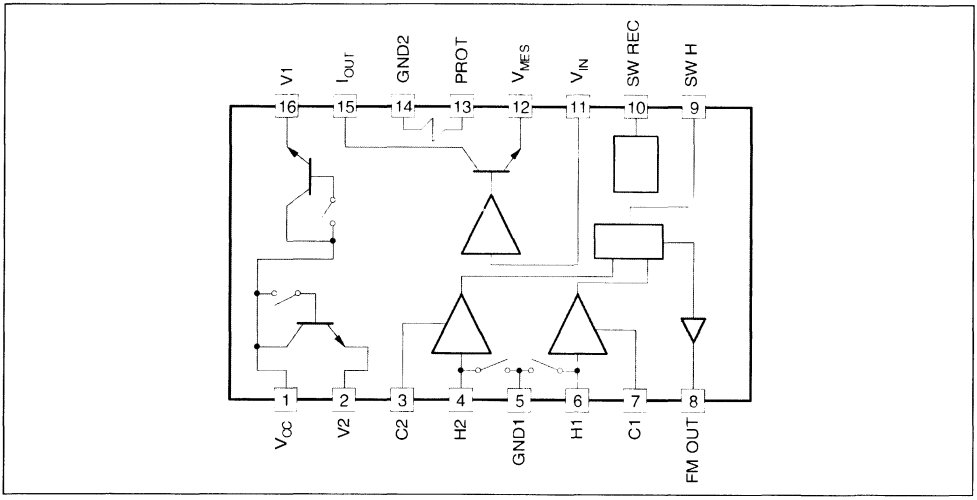
The STV5712 is an advanced two head FM audio record and play-back amplifier for VCR.

PIN CONNECTIONS



5712V-01.EPS

BLOCK DIAGRAM



5712V-02.EPS

FUNCTIONAL DESCRIPTION

STV5712 is intended for 2 heads FM audio VCR applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the STV5712 large capability to directly drive a coaxial cable in order to reduce number of external components.

Only one power supply is necessary for play-back and record modes. The mode can be chosen through a logic input. A special care has been taken to avoid current peaks through the rotary transformers.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two heads, the DC current and the AC characteristics can be very precisely controled with accurate external resistors. If recommended resistances are used, a ±5% transconductance accuracy is guaranted.

The recording amplifier includes a protection system which protects the IC and the application board against overheating in case of short circuit on the recording transconductance components.

STV5712 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
T_J	Junction Temperature	+ 150	°C

5712V-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Typ.	100	°C/W

5712V-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter	Play-Back		Record (1)	
	Typ.	Max.	Typ.	Max.
V_{CC} = 5V	25mA	35mA	60mA	80mA

5712V.03 TBL

Note : 1. R1 = 5.6Ω

Play-back Mode

V_{CC} = 5V, no load on Pin V_{OUT}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current			25	35	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
FM OUT						
G_{PB}	Pre-amplification Gain	Sinus wave 1.6MHz 400mV$_{PP}$ on output, Input on Pin H1 or H2	63	68	73	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin FM OUT between Channel 1 and Channel 2	Sinus wave 1.6MHz 0.1mV$_{PP}$ on inputs H1 or H2			1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1, H2		0.34	0.5	nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1, H2		3.6	5.0	pA/√Hz
CRT	Crosstalk	Sinus wave 1.6MHz 100µV$_{PP}$, All switches combinated		-45	-40	dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input Low High		 8	0.1	 MHz MHz
C_{IN}	Input Capacitance Pins H1, H2			45		pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2	At 1.6MHz		600		Ω
Z_{PB}	Output Impedance	DC		30	50	Ω
V_{DCPB}	DC Level at Pin FMOUT		1.8	2.4	3	V
ΔV_{DC}	Head Switch Offset				150	mV
SH_{PB1}	Second Harmonic	Sinus wave 1.6MHz 100µV$_{PP}$ on input 500Ω//100pF		-45	-40	dB

5712V.04 TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Record Mode

V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}

Transconductance network defined by : R1 = 5.6Ω 1% Pins PROT/V_{MES}
R2 = 1kΩ 1% Pins V_{MES}/V_{IN}
R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC2}	Current Supply	V_{CC} = 5V		60	80	mA
I_{OUT}						
I_{max}	Max. Record Current			70		mA_{PP}
I_{BIAS}	Biasing Current of the record amplifier		33	40	47	mA
TR	Transconductance	V_{IN} = 200mV_{PP}		220		mA/V
Z_{OUT}	Output Resistance		7	100		kΩ
SH_{REC}	Second Harmonic	Output Current 40mA_{PP} at 1.6MHz		-43	-38	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation Output current 60mA_{PP} Low High	 5	 	 0.1 	 MHz MHz
	Maximum Input Current on Pin PROT	5V on Pin PROT	150	250	400	mA
	Maximum Saturation Voltage on Pin PROT	Input current 50mA		100	150	mV
	Input Resistance	Equivalent value of R3 resistor	500	700	900	Ω

5712V-05.TBL

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH1}	Head Selection Pin SW	Head number 1 (high level)	2.4		V_{CC}	V
V_{SWL1}		Head number 2 (low level)	0		1.5	V
I_{SWH1}		Input current (high level)		20	50	µA
I_{SWL1}		Output current (low level)		20	50	µA
V_{SWH2}	Mode Selection Pin SW REC	Record mode (high level)	2.4		V_{CC}	V
V_{SWL2}		Play-back mode (low level)	0		1.5	V
I_{SWH2}		Input current (high level)		20	50	µA
I_{SWL2}		Output current (low level)		20	50	µA
t_{ON1}	Selection Pin SW Transient Response	Delay time selection ON (output signal appears on Pin FM OUT)		250	500	ns
t_{OFF1}		Delay time selection OFF (output signal disappears on Pin FM OUT)		250	500	ns
t_{ON2}	Selection Pin SW REC Transient Response	Delay time selection ON (output signal appears on Pin I_{OUT})		4	40	µs
t_{OFF2}		Delay time selection OFF (output signal appears on Pin FM OUT)		1.3	10	ms

5712V-06.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

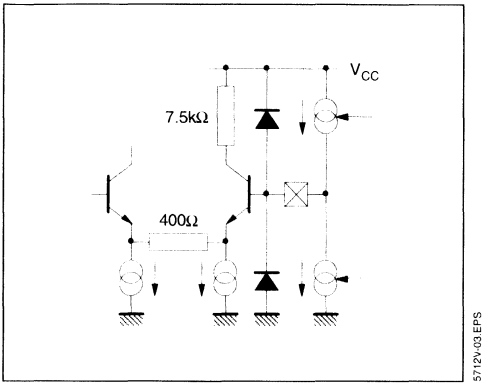
Power Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC} 75µV_{PP} on Pin H1, H2 Measurement on Pin FM OUT	15	20		dB

5712V-07.TBL

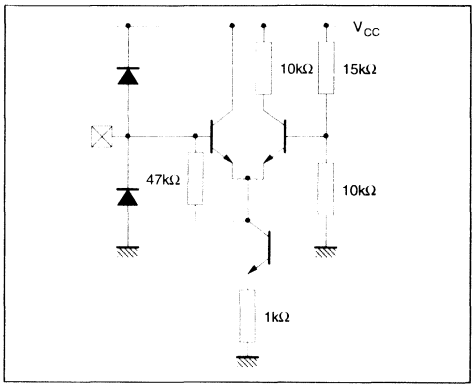
INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1, C2



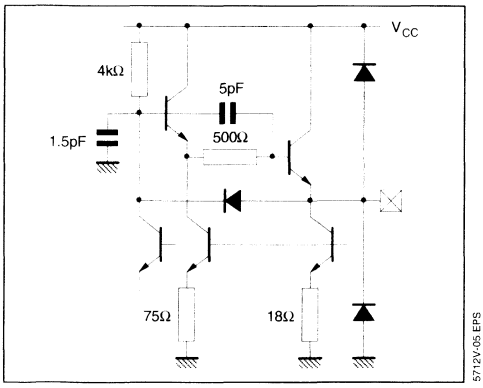
5712V-03.EPS

Pin : SW



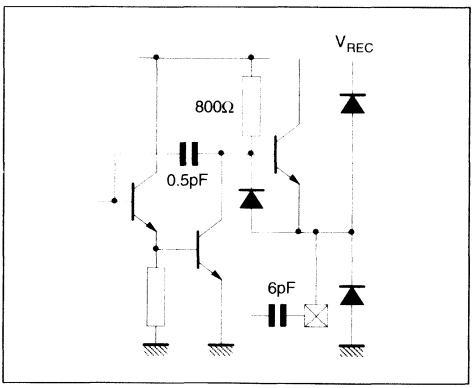
5712V-04.EPS

Pin . FM OUT



5712V-05.EPS

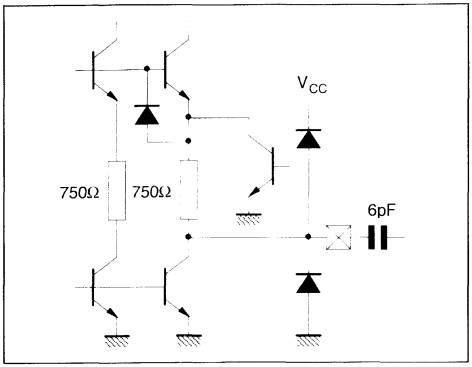
Pin : V_{MES}



5712V-06.EPS

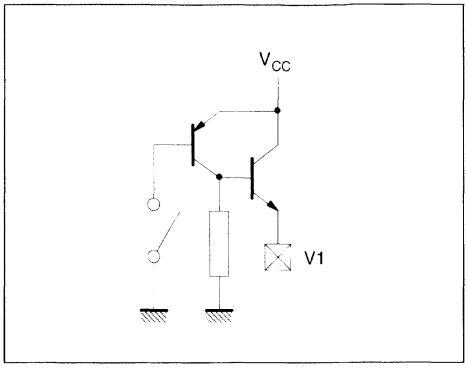
INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

Pin : V_{IN}



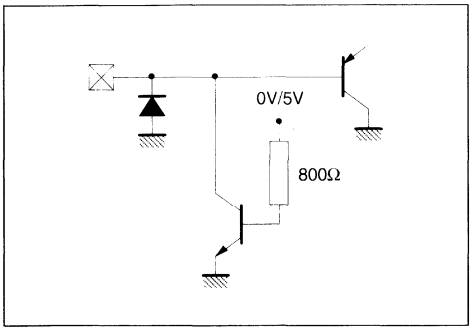
5/12V-07.EPS

Pin s : V_1, V_2



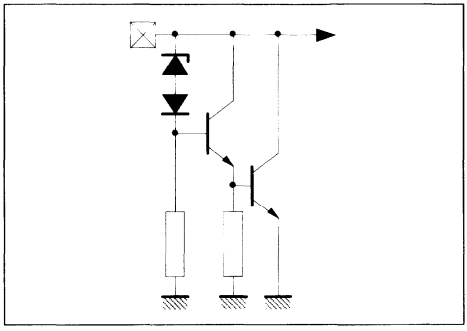
5/12V 08 EPS

Pin : PROT



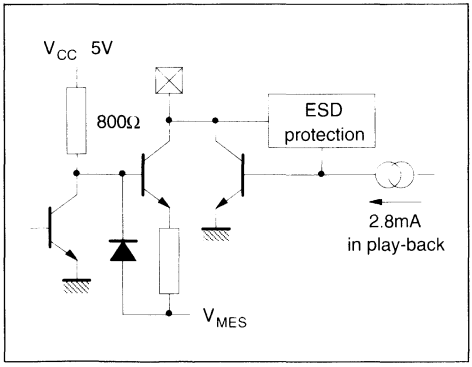
5-12V-09.EPS

Pin : V_{CC}



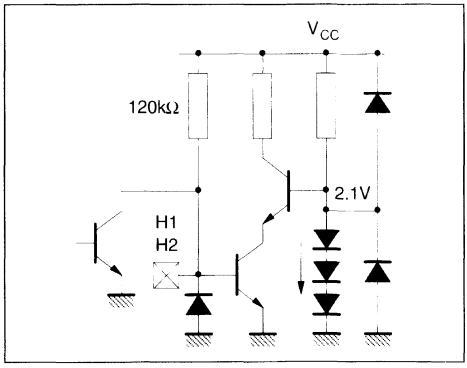
5/12V 10.EPS

Pin : I_{OUT}



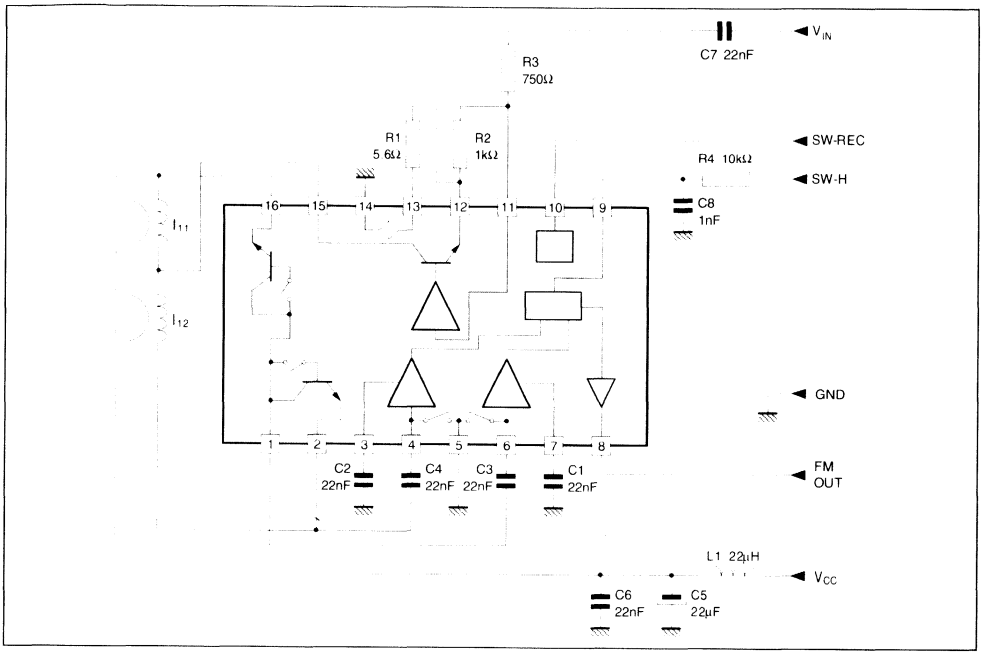
5/12V-11.EPS

Pins : H1, H2



5/12V-12.EPS

APPLICATION DIAGRAM



SGS-THOMSON MICROELECTRONICS

STV5715

ADVANCED 2-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

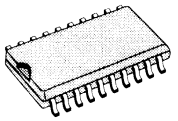
PRELIMINARY DATA

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV) WITH ADJUSTABLE GAIN

RECORD MODE

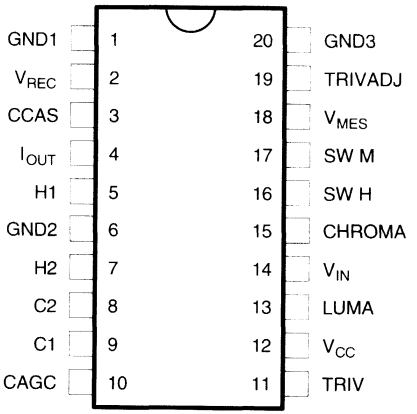
- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION



SO20 LARGE
(Plastic Micropackage)

ORDER CODE : STV5715

PIN DESCRIPTION



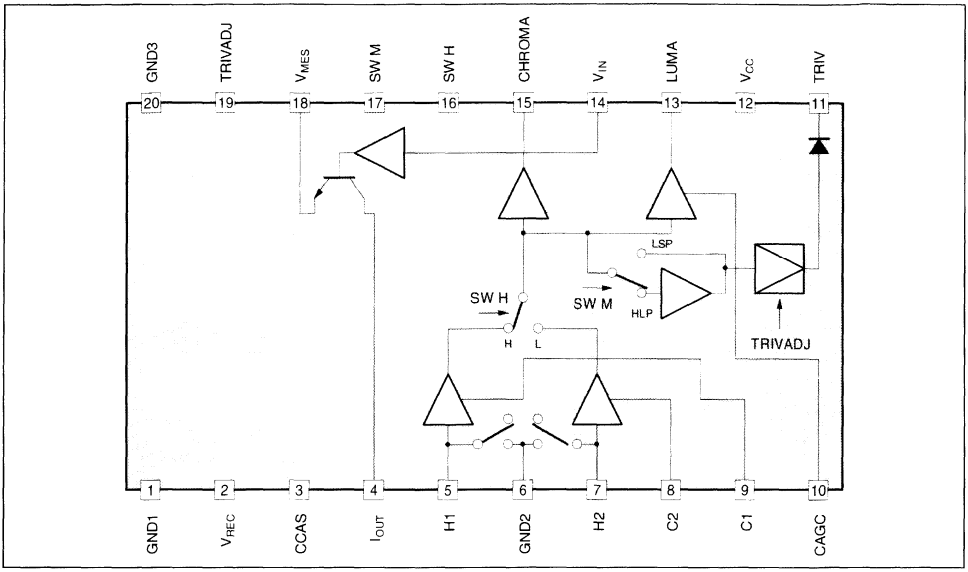
5715V-01.EPS

DESCRIPTION

The STV5715 is an advanced two head record and play-back amplifier for VCR.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

STV5715 is intended for 2 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications (10MHz bandwidth).

High performance technology allows very low noise levels (current and voltage), which are frequency independant in all the frequency range. In play-back mode a special feature suppresses the DC offset when switching the two channels. Optimized play-back output stage gives to the STV5715 large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other, dedicated to Luma processing, is phase opposite signal with a constant AC output level of 200mV_{PP} at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction. The transfer function has a gain of 2.5dB higher when a LP channel is selected. Adding to this, a gain control bloc allows to modify the gain (± 6dB) of the TRIV function for all the channels by applying a bias on pin TRIVADJ.

An automatic scanning of record supply voltage permits STV5715 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 3% transconductance accuracy is guaranteed.

STV5715 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

5715V-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Typ.	70	°C/W

5715V-02 TBL

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	4.5	5	5.5	V
V_{REC}	Power Supply Voltage Record	4.75	11.3	12.6	V
CAGC	Capacitance at Pin CAGC	4.7			nF

5715V-03 TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		42mA	52mA	25mA	38mA
V_{REC}		0mA	0mA	25mA	33mA
Total Consumption (2)	V_{CC} = 5V, V_{REC} = 9V	210mW		350mW	
	V_{CC} = 5.5V, V_{REC} = 9.45V		286mW		521mW

5715V-04 TBL

Notes : 1. R1 = 18Ω
2. Taking in account only the consumption through the IC.
A great care should be taken to the maximum power consumption : V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value. V_{REC} can be reduced as long as voltage on Pin I_{OUT} does not fall below 1V (to avoid output stage saturation).

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA,LUMA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		32	42	52	mA
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinewave 600 kHz, 400mV$_{PP}$ on output Input on Pin H1 or H2	57	60	63	dB
ΔG_{PB1}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2	Sinewave 600kHz 0.4mV$_{PP}$ on inputs H1 and H2	-1.2	0	1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1, H2, f = 600kHz		0.6		nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1, H2		1.7		pA/√Hz
CRT	Crosstalk	Sinewave 3.8MHz, 400µV$_{PP}$ on input, All the other inputs loaded with R_g = 15Ω		-45	-40	dB
R_{PB}	Playback Switch-on Resistance	ΔI = 10mA		2.0	5.0	Ω
F_{LCPB1}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low	8	13.5	0.1	MHz
F_{HCPB1}		High				MHz
C_{IN}	Input Capacitance Pins H1, H2	At 5MHz		30	40	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2	At 3.8MHz	400	600	900	Ω
Z_{CPB}	Output ImpedancePin CHROMA	DC		24	50	Ω

5715V-05 TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA,LUMA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMA OUTPUT (no AGC) (continued)						
V_{DCPB1}	DC Level at Play-back Output on Pin CHROMA		1.5	1.9	2.3	V
ΔV_{DC}	Head Switch Offset Pin CHROMA		-100	0	100	mV
SH_{PB1}	Second Harmonic Play-back Output Pin CHROMA	Sinewave 3.8MHz 400µV_{PP} on input		-45	-40	dB
LUMA OUTPUT (with AGC)						
Z_{LPB}	Output Impedance	DC		30	50	Ω
V_{DCPB2}	DC Level		1.1	1.5	2.1	V
F_{LCPB2} F_{HCPB2}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, AGC locked, 0dB at 3.8MHz Low High	 10	 12.5	 0.1	 MHz MHz
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1, H2	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1, H2	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1, H2		-44	-40	dB
CAGC						
I+	Positive Output Current	Input Signal 3.8MHz 200µV_{PP} on H1	15	30	50	µA
I-	Negative Output Current	Input Signal 3.8MHz 200µV_{PP} on H1	-50	-30	-15	µA
TRIV						
I_{TRIV}	Downloading Current		200	300	400	µA
V_{TRIV1}	Output Level (1)	With no signal, $V_{TRIVADJ}$ = 2.5V Mode LP (SW-M = high)	0.3	0.6	1.5	V
V_{TRIV2}	Output Level (2)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	1.91	2.31	2.91	V
V_{TRIV3}	Output Level (3)	V_{CHROMA} = 400mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	3.525	3.725	3.985	V
V_{TRIV4}	Output Level (4)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 1V, Mode LP (SW-M = high)	1.110	1.610	2.311	V
V_{TRIV5}	Output Level (5)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 4V, Mode LP (SW-M = high)	2.875	3.075	3.335	V
V_{TRIV6}	Output Level (6)	V_{CHROMA} = 400mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode SP (SW-M = low)	3.215	3.415	3.675	V
V_{TRIV7}	Output Level (7)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode SP (SW-M = low)	1.65	2.05	2.65	V
f_{TRIV1}	Response Lower Frequency	V_{CHROMA} = 400mV_{PP} at 4MHz and 1MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	-10	-6	-3	dB
f_{TRIV2}	Response Higher Frequency	V_{CHROMA} = 400mV_{PP} at 8MHz and 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	-2.5	-1	-0	dB
G_{TRIV}	High Level Input	LP : V_{CHROMA} = 100mV_{PP}, 300mV_{PP} at 4MHz, $V_{TRIVADJ}$ = 2.5V	4	5.5	7	V/V

5715V-06.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Record Mode

V_{REC} = 11.3V, V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}
Transconductance network defined by : R1 = 18Ω, 1% Pins GND/V_{MES}
R2 = 1.5kΩ, 1% Pins V_{MES}/V_{IN}
R3 = 0.750kΩ, 1% Pin V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 11.3V V_{CC} = 5V	17 15	25 25	33 38	mA mA
I_{max}	Max. Record Current	3.8MHz	35			mA_{PP}
TR	Transconductance	V_{IN} = 300mV_{PP}	45	55	65	mA/V
SH_{REC}	Second Harmonic	Output Current, 30mA_{PP} at 3.8MHz at Pin I_{OUT}		-54	-38	dB
 F_{LCR} F_{HCR}	Bandwidth Cut-off Frequency Pin IOUT	-3dB attenuation, 0dB at 3.8MHz Output current 30mA_{PP} Low High	 10		0.1	 MHz MHz
R_{VIN}	Input Resistance on Pin V_{IN}	Equivalent value of R3 resistor	500	700	900	Ω

5715V-07.TBL

Switching Levels

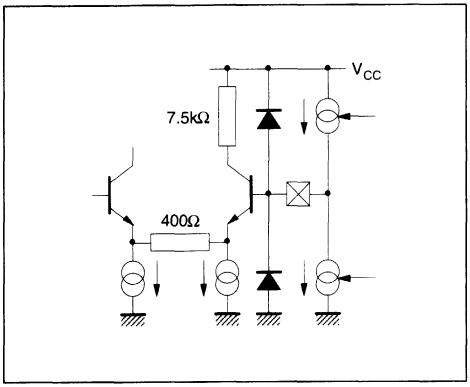
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWHH}	Head Selection Pin SW-H	Head number 1	2.4		V_{CC}	V
V_{SWHL}		Head number 2	0		1.5	V
I_{SWHH}		Input current (5V)	5	15	50	µA
I_{SWHL}		Output current (0V)	-50	-20	0	µA
V_{SWMH}	Mode Selection Pin SW-M	LP Mode	2.4		5	V
V_{SWML}		SP mode	0		1.5	V
I_{SWMH}		Input current (5V)	5	15	50	µA
I_{SWML}		Output current (0V)	-50	-20	0	µA
 t_{ON} t_{OFF}	Selection Pin SW-H Transient Response	Output signal appears on Pin CHROMA Delay time selection ON Delay time selection OFF		 100 100	 500 500	ns
V_{TH1}	Inhibition Threshold Hysteresis for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		10		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		32*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT})		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT})		11*		ms

5715V-08.TBL

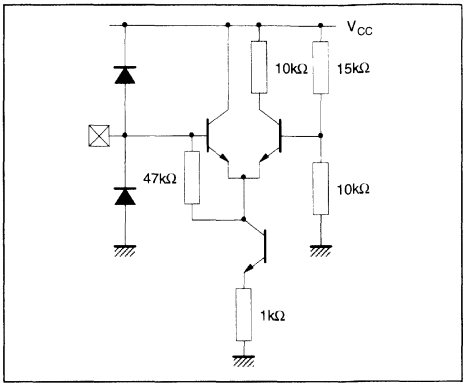
* Depending on capacitance on Pin V_{REC} ; above values are according to the application diagram at page 9.

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

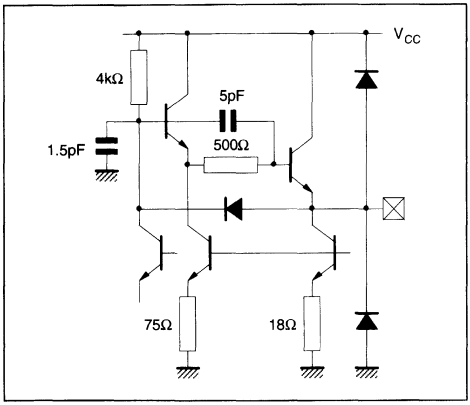
Pins : C1, C2



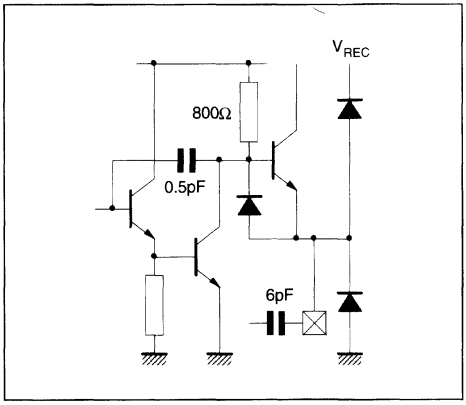
Pins : SW-H, SW-M



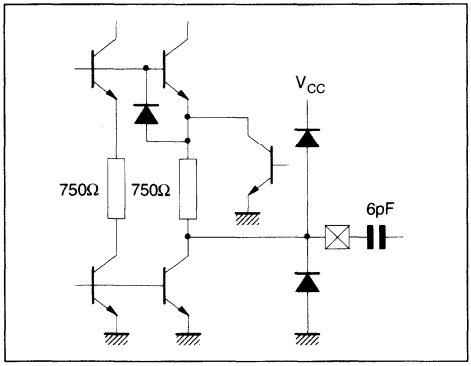
Pins : Chroma, Luma



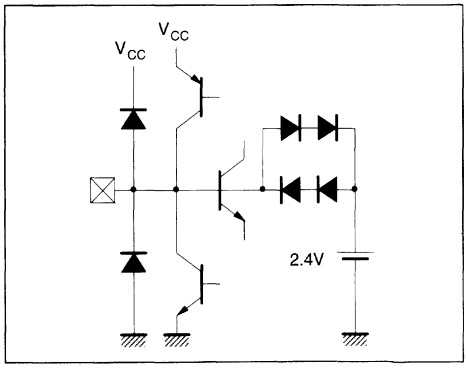
Pin : V_{MES}



Pin : V_{IN}

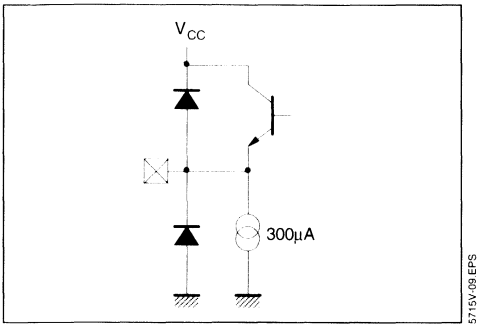


Pin : CAGC

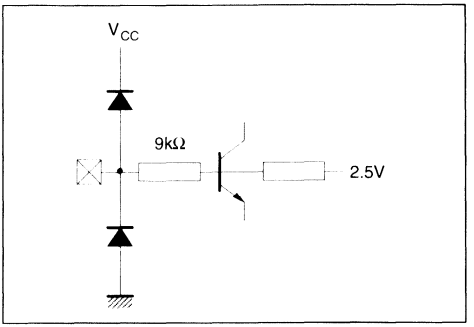


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

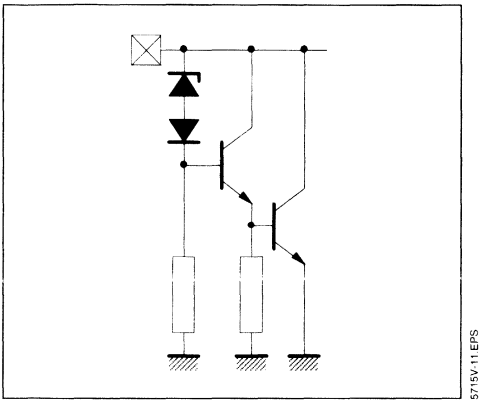
Pin : TRIV



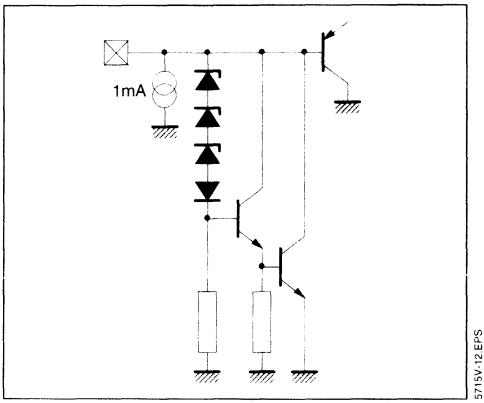
Pin : TRIVADJ



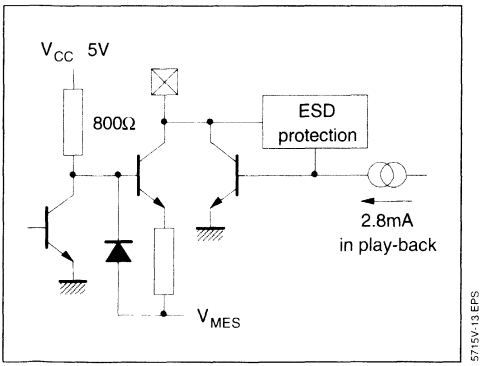
Pin : V_{CC}



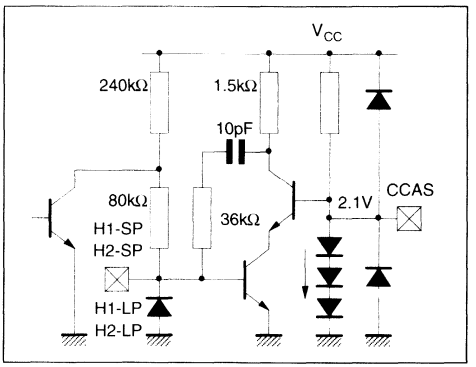
Pin : V_{REC}



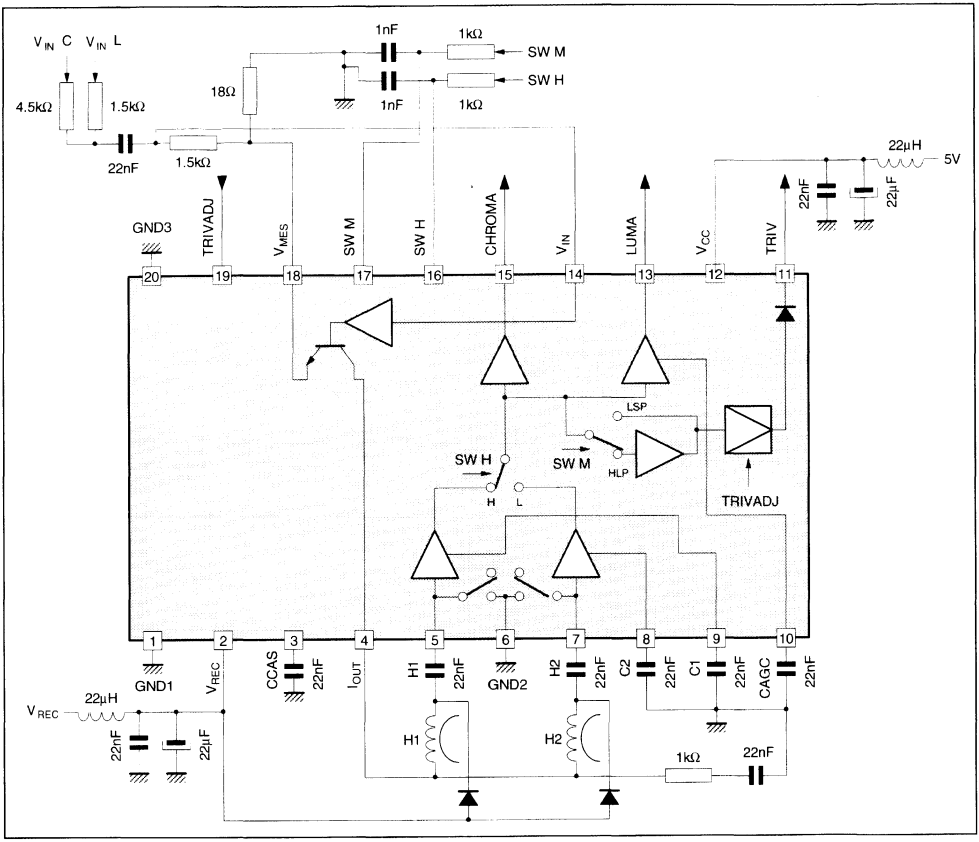
Pin : I_{OUT}



Pins : CCAS, H1, H2



APPLICATION DIAGRAM



SGS-THOMSON MICROELECTRONICS

STV5722

2-HEAD PLAYBACK AND RECORD AMPLIFIER FOR VCR

ADVANCE DATA

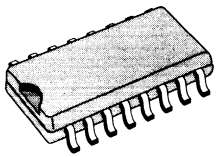
- ONE 5V POWER SUPPLY
- PLAYBACK/RECORD MODE SELECTION THROUGH A LOGIC INPUT
- SO16 PACKAGE
- NO ADJUSTMENT FOR LUMINANCE RECORDING

PLAYBACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAYBACK OUTPUT
- ONE OUTPUT FOR AUTOMATIC VIDEO TRACKING

RECORD MODE

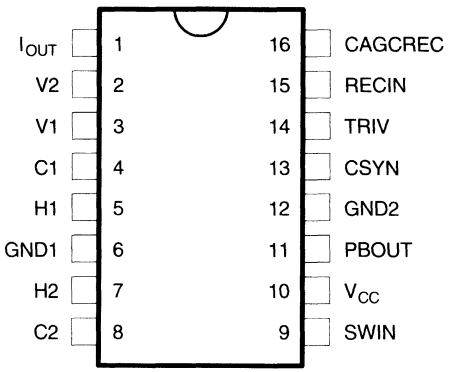
- RECORD AGC AMPLIFIER SAMPLED BY SYNCHRO SIGNAL
- RECORDING SIGNAL LEVEL ADJUSTABLE BY EXTERNAL RESISTOR



SO16 Narrow
(Plastic Package)

ORDER CODE : STV5722

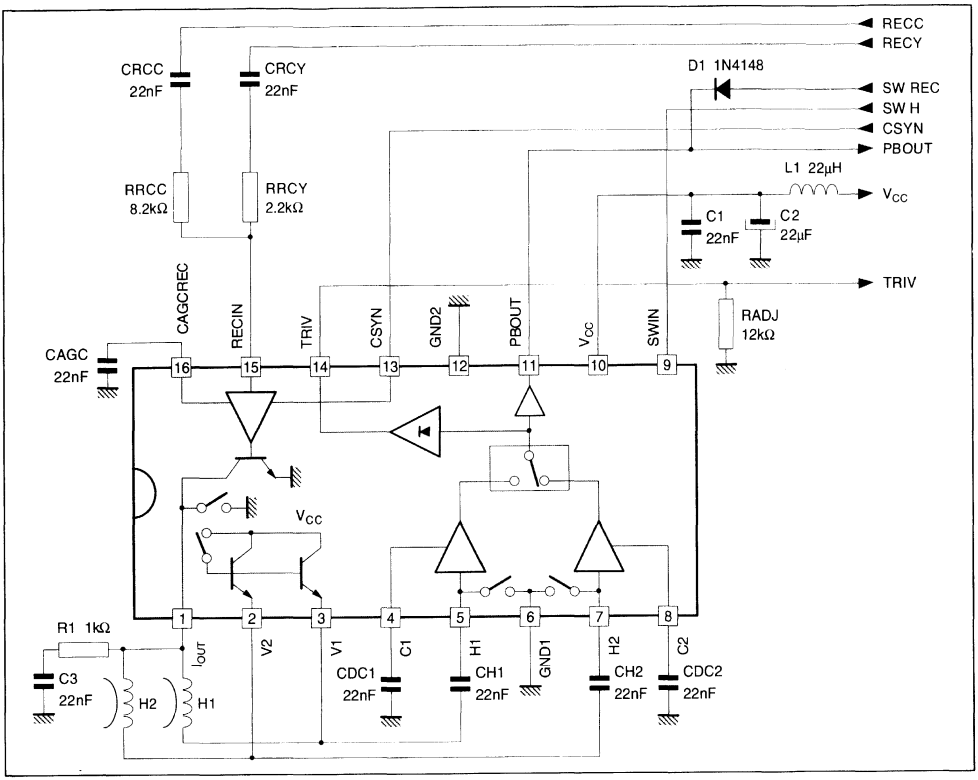
PIN CONNECTIONS



5722V-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

APPLICATION DIAGRAM



SGS-THOMSON MICROELECTRONICS

STV5726

4-HEAD PLAYBACK AND RECORD AMPLIFIER FOR VCR

ADVANCE DATA

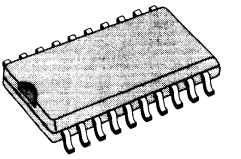
- ONE 5V POWER SUPPLY
- PLAYBACK/RECORD MODE SELECTION THROUGH A LOGIC INPUT
- SO20 PACKAGE
- NO ADJUSTMENT FOR LUMINANCE RECORDING

PLAYBACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAYBACK OUTPUT
- ONE OUTPUT FOR AUTOMATIC VIDEO TRACKING
- SP/LP ENVELOPE COMPARATOR
- SHORT-CIRCUIT SWITCHES ON UNUSED HEADS

RECORD MODE

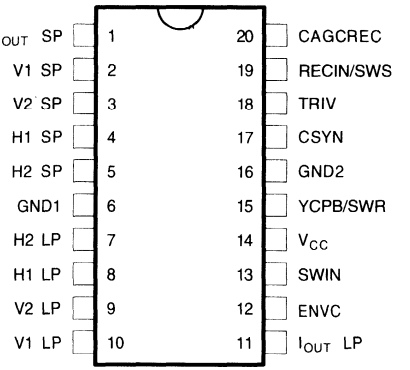
- RECORD AGC AMPLIFIER SAMPLED BY SYNCHRO SIGNAL
- RECORDING SIGNAL LEVEL ADJUSTABLE BY EXTERNAL RESISTOR
- SHORT-CIRCUIT SWITCHES ON UNUSED HEADS



SO20
(Plastic Package)

ORDER CODE : STV5726

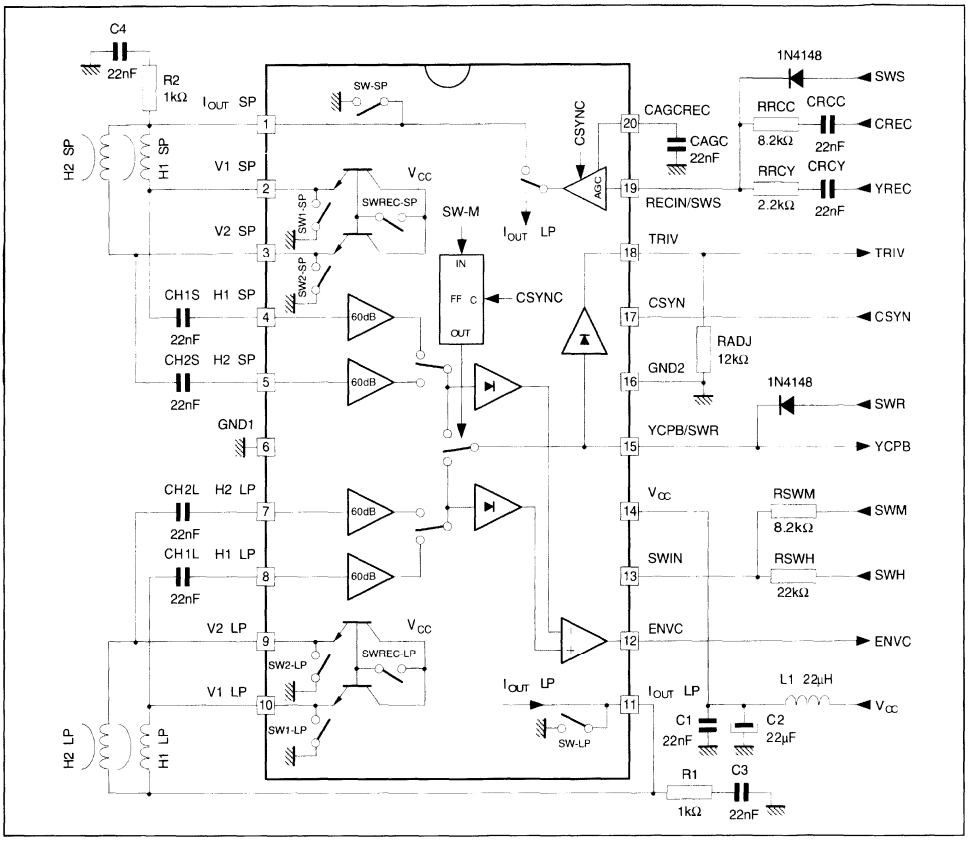
PIN CONNECTIONS



5726V-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

APPLICATION DIAGRAM



SWITCH TABLE

SW-R	SW-M	SW-S	SW-H	Channel	SW1-SP SW2-SP	SW1-LP SW2-LP	SW-SP	SW-LP	SWREC-SP	SWREC-LP	ENVC (SPLP)
L	L	L	L	2-SP	OFF	OFF	ON	ON	OFF	OFF	High IF LP > SP Low IF LP < SP
			H	1-SP							
	H		L	1-LP							
			H	2-LP							
	L	H	L	2-SP	OFF	ON					OFF (1)
			H	1-SP							
	H		L	1-LP	ON	OFF					
			H	2-LP							
H	L	L	L	SP	OFF	ON	OFF	ON	ON	OFF	0V (2)
			H								High Impedance (2)
	H		L	LP	ON	OFF	ON	OFF	OFF	ON	High Impedance (2)
			H								0V (2)

5726V 06 TBL

Notes : 1. Meaning of "OFF" : Unused heads pair (SP or LP) are grounded if SW-S is set high. Under those conditions although the ENVC output is still active, the delivered information must not be used by the microprocessor.

2. The recording current can be set different for each of the four heads. To perform it the ENVC output is either at low level or high impedance according to the selected head or mode. Then two external resistors with adequate value have to be connected respectively between the ENVC and TRIV and SWM and TRIV, playing so that on the equivalent value of the RADJ resistor.

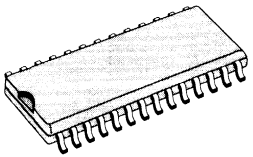
SGS-THOMSON MICROELECTRONICS

STV5730

MULTISTANDARD ON-SCREEN DISPLAY FOR VCR, PAY-TV, SATELLITE RECEIVER

ADVANCE DATA

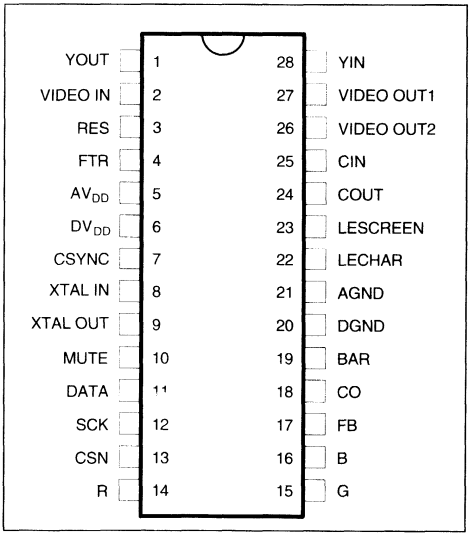
- A CHARACTER GENERATOR WITH ASCII RAM AND CHARACTER ROM :
  - 128 characters
  - 12 dots x 18 lines character composition
  - 11 rows x 28 characters page composition
- ACCURATE INTERNAL BANDGAP VOLTAGE REFERENCE
- LINE LOCKED PLL
- PLL PROTECTIONS AGAINST SYNC NOISE AND PLL INSENSITIVE TO VCR HEAD SWITCHING
- VIDEO TIMING GENERATOR
- INPUT CVBS CLAMP AND SYNC EXTRACTOR
- VERTICAL SYNC SEPARATOR
- INPUT CVBS SYNC RE-INSERTION
- INPUT CVBS PRESENCE DETECTOR
- PAL/NTSC CHROMA ENCODER
- DEDICATED PINS FOR LUMA AND CHROMA EXTERNAL FILTERING
- GAIN ON CVBS OUTPUT FOR EITHER 0dB OR 6dB CAPABILITY
- MULTISTANDARD TRANSLUCENT MIXED MODE
- OPAQUE MIXED MODE
- NORMAL FULL PAGE MODE
- VIDEO FULL PAGE MODE
- SUITABLE FOR S-VHS
- THREE DIFFERENT MARKERS CAN BE GENERATED SIMULTANEOUSLY
- THREE WIRE SERIAL INTERFACE FOR MICROPROCESSOR CONTROL



SO28
(Plastic Micropackage)

ORDER CODE : STV5730

PIN CONNECTIONS



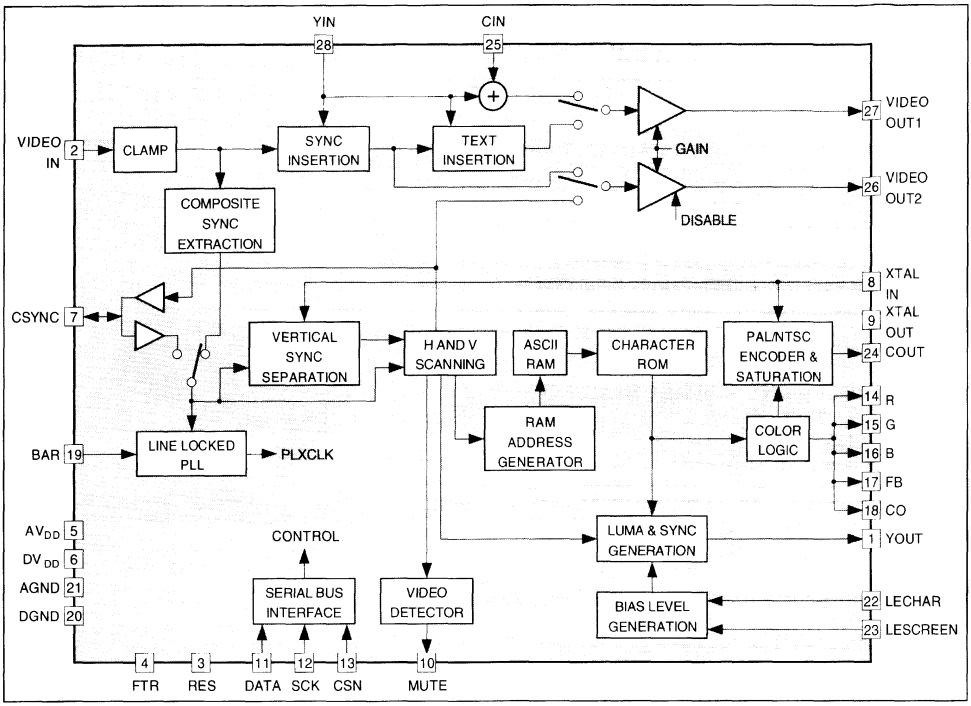
5730V-01.EPS

DESCRIPTION

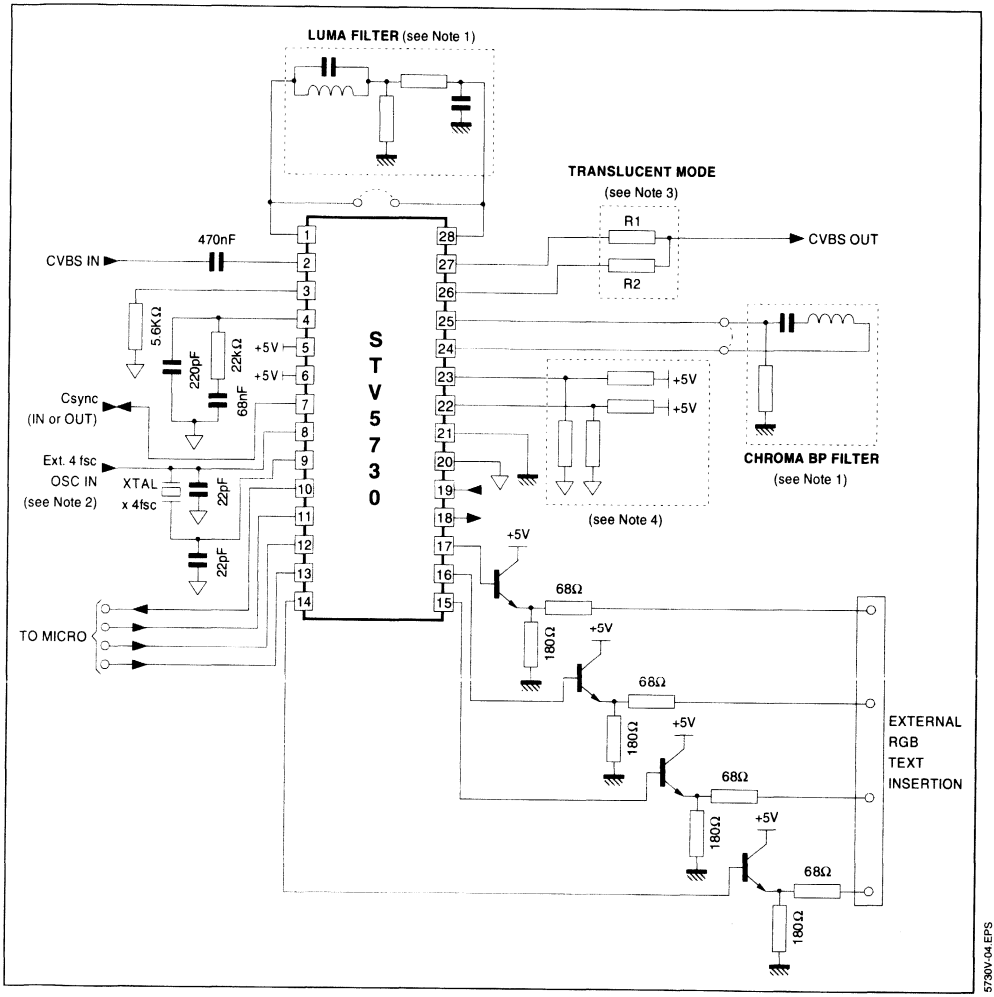
The STV5730 IC is intended to be used in VCR, Satellite receiver and PAY-TV systems for CVBS or R/G/B applications.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



TYPICAL PAL/NTSC/SECAM APPLICATION



Notes :
1. Optional filter. For low cost applications, short circuit.
2. The 4fsc (17.734MHz PAL, 14.318MHz NTSC) crystal may be ommited if this signal is alreadyavailable in a system.
3. The value of R1/R2 may be ratioed to give required level of translucent OSD.
4. External bias level can be set by resistor ratio is required. Anyhow the level at pins LECHAR and LESCREEN must be kept lower than 3.0 volts.

SGS-THOMSON MICROELECTRONICS

TEA5702A

ADVANCED 2-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

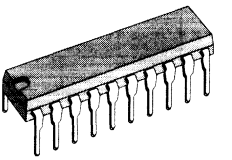
PRELIMINARY DATA

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 2 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- TWO PLAY-BACK OUTPUTS INCLUDING AGC (PHASE AND OPPOSITE PHASE)
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)

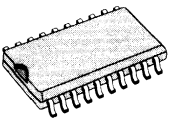
RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION



DIP20
(Plastic Package)

ORDER CODE : TEA5702A



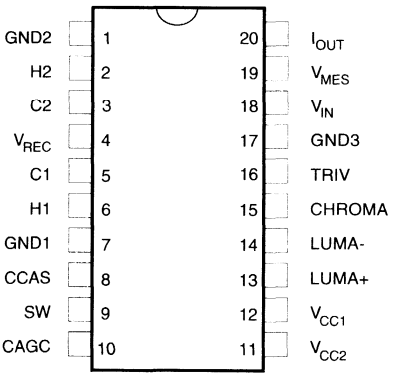
SO20 LARGE
(Plastic Micropackage)

ORDER CODE : TEA5702AD

DESCRIPTION

The TEA5702A is an advanced two head record and play-back amplifier for VCR.

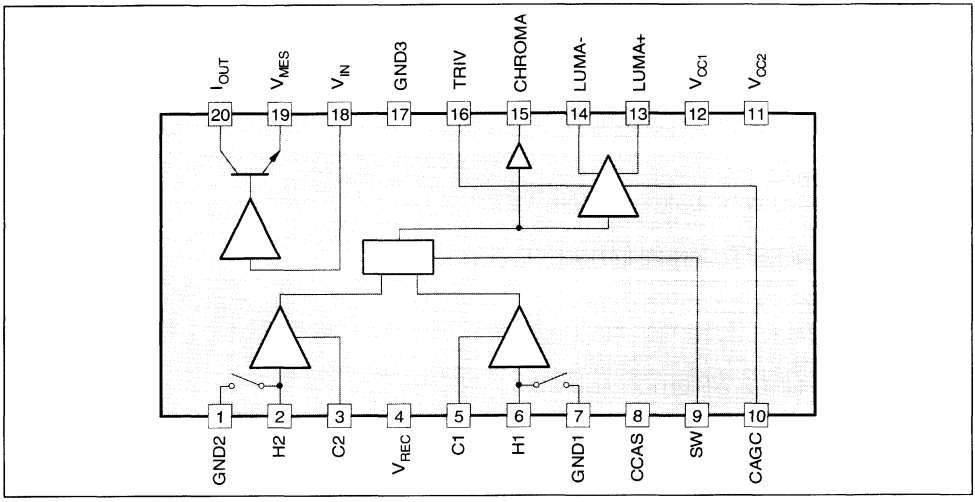
PIN DESCRIPTION



5702A-01.EPS

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5702A is intended for 2 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5702A large capability to drive directly a coaxial cable in order to reduce number of external components.

Three play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the two others, dedicated to Luma processing, are phase opposite signals with a constant AC output level of 200mV_{PP} at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5702A automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 3% transconductance accuracy is guaranteed.

TEA5702A is fully protected against ESD.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	150	°C
T_{oper}	Operating Temperature	0, +70	°C

5702A-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

5702A-02.TBL

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	4.75	5	5.25	V
V_{REC}	Power Supply Voltage Record	4.75	10	12.6	V
CAGC	Capacitance at Pin CAGC	4.7			nF

5702A-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		35mA	45mA	25mA	35mA
V_{REC}		0mA	0mA	45mA	55mA
Total Consumption (2)	V_{CC} = 5, V_{REC} = 10	175mW		530mW	
	V_{CC} = 5.25, V_{REC} = 10.5		240mW		760mW

5702A-04.TBL

Notes : 1. R1 = 10Ω
2. Taking in account only the consumption through the IC.
A great care should be taken to the maximum power consumption : V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value.

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		25	35	45	mA
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinus wave 600 kHz 400mV$_{PP}$ on output Input on Pin H1 or H2	56	60	62	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2	Sinus wave 3.8MHz 0.4mV$_{PP}$ on inputs H1 or H2			1.2	dB
e_N	Equivalent Input Voltage Noise Level (see note)	Input grounded via switching transistor on Pins H1, H2		0.6	0.85	nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1, H2		2	2.8	pA/√Hz
CRT	Crosstalk	Sinus wave 3.8MHz 400µV$_{PP}$, All switches combinated			-40	dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low High	8		0.1	MHz MHz
C_{IN}	Input Capacitance Pins H1, H2			30		pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2		400	600	900	Ω
Z_{CPB}	Output Impedance	Sinus wave 1MHz, 400µV$_{PP}$ on input		30	50	Ω
V_{DCPB1}	DC Level		1.5	1.9	2.5	V
ΔV_{DC}	Head Switch Offset				100	mV
SH_{PB1}	Second Harmonic	Sinus wave 600kHz, 400µV$_{PP}$ on input		-45	-40	dB
LUMA+, LUMA- OUTPUTS (with AGC)						
Z_{LPB}	Output Impedance	Sinus wave 1MHz, 400µV$_{PP}$ on input		30	50	Ω
V_{DCPB2}	DC Level		0.8	1.5	2.0	V

5702A-05.TBL

Note : These values can be adjusted to the application.

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA+, LUMA-

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LUMA+, LUMA- OUTPUTS (with AGC) (continued)						
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1, H2	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1, H2	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1, H2		-43	-35	dB
CAGC						
I+	Positive Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 1V on Pin CAGC	15	30	45	µA
I-	Negative Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1, 3.5V on Pin CAGC	-50	-30	-15	µA
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1} V_{TRIV3} V_{TRIV4} V_{TRIV5}	Output Level	V_{CHROMA} = 0mV_{PP} V_{CHROMA} = 400mV_{PP} at 4.5MHz V_{CHROMA} = 600mV_{PP} at 4.5MHz V_{CHROMA} = 800mV_{PP} at 4.5MHz	0 2.6 3.3 3.6	 3 3.7 4.2	1.2 3.4 4.1 4.5	V V V V
G_{TRIV1} G_{TRIV2}	Gain	V_{CHROMA} = 0mV_{PP}, 400mV_{PP} at 4.5MHz V_{CHROMA} = 400mV_{PP}, 600mV_{PP} at 4.5MHz		7.5 3.5		V/V_{PP} V/V_{PP}

5702A-06.TBL

Record Mode

V_{REC} = 10V, V_{CC} = 5V, Load resistor 100Ω on Pin I_{OUT}

Transconductance network defined by : R1 = 10Ω 1% Pins GND3/V_{MES}

R2 = 1kΩ 1% Pins V_{MES}/V_{IN}

R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 10V V_{CC} = 5V		45 25	55 35	mA mA
I_{OUT}						
I_{max}	Max. Record Current	3.8MHz	35			mA_{PP}
TR	Transconductance	V_{IN} = 300mV_{PP}	110	140	170	mA/V
SH_{REC}	Second Harmonic	Output Current 30mA_{PP} at 3.8MHz		-48	-40	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation, 0dB at 3.8MHz Output current 30mA_{PP} Low High	 8		 0.1	 MHz MHz

5706A-07.TBL

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH}	Head Selection Pin SW	Head number 1 (high level)	2.4		V_{CC}	V
V_{SWL}		Head number 2 (low level)	0		1.5	V
I_{SWH}		Input current (high level)		20	50	µA
I_{SWL}		Output current (low level)		20	50	µA
t_{ON}	Selection Pin SW Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	1000	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	1000	ns

5702A-08.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		2*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT})		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT})		4*		ms

5702A-09.TBL

* Depending on capacitance on Pin V_{REC}.

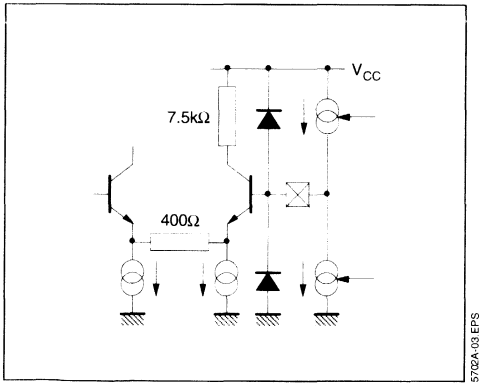
Power Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC} 75µV_{PP} on Pin H1, H2 Measurement on Pin Chroma	15	20		dB

5702A-10.TBL

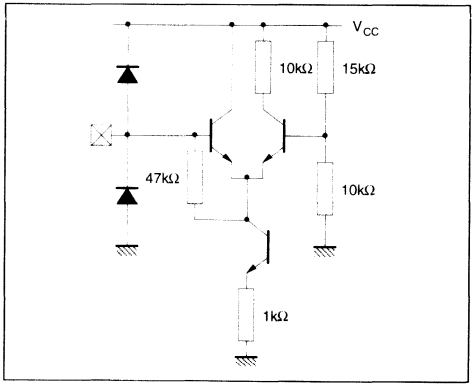
INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1, C2



5702A-03.EPS

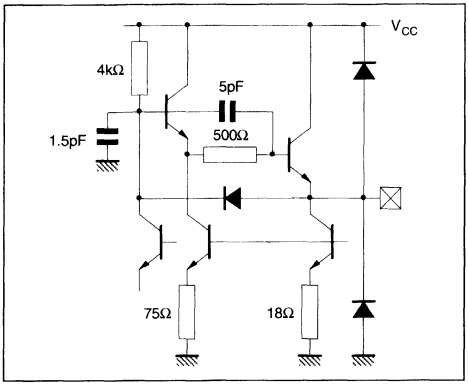
Pin : SW



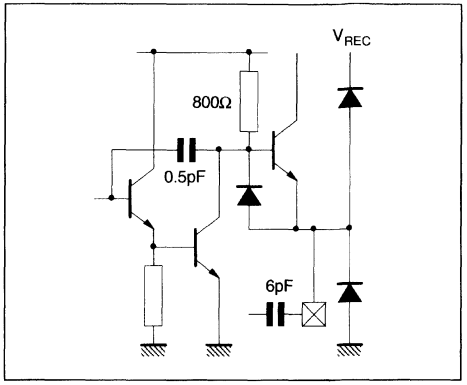
5702A-04.EPS

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

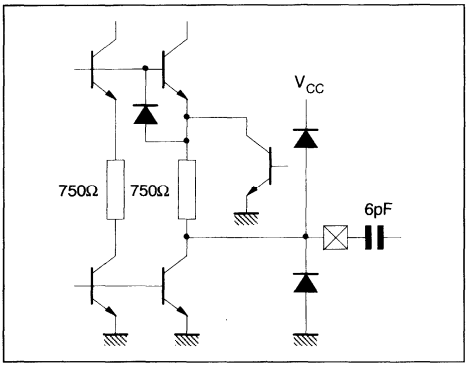
Pins : Chroma, Luma+, Luma-



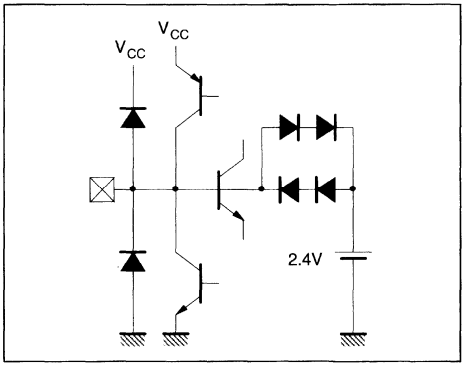
Pin : V_{MES}



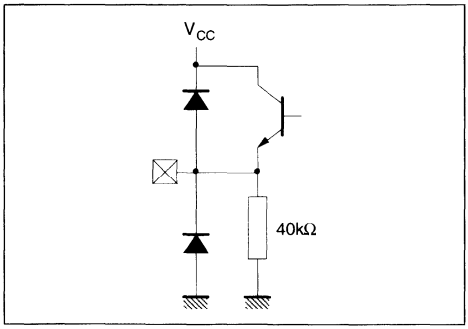
Pin : V_{IN}



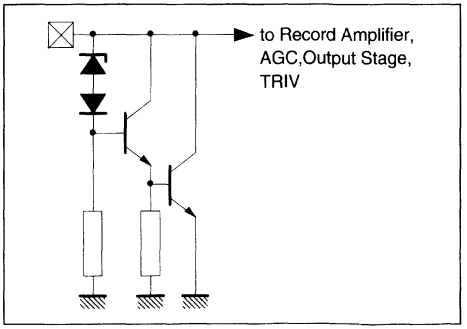
Pin : CAGC



Pin : TRIV

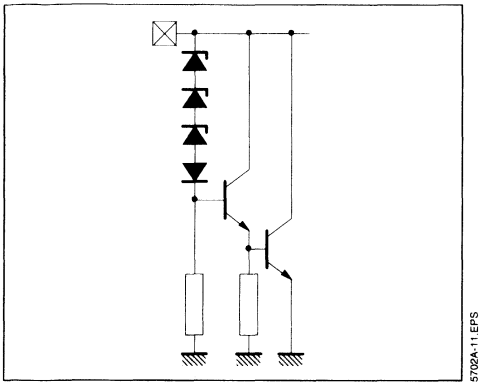


Pin : V_{CC1}

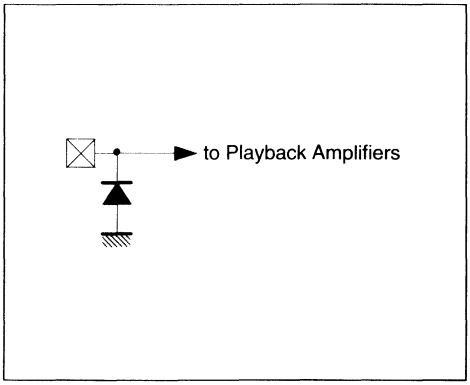


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

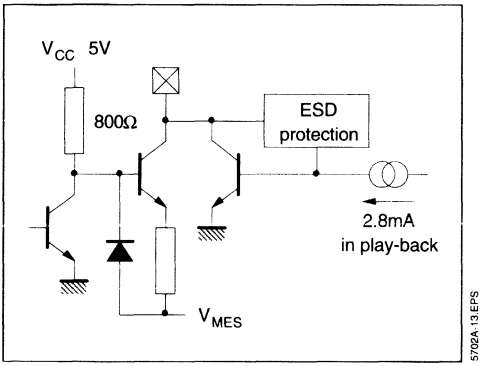
Pin : V_{REC}



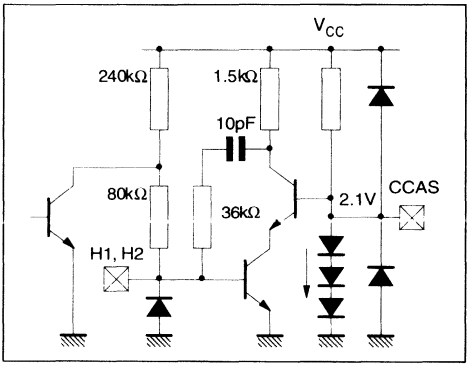
Pin : V_{CC2}



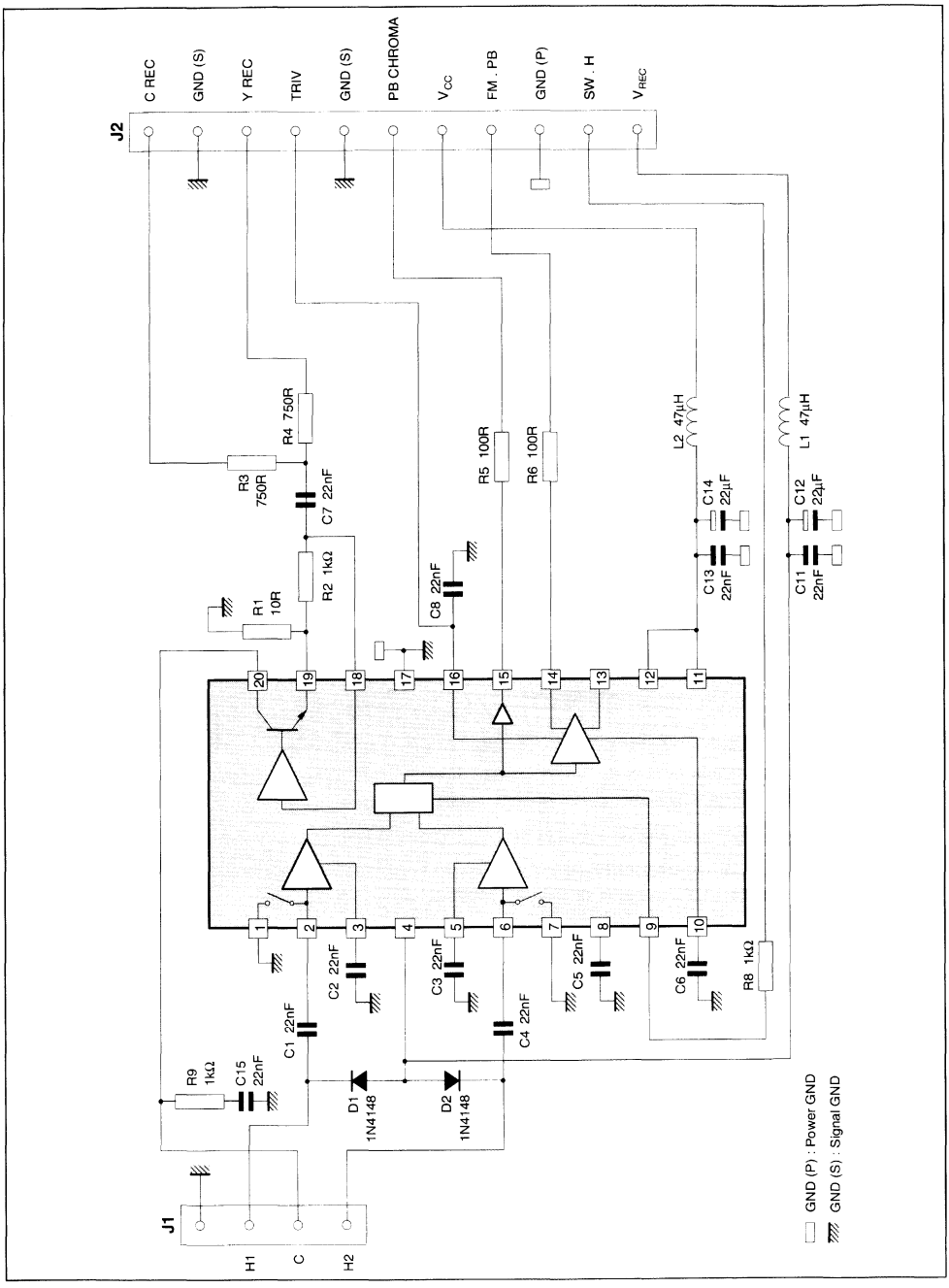
Pin : I_{OUT}



Pins : H1, H2, CCAS



TYPICAL APPLICATION DIAGRAM



SGS-THOMSON MICROELECTRONICS

TEA5703

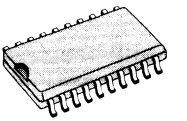
ADVANCED 3-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 3 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 3 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC (OPPOSITE PHASE)
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)

RECORD MODE

- ONE INTEGRATED I/I CONVERTER WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION
- RECORD AMPLIFIER WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT



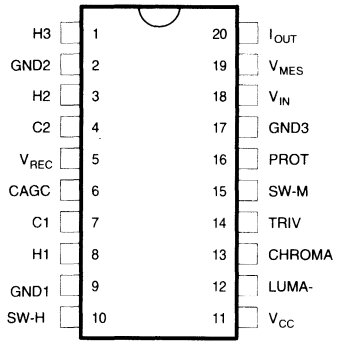
SO20 LARGE
(plastic micropackage)

ORDER CODE : TEA5703

DESCRIPTION

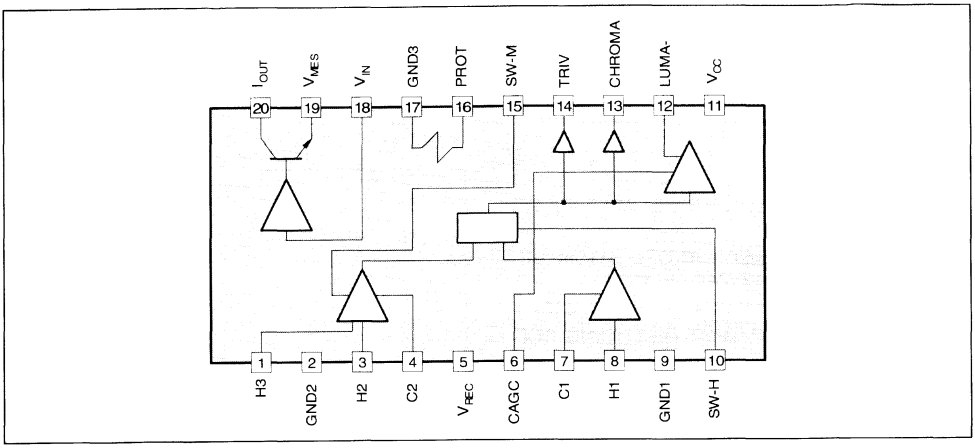
The TEA5703 is an advanced three head record and play-back amplifier for VCR.

PIN CONNECTIONS



5703-01.EPS

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5703 is intended for 3 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications.

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5703 large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other one, dedicated to Luma processing, is phase opposite signal with a constant AC output level of 200mV$_{PP}$ at 3.8MHz signal.

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5703 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for the two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 5% transconductance accuracy is guaranteed.

Against short circuit on the recording transconductance components, the recording amplifier includes an overheating protection system for the IC and the application board.

TEA5703 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	150	°C

5703-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	Typ.	70	°C/W

5703-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		45mA	55mA	35mA	45mA
V_{REC}		0mA	0mA	30mA	40mA
Total Consumption	V_{CC} = 5, V_{REC} = 10	225mW		450mW	
	V_{CC} = 5.25, V_{REC} = 10.5		290mW		620mW

5703-03.TBL

Notes : 1. R1 = 10Ω

Play-back Mode (V_{CC} = 5V, no load on Pins CHROMA, LUMA-.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		30	45	55	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinus wave 600 kHz 400mV_{PP} on output Input on Pin H1, H2 or H3	57	60	63	dB
ΔG_{PB}	Gain Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2	Sinus wave 3.8MHz 0.4mV_{PP} on inputs H1, H2 or H3			1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1, H2, H3		0.45	0.63	$nV/\sqrt{Hz}$
i_N	Equivalent Input Current Noise	Pins H1, H2, H3		2.6	3.4	$pA/\sqrt{Hz}$
CRT21/31 CRT	Crosstalk	Sinus wave 3.8MHz, 400μV_{PP}, H2-H1, H3-H1 All combinations but H2-H1, H3-H1			- 25.5 - 40	dB dB
F_{LCPB} F_{HCPB}	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz Low High	8		0.1	MHz MHz
C_{IN}	Input Capacitance Pins H1, H2,H3			35	50	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1, H2, H3		350	600	850	Ω
Z_{CPB}	Output Impedance	Sinus wave 0.1MHz 400μV_{PP} on input		30	50	Ω
V_{DCPB1}	DC Level at Chroma		1	1.5	2	V
ΔV_{DC}	Head Switch Offset				50	mV
SH_{PB1}	Second Harmonic	Sinus wave 3.8MHz H1, H2, H3 400μV_{PP} on input with load resistor 500Ω		- 45	- 40	dB
LUMA- OUTPUT (with AGC)						
Z_{LPB}	Output Impedance	Sinus wave 0.1MHz 400μV_{PP} on input		30	50	Ω
V_{DCPB2}	DC Level		1	1.6	2.2	V
V_{LPB}	Output Amplitude	Input signal 200μV_{PP} at 3.8MHz on Pins H1, H2, H3	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200μV_{PP} at +6dB or -5dB on Pins H1, H2, H3	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400μV_{PP} on Pins H1, H2, H3 500Ω//100pF		- 43	- 38	dB

5703-04.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Play-back Mode (V_{CC} = 5V, no load on Pins CHROMA, LUMA-.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LUMA- OUTPUT (with AGC) (continued)						
I+	Positive Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1	15	30	45	µA
I-	Negative Output Current on Pin CAGC	Input Signal 3.8MHz 200µV_{PP} on H1	-45	-30	-15	µA
	Input Capacitance on Pin CAGC		4.7			nF
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1} V_{TRIV2} V_{TRIV3} V_{TRIV4}	Output Level	V_{CHROMA} = 0mV_{PP} V_{CHROMA} = 100mV_{PP} V_{CHROMA} = 400mV_{PP} V_{CHROMA} = 600mV_{PP}	0.2	0.4 1.6 3.5	 4.5	V V V V
G_{TRIV1} G_{TRIV2}	Gain	V_{CHROMA} = 300, 400mV_{PP} V_{CHROMA} = 50, 100mV_{PP}		3 12		V/V_{PP} V/V_{PP}

5703-05.TBL

Record Mode (V_{REC} = 10V, V_{CC} = 5V, Load resistor 100Ω on Pin I_{OUT})

Transconductance network defined by : R1 = 10Ω 1% Pins PROT/V_{MES}
R2 = 1kΩ 1% Pins V_{MES}/V_{IN}
R3 = 750Ω 1% Pins V_{IN}

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 10V V_{CC} = 5V	20 25	30 35	40 45	mA mA
I_{OUT}						
I_{max}	Max. Record Current	3.8MHz	35			mA_{PP}
TR	Transconductance	V_{IN} = 300mV_{PP}		140		mA/V
SH_{REC}	Second Harmonic	Output Current 30mA_{PP} at 3.8MHz		- 40	-38	dB
F_{LCREC} F_{HCREC}	Bandwidth Cut-off Frequency	-3dB attenuation Output current 30mA_{PP} Low High	 8		 0.1	 MHz MHz
	Output Resistance		7	100		kΩ
	Maximum Input Current on Pin PROT	5V on Pin PROT	150	250	400	mA
	Maximum Saturation Voltage on Pin PROT	Input current 50mA		100	150	mV
	Input Resistance	Equivalent value of R3 resistor		700		Ω

5703-06.TBL

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWH1}	Head Selection Pin SW-H	Head number 1	2.4		V_{CC}	V
V_{SWL1}		Head number 2	0		1.5	V
I_{SWHH}		Input Current (high level)		20	50	µA
I_{SWHL}		Output Current (low level)		20	50	µA
V_{SWH2}	Head Selection Pin SW-M	Head number 2 or 1	2.4		V_{CC}	V
V_{SWL2}		Head number 3	0		1.5	V
I_{SWMH}		Input Current (high level)		20	50	µA
I_{SWML}		Output Current (low level)		20	50	µA

5703-07.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Selection Pin SW-H Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	1000	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	1000	ns
t_{H2}	Selection Pin SW-M Transient Response	Delay time H2 selection (output signal appears on Pin CHROMA)		1	10	ms
t_{H3}		Delay time H3 selection (output signal appears on Pin CHROMA)		1	10	ms
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		20*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT})		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT})		4*		ms

5703-08 TBL

* Depending on capacitance on Pin V_{REC}.

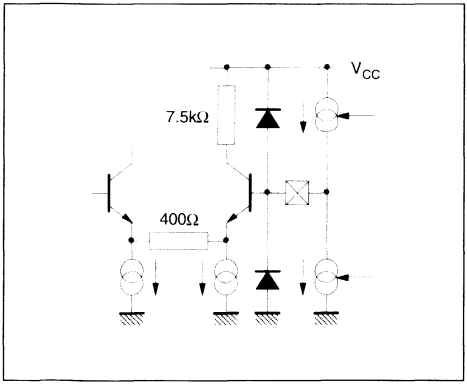
Power Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Positive Supply Voltage Pin V_{CC}		4.75	5	5.25	V
V_{REC}	Record Voltage Pin V_{REC}		4.75	10	12.6	V
SVR	Supply Voltage Rejection	0.5mV$_{PP}$ on Pin V_{CC} 75µV$_{PP}$ on Pin H1, H2,H3 Measurement on Pin Chroma	15	20		dB

5703-09 TBL

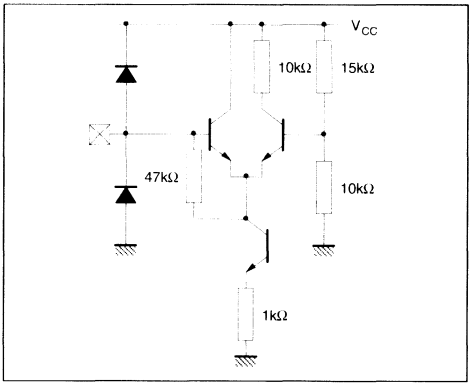
INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1, C2



5703-03.EPS

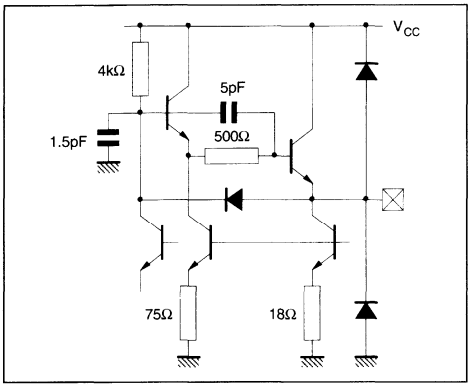
Pin : SW-H, SW-M



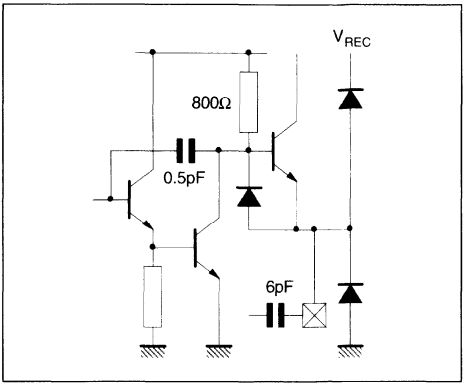
5703-04.EPS

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

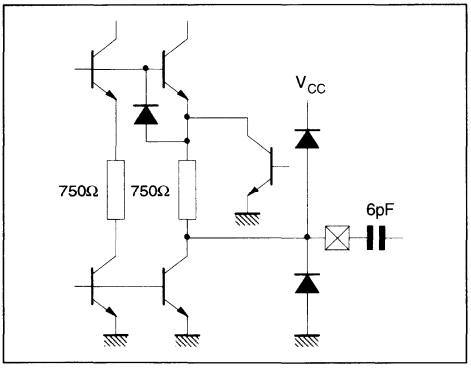
Pins : Chroma, Luma-



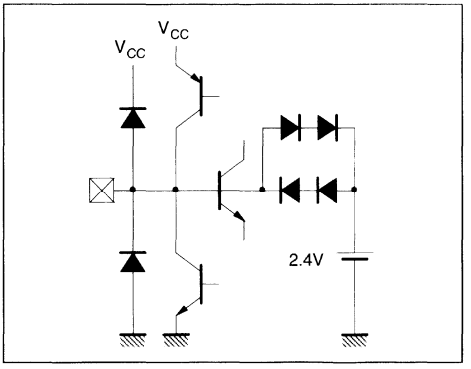
Pin : V_{MES}



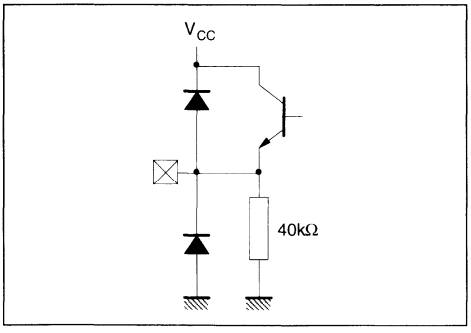
Pin : V_{IN}



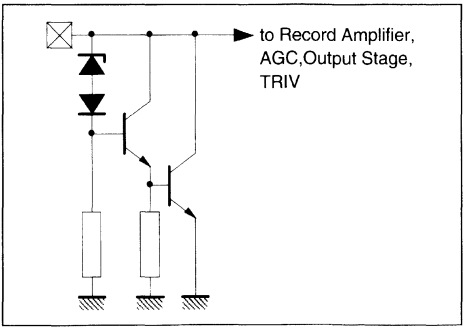
Pin : CAGC



Pin : TRIV

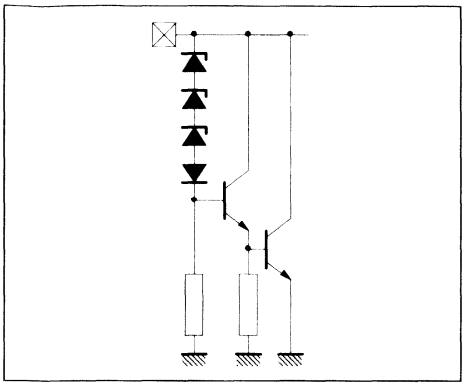


Pin : V_{CC1}

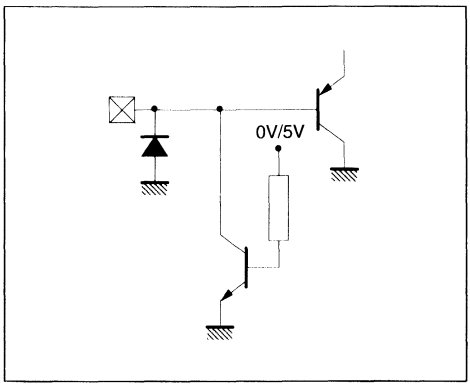


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

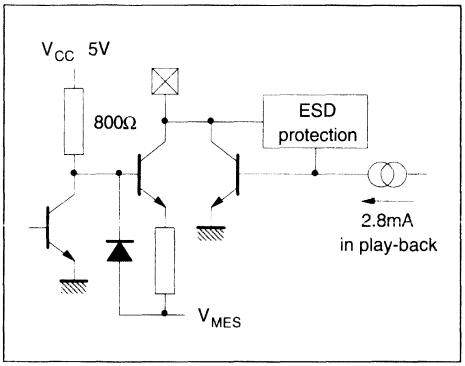
Pin : V_{REC}



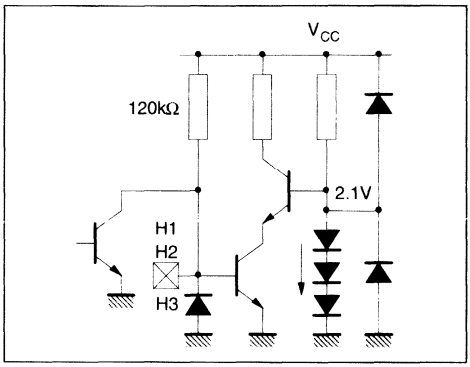
Pin : PROT



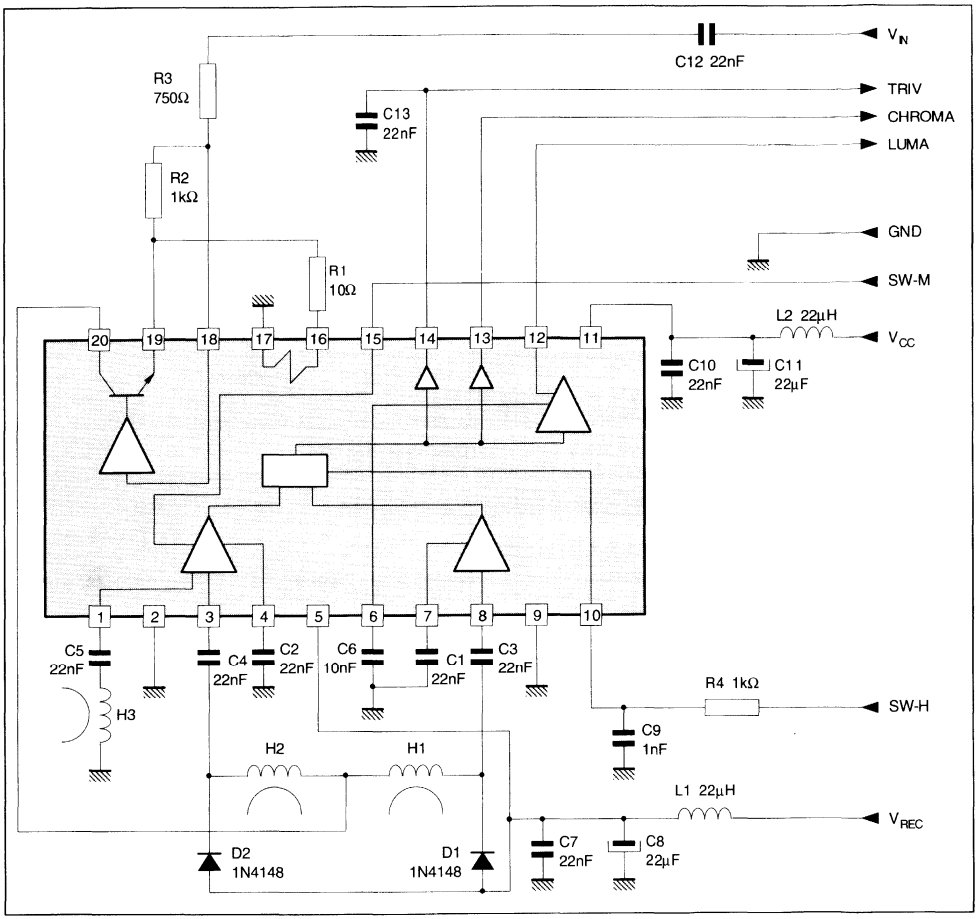
Pin : I_{OUT}



Pins : H1, H2, H3



APPLICATION DIAGRAM



SGS-THOMSON MICROELECTRONICS

TEA5705

ADVANCED 4-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

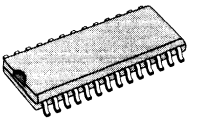
For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUTS GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV) WITH ADJUSTABLE GAIN
- SHORT PLAY/LONG PLAY ENVELOPE COMPARATOR WITH SCHMIDT TRIGGER OUTPUT

RECORD MODE

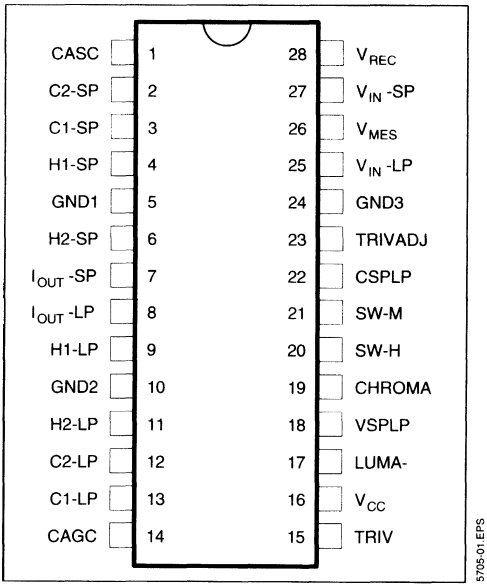
- TWO INTEGRATED I/I CONVERTERS WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION



SO28 LARGE
(Plastic Micropackage)

ORDER CODE : TEA5705

PIN DESCRIPTION

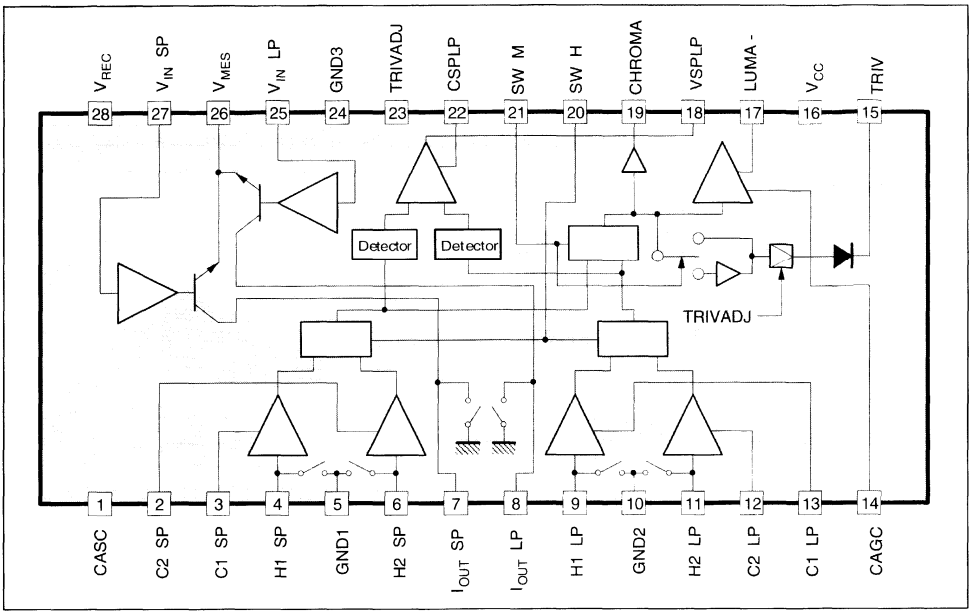


5705-01.EPS

DESCRIPTION

The TEA5705 is an advanced four head record and play-back amplifier for VCR.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5705 is intended for 4 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications (10MHz bandwidth).

High performance technology allows very low noise levels (current and voltage), which are frequency independant in all the frequency range. In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5705 large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other, dedicated to Luma processing, is phase opposite signal with a constant AC output level of 200mV$_{PP}$ at 3.8MHz signal.

A tracki] information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction. The transfer function has a gain of 2.5dB higher when a LP channel is selected. Adding to this, a gain control bloc allows to modify the gain (± 6dB) of the TRIV function for all the channels by applying a bias on pin TRIVADJ.

An automatic scanning of record supply voltage permits TEA5705 automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 3% transconductance accuracy is guaranteed. Feedback loop gains of SP channel and LP channel can be different.

A particular feature is the SP/LP envelope comparator and detector. This system can be used in search mode, still mode, slow mode... The output signal is an output current feeding a capacitor (CSPLP) which is bufferised through a schmidt trigger circuit to VSPLP. This output is high in record mode. By varying the capacitance on CSPLP a good compromise can be found between short delay time and spike free signal.

TEA5705 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

5705-01 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Typ.	70	°C/W

5705-02 TBL

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	4.5	5	5.5	V
V_{REC}	Power Supply Voltage Record	4.75	11.3	12.6	V
CAGC	Capacitance at Pin CAGC	4.7			nF
CSPLP	Capacitance at Pin CSPLP		4.7		nF

5705-03 TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		55mA	70mA	40mA	50mA
V_{REC}		0mA	0mA	27mA	33mA
Total Consumption (2)	V_{CC} = 5V, V_{REC} = 9V	250mW		478mW	
	V_{CC} = 5.5V, V_{REC} = 9.45V		385mW		630mW

5705-04 TEL

Notes : 1. R1 = 18Ω

2. Taking in account only the consumption through the IC.
A great care should be taken to the maximum power consumption : V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value. V_{REC} can be reduced as long as voltage on Pins I_{OUT}-SP, I_{OUT}-LP is not going under 1V (to forbid output stage saturation).

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA,LUMA-

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		45	55	70	mA
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinewave 600 kHz 400mV$_{PP}$ on output Input on Pin H1-SP or H2-SP, H1-LP or H2-LP	57	60	63	dB
ΔG_{PB1}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in SP Mode	Sinewave 600kHz 0.4mV$_{PP}$ on inputs H1-SP and H2-SP	-1.2	0	1.2	dB
ΔG_{PB2}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in LP Mode	Sinewave 600kHz 0.4mV$_{PP}$ on inputs H1-LP and H2-LP	-1.2	0	1.2	dB
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1-SP, H2-SP, H1-LP, H2-LP, F = 600kHz		0.6		nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1-SP, H2-SP, H1-LP, H2-LP		1.7		pA/√Hz

5705-05 TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA,LUMA-

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMA OUTPUT (no AGC) (continued)						
CRT	Crosstalk	Sine wave 3.8MHz 400µV_{PP} on input, All the other inputs loaded with R_g = 15Ω		-45	-40	dB
R_{PB}	Playback Switch-on Resistance	ΔI = 10mA		2.0	5.0	Ω
	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz				
F_{LCPB1}		Low			0.1	MHz
F_{HCPB1}		High	8	13.5		MHz
C_{IN}	Input Capacitance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 5MHz		30	40	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 3.8MHz	400	600	900	Ω
Z_{CPB}	Output ImpedancePin CHROMA	DC		24	50	Ω
V_{DCPB1}	DC Level at Play-back Output on Pin CHROMA		1.5	1.9	2.3	V
	Head Switch Offset Pin CHROMA					
ΔV_{DCSP}			-100	0	100	mV
ΔV_{DCLP}			-100	0	100	mV
SH_{PB1}	Second Harmonic Play-back Output Pin CHROMA	Sinus wave 3.8MHz 400µV_{PP} on input		-45	-40	dB
LUMA- OUTPUT (with AGC)						
Z_{LPB}	Output Impedance	DC		30	50	Ω
V_{DCPB2}	DC Level		1.1	1.5	2.1	V
	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, AGC locked, 0dB at 3.8MHz				
F_{LCPB2}		Low			0.1	MHz
F_{HCPB2}		High	10	12.5		MHz
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1-SP, H2-SP, H1-LP, H2-LP	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1-SP, H2-SP, H1-LP, H2-LP	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1-SP, H2-SP, H1-LP, H2-LP		-44	-40	dB
CAGC						
I+	Positive Output Current	Input Signal 3.8MHz 200µV_{PP} on H1-SP	15	30	50	µA
I-	Negative Output Current	Input Signal 3.8MHz 200µV_{PP} on H1-SP	-50	-30	-15	µA
TRIV						
I_{TRIV}	Downloading Current		200	300	400	µA
V_{TRIV1}	Output Level (1)	With no signal, $V_{TRIVADJ}$ = 2.5V Mode LP (SW-M = high)	0.3	0.6	1	V
V_{TRIV2}	Output Level (2)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	1.91	2.31	2.71	V
V_{TRIV3}	Output Level (3)	V_{CHROMA} = 400mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	3.525	3.725	3.925	V
V_{TRIV4}	Output Level (4)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 1V, Mode LP (SW-M = high)	1.11	1.61	2.11	V
V_{TRIV5}	Output Level (5)	V_{CHROMA} = 100mV_{PP} at 4MHz $V_{TRIVADJ}$ = 4V, Mode LP (SW-M = high)	2.875	3.075	3.275	V
V_{TRIV6}	Output Level (6)	V_{CHROMA} = 400mV_{PP} at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode SP (SW-M = low)	3.215	3.415	3.615	V

5705-06.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA,LUMA-

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TRIV (continued)						
V_{TRIV7}	Output Level (7)	V_{CHROMA} = 100mV$_{PP}$ at 4MHz $V_{TRIVADJ}$ = 2.5V, Mode SP (SW-M = low)	1.65	2.05	2.45	V
f_{TRIV1}	Response Lower Frequency	V_{CHROMA} = 360mV$_{PP}$ at 4MHz and 1MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	-10	-6	-3	dB
f_{TRIV2}	Response Higher Frequency	V_{CHROMA} = 360mV$_{PP}$ at 8MHz and 4MHz $V_{TRIVADJ}$ = 2.5V, Mode LP (SW-M = high)	-2.5	-1	-0	dB
G_{TRIV}	High Level Input	LP : V_{CHROMA} = 100mV$_{PP}$, 300mV$_{PP}$ at 4MHz, $V_{TRIVADJ}$ = 2.5V	4	5.5	7	V/V
SP/LP ENVELOPE DETECTOR						
I_{DET+}	Current Output on Pin CSPLP	200µVPP on Pins H1-SP or H2-SP	25	55	85	µA
I_{DET-}	Current Output on Pin CSPLP	200µVPP on Pins H1-LP or H2-LP	-85	-55	-25	µA
V_{DETH}	Sensitivity 1 on Pin CSPLP	50µV$_{PP}$ to 600µV$_{PP}$ on SP, LP short circuited	4	4.5	5	V
V_{DETL}	Sensitivity 2 on Pin CSPLP	50µV$_{PP}$ to 600µV$_{PP}$ on LP, SP short circuited	0	0.5	1	V
V_{TH}	Upper Threshold on Pin VSPLP	Scanning through Pin CSPLP		3.33		V
V_{TL}	Lower Threshold on Pin VSPLP	Scanning through Pin CSPLP		1.66		V
R_{OH} R_{OL}	Output Resistance on Pin VSPLP	Output high Output low	7.5 1.5	12.5 2.5	17.5 3.5	kΩ kΩ

Record Mode

V_{REC} = 11.3V, V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}-SP, I_{OUT}-LP

Transconductance network defined by :

R1 = 18Ω, 1%	Pins GND/V_{MES}
R2-SP = 2kΩ, 1%	Pins V_{MES}/V_{IN}-SP
R2-LP = 1.5kΩ, 1%	Pins V_{MES}/V_{IN}-SP
R3-SP = 1.5kΩ, 1%	Pin V_{IN}- SP
R3-LP = 1.5kΩ, 1%	Pin V_{IN}- LP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 11.3V V_{CC} = 5V	17 30	25 43	33 56	mA mA
I_{max}	Max. Record Current on SP or LP Current Amplifier	3.8MHz	35			mA$_{PP}$
TR	Transconductance	V_{IN}-SP = 300mV$_{PP}$ V_{IN}-LP = 300mV$_{PP}$	55 45	74 55	85 65	mA/V mA/V
SH_{REC}	Second Harmonic	Output Current, 30mA$_{PP}$ at 3.8MHz at Pin I_{OUT}-SP at Pin I_{OUT}-LP		 -54 -54	 -38 -38	 dB dB
F_{LCRSP} F_{HCRSP}	Bandwidth Cut-off Frequency Pin I_{OUT}-SP	-3dB attenuation, 0dB at 3.8MHz Output current 30mA$_{PP}$ Low High	 10	 	 0.1 	 MHz MHz
V_{SPLPV}	DC Level at Pin VSPLP		4			V
F_{LCRLP} F_{HCRLP}	Bandwidth Cut-off Frequency Pin I_{OUT}-LP	-3dB attenuation, 0dB at 3.8MHz Output current 30mA$_{PP}$ Low High	 10	 	 0.1 	 MHz MHz
R_{VIN-SP} R_{VIN-LP}	Input Resistance on Pins V_{IN}-LP, V_{IN}-SP	Equivalent value of R3 resistor	500	700	900	Ω

5705-07.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified) (continued)

Switching Levels

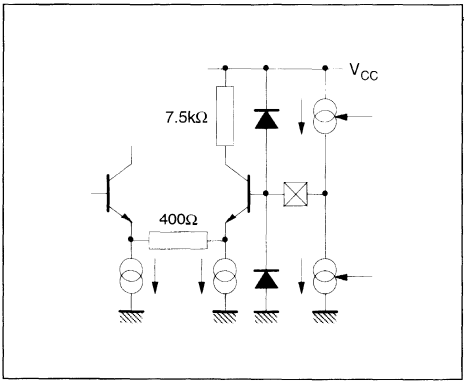
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWHH}	Head Selection Pin SW-H	Head number 1 in SP mode, 2 in LP mode	2.4		V_{CC}	V
V_{SWHL}		Head number 2 in SP mode, 1 in LP mode	0		1.5	V
I_{SWHH}		Input current (5V)	5	15	50	µA
I_{SWHL}		Output current (0V)	-50	-20	0	µA
V_{SWMH}	Mode Selection Pin SW-M (Record mode and play-back mode)	LP Mode	2.4		5	V
V_{SWML}		SP mode	0		1.5	V
I_{SWMH}		Input current (5V)	5	15	50	µA
I_{SWML}		Output current (0V)	-50	-20	0	µA
t_{ON} t_{OFF}	Selection Pin SW-H or SW-M Transient Response	Output signal appears on Pin CHROMA Delay time selection ON Delay time selection OFF		 100 100	 500 500	ns
V_{TH1}	Inhibition Threshold Hysteresis for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		10		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		32*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT}-SP, I_{OUT}-LP)		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT}-SP, I_{OUT}-LP)		11*		ms

5705-08.TBL

* Depending on capacitance on Pin V_{REC} ; above values are according to the application diagram at page 9.

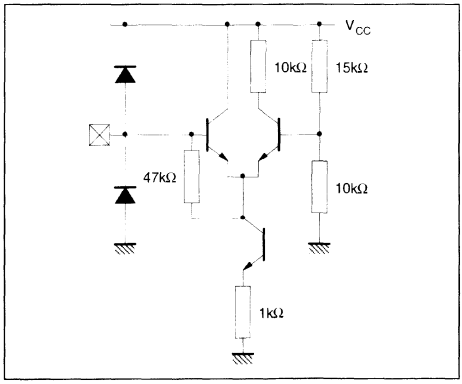
INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1-SP, C2-SP, C1-LP, C2-LP



5705-03.EPS

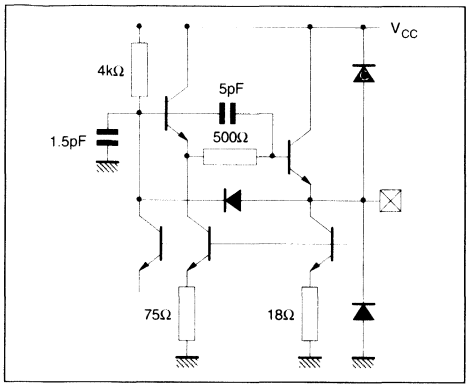
Pins : SW-H, SW-M



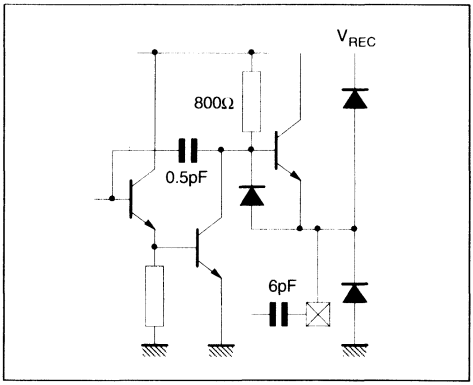
5705-04.EPS

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

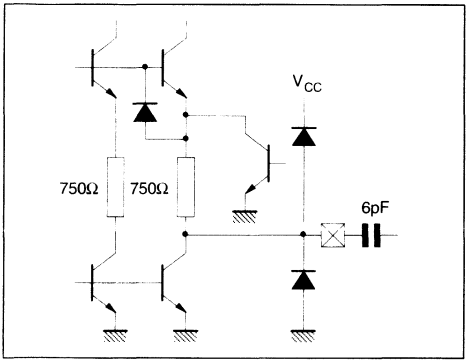
Pins : Chroma, Luma-



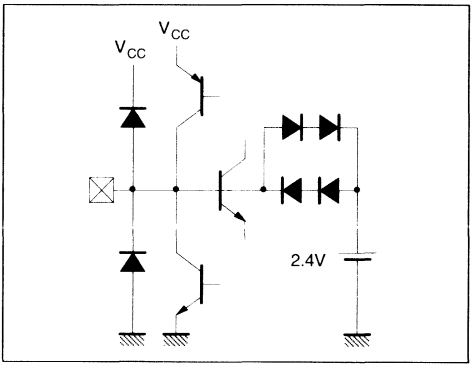
Pin : V_{MES}



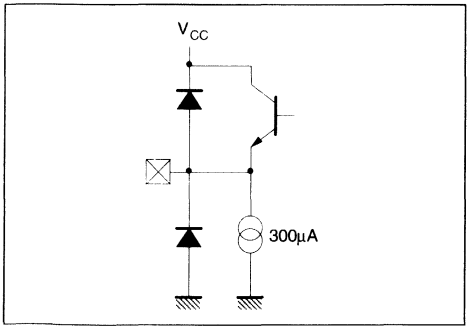
Pin : V_{IN}-SP, V_{IN}-LP



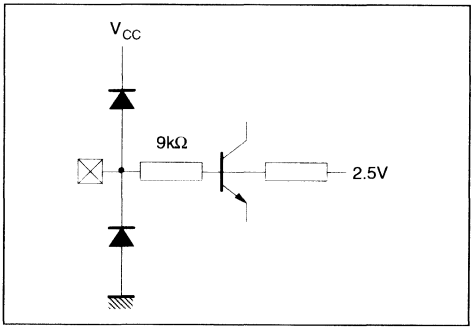
Pin : CAGC



Pin : TRIV

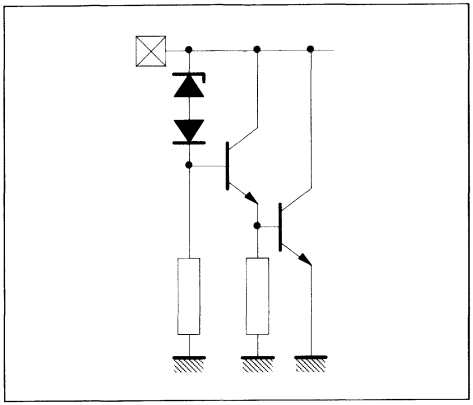


Pin : TRIVADJ

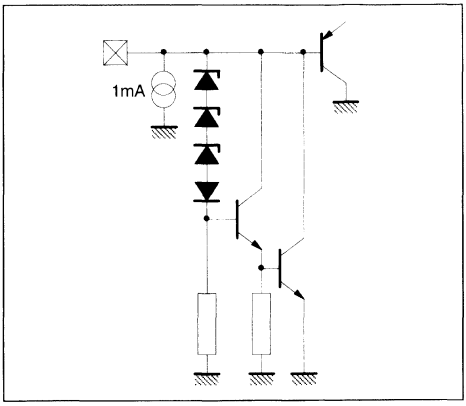


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

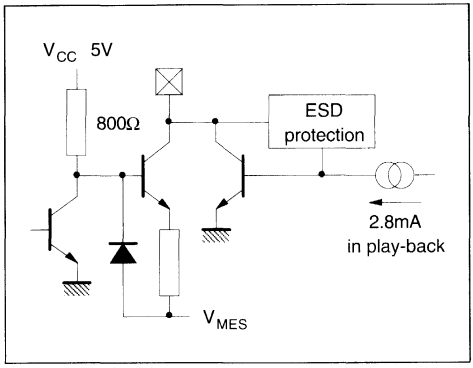
Pin : V_{CC}



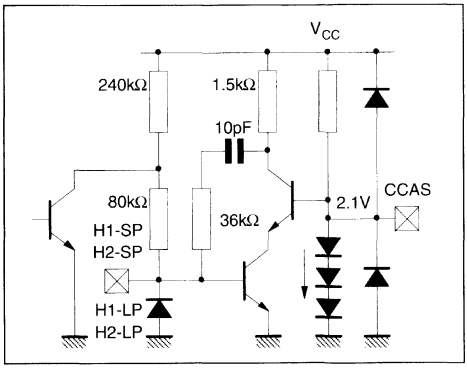
Pin : V_{REC}



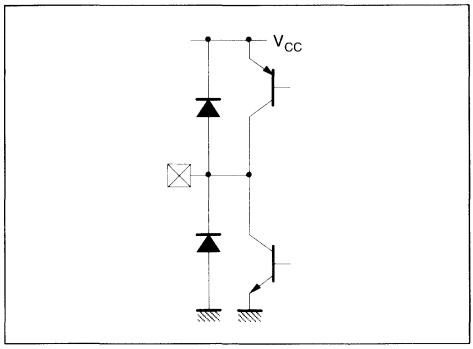
Pin : I_{OUT}-SP, I_{OUT}-LP



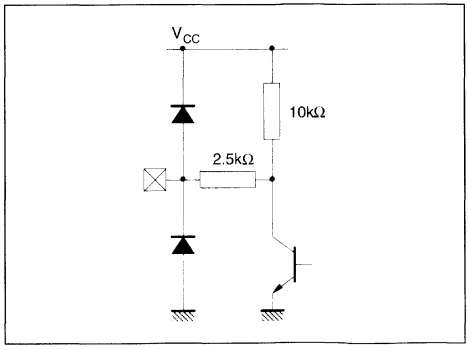
Pins : CCAS, H1-SP, H2-SP, H1-LP, H2-LP



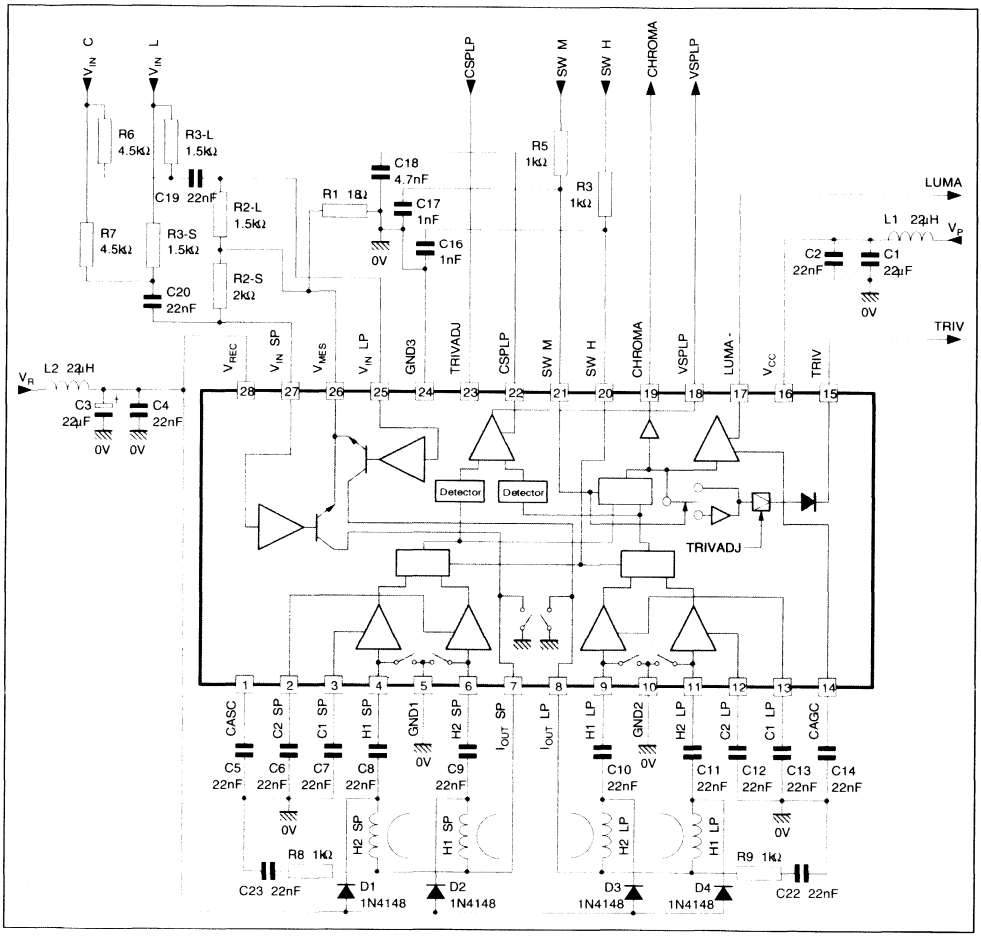
Pin : CSPLP



Pin : VSPLP



APPLICATION DIAGRAM



5705-17.EPS

SGS-THOMSON MICROELECTRONICS

TEA5706A

ADVANCED 4-HEAD PLAY-BACK AND RECORD AMPLIFIER FOR VCR

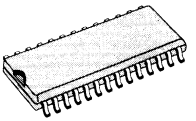
For complete specifications refer to "AUDIO POWER & PROCESSING ICs"

PLAY-BACK MODE

- LOW NOISE AND WIDE BAND AMPLIFIERS FOR 4 HEADS
- AUTOMATIC OFFSET CANCELLATION BETWEEN THE 2 SELECTED HEADS
- ONE PLAY-BACK OUTPUT WITHOUT AGC
- ONE PLAY-BACK OUTPUT INCLUDING AGC
- RECORD AMPLIFIER INHIBITION AND RECORD OUTPUT GROUNDED
- OUTPUT FOR TRACKING VIDEO INFORMATION (TRIV)
- SHORT PLAY/LONG PLAY ENVELOPE COMPARATOR WITH A SCHMIDT TRIGGER

RECORD MODE

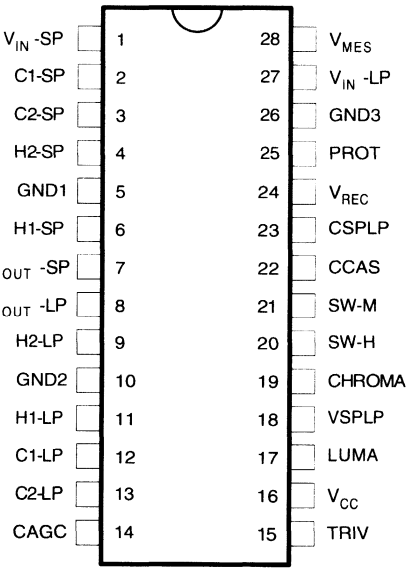
- TWO INTEGRATED I/I CONVERTERS WITH ACCURATE CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC PLAY-BACK/RECORD SWITCHING BY SCANNING OF RECORD SUPPLY
- PLAY-BACK LOOP INHIBITION
- RECORD AMPLIFIERS WITH AUTOMATIC PROTECTION AGAINST SHORT CIRCUIT



SO28 LARGE
(Plastic Micropackage)

ORDER CODE : TEA5706A

PIN CONNECTIONS



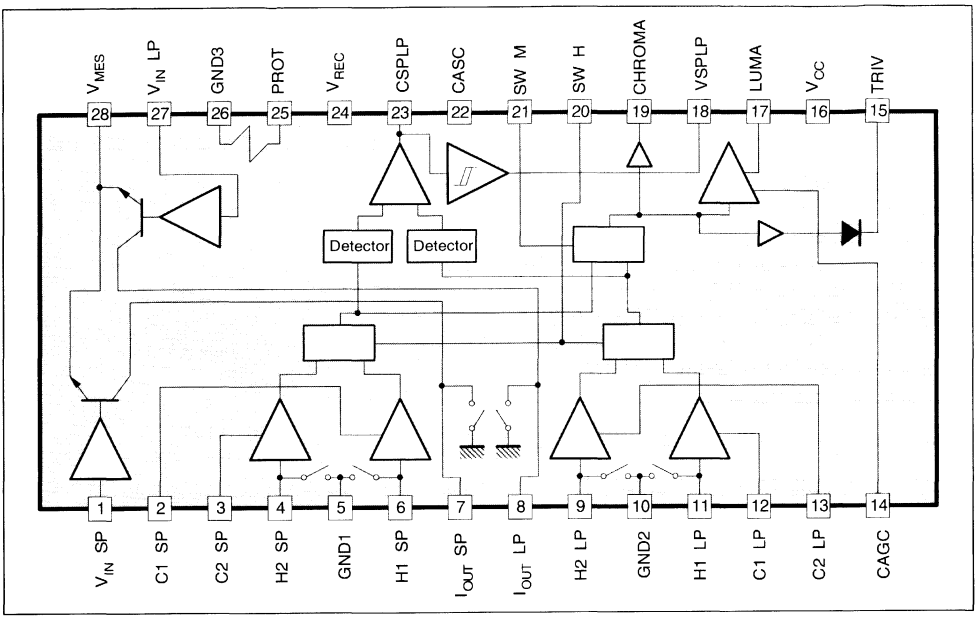
5706A-01.EPS

DESCRIPTION

The TEA5706A is an advanced four head record and play-back amplifier for VCR.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

TEA5706A is intended for 4 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and S-VHS applications (10MHz bandwidth).

High performance technology allows very low noise levels (current and voltage), which are frequency dependant in all the frequency range. In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5706A large capability to drive directly a coaxial cable in order to reduce number of external components.

Two play-back outputs are availabe : one, dedicated to Chroma processing, is a 60dB voltage amplifier output, the other, dedicated to Luma processing, has a constant AC output level of 200mV$_{PP}$ at 3.8MHz signal (phase is opposite to the chroma dedicated one).

A tracking information for video signal (TRIV) is Luma amplitude proportional and allows automatic phase correction.

An automatic scanning of record supply voltage permits TEA5706A automatically switching either in play-back or in record mode. The switching threshold voltage is fixed to a value which forbids high current peaking through the heads.

During play-back mode, record output is grounded via an internal transistor and during record mode preamplifiers are turned off.

There is one output current for two recording heads, the DC current and the AC characteristics can be very precisely controlled with accurate external resistors. If recommended resistances are used, a ± 5% transconductance accuracy is guaranteed.

Feedback loop gains of SP channel and LP channel can be different.

The recording amplifiers include a protection system which protexts the IC and the application board against overheating in case of short circuit on the recording transconductance components.

A particular feature is the SP/LP envelope comparator and detector. This system can be used in search mode, still mode, slow mode... The output signal is an output current feeding a capacitor (CSPLP) which is bufferised through a schmidt trigger circuit to VSPLP. This output is high in record mode. By varying the capacitance on CSPLP a good compromise can be found between short delay time and spike free signal.

TEA5706A is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	6	V
V_{REC}	Power Supply Voltage Record	15	V
T_J	Junction Temperature	+150	°C
T_{oper}	Operating Temperature	0, +70	°C

5706A-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance (Typ.)	70	°C/W

5706A-02.TBL

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	4.5	5	5.5	V
V_{REC}	Power Supply Voltage Record	4.75	9	12.6	V
CAGC	Capacitance at Pin CAGC	4.7			nF
CSPLP	Capacitance at Pin CSPLP		4.7		nF

5706A-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Power Consumption

Parameter		Play-Back		Record (1)	
		Typ.	Max.	Typ.	Max.
V_{CC}		60mA	75mA	40mA	55mA
V_{REC}		0mA	0mA	45mA	55mA
Total Consumption (2)	V_{CC} = 5V, V_{REC} = 9V	300mW		600mW	
	V_{CC} = 5.25V, V_{REC} = 9.45V		375mW		750mW

5706A-04.TBL

Notes : 1. R1 = 5.6Ω

2. Taking in account only the consumption through the IC.
A great care should be taken to the maximum power consumption : V_{REC} can be increased to 12.6V if the DC current flowing through the head is reduced. This can be done by increasing R1 value. V_{REC} can be reduced as long as voltage on Pins I_{OUT}-SP, I_{OUT}-LP is not going under 1V (to forbid output stage saturation).

Play-back Mode

V_{CC} = 5V, no load on Pins CHROMA, LUMA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC1}	Supply Current		45	60	75	mA
V_{CC}	Supply Voltage		4.75	5	5.25	V
CHROMA OUTPUT (no AGC)						
G_{PB}	Pre-amplification Gain	Sinewave 600 kHz 400mV$_{PP}$ on output Input on Pin H1-SP or H2-SP, H1-LP or H2-LP	56	60	62	dB
ΔG_{PB1}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in SP Mode	Sinewave 600kHz 0.4mV$_{PP}$ on inputs H1-SP and H2-SP			1.2	dB
ΔG_{PB2}	Difference of Output Signal on Pin CHROMA between Channel 1 and Channel 2 in LP Mode	Sinewave 600kHz 0.4mV$_{PP}$ on inputs H1-LP and H2-LP			1.2	dB

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ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)
Play-back Mode (V_{CC} = 5V, no load on Pins CHROMA, LUMA)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CHROMA OUTPUT (no AGC) (continued)						
e_N	Equivalent Input Voltage Noise Level	Input grounded via switching transistor on Pins H1-SP, H2-SP, H1-LP, H2-LP, f = 600kHz		0.6	0.85	nV/√Hz
i_N	Equivalent Input Current Noise	Pins H1-SP, H2-SP, H1-LP, H2-LP		2	2.8	pA/√Hz
CRT	Crosstalk	Sinewave 3.8MHz 400µV_{PP}, All switches combinated			-40	dB
	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, 0dB at 600kHz				
F_{LCPB1}		Low			0.1	MHz
F_{HCPB1}		High	8			MHz
C_{IN}	Input Capacitance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 5MHz		30	40	pF
R_{IN}	Pre-amplifier Input Resistance Pins H1-SP, H2-SP, H1-LP, H2-LP	At 3.8MHz	400	600	900	Ω
Z_{CPB}	Output ImpedancePin CHROMA	Sinus wave 600kHz 400µV_{PP} on input		30	50	Ω
V_{CPB}	DC Level at Play-back Output on Pin CHROMA		1.5	1.9	2.5	V
	Head Switch Offset Pin CHROMA					
ΔV_{CPBS}					100	mV
ΔV_{CPBL}					100	mV
SH_{PB1}	Second Harmonic Play-back Output Pin CHROMA	Sinus wave 3.8MHz 400µV_{PP} on input with load 500Ω//100pF		-45	-40	dB
LUMA OUTPUT (with AGC)						
Z_{LPB}	Output Impedance	DC		30	50	Ω
V_{DCPB2}	DC Level		0.8	1.4	2	V
	Bandwidth Cut-off Frequency	-3dB attenuation 50Ω in parallel on the input, AGC locked, 0dB at 3.8MHz				
F_{LCPB2}		Low			0.1	MHz
F_{HCPB2}		High	10	12		MHz
V_{LPB}	Output Amplitude	Input signal 200µV_{PP} at 3.8MHz on Pins H1-SP, H2-SP, H1-LP, H2-LP	140	200	270	mV_{PP}
ΔV_{LPB}	AGC Control Sensitivity	Input signal 200µV_{PP} at +6dB or -5dB on Pins H1-SP, H2-SP, H1-LP, H2-LP	-2		+1	dB
SH_{PB2}	Second Harmonic Play-back Output	Input Signal 3.8MHz 400µV_{PP} on Pins H1-SP, H2-SP, H1-LP, H2-LP with load 500Ω//100pF		-42	-35	dB
CAGC						
I+	Positive Output Current	Input Signal 3.8MHz 200µV_{PP} on H1-SP	15	30	45	µA
I-	Negative Output Current	Input Signal 3.8MHz 200µV_{PP} on H1-SP	-45	-30	-15	µA
TRIV						
R_{TRIV}	Downloading Resistance		20	40	80	kΩ
V_{TRIV1}	Output Level	V_{CHROMA} = 0mV_{PP}	0		1.2	V
V_{TRIV3}		V_{CHROMA} = 400mV_{PP} at 4.5MHz	2.6	3	3.4	V
V_{TRIV4}		V_{CHROMA} = 600mV_{PP} at 4.5MHz	3.3	3.7	4.1	V
V_{TRIV5}		V_{CHROMA} = 800mV_{PP} at 4.5MHz	3.6	4.2	4.5	V
G_{TRIV1}	Gain	V_{CHROMA} = 0mV_{PP}, 400mV_{PP} at 4.5MHz		7.5		V/V_{PP}
G_{TRIV2}		V_{CHROMA} = 400mV_{PP}, 600mV_{PP} at 4.5MHz		3.5		V/V_{PP}

ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)
Play-back Mode (V_{CC} = 5V, no load on Pins CHROMA, LUMA)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SP/LP ENVELOPE DETECTOR						
I_{DET+}	Current Output on Pin CSPLP	200µV_{PP} on Pins H1-SP or H2-SP	25	50	75	µA
I_{DET-}	Current Output on Pin CSPLP	200µV_{PP} on Pins H1-LP or H2-LP	-75	-50	-25	µA
V_{DETH}	Sensitivity 1 on Pin CSPLP	50µV_{PP} to 600µV_{PP} on SP, LP short circuited	4	4.5	5	V
V_{DETL}	Sensitivity 2 on Pin CSPLP	50µV_{PP} to 600µV_{PP} on LP, SP short circuited	0	0.5	1	V
V_{TH}	Upper Threshold on Pin VSPLP	Scanning through Pin CSPLP		3.33		V
V_{TL}	Lower Threshold on Pin VSPLP	Scanning through Pin CSPLP		1.66		V
R_{OH} R_{OL}	Output Resistance on Pin VSPLP	Output high Output low	7.5 1.5	12.5 2.5	17.5 3.5	kΩ kΩ

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Record Mode

V_{REC} = 9V, V_{CC} = 5V, Load resistor 50Ω on Pin I_{OUT}-SP, I_{OUT}-LP
Transconductance network defined by : R1 = 5.6Ω, 1% Pins PROT/V_{MES}
R2-SP = 2kΩ, 1% Pins V_{MES}/V_{IN}-SP
R2-LP = 1.5kΩ, 1% Pins V_{MES}/V_{IN}-SP
R3-SP = 1.5kΩ, 1% Pin V_{IN}- SP
R3-LP = 1.5kΩ, 1% Pin V_{IN}- LP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{REC} I_{CC2}	Current Supply	V_{REC} = 9V V_{CC} = 5V		45 40	55 55	mA mA
I_{max}	Max. Record Current on SP or LP Current Amplifier	3.8MHz	65			mA_{PP}
TR	Transconductance	V_{IN}-SP = 300mV_{PP} V_{IN}-LP = 300mV_{PP}	180 150	230 180	280 210	mA/V mA/V
SH_{REC}	Second Harmonic	Output Current, 30mA_{PP} at 3.8MHz at Pin I_{OUT}-SP at Pin I_{OUT}-LP		 -50 -50	 -38 -38	 dB dB
F_{LCRSP} F_{HCRSP}	Bandwidth Cut-off Frequency Pin I_{OUT}-SP	-3dB attenuation, 0dB at 3.8MHz Output current 30mA_{PP} Low High	 10		 0.1	 MHz MHz
V_{SPLP}	DC Level at Pins CSPLP and VSPLP		4			V
F_{LCRLP} F_{HCRLP}	Bandwidth Cut-off Frequency Pin I_{OUT}-LP	-3dB attenuation, 0dB at 3.8MHz Output current 30mA_{PP} Low High	 10		 0.1	 MHz MHz
I_{PROT}	Maximum Input Current on Pin PROT	5V on Pin V_{MES}	150	250	400	mA
V_{SAT}	Maximum Saturation Voltage on Pin V_{MES}	Input current 80mA		50	150	mV
R_{VINLP} R_{VINSP}	Input Resistance on Pins V_{IN}-LP, V_{IN}-SP	Equivalent value of R3 resistor	500	700	900	Ω

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ELECTRICAL OPERATING CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Switching Levels

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SWHH}	Head Selection Pin SW-H	Head number 1 in SP mode, 2 in LP mode (high level)	2.4		V_{CC}	V
V_{SWHL}		Head number 2 in SP mode, 1 in LP mode (low level)	0		1.5	V
I_{SWHH}		Input current (high level)		20	50	µA
I_{SWHL}		Output current (low level)		20	50	µA
V_{SWMH}	Mode Selection Pin SW-M (Record mode and play-back mode)	LP Mode (high level)	2.4		5	V
V_{SWML}		SP mode (low level)	0		1.5	V
I_{SWMH}		Input current (high level)		20	50	µA
I_{SWML}		Output current (low level)		20	50	µA
t_{ON}	Selection Pin SW-H or SW-M Transient Response	Delay time selection ON (output signal appears on Pin CHROMA)		250	1000	ns
t_{OFF}		Delay time selection OFF (output signal disappears on Pin CHROMA)		250	1000	ns
V_{TH1}	Inhibition Threshold for Switching from Play-back to record on Pin V_{REC}	V_{CC} = 5V	0.15	0.3	0.5	V
V_{TH2}	Inhibition Threshold Hysteresis for Switching from Record to Play-back on Pin V_{REC}	V_{CC} = 5V		80		mV
t_1	Transient Response of Record Scanning on Pin V_{REC}	Delay from play-back to record (signal disappears on Pin CHROMA)		30		µs
t_2		Delay from record to play-back (signal appears on Pin CHROMA)		35*		ms
t_3		Delay from play-back to record (signal appears on Pin I_{OUT}-SP, I_{OUT}-LP)		0.2		ms
t_4		Delay from record to play-back (signal disappears on Pin I_{OUT}-SP, I_{OUT}-LP)		8*		ms

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* Depending on capacitance on Pin V_{REC}.

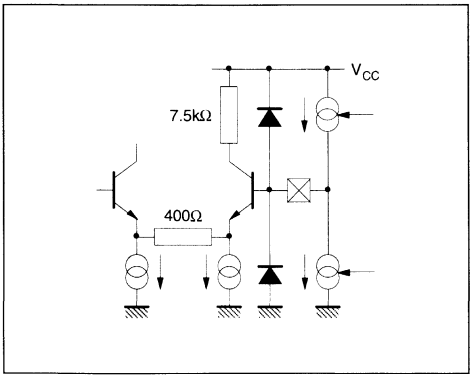
Power Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SVR	Supply Voltage Rejection	0.5mV_{PP} on Pin V_{CC}, 75µV_{PP} on Pin H1-SP, H2-SP, H1-LP, H2-LP, Measurement on Pin Chroma	15	20		dB

5706A-10.TBL

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

Pins : C1-SP, C2-SP, C1-LP, C2-LP



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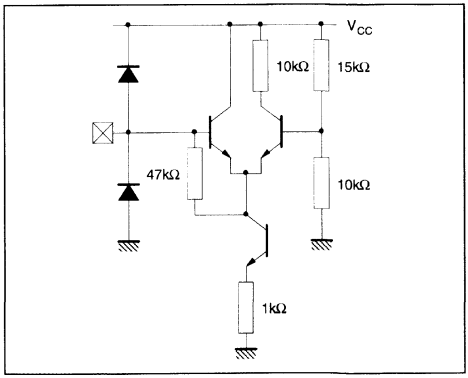
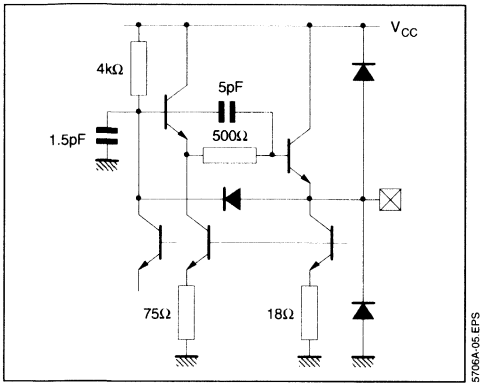
Pins : SW-H, SW-M



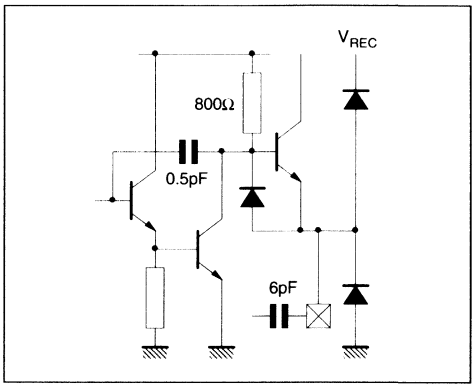
5706A-04.EPS

INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

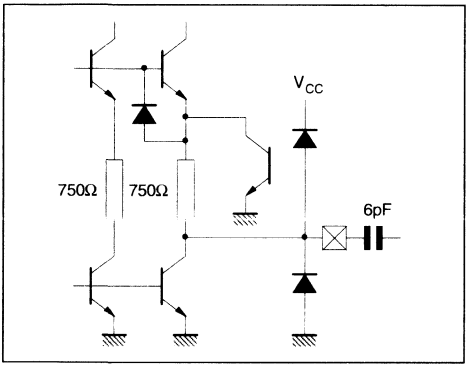
Pins : Chroma, Luma



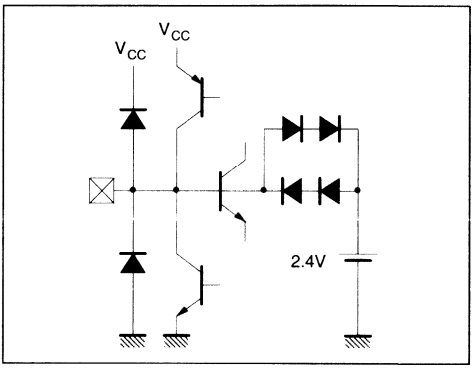
Pin : V_{MES}



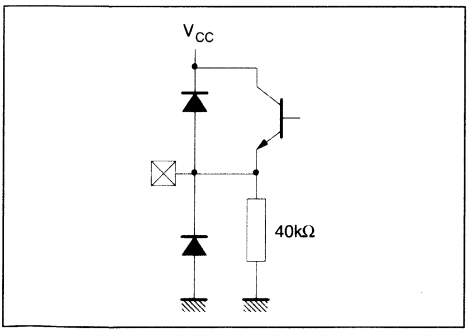
Pin : V_{IN}-SP, V_{IN}-LP



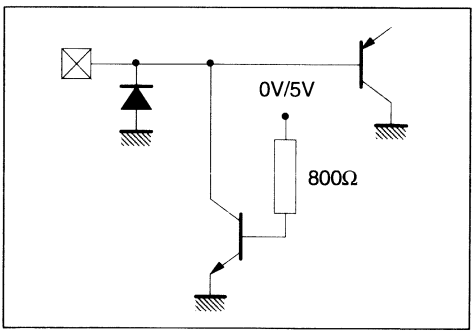
Pin : CAGC



Pin : TRIV

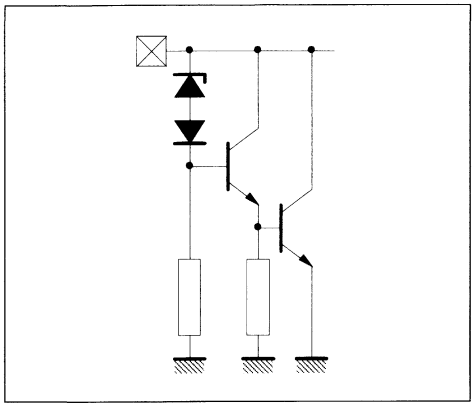


Pin : PROT

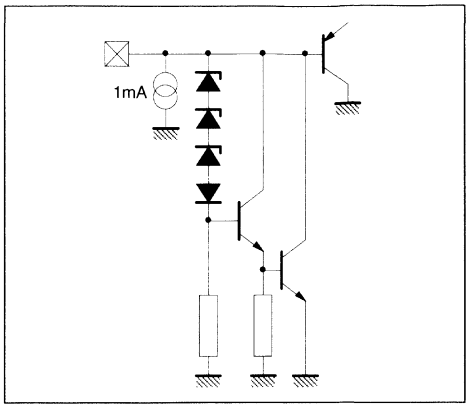


INPUT/OUTPUTS EQUIVALENT INTERNAL DIAGRAM (continued)

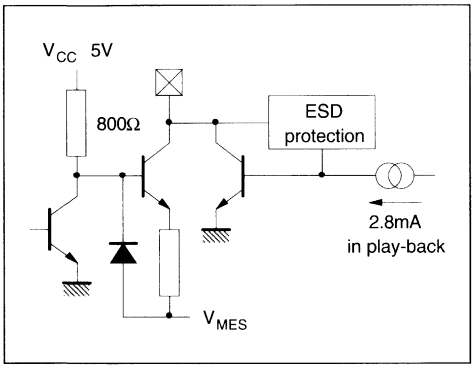
Pin : V_{CC}



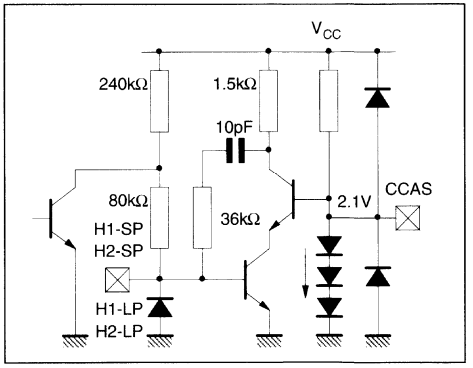
Pin : V_{REC}



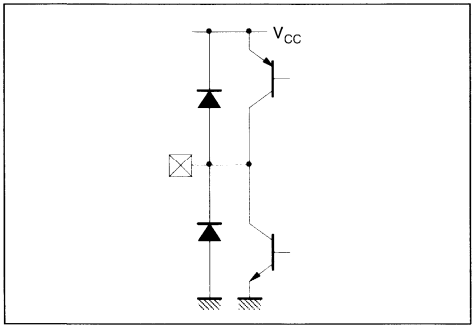
Pin : I_{OUT}-SP, I_{OUT}-LP



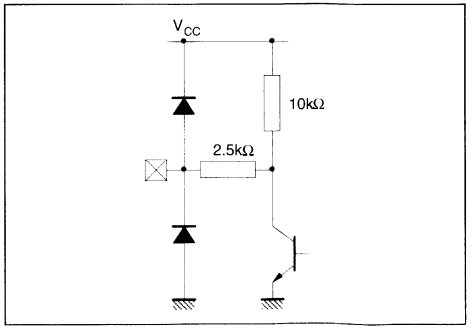
Pins : CCAS, H1-SP, H2-SP, H1-LP, H2-LP



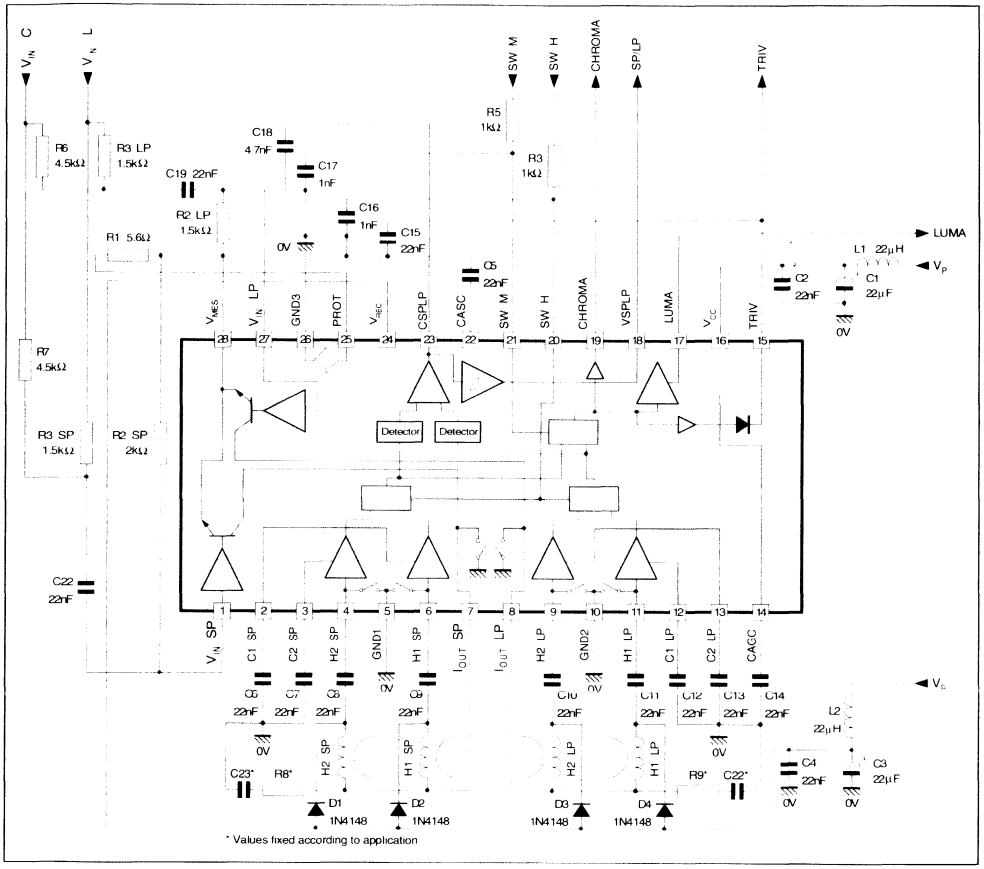
Pin : CSPLP



Pin : VSPLP



TYPICAL APPLICATION



TELETEXT DECODER

SGS-THOMSON MICROELECTRONICS

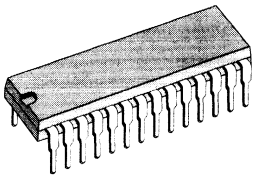
SAA5231

DATA SLICER FOR TELETEXT PROCESSOR

- SEPARATION OF TELETEXT DATA FROM THE COMPOSITE VIDEO SIGNAL
- SEPARATION OF HORIZONTAL AND VERTICAL SYNCHRONIZATION SIGNALS FROM THE COMPOSITE VIDEO SIGNAL
- EXTERNAL OSCILLATOR GENERATING 6MHz SIGNAL SYNCHRONIZED TO A MULTIPLE OF THE LINE FREQUENCY BY PLL
- A 6.9375MHz CLOCK GENERATED FROM AN EXTERNAL QUARTZ CRYSTAL
- "AFTER-HOURS" SYNCHRONIZATION OPTION
- PROGRAMMABLE LEVELS FOR THE INPUT COMPOSITE VIDEO SIGNAL (1V OR 2.5V)
- PROCESSING OF EXTERNAL TELETEXT DATA
- OUTPUT OF POSITIVE OR NEGATIVE SYNCHRONIZING SIGNALS
- 28 PIN DIP PACKAGE
- HDS2P2 TECHNOLOGY

DESCRIPTION

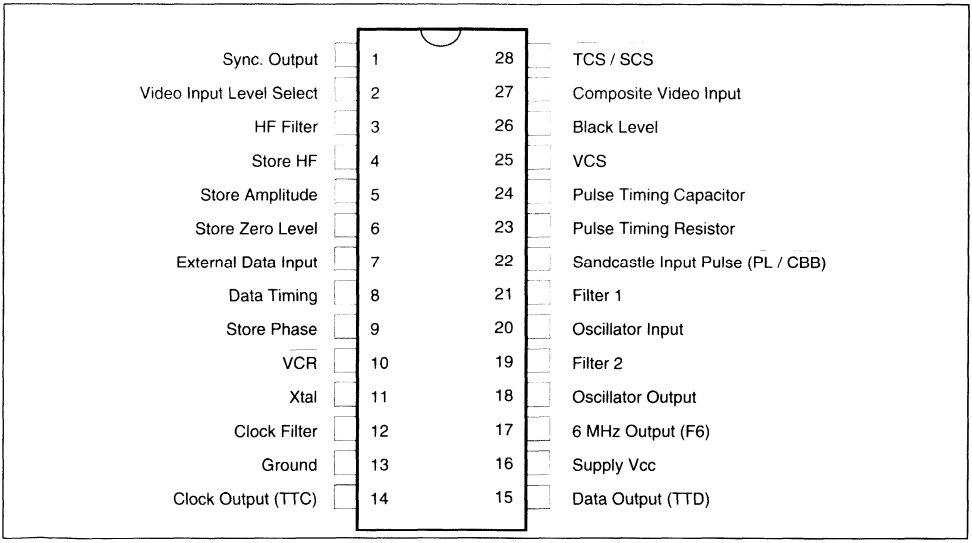
The SAA5231 is a monolithic integrated circuit in 28 Pin DIP package designed to separate Teletext signals from TV signal.



DIP28
(Plastic Package)

ORDER CODE : SAA5231

PIN CONNECTIONS



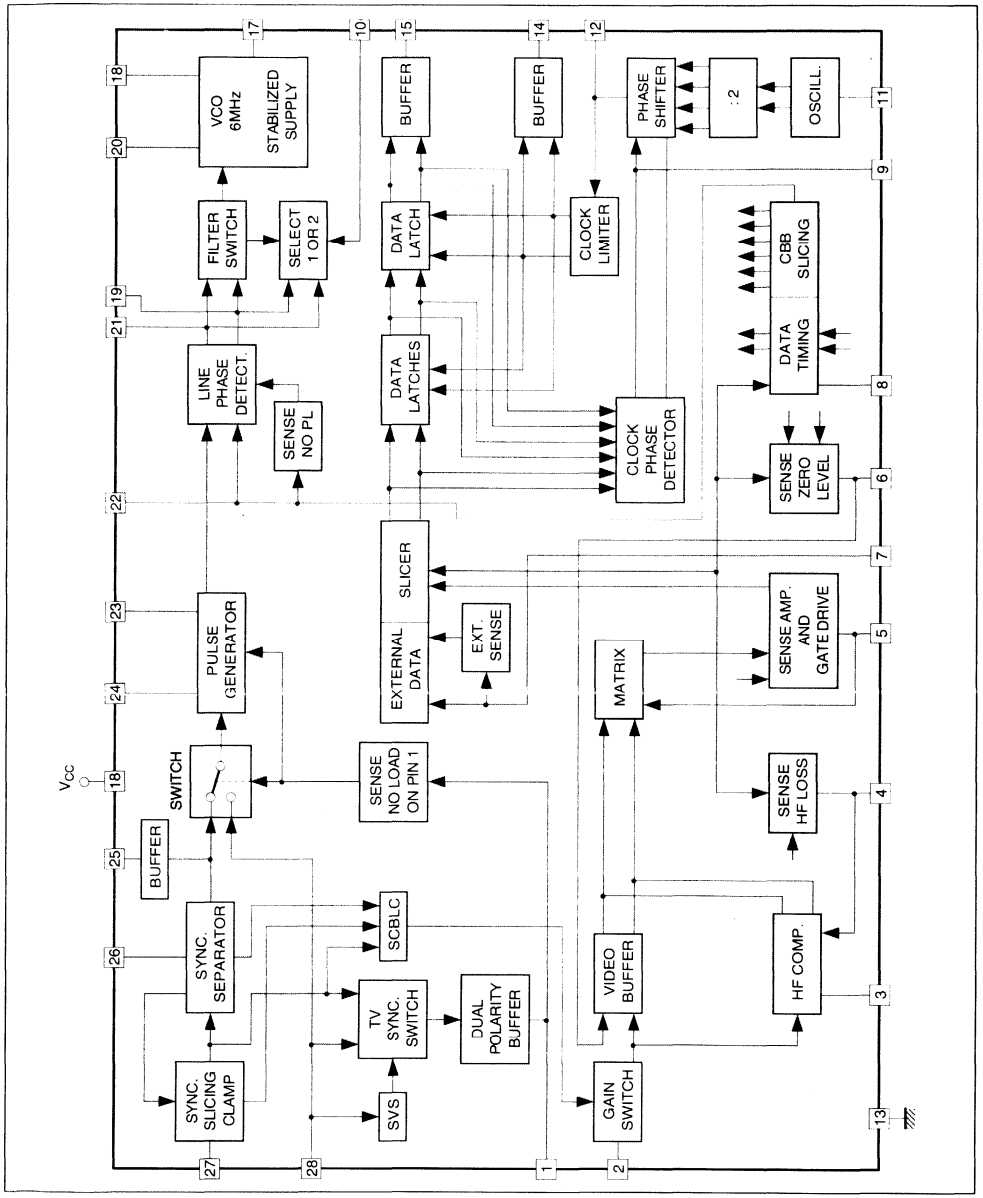
5231-01.EPS

PIN DESCRIPTION

Pin	Function	Description
1	Display Synchronization Outputs	Synchronization signal output available as positive or negative
2	Input video signal level	Input level selected as 1V (Pin 2 low) or 2.5V (Pin 2 not connected)
3	H.F. filter	Video signal filtering using an external capacitor of 15pF
4-5-6	"Store HF" "Store amplitude" "Store zero level"	Three external capacitors used to store : 1/ HF amplitude 2/ Amplitude of adaptative data slicer 3/ Zero level
7	External data input	"Teletext data slice" input from external circuit
8	Data timing	Connection of an external 270pF capacitor for the timing of the adaptative data slicer
9	Store phase	Storage on an external capacitor of the output signal "Clock phase detector"
10	"Video Tape Recorder" mode ($\overline{VCR}$)	Control signal for the PLL in the low-time constant mode
11	Crystal	External connection for a 13.875MHz crystal. This frequency, divided by 2, yields the 6.9375MHz cloc
12	Clock filter	Filter for 6.9375MHz clock
13	Ground	
14	Teletext clock output	Clock output for the SDA5243
15	Teletext data output	Output of Teletext data for the SDA5243
16	Supply V_{CC}	
17	6MHz clock output	6MHz clock output for the SDA5243
18/20	Oscillator output/input	An external resonant circuit between Pins 18 and 20 is connected to the 6MHz internal V_{CO}
19	Filter 2	Low time constant filter for phase detection of the horizontal signal
21	Filter 1	High time constant filter for phase detection of the horizontal signal
22	"Sandcastle" input pulse	Input of the sandcastle signal produced by the SDA5243 from the PL and CBB signals
23	Pulse timing resistor	External resistor of 68 kohms used to define the current for the pulse generator
24	Pulse timing capacitor	External capacitor of 270pF to define the timing of the pulse generator
25	Composite video synchronizing output (VCS)	Synchronizing output for the SDA5243
26	Black level	Storage of the black level for the adaptive sync. Separator on an external 68nF capacitor
27	Composite video input	Composite video signal input for the adaptive sync. Separator via an external capacitor of 2.2µF
28	Teletext composite sync. input ($\overline{TCS}$) or Scan composite sync. input ($\overline{SCS}$)	$\overline{TCS}$ input from the SDA5243 or $\overline{SCS}$ input from an alternative synchronizing circuit.

5231-01 TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{16}	Supply Voltage	13.2	V
$-I_{25}$	Output Current VCS	5	mA
$-I_{15}$	Output Current TTD	10	mA
$-I_{14}$	Output Current TTC	10	mA
$-I_{17}$	Output Current F6	10	mA
I_1	Output Current Sync.	5	mA
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Junction	0, +150	°C
T_{amb}	Ambient Temperature	0, +70	°C

5231-02 TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-Ambient	Max.	70	°C/W

5231-03 TBL

ELECTRICAL CHARACTERISTICS (V_S = 12 V , T_A = 25°C , unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
POWER SUPPLY (Pin 16)					
V_S	Supply Voltage	10.8	12	13.2	V
I_S	Supply Current		70		mA
CVBS INPUT (Pin 27)					
V_{27}	Input Signal Level Pin 2 to ground Pin 2 open	 0.7 1.75	 1 2.5	 1.4 3.5	 v v
$V_{27(p-p)}$	Synchronism Signal Amplitude	0.1	-	1	V
$V_{27(txt)}$	Teletext Data Level Pin 2 to ground Pin 2 open	 0.3 0.75	 0.46 1.15	 0.7 1.75	 v v
R_{G27}	Generator Resistance			250	Ω
VIDEO INPUT LEVEL SELECT (Pin 2)					
V_{2L}	Low Voltage (V_{27} = 1V)	0		0.8	V
V_{2H}	High Voltage (V_{27} = 2.5V)	2		5.5	V
$-I_{2L}$	Low Current	0		150	µA
I_{2H}	High Current	0		1.3	mA
TELETEXT DATA (Pin 5)					
$V_{15(p-p)}$	Signal TTD Output	2.5	3.5	4.5	V
t_r , t_f	Transition Times	20	30	45	ns
C_{15}	Load Capacitance			40	pF
V_{15DC}	DC Voltage at Output		4		V
DATA CLOCK (Pin 14)					
$V_{14(p-p)}$	Signal TTC	2.5	3.5	4.5	V
t_r , t_f	Transition Times	20	30	45	ns
C_{14}	Load Capacitance			40	pF
t_D	Time Deviation with Respect to TTD	-20	0	20	ns
V_{14DC}	DC Voltage at Output		4		V
SYNC. PULSE SEPARATION VCS (to SDA5243) (Pin 25)					
V_{25L}	Low Output Voltage	0		0.4	V
V_{25H}	High Output Voltage	2.1		5.5	V

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ELECTRICAL CHARACTERISTICS (V_S = 12 V , T_A = 25°C ,unless otherwise specified) (continued)

Symbol	Parameter	Min	Typ	Max	Unit
SYNC. PULSE SEPARATION VCS (to SDA5243) (Pin 25)					
I_{25L}	Low Output Current			0.5	mA
$-I_{25H}$	HighOutput Current			1.5	mA
t_D	Delay with respect to CVBS sync.		0.5		µs
SYNC. OUTPUT DRIVER (to TV set) (Pin 1)					
$V_{1(p-p)}$	Output Voltage TCS Operation CVBS Operation		0.45	 1	 V V
V_{1DC}	DC voltage with load resistor to ground (positive synchronous signal)		1.4		V
$-I_1$	Output Current			3	mA
V_{1DC}	DC voltage with load resistor to V_S (negative synchrononous signal)		10.1		V
I_1	Output Current			3	mA
6MHz CLOCK F6 (Pin 7)					
$V_{17(p-p)}$	F6 Output Signal (negligible harmonic content)	1	2	3	V
t_r , t_f	Transition Times	20		40	ns
C_{17}	Load Capacitance			40	pF
V_{17DC}	DC Voltage	4		8.5	V
SYNCHRONIZATION SELECTION (Pin 28)					
$-I_{28}$	Input Current TCS Operation (V_{28} = 0 to 7 V)	40	70	100	µA
I_{28}	Input Current CVBS Operation (V_{28} = 10 to V_S)	-5	0	5	µA
V_{28L}	Low Input voltage (TCS operation) (load resistor at Pin 1)	0		0.8	V
V_{28H}	High Input voltage (TCS operation) (load resistor at Pin 1)	2		6.1	V
V_{28L}	Low Input Voltage (SCS operation) (Pin 1 open)	0		1.5	V
V_{28H}	High Input Voltage (SCS operation) (Pin 1 open)	3.5		6.1	V
t_p	Line Synchronous Pulse Width TCS Operation SCS Operation		 2 3		 µs µs
VCR OPERATION (Pin 10)					
V_{10L}	Low Input Voltage VCR Operation	0		0.8	V
V_{10H}	High Input Voltage Standard Operation	2		V_S	V
I_{10}	Input Current	-10	0	10	A
SANDCASTLE PULSE INPUT (Pin 22)					
V_{22L}	Phase Locked Mode Input Low Voltage PL	0		3	V
V_{22H}	Phase Locked Mode Input High Voltage PL	3.9		5.5	V
t_{pl}	PL - low time for free-wheeling oscillator	100			ms
V_{22L}	Reset Pulse for Data Separation Input Low Voltage CBB	0		0.5	V
V_{22H}	Reset Pulse for Data Separation Input High Voltage CBB	1		5.5	V
I_{22}	Input Current	-10		10	µA
EXTERNAL DATA INPUT (CURRENT SOURCE DRIVING) (Pin 7)					
	Internal Data Processing Input				
I_7	Current	-10	0	100	µA
V_7	Voltage (I_7 = -10 to 100µA)		10		V
	External Data Processing Input				
I_{7L}	Current for low Level	-175	-40	-25	µA
I_{7H}	Current for High Level	-1000	-500	-325	µA
V_7	Voltage (I_7 = -1000 to -25µA)	7	8		V

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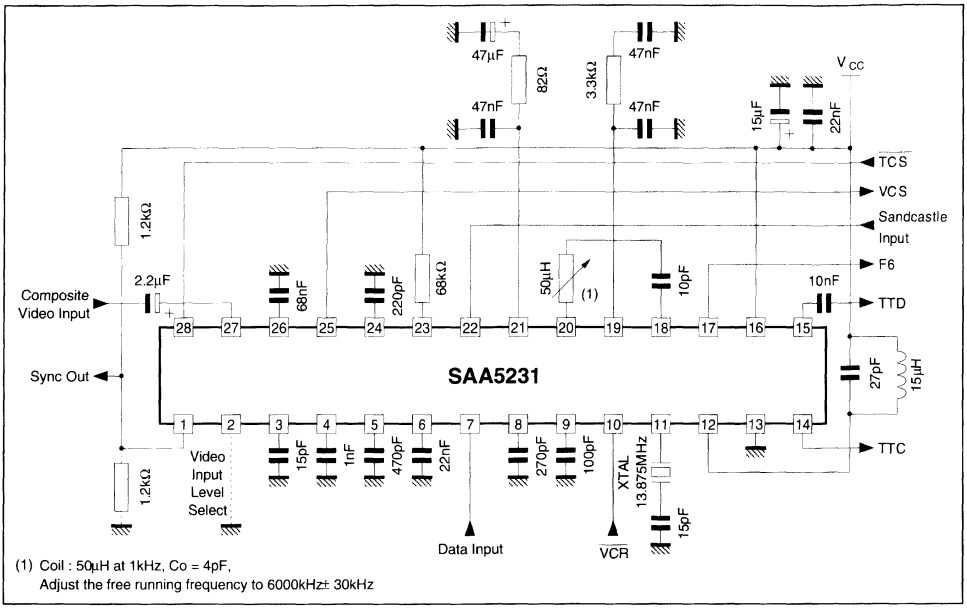
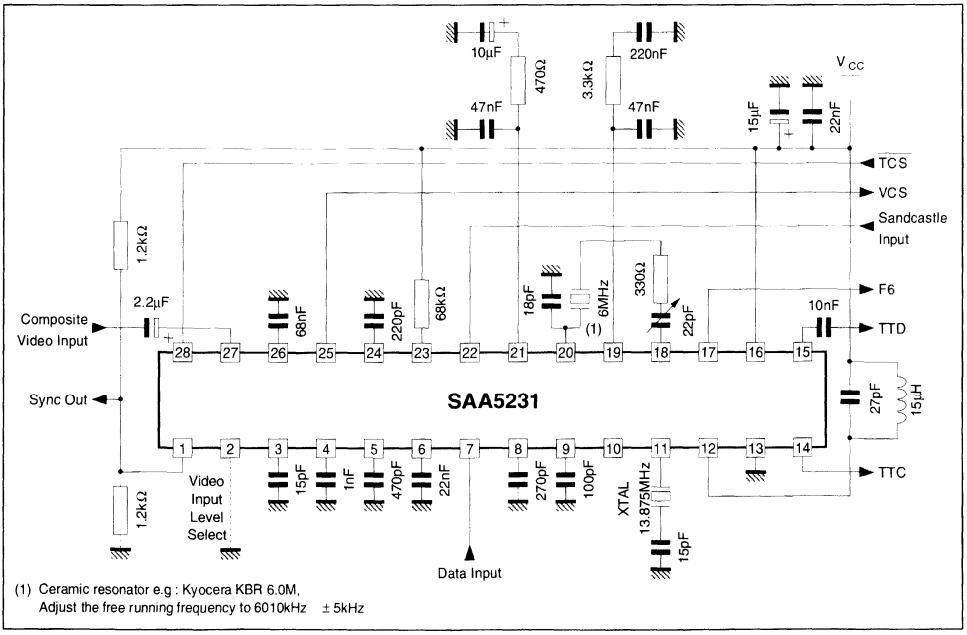
APPLICATION DIAGRAMS

Figure 1a : Application Diagram with LC Circuit in 6MHz PLL



(1) Coil : 50µH at 1kHz, Co = 4pF,
Adjust the free running frequency to 6000kHz± 30kHz

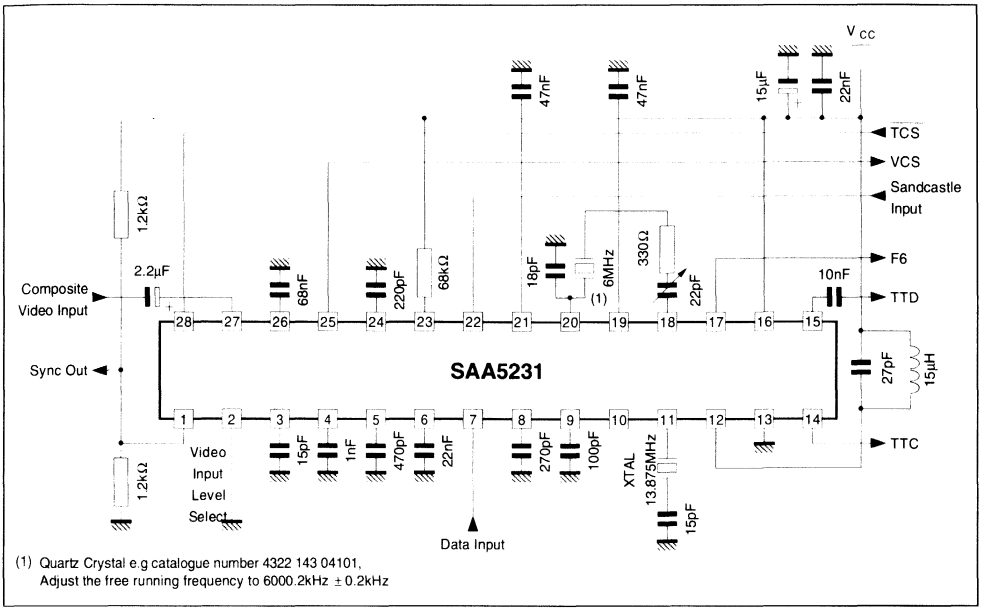
Figure 1b : Application Diagram with Ceramic Resonator in 6MHz PLL



(1) Ceramic resonator e.g : Kyocera KBR 6.0M,
Adjust the free running frequency to 6010kHz ± 5kHz

APPLICATION DIAGRAMS (continued)

Figure 1c : Application Diagram with Quartz Crystal in 6MHz PLL

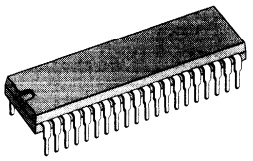


SGS-THOMSON MICROELECTRONICS

SDA5243
SDA5243/H

COMPUTER-CONTROLLED TELETEXT DECODER

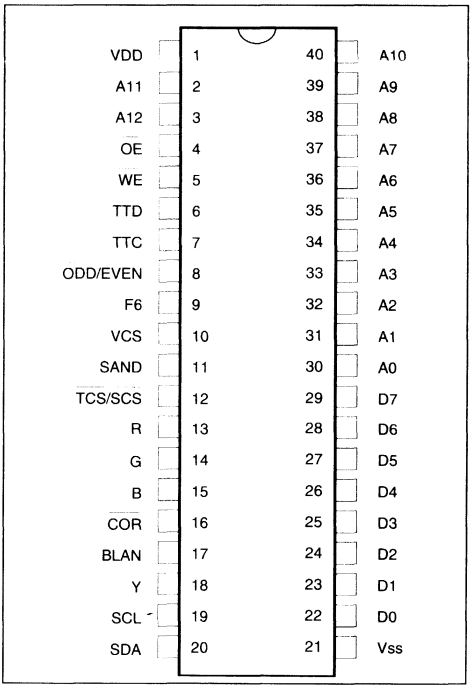
- AUTOMATIC SELECTION OF UP TO SEVEN NATIONAL LANGUAGES
- FOUR SIMULTANEOUS PAGE REQUESTS
- DISPLAY OF THE 25TH STATUS ROW
- MICROPROCESSOR CONTROL VIA AN I^2C BUS (SLAVE ADDRESS 0010001 R/$\overline{W}$)
- DATA ACQUISITION AVAILABLE FROM LINES 2 TO 22 OR FROM A COMPLETE FIELD.
- DIRECT INTERFACE TO A STATIC RAM OF UP TO 8kBYTES
- HIGH QUALITY DISPLAY USING A CHARACTER MATRIX OF 12 x 10 DOTS.
- SINGLE + 5V SUPPLY VOLTAGE
- ON-CHIP MASK PROGRAMMABLE ROM CHARACTER GENERATORS
- NMOSH2 PROCESS



DIP40
(Plastic Package)

ORDER CODES :
SDA5243 - West European Languages
SDA5243/H - East European Languages

PIN CONNECTIONS



5243-01.EPS

DESCRIPTION

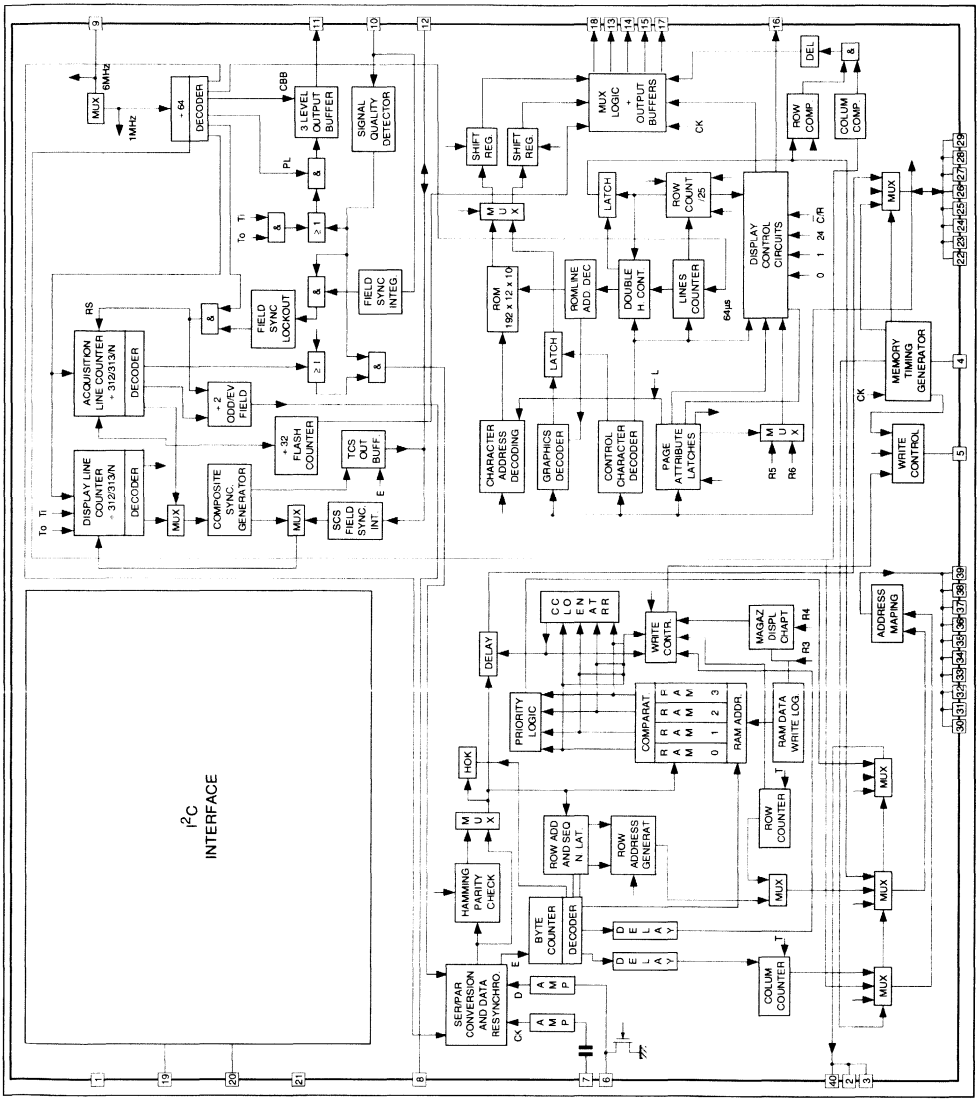
The SDA5243 is a NMOSH2 integrated circuit which performs all the processing of logical data within a 625 line system teletext decoder. It is designed to operate in conjunction with at least two chips : the SAA5231 integrated chip which extracts Teletext information embedded in a composite video signal and up to eight kilobytes of static RAM memory which can be used to store a maximum of 8 pages of display data. A complete system also comprises a microprocessor controling the SDA5243 via a 2-wire serial bus. An on-chip ROM memory contains the character sets. The SDA5243 performs automatic selection of one of up to seven natural languages. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

PIN DESCRIPTION

Pin	Symbol	Function	Description
1	V_{DD}	+5V	Positive supply voltage
2, 3, 40	A11, A12, A10	Chapter address	Address selection outputs for 1 of 8 static RAM chapters each of 1 kBytes.
4	$\overline{OE}$	Output enable	Active-low RAM output enable control signal.
5	$\overline{WE}$	Write enable	Active-low RAM write enable control signal. It supports write-cycles interleaved with read-cycles.
6	TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
7	TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
8	$\overline{ODD}$/EVEN	Interlaced mode state output	High for even numbered and low for odd-numbered frames. The value is valid 2µs before the end of lines 311 and 624.
9	F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.
10	VCS	Video composite synchronization input signal	Active high VCS input.
11	SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
12	$\overline{TCS}/\overline{SCS}$	Input / output composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization or Text composite sync. ($\overline{TCS}$) output signal to the SAA5231. Both signals are active low.
13, 14, 15	R G B	Red, green, blue	Character and background colors active-high open-drain outputs.
16	$\overline{COR}$	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation.
17	BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
18	Y	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
19	SCL	Serial clock	Microprocessor clock input via serial bus.
20	SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
21	V_{SS}	0 Volt	Ground.
22-29	D0-D7	Parallel data input / output	Eight tri-state input/output for data read/write from/to an external RAM.
30-39	A0-A9	Address signals	Ten addresses output pins for accessing to individual Bytes of a 1 kByte chapter stored in an external Static RAM.

5243-01.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	-0.3, +7.5	V
INPUT VOLTAGE RANGE :			
V_I	VCS,SDA,SCL,D0-D7 TTD,F6,TCS/SCS,TTC	-0.3, +7.5 -0.3, +10	V V
OUTPUT VOLTAGE RANGE :			
V_O	SAND, A0-A12,OE, WE, D0-D7,SDA,ODD/EVEN,R,G,B, BLAN, COR, Y, TCS/SCS	-0.3 , +7.5 -0.3, +10	V V
T_{stg}	Storage Temperature Range	-20, +125	°C
T_A	Operating Ambient Temperature Range	-20, +70	°C

5243-02.TBL

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current	-	140	200	mA
INPUTS					
	TTD (Pin 6)				
C_{EXT}	Ext. Coupling Capacitor	-	-	50	nF
$V_{I(p-p)}$	Input Voltage p-p	2	-	7	V
t_r , t_f	Input Rise / Fall Times	10	-	80	ns
t_{DS}	Input Set-up Time	40	-	-	ns
t_{DH}	Input Hold Time	40	-	-	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-	-	20	µA
C_I	Input capacitance	-	-	7	pF
	TTC, F6 (Pins 7,9)				
V_I	DC Input Voltage	- 0.3	-	+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5	- -	7 7	V V
$\pm V_P$	Input Peak Rel. 50 % Duty	0.2	-	3.5	V
f_{TTC}	TTC Clock Frequency	4	6.9375	8	MHz
f_{F6}	F6 Clock Frequency	4	6	8	MHz
t_r , t_f	Clock Rise / Fall Times	10	-	80	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-	-	20	µA
C_I	Input Capacitance	-	-	7	pF
	VCS (Pin 10)				
V_{IL}	Low Level Input Voltage	0	-	0.8	V
V_{IH}	High Level Input Voltage	2	-	V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
	SCL (Pin 19)				
V_{IL}	Low Level Input Voltage	0	-	1.5	V
V_{IH}	High Level Input Voltage	3	-	V_{DD}	V
f_{SCL}	SCL Clock Frequency	-	-	100	kHz
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF

5243-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
INPUT/OUTPUTS					
	$\overline{TCS}$(output), $\overline{SCS}$(input) (Pin12)				
V_{IL}	Low Level Input Voltage	0	-	1.5	V
V_{IH}	High Level Input Voltage	3	-	8	V
t_r , t_f	Input Rise / Fall Times	-	-	500	ns
$\pm I_{I(L)}$	Input Leakage Current (V_I = 0 to 5.5V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0	-	0.4	V
V_{OH}	High Level Output Voltage $-I_{OH}$ = 0.2mA I_{OH} = 0.1mA	 2.4 2.4	 - -	 V_{DD} 5.5	 V V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	100	ns
C_I	Load Capacitance	-	-	50	pF
	SDA (Pin 20) (see Figure 4)				
V_{IL}	Low Level Input Voltage	0	-	1.5	V
V_{IH}	High Level Input Voltage	3	-	V_{DD}	V
t_r , t_f	Input Rise / Fall Times	-	-	2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 5.5V with output off)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0	-	0.5	V
t_f	Output Fall Time between 3.0V and 1.0V	-	-	200	ns
C_i	Load Capacitance	-	-	400	pF
	D0-D7 (Pins 22-29), (see Figure 5)				
V_{IL}	Low Level Input Voltage	0	-	0.8	V
V_{IH}	High Level Input Voltage	2	-	V_{DD}	V
$\pm I_{I(L)}$	Input Leakage Current (V_I = 0 to 5.5V and output in high impedance state)	-	-	10	µA
C_I	Input Capacitance	-	-	7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 1.6mA)	0	-	0.4	V
V_{OH}	Hogh Level Output Voltage ($-I_{OH}$ = 0.2mA)	2.4	-	V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_I	Load Capacitance	-	-	120	pF
OUTPUTS					
	A0-A12, $\overline{OE}$, $\overline{WE}$ (Pins 30-40,2,3,4,5,)				
V_{OL}	Low Level Output Voltage (I_{OL} = 1.6mA)	0	-	0.4	V
V_{OH}	High Level Output Voltage ($-I_{OH}$ = 0.2mA)	0.4	-	V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V	-	-	50	ns
C_L	Load Capacitance	-	-	120	pF
	$\overline{ODD}$/EVEN (Pin 8)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0	-	0.4	V
V_{OH}	HIgh Level Output Voltage ($-I_{OH}$ = 0.2mA)	2.4	-	V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V				
C_L	Load Capacitance				

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ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
OUTPUTS					
	SAND (Pin 11)(see Figure 1)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.2mA)	0	-	0.25	V
V_{OI}	Middle Level Output Voltage (I_{OL} = ± 10 µA)	1.1	-	2.9	V
V_{OH}	High Level Output Voltage (I_{OH} = 0/-10µA)	4	-	V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : V_{OL} to V_{OI} from 0.4 to 1.1V V_{OI} to V_{OH} from 2.9 to 4.0V	- -	- -	400 200	ns
t_f	Output Fall Time V_{OH} to V_{OI} from 4.0 to 0.4V	-	-	50	ns
C_I	Load Capacitance	-	-	30	pF
	R, G, B, $\overline{COR}$, BLAN, Y (Pins 13-18), (see Figure 4)				
V_{OL}	Low Level Output Voltage : I_{OL} = 2mA I_{OL} = 5mA	 0 0	 - -	 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to 5V)	-	-	5	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to 5V)	-	-	20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to 5V)	-	-	20	ns
C_L	Load Capacitance	-	-	25	pF
I_{LO}	Output Leakage Current (V_{PU} = 0 to 6V output off)	-	-	20	µA
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW}	Low Period Clock	4	-	-	µs
t_{HIGH}	High Period Clock	4	-	-	µs
t_{SU} , d_{AT}	Data Set-up Time	250	-	-	ns
t_{HD} , d_{AT}	Data Hold Time	170	-	-	ns
t_{SU} , s_{TO}	Stop Set-up Time from Clock High	4	-	-	µs
t_{BUF}	Start Set-up Time Following a Stop	4	-	-	µs
t_{HD} , s_{TA}	Start Hold Time	4	-	-	µs
t_{SU} , s_{TA}	Start Set-up Time Following Clock Low to High Transition	4	-	-	µs
	MEMORY INTERFACE referred to V_{IL} = 1.5V				
t_{CY}	Cycle Time	-	500	-	ns
t_{OE}	Adress Change to $\overline{OE}$ Low	60	-	-	ns
t_{ADDR}	Address Active Time	450	500	-	ns
t_{OEW}	$\overline{OE}$ Pulse Duration	320	-	-	ns
t_{ACC}	Access Time from $\overline{OE}$ to Data Valid	-	-	200	ns
t_{DH}	Data Hold Time from $\overline{OE}$ High or Address Change	0	-	-	ns
t_{WE}	Address Change to $\overline{WE}$ Low	40	-	-	ns
t_{WEW}	$\overline{WE}$ Pulse Duration	200	-	-	ns
t_{DS}	Data Set-up Time to $\overline{WE}$ High	100	-	-	ns
t_{DHWE}	Data Hold Time from $\overline{WE}$ High	20	-	-	ns
t_{WR}	Write Recovery Time	25	-	-	ns

5243-05.TBL

Figure 1 : F6, TTC, TTD Input Internal Connections

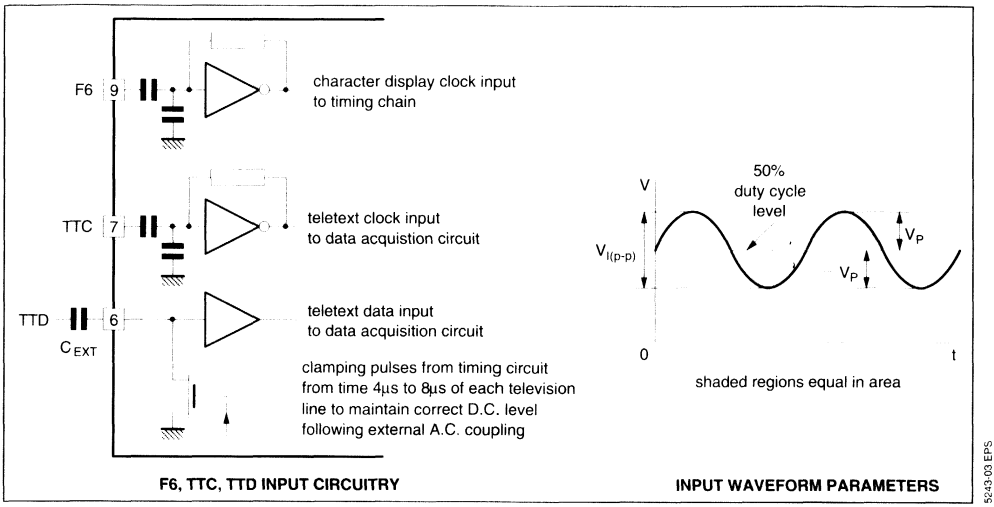


Figure 2 : Teletext Data Input Timing

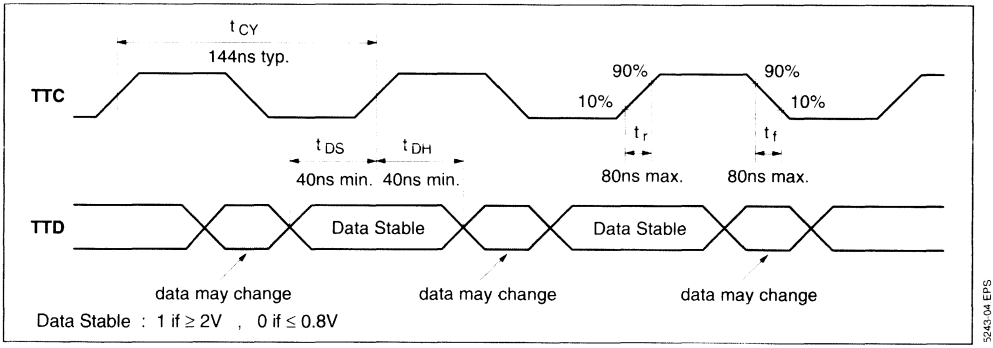


Figure 3 : Synchronization Timing

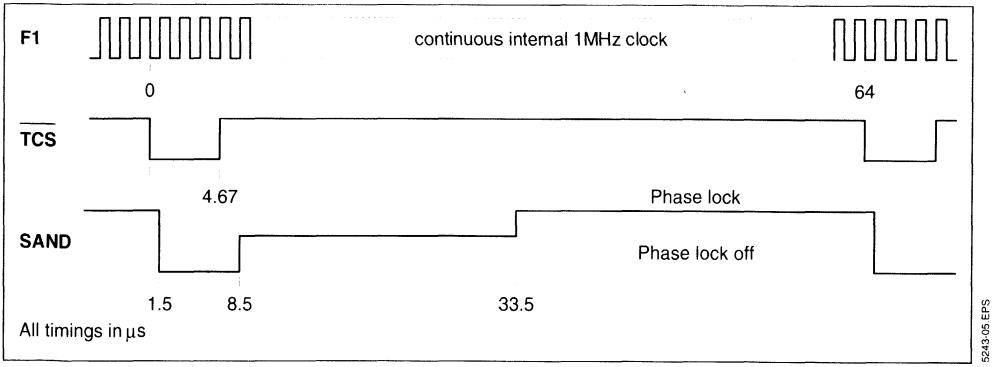
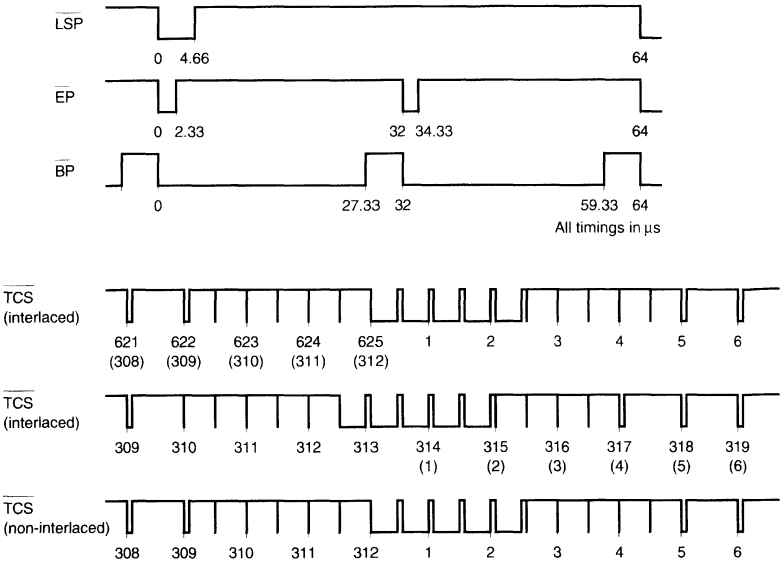


Figure 4 : Composite Sync. Waveforms

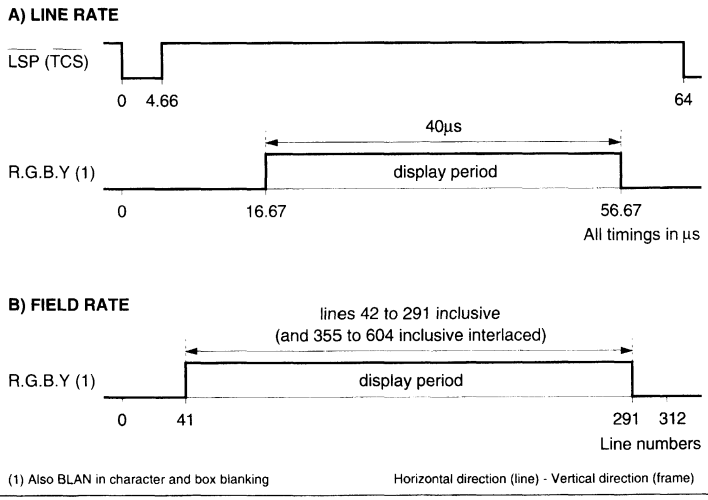


The number positions indicate the end of lines.
The Teletext composite synchronization signal (TCS), whether interlacing is present or not, comprise three components.
a) the line-synchronization pulses (LSP).
b) the equalization pulses (EP)
c) the frame-synchronization pulses (BP).

The timing reference is specified by the descending edge of the signal LSP, with a tolerance spread of ± 100ns.

5243-06.EPS

Figure 5 : Display Output Timing



(1) Also BLAN in character and box blanking

Horizontal direction (line) - Vertical direction (frame)

5243-07.EPS

Figure 6 : Serial Bus Timing

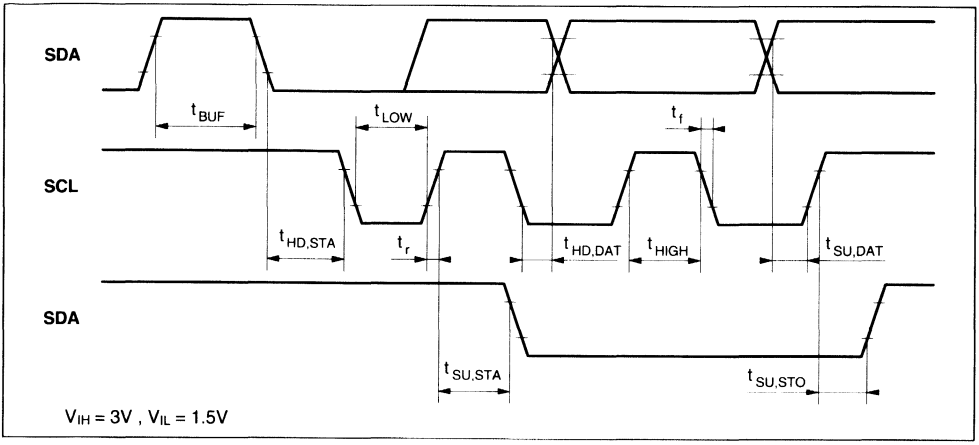
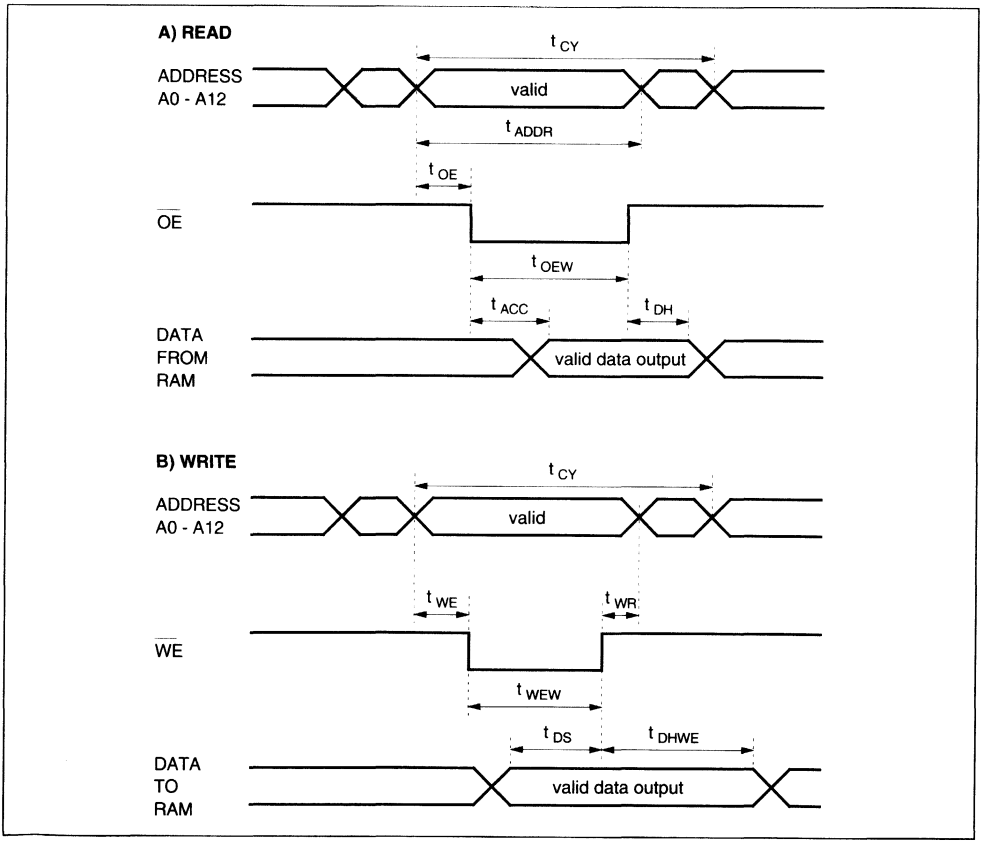
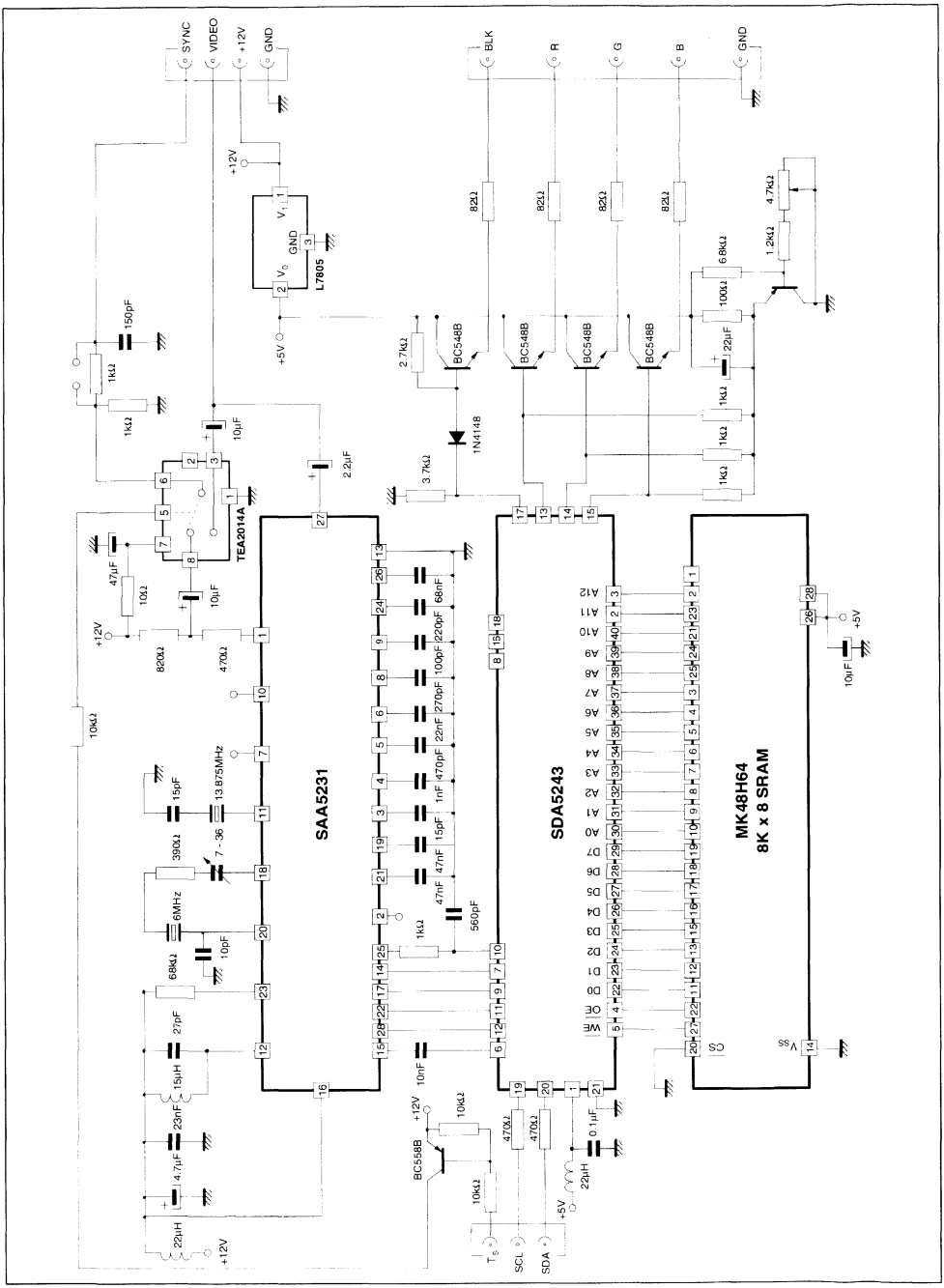


Figure 7 : Memory Interface Timing



APPLICATION DIAGRAM



APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown in Figure 6. In contrast with the first generation of Teletext Decoders the new CCT (Computer Controlled Teletext) chip provides a display format of 25 rows of 40 characters per row.

Row number twenty-four is used by the microprocessor for the display of information.

Row zero contains the page header.

The organization is as follows :

The first seven characters (0 - 6) are used for messages regarding the operational status.

The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white ; when it is "green" the operational state corresponds to "search mode" and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.

Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANIZATION
Figure 8

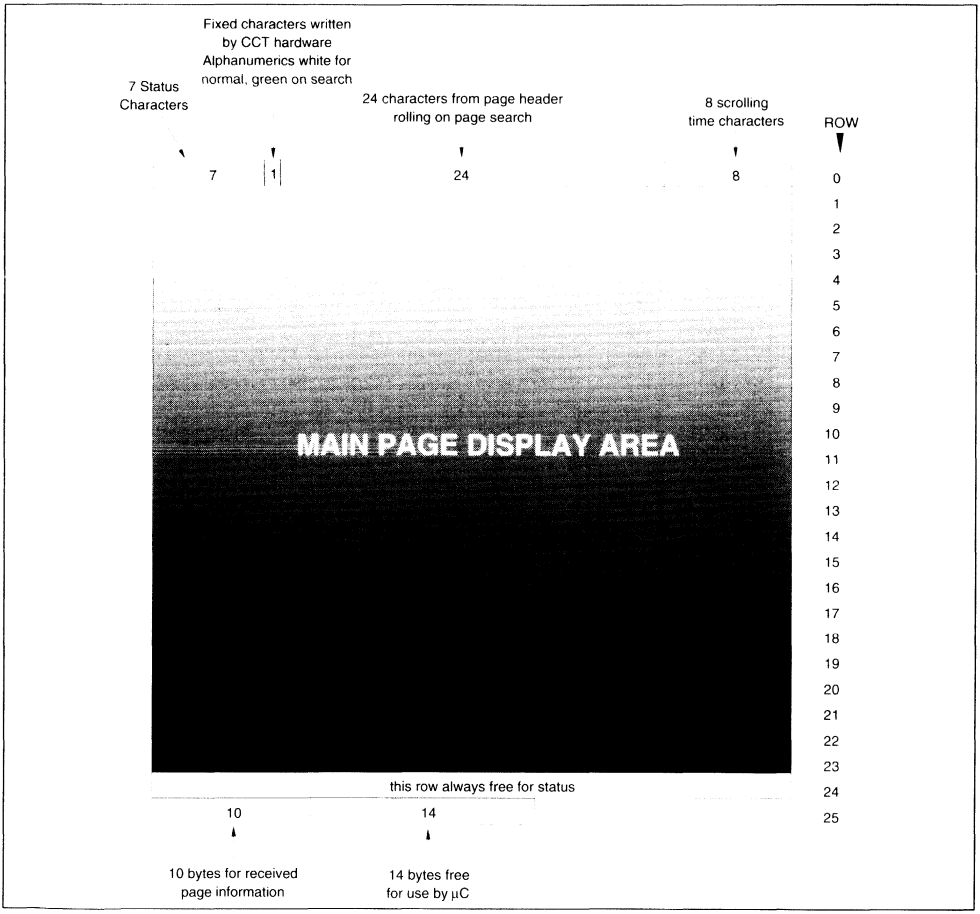


Table 1 : Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

Page number : - MAG = magazine, PU = page units, PT = page tens.
Page sub-code : - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

5243-06.TBL

REGISTER MAP (see Table 2)
Registers R1 to R10 are write only whilst R11 is a read/write register respect to the microprocessor.
The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TA and TB should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R1 to R10 are cleared to zero with the exception of bits D0 an D1 in registers R5 and R6 which are set to logical one.
After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{7+P}$/ 8 BIT	$\underline{\text{ACQ.}}$ $\overline{\text{ON/OFF}}$	GHOST ROW ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
-	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
-	-	-	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
-	-	-	-	-	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS $\underline{\text{ROW}}$ $\overline{\text{BTM/TOP}}$	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL	TOP/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
-	-	-	-	CLEAR MEM.	A2	A1	A0	R8	Active chapter
-	-	-	R4	R3	R2	R1	R0	R9	Active row
-	-	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

- bit does not exist

5243-07.TBL

REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R1	Mode controls	T0,T1 (D0,D1)	These bits control the frame display format. Interlaced or non-interlaced,312/313 or 312/312.
		TCS ON (D2)	This bit determines the character display synchronization mode. Teletext composite synchronism (TCS ON = 1) or direct broadcast synchronism (TCS ON = 0).
		DEW/FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1) for recovering of Teletext data.
		GHOST ROW ENABLE (D4)	Selection of ghost row mode (D4 = 1)
		ACQUISITION ON/OFF (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		7 bits + parity or 8 bits without parity (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
		TA (D7)	Test bit equal to "0" in the normal operating mode.
R2	Addressing information for a page request	SC0,SC1,SC2 (D0,D1,D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit equal to "0" in the normal working mode.
		A0,A1 (D4,D5)	Address a group of four consecutive pages currently used for data acquisition;
		A2 (D6)	Address of one of the two groups of four pages for acquisition in normal mode.
R3	Data relative to the requested page (see Table 3).	PRD0-PRD4 (D0-D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4	Selection of one of eight pages to display.	A0,A1,A2 (D0,D1,D2)	These three bits correspond to the logical states of the three address lines (A12,A11,A10) during memory read cycles.
R5	Display control for normal operation.	PON (D0,D1)	Picture on (IN: D0, OUT: D1)
		TEXT (D2,D3)	Text on (IN: D2, OUT: D3)
		COR (D4,D5)	Contrast reduction on (IN: D4, OUT: D5)
		BKGND (D6,D7)	Background colour on (IN: D6, OUT: D7)
		IN/OUT	Enable inside/outside the box
R6	Display control for news-flash subtitle generation.	See R5	See R5
R7	Display mode	BOX ON 0,1-23,24 (D0,D1,D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		STATUS ROW BTM/TOP (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).
R8 to R11	Active chapter address (R8), active row address (R9), active column address (R10). Data contained in R11 read (written) from (to) memory by microprocessor via I^2C bus.		

5243-08.TBL

Table 3 : Register R3

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	HOLD	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one difined as "timed" may be selected.
If "HOLD" is low the page is held. The addressing of successive bytes via the I^2C bus is automatic.

5243-09.TBL

CHARACTER SETS

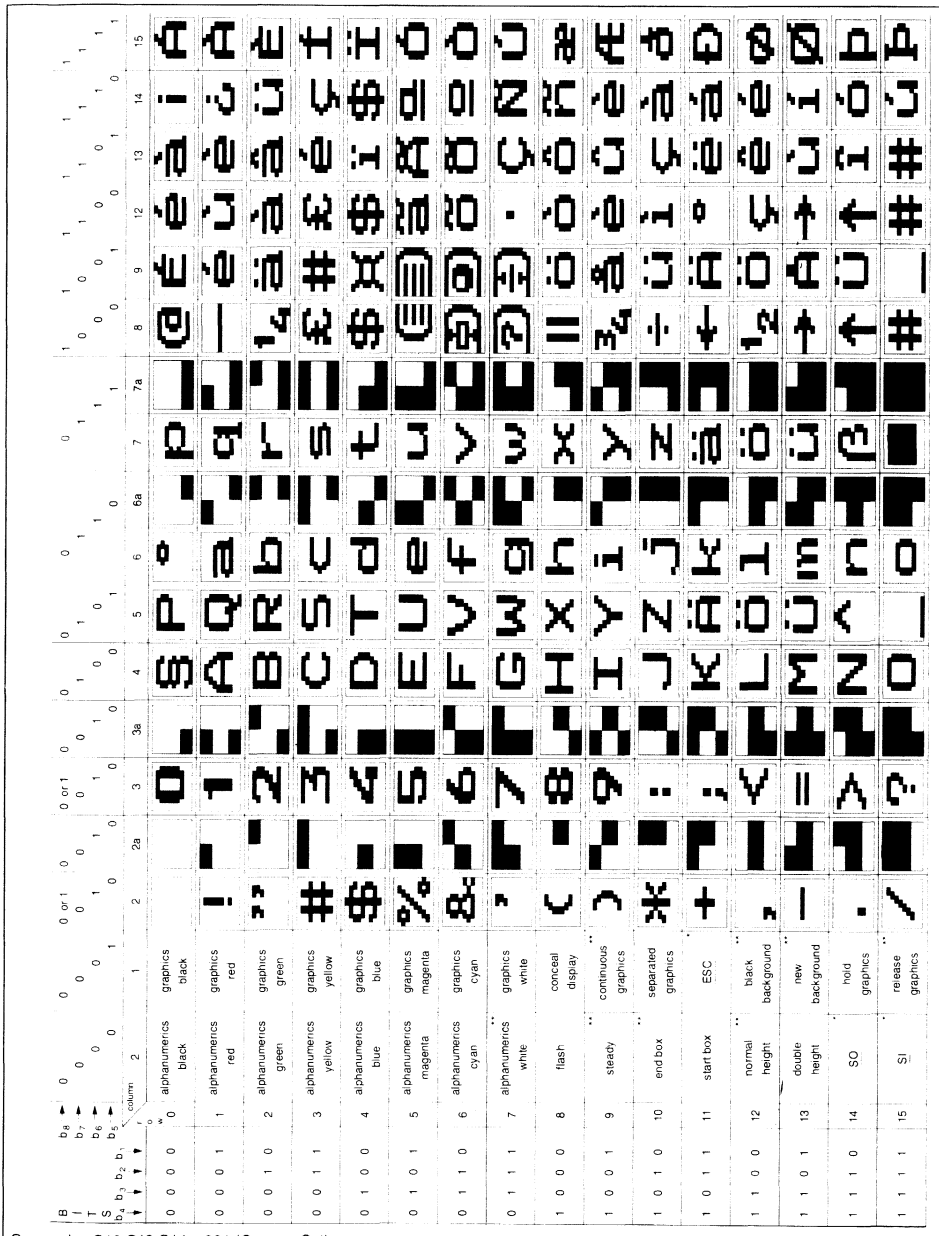
The complete character set with 8-bit decoding is given in Table 4.

Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.

A rectangle may be represented as follows : ☐

The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5. The 13 national characters are placed in columns with bit 8 = 0.

Table 4a : Complete character set (with 8 bit codes) - West European Languages

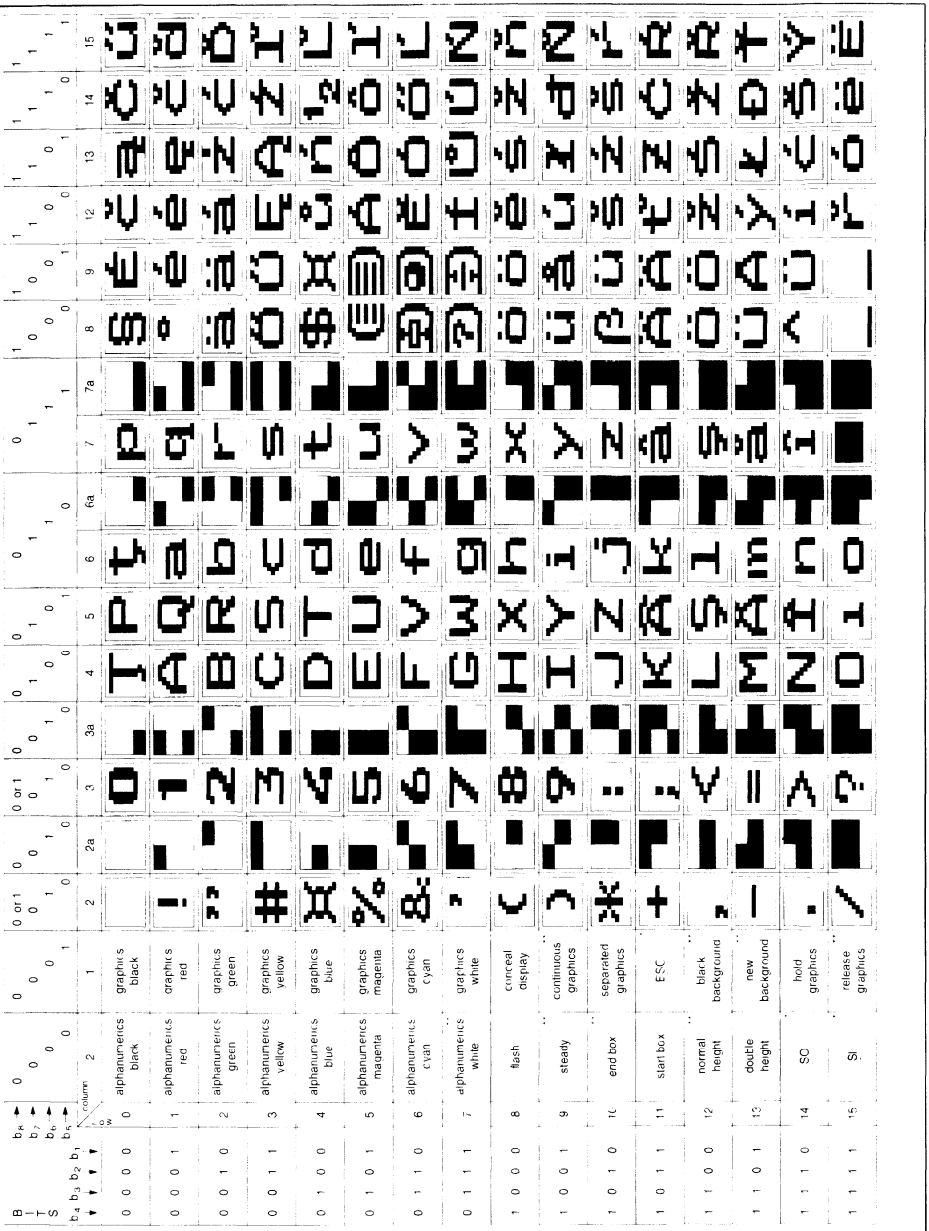


Case using C12 C13 C14 = 001 (German Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

5243-12.EPS

Table 4b : Complete character set (with 8 bit codes) - East European Languages



Case using C12 C13 C14 = 111 (Rumanian Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

NATIONAL OPTION CHARACTER SETS

The basic set of the 96 characters is shown in Table 5.The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Tables 6 and 7.

Table 5 : Basic character set.

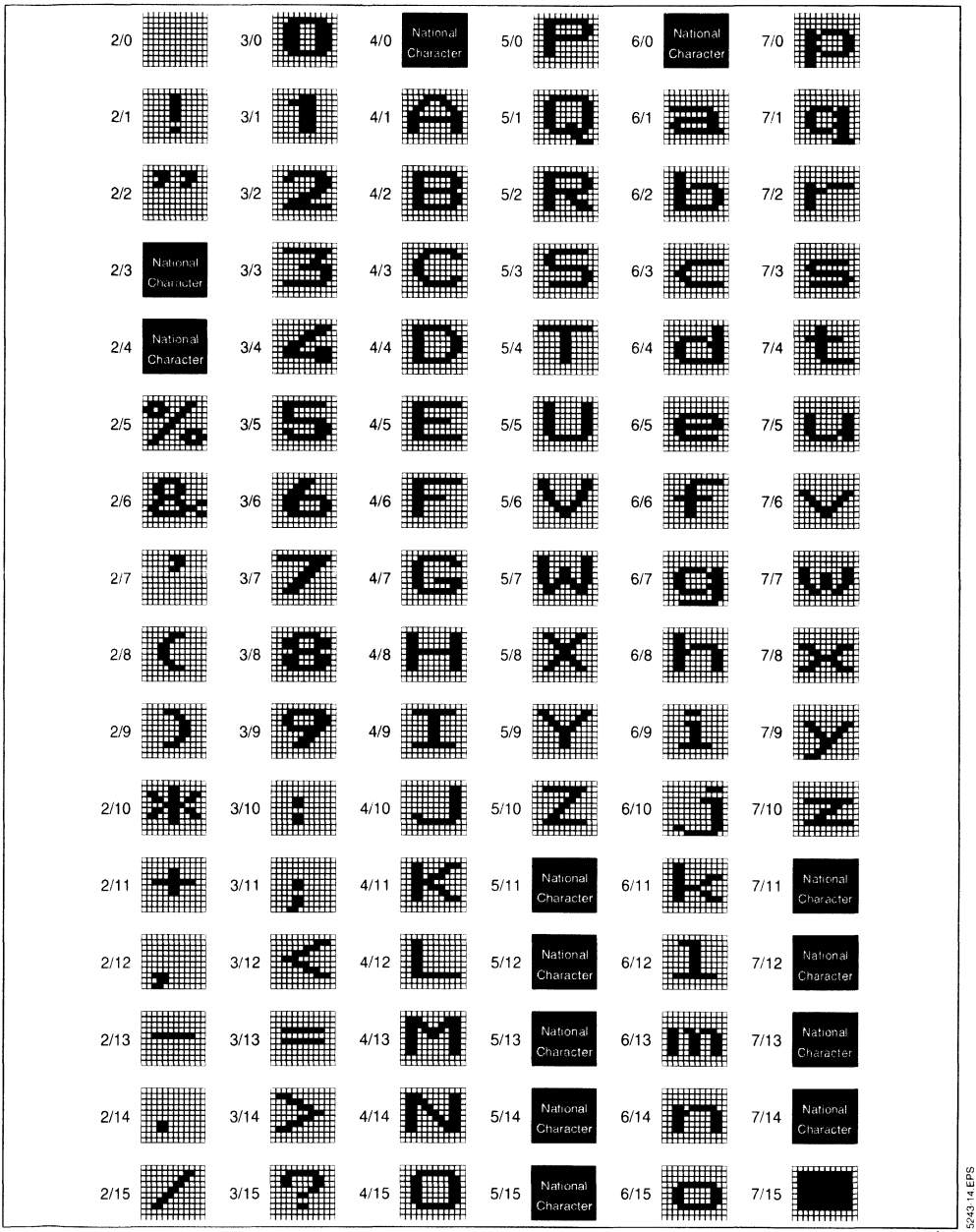
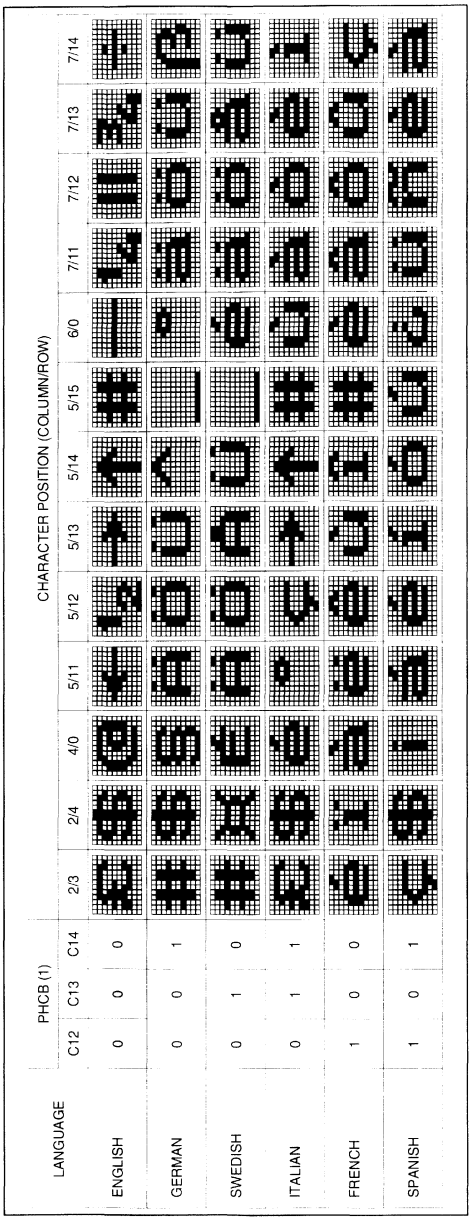
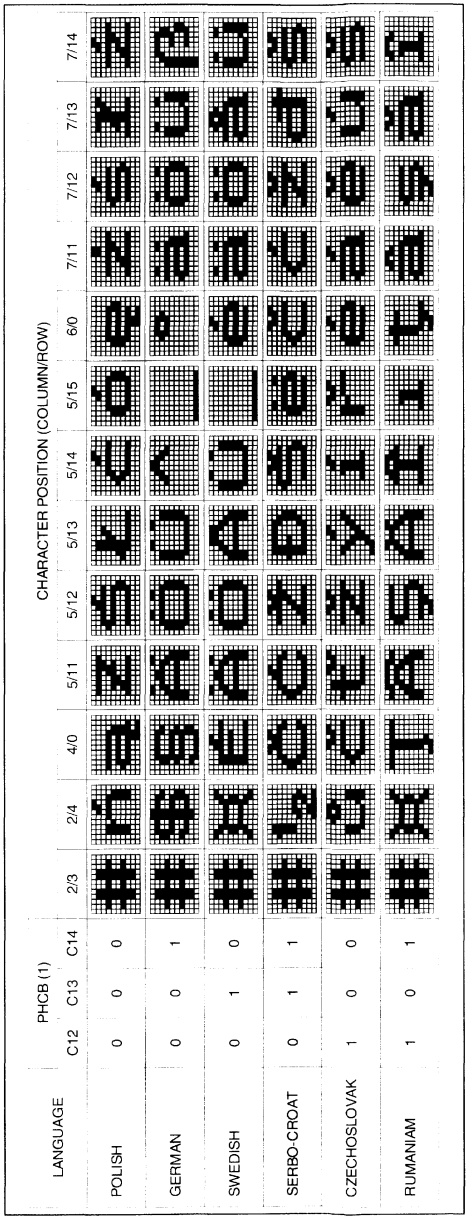


Table 6 : Character Set for SDA5243 West European Languages



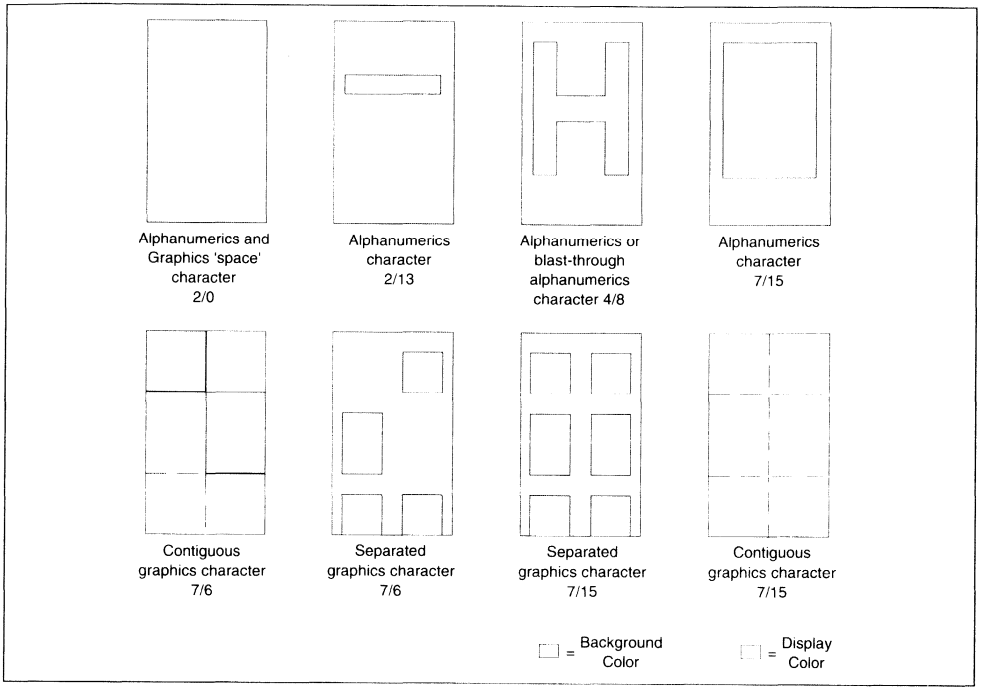
Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to English. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

Table 7 : Character Set for SDA5243 East European Languages



Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to German. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

Figure 9 : Character Format



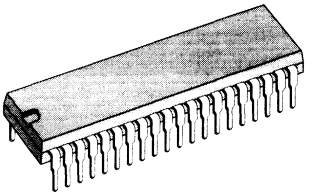
SGS-THOMSON MICROELECTRONICS

STV5345
STV5345/H - STV5345/T

TELETEXT DECODER WITH 8 INTEGRATED PAGES

PRELIMINARY DATA

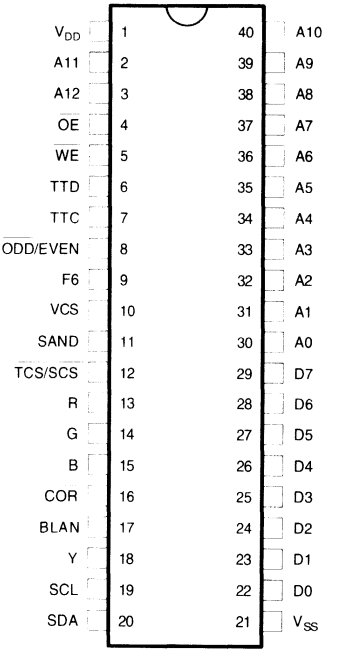
- COMPLETE TELETEXT DECODER INCLUDING ON-CHIP 8 PAGES MEMORY, REDUCING EMC RADIATIONS
- UPWARD SOFTWARE AND HARDWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON's DECODER SDA5243
- DIRECT INTERFACE TO AN EXTERNAL STATIC RAM OF 8kBYTES FOR UP TO 16 PAGES APPLICATION
- AUTOMATIC SELECTION OF UP TO SIX NATIONAL LANGUAGES
- FOUR SIMULTANEOUS PAGE REQUESTS
- DISPLAY OF THE 25TH STATUS ROW
- MICROPROCESSOR CONTROL VIA AN I^2C BUS (SLAVE ADDRESS 0010001 R/$\overline{W}$)
- DATA ACQUISITION AVAILABLE FROM LINES 2 TO 22 OR FROM A COMPLETE FIELD
- HIGH QUALITY DISPLAY USING A CHARACTER MATRIX OF 12 x 10 DOTS
- SINGLE + 5V SUPPLY VOLTAGE
- ON-CHIP MASK PROGRAMMABLE ROM CHARACTER GENERATORS
- HCMOS PROCESS



DIP40
(Plastic Package)

ORDER CODE : STV5345 West European
STV5345/H East European
STV5345/T Turkish & European

PIN CONNECTIONS



5345V-01.EPS

DESCRIPTION

The STV5345 is a HCMOS integrated circuit which performs all the processing of logical data within a 625 lines system teletext decoder. It is designed to operate in conjunction with one-chip : the SAA5231 integrated chip which extracts Teletext information embedded in a composite video signal. Up to 8 pages of display data can be stored in internal memory. Using 8Kbytes of external memory leads to a 16 pages application. A complete system also comprises a microprocessor controlling the STV5345 via a 2-wires serial bus. An on-chip ROM memory contains the character sets. The STV5345 performs automatic selection of one of up to six natural languages. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

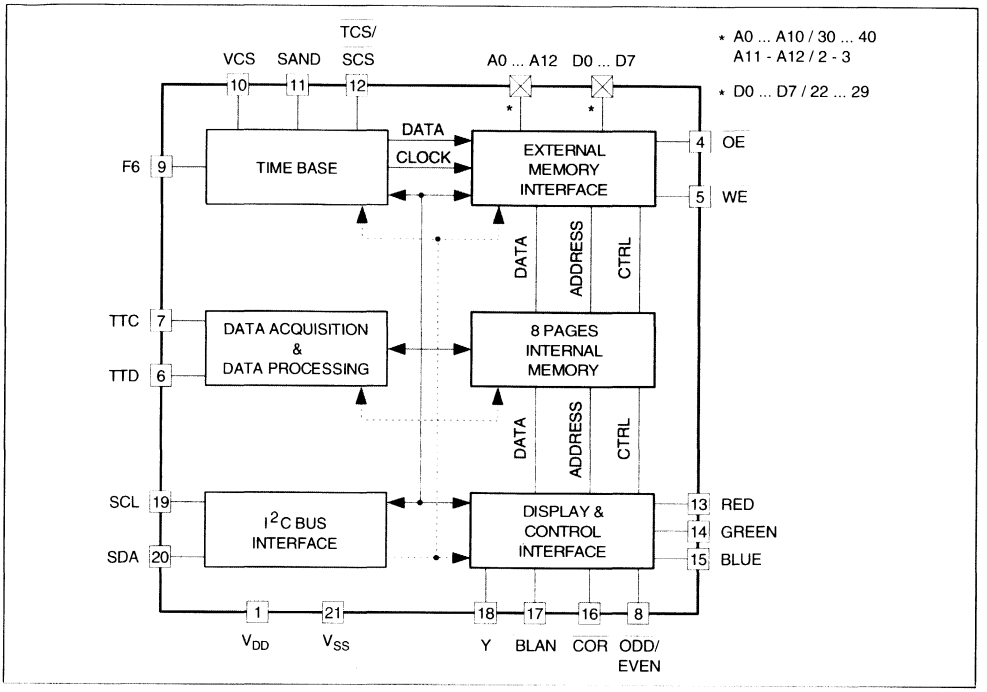
PIN DESCRIPTION

Pin	Symbol	Function	Description
1	V_{DD}	+5V	Positive supply voltage
2,3,40 *	A11, A12, A10	Chapter address	Address selection outputs for 1 of 8 external static RAM chapters each of 1 kBytes.
4 *	$\overline{OE}$	Output enable	Active-low external static RAM output enable control signal.
5 *	$\overline{WE}$	Write enable	Active-low external static RAM write enable control signal. It supports write-cycles interleaved with read-cycles.
6	TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
7	TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
8	ODD/EVEN	Interlaced mode state output	High for even numbered and low for odd-numbered frames. The value is valid 2µs before the end of lines 311 and 624.
9	F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.
10	VCS	Video composite synchronization input signal	Active high VCS input.
11	SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
12	TCS/$\overline{SCS}$	Input / output composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization or Text composite sync. (TCS) output signal to the SAA5231. Both signals are active low.
13,14,15	R G B	Red, green, blue	Character and background colors active-high open-drain outputs.
16	$\overline{COR}$	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation.
17	BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
18	Y	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
19	SCL	Serial clock	Microprocessor clock input via serial bus.
20	SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
21	V_{SS}	0 Volt	Ground.
22-29 *	D0-D7	Parallel data input / output	Eight tri-state input/output for data read/write from/to an external static RAM.
30-39 *	A0-A9	Address signals	Ten addresses output pins for accessing to individual Bytes of a 1 kByte chapter stored in an external Static RAM.

5345V-01.TBL

* Pins only activated when 8KBytes of external memory are addressed, otherwise pins $\overline{OE}$ and $\overline{WE}$ remain high, and others remain low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	-0.3, +6.0	V
INPUT VOLTAGE RANGE :			
V_I	VCS,SDA,SCL,D0-D7	-0.3, V_{DD} + 0.5	V
V_I	TTD,F6,$\overline{TCS}$/$\overline{SCS}$,TTC	-0.3, +10	V
OUTPUT VOLTAGE RANGE :			
V_O	SAND,A0-A12,$\overline{OE}$,$\overline{WE}$,D0-D7,SDA,ODD/EVEN,R,G,B	-0.3 , V_{DD}	V
V_O	BLAN,$\overline{COR}$, Y, $\overline{TCS}$/$\overline{SCS}$	-0.3 , V_{DD}	V
T_{stg}	Storage Temperature Range	-20, +125	°C
T_A	Operating Ambient Temperature Range	-20, +70	°C

5345V-02.TBL

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (Pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current (operating mode)		TBD		mA

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ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
INPUTS					
	TTD (Pin 6)				
C_{EXT}	Ext. Coupling Capacitor			50	nF
$V_{I(p-p)}$	Input Voltage p-p	2		7	V
t_r , t_f	Input Rise / Fall Times	10		80	ns
t_{DS}	Input Set-up Time	40			ns
t_{DH}	Input Hold Time	40			ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input capacitance			7	pF
	TTC, F6 (Pins 7,9)				
V_I	DC Input Voltage	- 0.3		+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5		7 7	V V
± V_P	Input Peak Rel. 50 % Duty	0.2		3.5	V
f_{TTC}	TTC Clock Frequency		6.9375		MHz
f_{F6}	F6 Clock Frequency		6		MHz
t_r , t_f	Clock Rise / Fall Times	10		80	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-10		+10	µA
C_I	Input Capacitance			10	pF
	VCS (Pin 10)				
V_{IL}	Low Level Input Voltage	0		0.8	V
V_{IH}	High Level Input Voltage	2		V_{DD}	V
t_r , t_f	Input Rise / Fall Times			500	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input Capacitance			7	pF
	SCL (Pin 19)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input Capacitance			7	pF
INPUT/OUTPUTS					
	$\overline{TCS}$(output), $\overline{SCS}$(input) (Pin12)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		8	V
t_r , t_f	Input Rise / Fall Times			500	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0		0.4	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			100	ns
C_L	Load Capacitance			50	pF

5345V-04 TBL

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
INPUT/OUTPUTS (continued)					
	SDA (Pin 20)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		V_{DD}	V
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_f	Output Fall Time between 3.0V and 1.0V			200	ns
C_L	Load Capacitance			400	pF
	D0-D7 (Pins 22-29)				
V_{IL}	Low Level Input Voltage	0		0.8	V
V_{IH}	High Level Input Voltage	2		V_{DD}	V
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			50	ns
C_L	Load Capacitance			120	pF
OUTPUTS					
	A0-A12, $\overline{OE}$, $\overline{WE}$ (Pins 30-40,2,3,4,5,)				
V_{OL}	Low Level Output Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			50	ns
C_L	Load Capacitance			120	pF
	$\overline{ODD/EVEN}$ (Pin 8)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0		0.4	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			100	ns
C_L	Load Capacitance			50	pF
	SAND (Pin 11)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.2mA)	0	-	0.25	V
V_{OI}	Middle Level Output Voltage (I_{OL} = ± 10 µA)	1.1	-	2.9	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0 to 10µA)	4		V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : • V_{OL} to V_{OI} from 0.4 to 1.1V • V_{OI} to V_{OH} from 2.9 to 4.0V	- -	- -	400 200	ns
t_f	Output Fall Time V_{OH} to V_{OI} from 4.0 to 0.4V	-	-	50	ns
C_L	Load Capacitance	-	-	30	pF

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ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
OUTPUTS (continued)					
	R, G, B, $\overline{COR}$, BLAN, Y (Pins 13-18)				
V_{OL}	Low Level Output Voltage : • I_{OL} = 2mA • I_{OL} = 5mA	 0 0	 - -	 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to V_{DD})	-	-	V_{DD}	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to V_{DD})	-	-	20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to V_{DD})	-	-	20	ns
C_L	Load Capacitance	-	-	25	pF
I_{LO}	Output Leakage Current (V_{PU} = 0 to V_{DD} output off)	-	-	20	µA
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V) (see Fig. 6)				
t_{LOW}	Low Period Clock	4	-	-	µs
t_{HIGH}	High Period Clock	4	-	-	µs
$t_{SU,DAT}$	Data Set-up Time	250	-	-	ns
$t_{HD,DAT}$	Data Hold Time	170	-	-	ns
$t_{SU,STO}$	Stop Set-up Time from Clock High	4	-	-	µs
t_{BUF}	Start Set-up Time Following a Stop	4	-	-	µs
$t_{HD,STA}$	Start Hold Time	4	-	-	µs
$t_{SU,STA}$	Start Set-up Time Following Clock Low to High Transition	4	-	-	µs
	MEMORY INTERFACE referred to V_{IL} = 1.5V (see Fig. 7)				
t_{CY}	Cycle Time	-	500	-	ns
t_{OE}	Adress Change to $\overline{OE}$ Low	60	-	-	ns
t_{ADDR}	Address Active Time	450	500	-	ns
t_{OEW}	$\overline{OE}$ Pulse Duration	320	-	-	ns
t_{ACC}	Access Time from $\overline{OE}$ to Data Valid	-	-	200	ns
t_{DH}	Data Hold Time from $\overline{OE}$ High or Address Change	0	-	-	ns
t_{WE}	Address Change to $\overline{WE}$ Low	40	-	-	ns
t_{WEW}	$\overline{WE}$ Pulse Duration	200	-	-	ns
t_{DS}	Data Set-up Time to $\overline{WE}$ High	100	-	-	ns
t_{DHWE}	Data Hold Time from $\overline{WE}$ High	20	-	-	ns
t_{WR}	Write Recovery Time	25	-	-	ns

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Figure 1 : F6, TTC, TTD Input Internal Connections

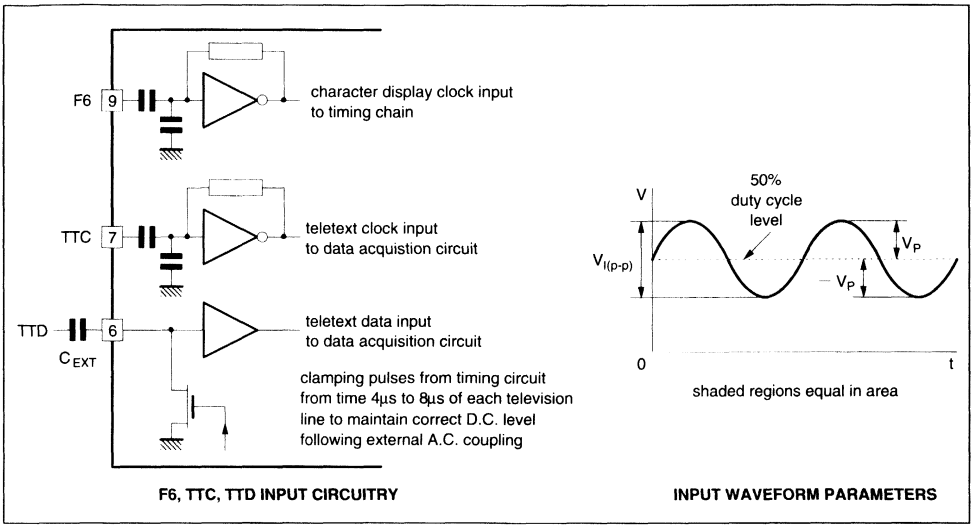

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Figure 2 : Teletext Data Input Timing

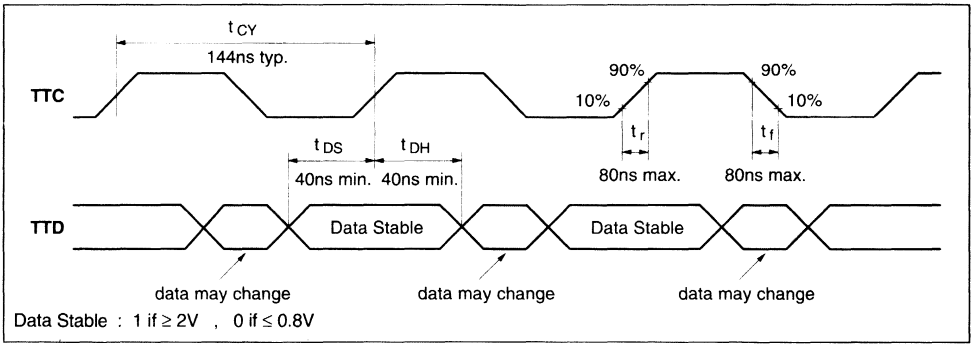

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Figure 3 : Synchronization Timing

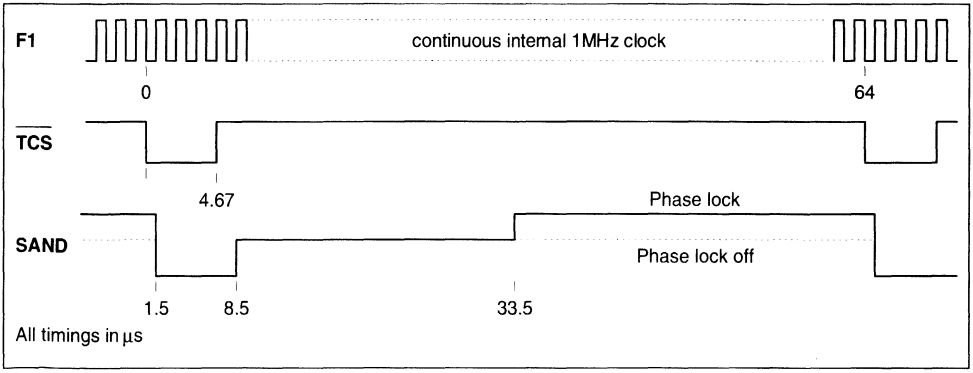

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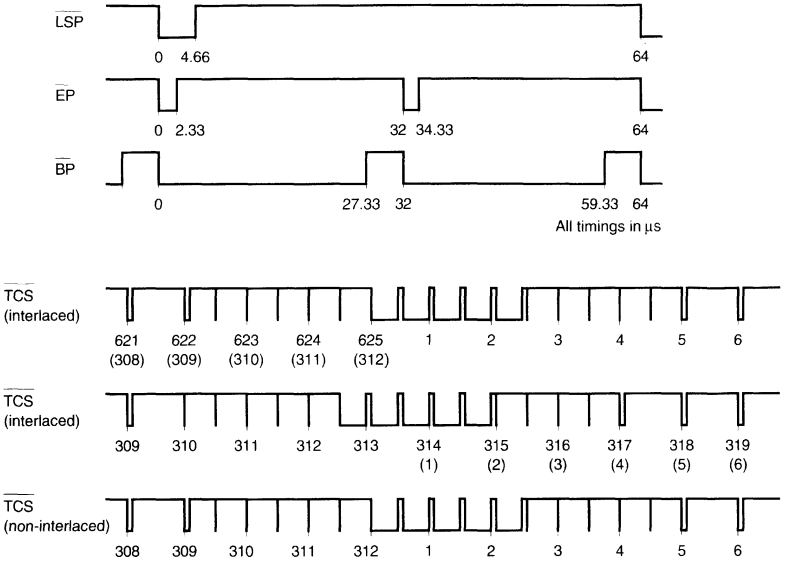
Figure 4 : Composite Sync. Waveforms



The number positions indicate the end of lines.
The Teletext composite synchronization signal (TCS), whether interlacing is present or not, comprise three components.
a) the line-synchronization pulses (LSP).
b) the equalization pulses (EP)
c) the frame-synchronization pulses (BP).

The timing reference is specified by the descending edge of the signal LSP, with a tolerance spread of ± 100ns.

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Figure 5 : Display Output Timing

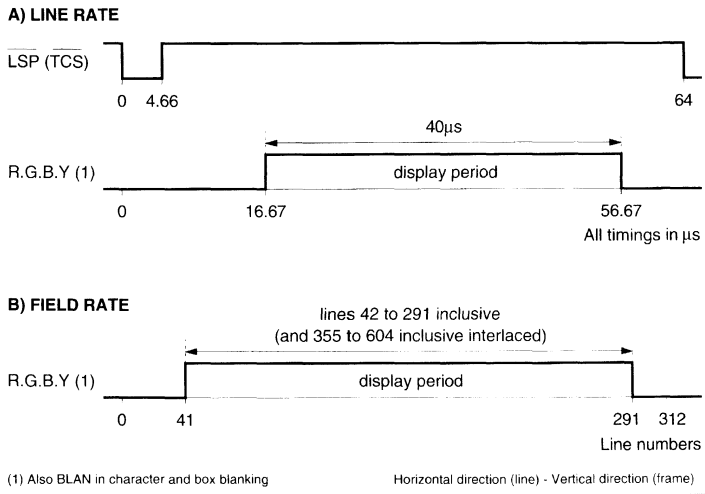

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Figure 6 : Serial Bus Timing

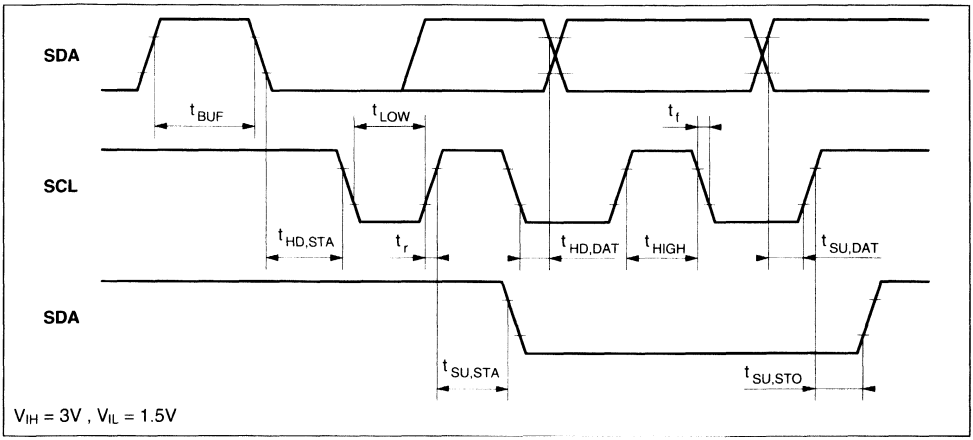


Figure 7 : Memory Interface Timing

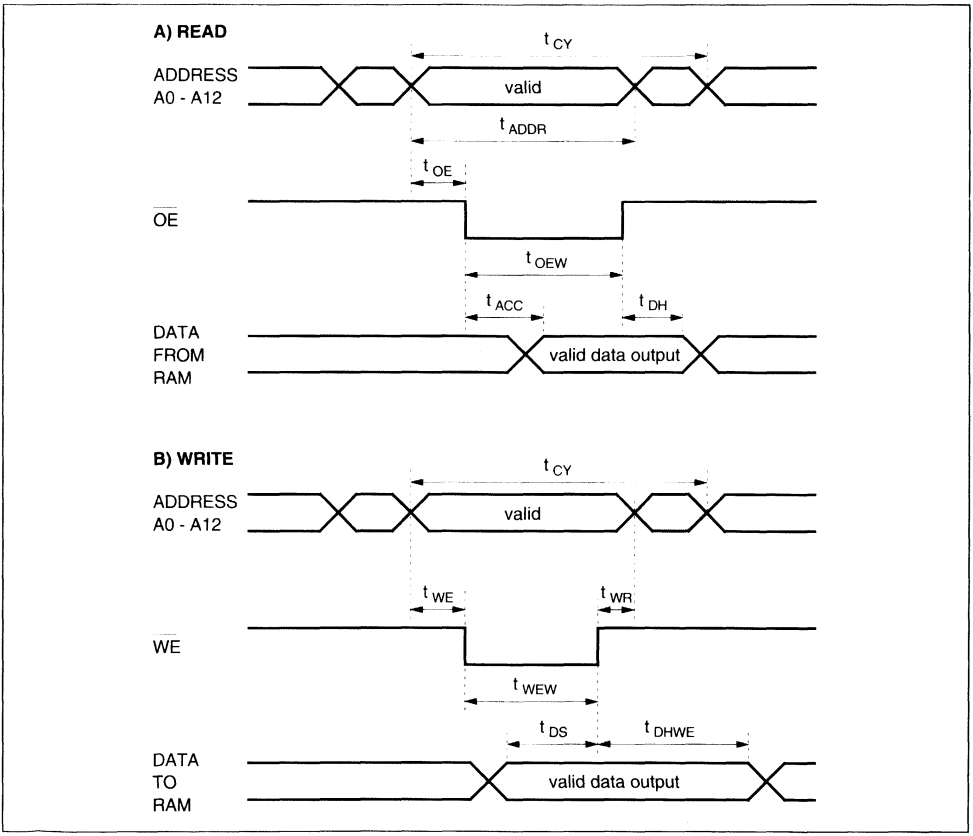


Figure 8 : Master Synchronization Mode

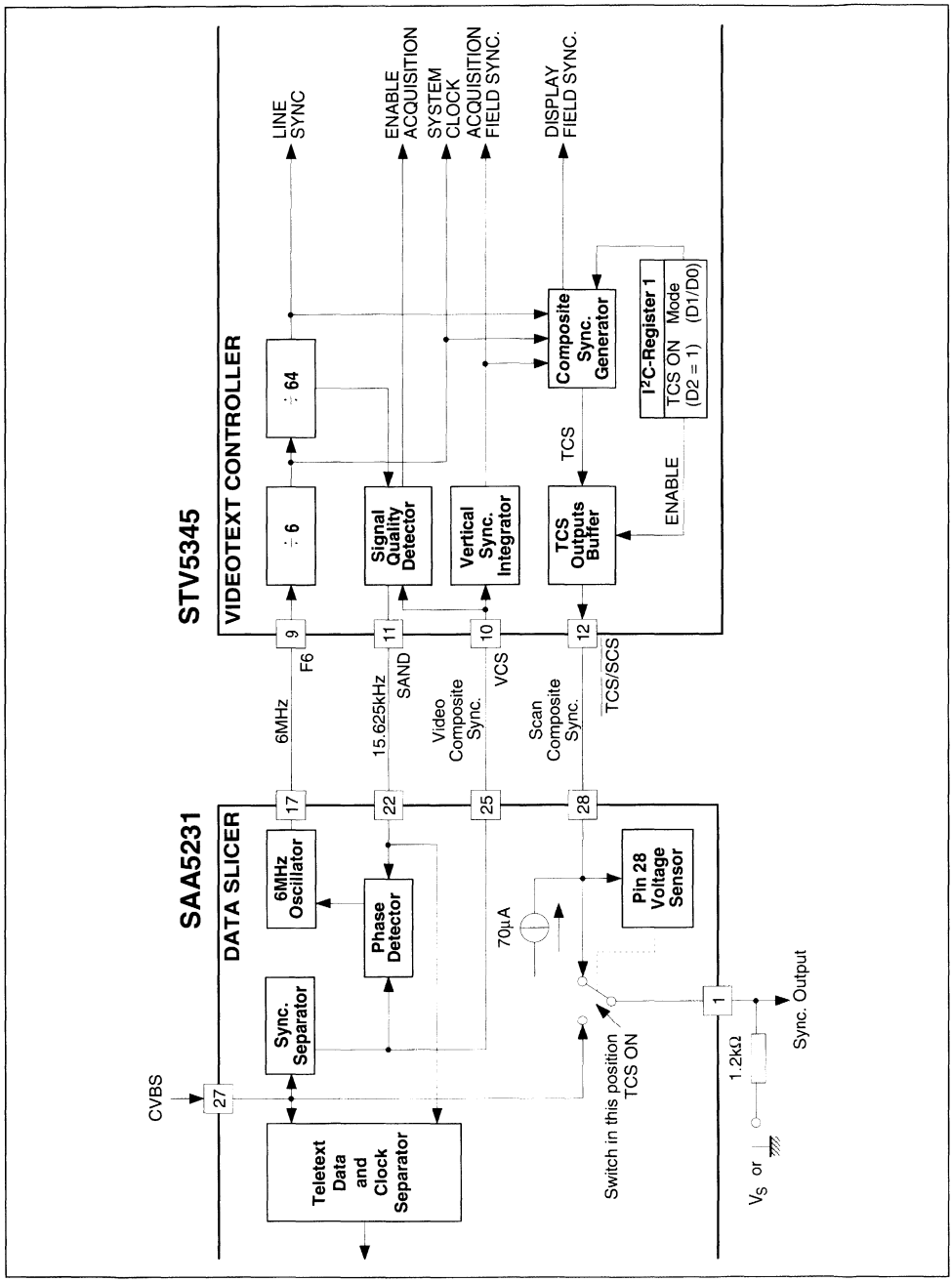
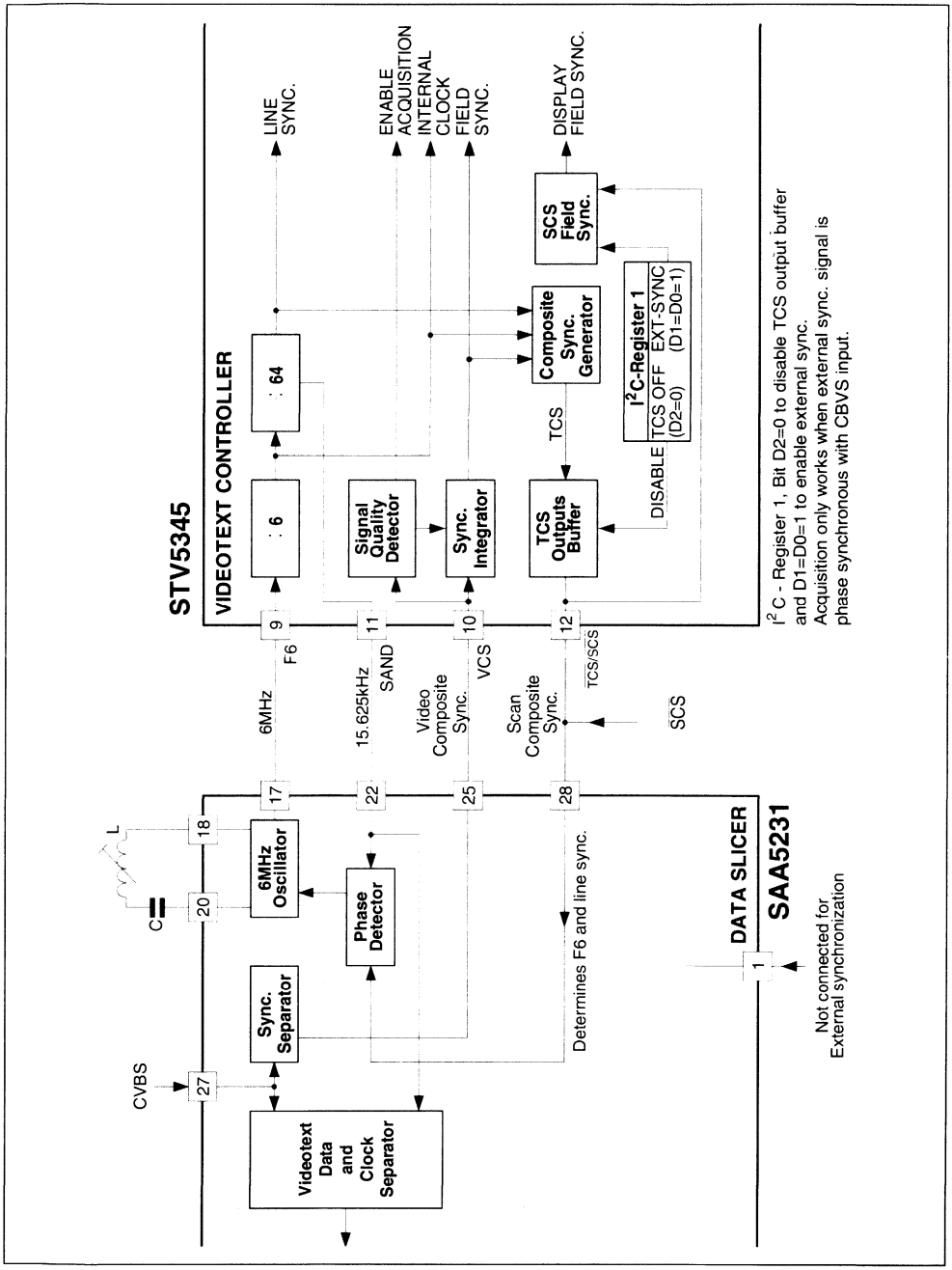
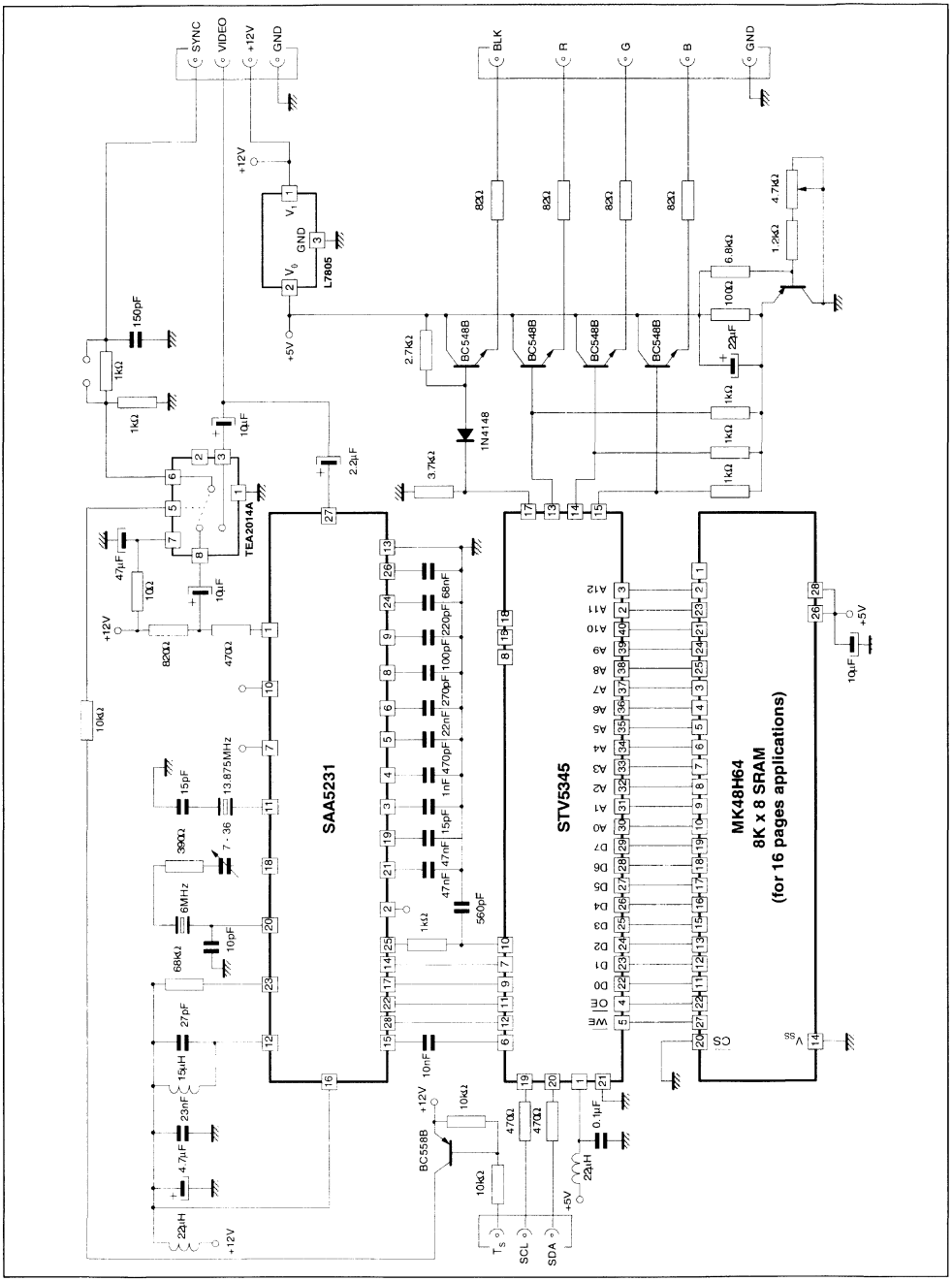


Figure 9 : Slave Synchronization Mode



APPLICATION DIAGRAM

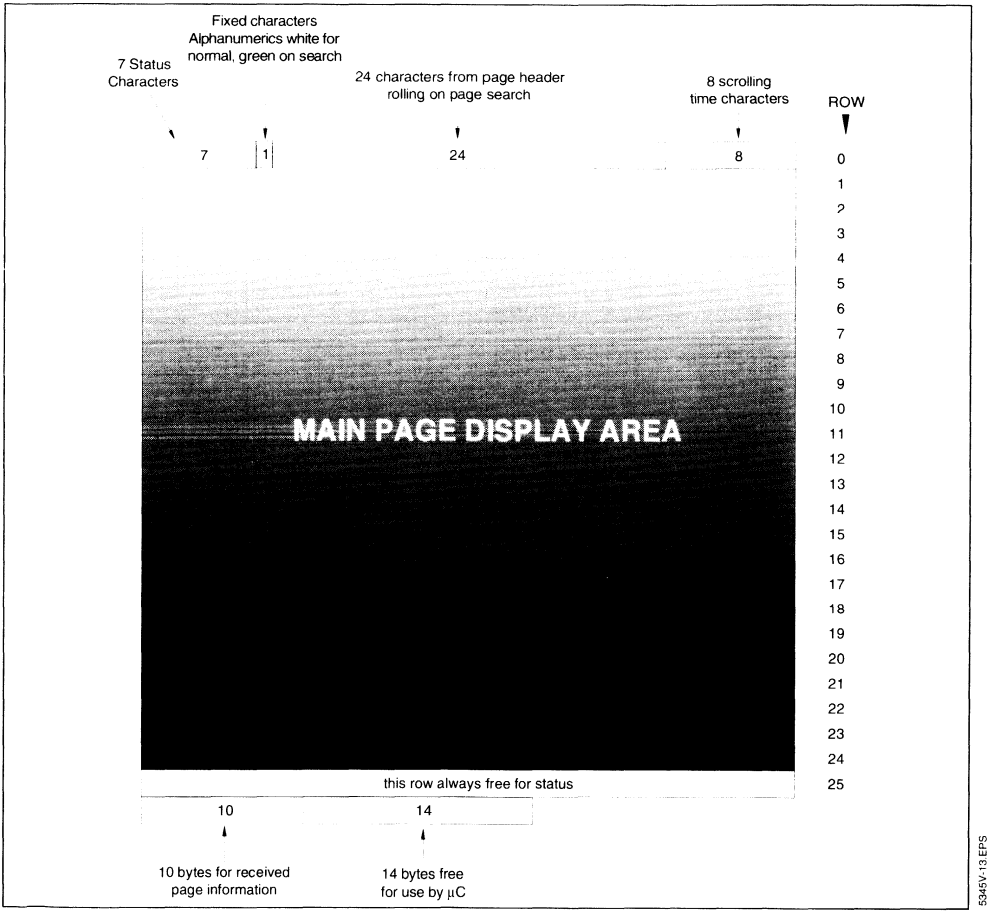


APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown in Figure 10.
The STV5345 chip provides a display format of 25 rows of 40 characters per row.
The organization is as follows :
Row zero contains the page header.
The first seven characters (0 - 6) are used for messages regarding the operational status.
The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white ; when it is "green" the operational state corresponds to "search mode" and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.
Row number twenty-four is used by the microprocessor for the display of information.
Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANISATION
Figure 10



GHOST ROW STORAGE ORGANIZATION

Row Address of Stored Data	Designation Code	Row (Packet) Number	Function
0	0 0 0 0	X / 26	Enhanced display facilities
1	0 0 0 1		
2	0 0 1 0		
3	0 0 1 1		
4	0 1 0 0		
5	0 1 0 1		
6	0 1 1 0		
7	0 1 1 1		
8	1 0 0 0		
9	1 0 0 1		
10	1 0 1 0		
11	1 0 1 1		
12	1 1 0 0		
13	1 1 0 1		
14	1 1 1 0		
15	0 0 1 0	X / 28	Page related character set
16	0 0 0 0	X / 27	Linked pages
17	0 0 0 1		
18	0 0 1 0		
19	0 0 1 1		
20		X / 24	Page extension
21		X / 25	Page extension
22	0 0 0 0	X / 28	Magazine related character set
23	X X X X	8 / 30	Broadcasting service data packet
24	Not used		
25	Not used		

Page related data stored in chapter corresponding to level 1 data, i.e. For 0 goes in 4
" 1 " " 5
" 2 " " 6
" 3 " " 7

Stored in chapter 4 only

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Table 1 : Row 25 received page control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

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Page number : - MAG = magazine, PU = page units, PT = page tens.
Page sub-code : - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

REGISTER MAP (see Table 2)

Registers R0 to R10 and R12 are write only whilst R11A is a read/write and R11B is a read only register respect to the microprocessor.
The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TA, TB and TC should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R0 to R12 are cleared to zero with the exception of bits D0 and D1 in registers R5 and R6 which are set to logical one.
After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification

D7	D6	D5	D4	D3	D2	D1	D0		
*	*	*	*	*	EVEN OFF	TC	SEL11B	R0	Mode 0
TA	7 + P/ 8 BIT	ACQ. ON/OFF	GHOST ROW ENABLE	DEW/ FULL FIELD	TCS ON	T1	T0	R1	Mode 1
BLOCK SELECT A3	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
*	*	*	*	A3	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS ROW BTM/TOP	CURSOR ON	CONCEAL/ REVEAL	TOP/ BOTTOM	SINGLE/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
*	*	*	A3	CLEAR MEM.	A2	A1	A0	R8	Active chapter
*	*	*	R4	R3	R2	R1	R0	R9	Active row
*	*	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11A	Active data
60Hz	0	0	0	0	0	0	VCS signal quality	R11B	Status
*	*	EROD	A1	A0	*	*	*	R12	Page request address

* Reserved register bits : must be set to 0

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REFRESH ON DISPLAY FUNCTION

This function allows independently to fill the memory using 3 acquisition circuits when the 4th one refreshes the displayed page.
When EROD (D5 of Reg. 12) is 0, refresh on display function is not active. Four teletext pages are filled into memory corresponding to addresses of acquisition registers.
Two blocks of 8 pages are selected with A3 (D7of Reg. 2)
Upper or lower bank of 4 pages is selected with A2 (D6 of Reg. 2).
Acquisition circuits are selected with A1/A0 (D5/D4 of Reg. 2). This 2 bits also determine the 1KByte of RAM (the chapter) allocated to each acquisition circuit.
When EROD = 1, refresh on display function is active.
3 acquisition circuits store pages as described above. The 4th one stores data into the current displayed chapter. The chapter is selected with addresses A3/A2/A1/A0 (D3/D2/D1/D0 of Reg. 4). Notice that A1/A0 (D1/D0 of Reg. 4) give the circuit number to be used to refresh this displayed chapter. That means A1/A0 of refresh on display function (D4/D3 of Reg. 12) have to be written identical to A1/A0 (D1/D0 of Reg. 4), as A2 of acquisition circuit (D6 of Reg. 2) has to be identical to A2 of displayed chapter (D2 of Reg. 4).

REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R0 Address 00H	R11 adressing and pin functions control	SEL 11B (D0)	Selection of register 11B (D0 = 1) or 11A (D0 = 0)
		TC (D1)	Test bit, must be cleared in the normal working mode
		EVEN OFF (D2)	Control of ODD/EVEN pin : EVEN signal output (D2 = 0) or grounded (D2 = 1)
R1 Address 01H	Operating mode controls	T1 T0 0 0 0 1 1 0 1 1	312/313 line MIX - mode with interlace 312/313 line TEXT - mode without interlace 312/312 line Terminal mode without interlace External synchronization TCS/SCS is an input
		TCS ON (D2)	D2 = 1, TCS output on Pin TCS/SCS D2 = 0, SCS input on Pin TCS/SCS
		DEW / FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1)
		GHOST ROW ENABLE (D4)	Selection of ghost row mode (D4 = 1)
		ACQUISITION ON / OFF (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		7 bits + parity or 8 bits without parity (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
		TA (D7)	Test bit, must be cleared in the normal working mode
R2 Address 02H	Addressing information for a page request	SC0, SC1, SC2 (D0, D1, D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit, must be cleared in the normal working mode.
		A0, A1 (D4, D5)	Address a group of four consecutive pages currently used for data acquisition;
		A2 (D6)	Address of one of the two groups of four pages for acquisition in normal mode.
		A3 (D7)	Block select: D7 = 0 internal memory, D7 = 1 external memory
R3 Address 03H	Data relative to the requested page (see Table 3)	PRD0 - PRD4 (D0 - D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4 Address 04H	Selection of one of 16 pages to display	A0, ... A3 (D0, ... D3)	These 4 bits correspond to the logical states of the 4 address lines (A10, ... A13) during memory read cycles.
R5 Address 05H	Display control for normal operation	PON (D0, D1)	Picture on (IN: D0, OUT: D1)
		TEXT (D2, D3)	Text on (IN: D2, OUT: D3)
		COR (D4, D5)	Contrast reduction on (IN: D4, OUT: D5)
		BKGND (D6, D7)	Background colour on (IN: D6, OUT: D7)
		IN / OUT	Enable inside/outside the box
R6 Address 06H	Display control for news-flash subtitle generation	See R5	See R5
R7 Address 07H	Display mode	BOX ON 0, 1-23,24 (D0, D1, D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		STATUS ROW BTM / TOP (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).
R8 to R11A Address 08H to 0BH*	Active chapter address (R8), active row address (R9), active column address (R10). Data contained in R11A read (written) from (to) memory by microprocessor via I^2C.		

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REGISTER FUNCTIONS (continued)

Register	Function	Bit(s)	Description
R11B Address 0BH*	Status	VCS Signal Quality (D0)	Good VCS quality signal detected (D0 = 1) or disturbed (D0 = 0)
		60Hz (D7)	VCS received with 60Hz frequency (D7 = 1) or 50Hz (D7 = 0). Only valid when VCS is good (D0 = 1)
R12 Address 0CH	Page request address	A0, A1 (D3, D4)	A0, A1 addresses of displayed page to refresh when using refresh on display function
		EROD (D5)	Enable refresh on displayed page function when = 1 normal acquisition storage if EROD = 0

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* Reading of R11A or R11B is determined by register 0, bit D0. Nevertheless, write operation is always performed on R11A register.

Table 3 : Register R3

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

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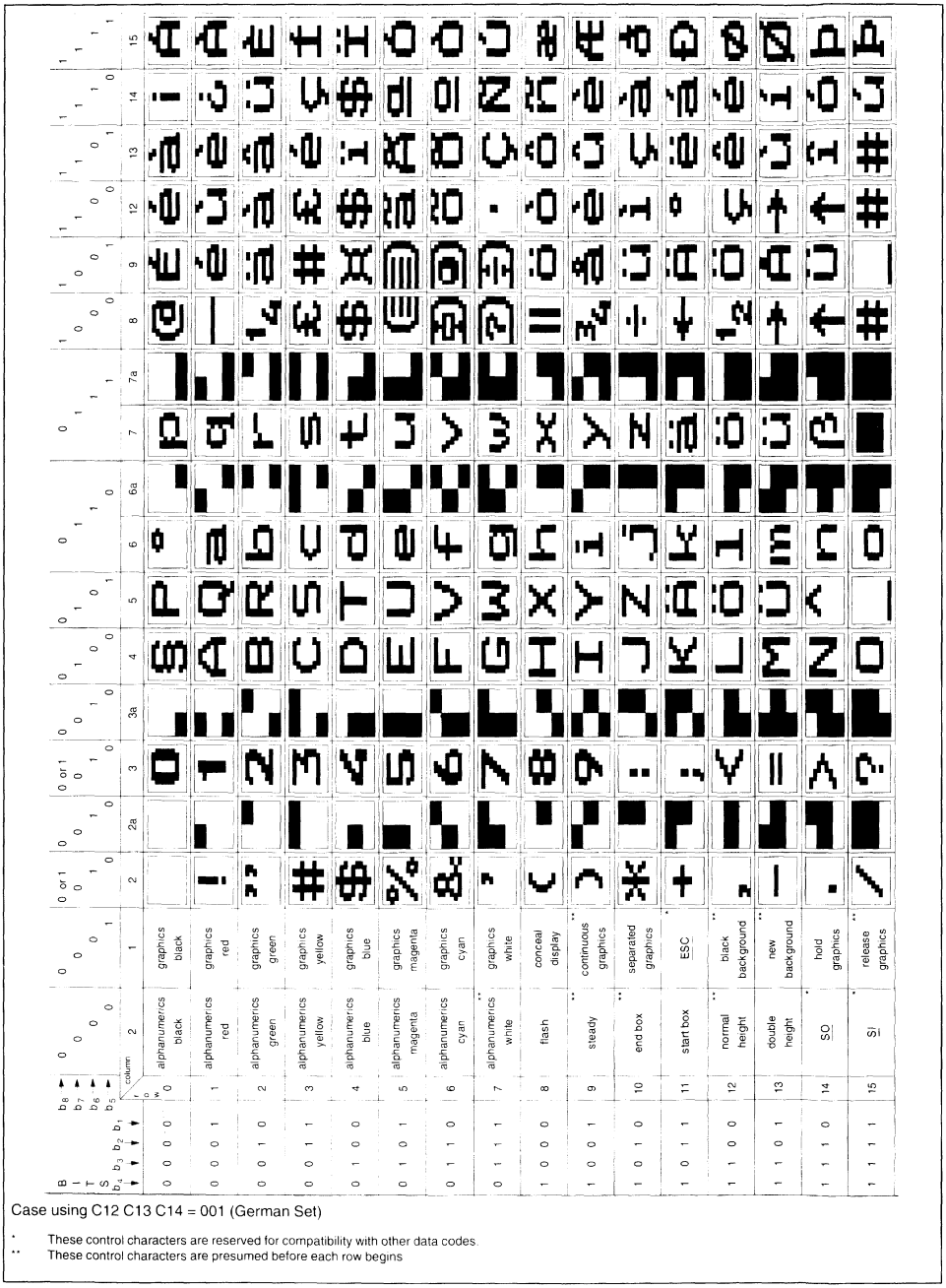
The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one defined as "timed" may be selected.
If "HOLD" is low the page is held. The addressing of successive bytes via the I^2C bus is automatic.

CHARACTER SETS

The complete character set with 8-bit decoding is given in Tables 4a, 4b and 4c.
Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.
A rectangle may be represented as follows : ▯
The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.
The 13 national characters are placed in columns with bit 8 = 0.

Table 4a : Complete character set (with 8 bit codes) - West European Languages (STV5345)



Case using C12 C13 C14 = 001 (German Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

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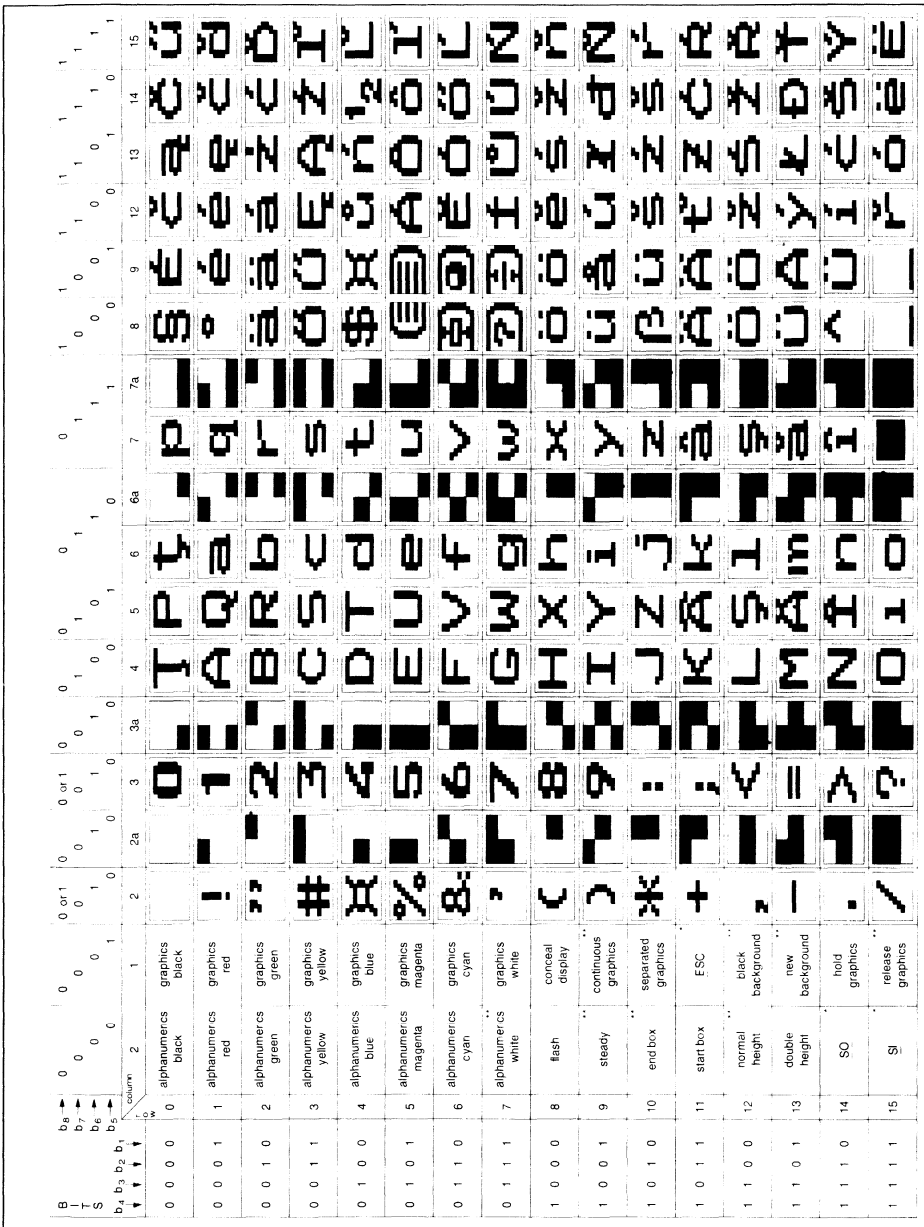
Table 4b : Complete character set (with 8 bit codes) - East European Languages (STV5345/H)



Case using C12 C13 C14 = 111 (Rumanian Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

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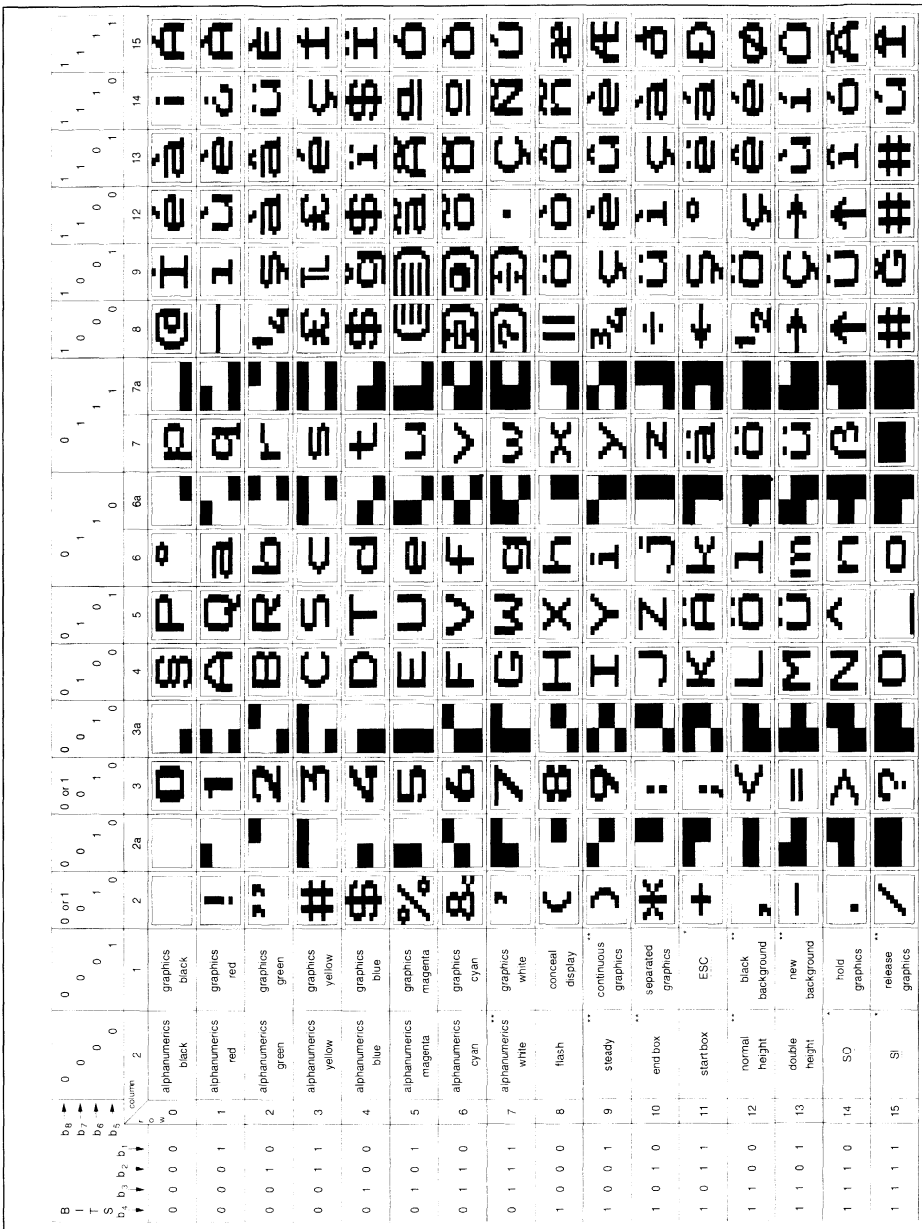
Table 4c : Complete character set (with 8 bit codes) - Turkish European Languages (STV5345/T)



Case using C12 C13 C14 = 001 (German Set)

* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

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The basic set of the 96 characters is shown in Table 5.The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Tables 6, 7 and 8.

Table 5 : Basic character set.

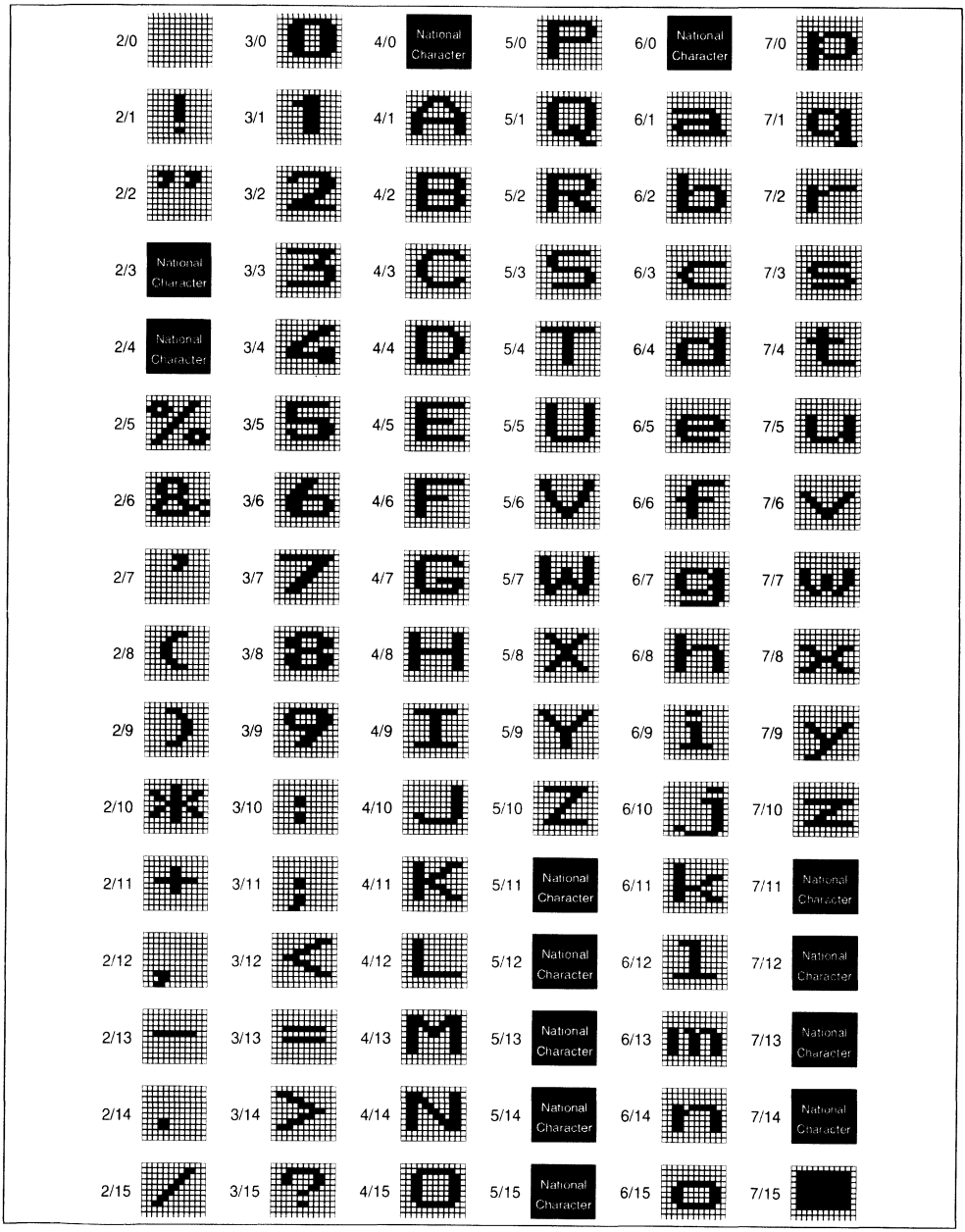
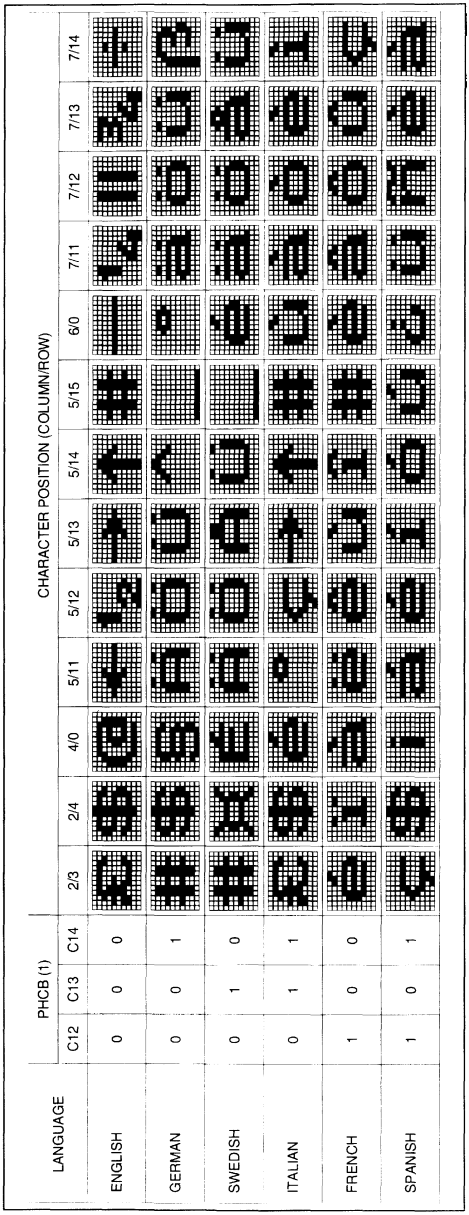
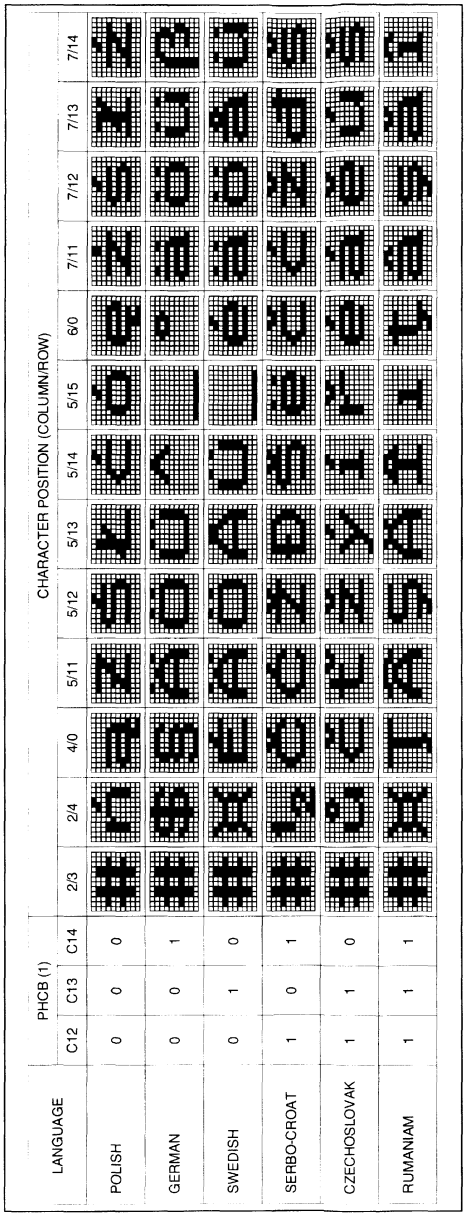


Table 6 : Character Set for SDA5243 West European Languages



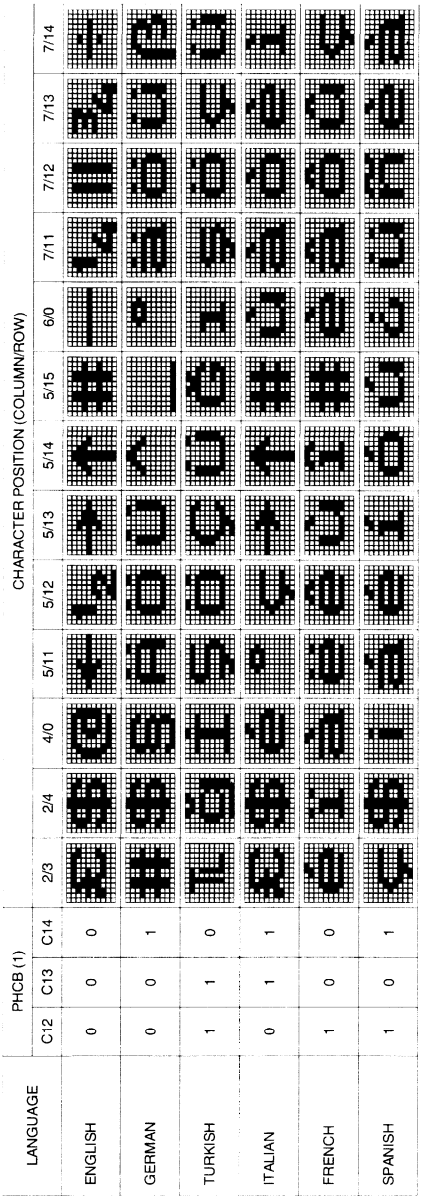
Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to English. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

Table 7 : Character Set for SDA5243 East European Languages



Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to German. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

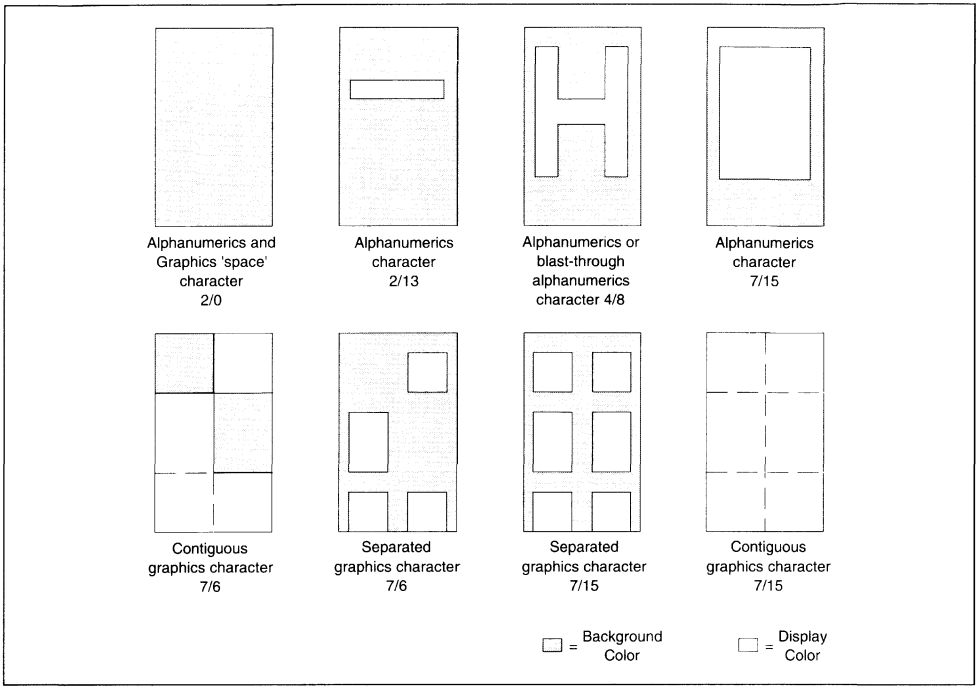
Table 8 : Character Set for SDA5243 Turkish European Languages



5345V-20.EPS

Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to Turkish. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

Figure 11 : Character Format



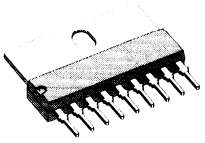
SWITCH MODE POWER SUPPLY

SGS-THOMSON MICROELECTRONICS

TDA4601

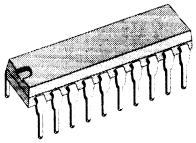
SWITCH-MODE POWER SUPPLY CONTROLLER

- LOW START-UP CURRENT
- DIRECT CONTROL OF SWITCHING TRANSISTOR
- COLLECTOR CURRENT PROPORTIONAL TO BASE-CURRENT INPUT
- REVERSE-GOING LINEAR OVERLOAD CHARACTERISTIC CURVE



SIP9
(Plastic Package)

ORDER CODE : TDA4601



DIP 9+9
(Plastic Package)

ORDER CODE : TDA4601B

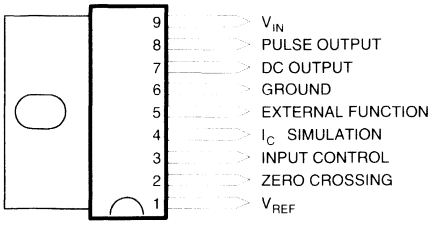
DESCRIPTION

The TDA4601 is a monolithic integrated circuit desi-gned to regulate and control the switching transistor in a switching power supply.

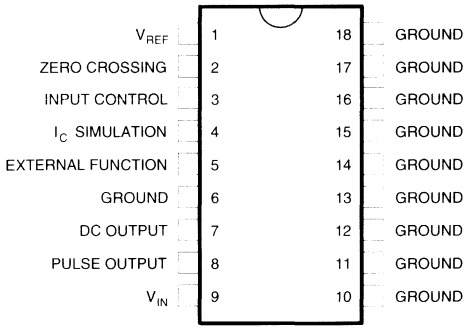
Because of its wide operational range and high vol-tage stability even at high load changes, this IC can be used not only in TV receivers and video recorders but also in power supplies in Hi-Fi sets and active speakers.

PIN CONNECTIONS

SIP9

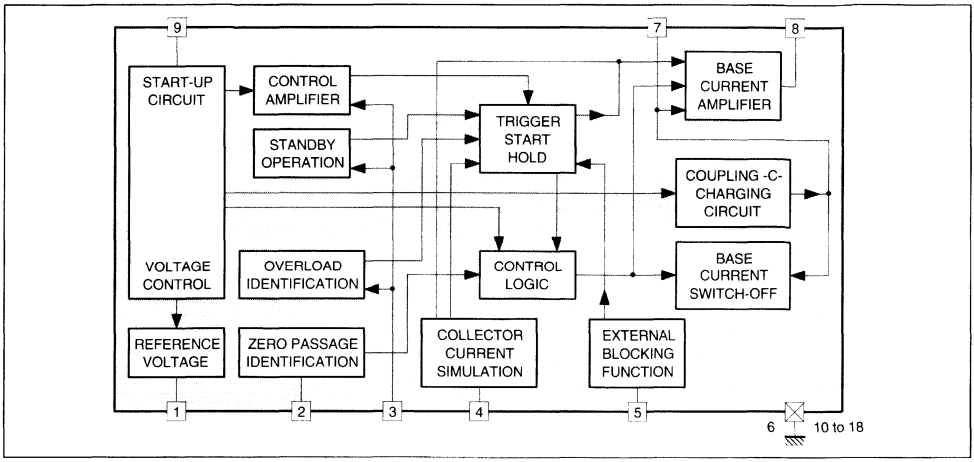


DIP 9+9



4601-01.EPS - 4601-02.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Supply Voltage	20	V
V_1	Reference Output	6	V
V_2	Identification Input	– 0.6, 0.6	V
V_3	Controlled Amplifier	3	V
V_4, V_5		8	V
V_7, V_8		V_9	
I_2, I_3		– 3, 3	mA
I_4		5	mA
I_5		5	mA
I_7		1.5	A
I_8		– 1.5	A
T_{oper}	Operating Ambient Temperature	0, 85	°C
T_{stg}	Storage Temperature	– 40, 150	°C
T_j	Junction Temperature	– 40, 125	°C

4601-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-pins	Max.	15	°C/W
$R_{th\ (j-a)}$	Thermal Resistance Junction–ambient	Max.	70	°C/W

4601-02.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_9	Operating Supply Voltage Range		7.8		18	V
START CONDITION (according to test circuit of fig. 1)						
I_9	Supply Current (V_1 not yet switched on)	V_9 = 2 V V_9 = 5 V V_9 = 10 V		 1.5 2.4	0.5 2.0 3.2	mA mA mA
V_9	Switch Threshold (V_1)		11	11.8	12.3	V

4601-03.TBL

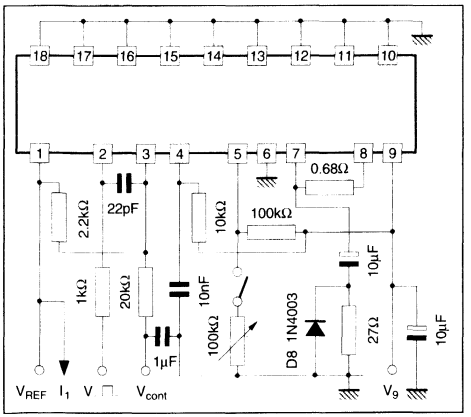
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
NORMAL OPERATION (V_9 = 10V, V_{cont} = – 10V, V_{clock} = ± 0.5V, f = 20kHz, duty cycle 1:2 after switch on)						
I_9	Supply Current	V_{cont} = – 10V V_{cont} = 0V	110 50	135 75	160 100	mA mA
V_{ref}	Voltage Reference at Pin 1	I_1 < 0.1mA I_1 = 5mA	4 4	4.2 4.2	4.5 4.4	V V
V_3	Control Voltage	V_{cont} = 0V	2.3	2.6	2.9	V
V_4	Collector Current Simulation Voltage	V_{cont} = 0V, see note 1	1.8	2.2	2.5	V
ΔV_4	Collector Current Simulation Voltage	V_{cont} = 0V to –10V, see note 1	0.3	0.4	0.5	V
V_5	External Protection Threshold		6	7	8	V
V_7	Pin 7 Output Voltage	V_{cont} = 0V, see note 1	2.7	3.3	4.0	V
V_8	Pin 8 output Voltage	V_{cont} = 0V, see note 1	2.7	3.4	4.0	V
ΔV_8	Pin 8 Output Voltage Change	V_{cont} = 0V to –10V, see note 1	1.6	2	2.4	V
V_2	Feedback Voltage	see note 1		0.2		V
T_{K1}	Reference Voltage Temperature Coefficient			10^{-3}		1/°K
PROTECTION OPERATION (V_9 = 10V ; V_{cont} = – 10V ; V_{clock} = ± 0.5V ; f = 20kHz ; duty cycle 1 : 2)						
I_9	Supply Current	$V_5 \leq 1.8$ V	14	22	28	mA
V_7	Switch–off Voltage	$V_5 \leq 1.8$ V	1.3	1.5	1.8	V
V_4	Switch-off Voltage	$V_5 \leq 1.8$ V	1.8	2.1	2.5	V
V_5	Blocking Voltage	V_{cont} = 0 V	$\frac{V_1}{2}$ – 0.1	$\frac{V_1}{2}$		V
V_9	Supply Voltage for V_8 Blocked	V_{cont} = 0 V	6.7	7.4	7.8	V
ΔV_9	Supply Voltage for V_1 off While Further Decreasing V_9		0.3	0.6	1	V
ELECTRICAL CHARACTERISTICS (according to test circuit of fig. 2)						
t_{on}	Secondary Voltage Switching Time			350	450	ms
ΔV_2	Voltage Variation with Load	S_3 Closed, P_3 = 20 W		0.1	0.5	V
		S_2 Closed, P_2 = 15 W		0.5	1	V
ΔV_2	Stand by Condition	S_1 Open P_{load} = 3 W		20	30	V
f	Stand by Frequency		70	75		kHz
P_P	Primary Power Consumption in Stand by Condition			10	12	VA

4601-04 TBL

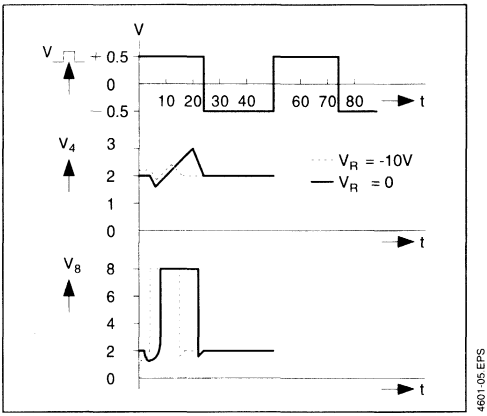
Note 1 : Only DC component

Figure 1 : Test Circuit



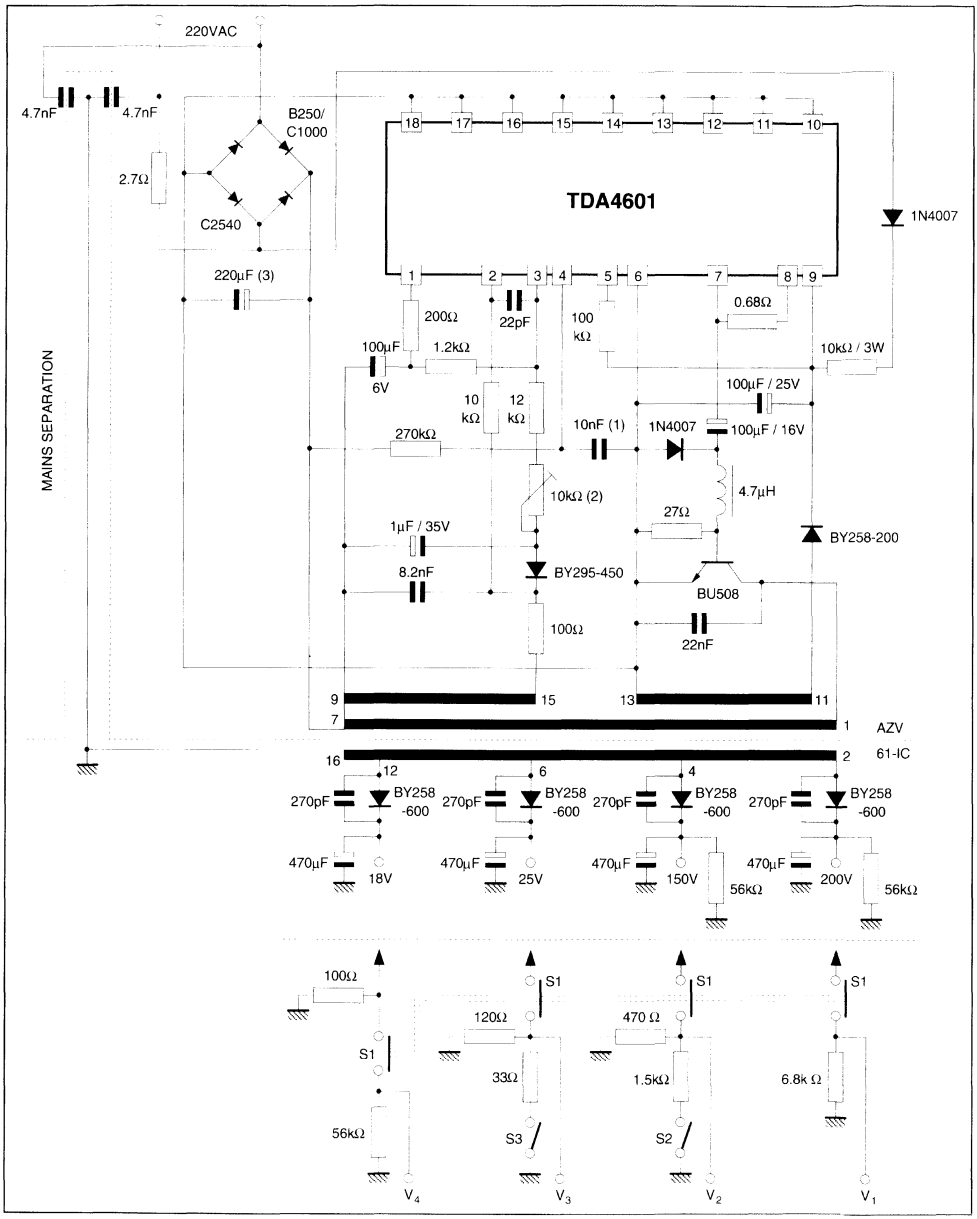
4601-04.EPS

Test Diagram : Overload Operation



4601-05.EPS

Figure 2 : Test and Application Circuit



(1) C limits the max. collector current of BU508 at overshooting the permissible output power.
(2) Adjustement of secondary voltage.
(3) Must be discharged before IC change.

CIRCUIT DESCRIPTION

The TDA4601 regulates, controls, and protects the switching transistor in reverse converter power supplies at starting, normal, and overload operation.

Starting Behaviour

During the start-up, three consecutive operation states are passed.

1. An internal reference voltage is built up which supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. Up to a supply voltage of $V_9 \approx 12V$, the current I_9 is less than 3.2mA.
2. Release of the internal reference voltage $V_1 = 4V$. This voltage is abruptly available when $V_9 \approx 12V$ and enables all parts of the IC to be supplied from the control logic with a thermally stable and overload protected current supply.
3. Release of control logic. As soon as the reference voltage is available, the control logic is switched on through an additional stabilization circuit. Thus, the IC is ready for operation.

This start-up sequence is necessary to guarantee the supply through the coupling electrolytic capacitor to the switching transistor. Correct switching of the transistor is only guaranteed in this way.

Normal Operation

Zero crossing of the feedback coil is registered at pin 2 and passed to the control logic.

At pin 3 (regulation of input, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating amplifier works with an input voltage of about 2V and a current of about 1.4 mA.

Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 and internally set threshold voltages. By increasing the capacitance (10nF) the max. collector current of the switching transistor rises, thus setting the required operating range. The extent of the regulation lies between a 2V clamped DC voltage and an AC voltage rising in a sawtooth waveform, which may vary up to a maximum amplitude of 4V (ref. voltage).

A reduction of the secondary load down to 20 watts causes the switching frequency to rise to about 50kHz at an almost constant pulse duty factor (period to on-time approx. 3). A further reduction of the secondary load down to about 1 watt results in changing the switching frequency to approx. 70kHz, and additionally the pulse duty factor rises to approx. 11. At the same time the collector peak current falls below 1A.

In the trigger the output level of the regulating amplifier, the overload recognition, and the collector current simulation are compared and instructions are given to the control logic. There is an additional triggering and blocking possibility by means of pin 5. The output at pin 8 is blocked at a voltage of less than 2.2V at pin 5.

Depending on the start-up circuit, the zero crossing identification, and the release with the aid of the trigger, the control logic flip flops are set which control the base current amplifier and the base current shut-down. The base current amplifier moves the sawtooth voltage V_4 to pin 8. A current feed-back having an external resistance of $R = 0.68\Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base driving current for the switching transistor.

Protective Measures

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6V and thus blocks driving of the switching transistor. This protective measure will be released if the voltage at pin 9 reaches a value $\leq$ typ. 7.4V or if voltages of $\leq$ typ. 2.2V occur at pin 5. In the case of a short circuit of the secondary windings of the P.S.U., the IC continuously monitors the fault condition.

With the load completely removed from the secondary winding of the P.S.U., the IC is set to a low pulse duty factor. The total power consumption of the P.S.U. is held below 6 to 10 watts in both operating conditions. After having blocked the output, caused at a supply voltage $\leq$ typ. 7.4V, a further voltage reduction with $\Delta V_9 = 0.6V$ results in switching off the reference voltage (4V).

Figure 3 : Frequency versus Output Power (Test Circuit of Figure 2)

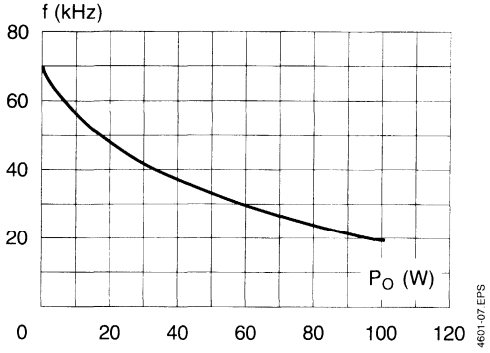


Figure 4 : Efficiency versus Output Power (Test Circuit of Figure 2)

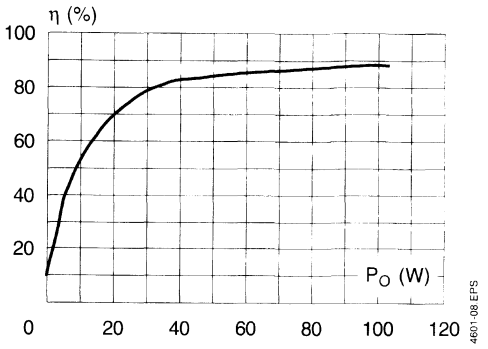


Figure 5 : Load Characteristics V_2-f (Iq2) (Test Circuit of Figure 2)

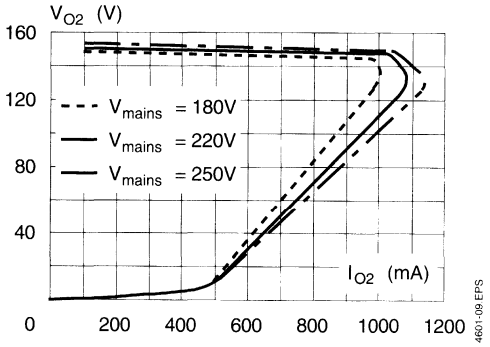


Figure 6 : Output Voltage V_2 (mains change) (Test Circuit of Figure 2)

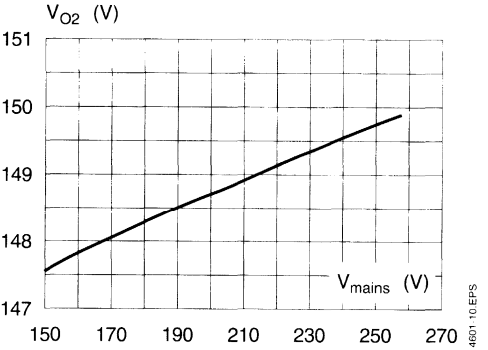
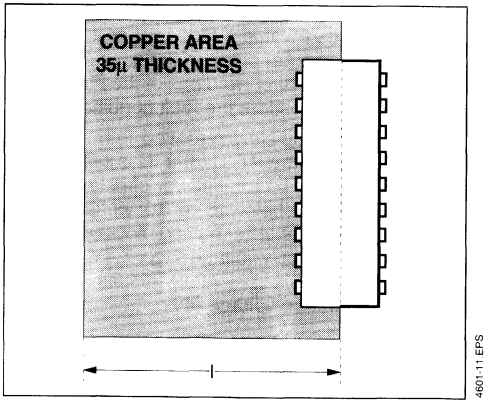


Figure 7 : Example of a PC Heatsink (35°C/W)

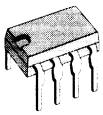


SGS-THOMSON MICROELECTRONICS

TDA4605

CONTROL CIRCUIT FOR SWITCH MODE POWER SUPPLIES USING MOS TRANSISTORS

- FOLD-BACK CHARACTERISTIC PROVIDES OVERLOAD PROTECTION FOR EXTERNAL DIODES
- BURST OPERATION UNDER SHORT-CIRCUIT AND NO LOAD CONDITIONS
- LOOP ERROR PROTECTION
- SWITCH-OFF IN CASE OF TOO LOW LINE VOLTAGE (under voltage switch-off)
- LINE VOLTAGE COMPENSATION OF OVERLOAD POINT
- SOFT-START FOR SMOOTH START-UP
- CHIP OVER-TEMPERATURE PROTECTION (thermal shutdown)
- ON-CHIP PARASITIC TRANSFORMER OSCILLATION SUPPRESSION CIRCUITRY
- DECREASE OF REGULATED VOLTAGE FOR LOW POWER CONSUMPTION



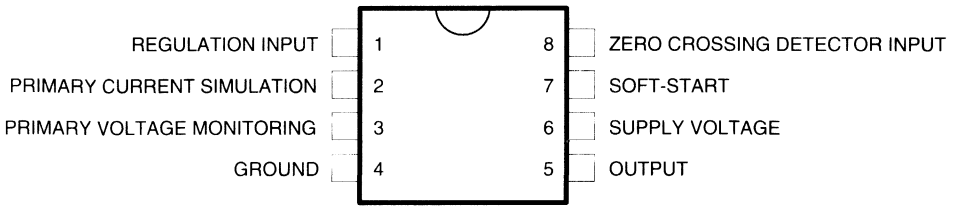
DIP8
(Plastic Package)

ORDER CODE : TDA4605

DESCRIPTION

The IC TDA4605 controls the MOS Power Transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Since good load regulation over a wide load range is attained, this IC is particularly suitable for Consumer as well as Industrial Power Supplies.

PIN CONNECTIONS



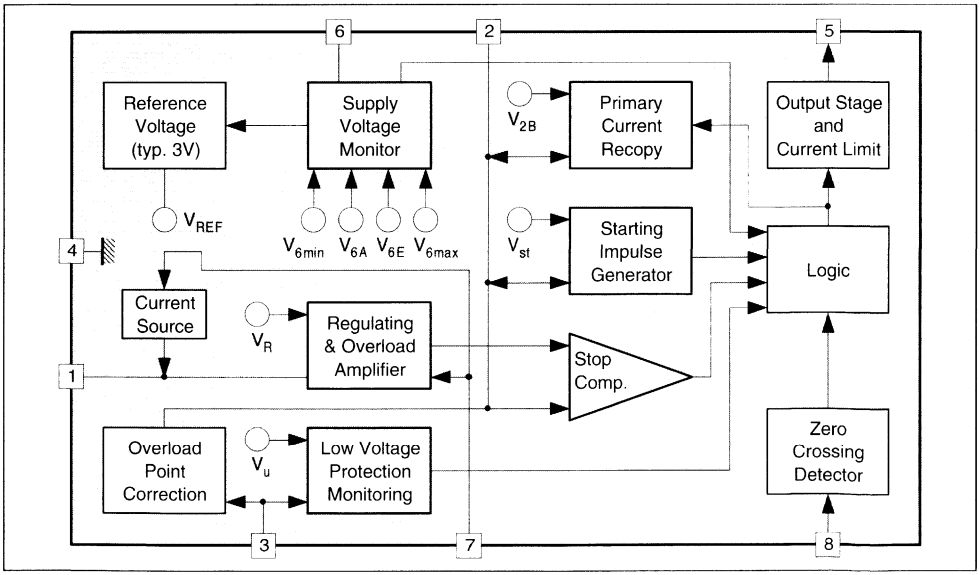
4605-01.EPS

PIN CONFIGURATION

Pin Number	Description
1	Regulating voltage : information input concerning secondary voltage. By comparing the regulating voltage obtained from the regulating winding of the transformer with the internal reference voltage, the output pulse width on Pin 5 is adapted to the load of the secondary side (normal, overload, short circuit, no load)
2	Primary current simulation : information input regarding the primary current. The primary current rise in the primary winding is simulated at Pin 2 as a voltage rise by means of external RC element. When a value is reached that is derived from the regulating voltage at Pin 1, the output pulse at Pin 5 is terminated. The RC element serves to set the maximum power at the overload point.
3	Primary voltage detector : input for primary voltage monitoring. When the line voltage is too low the IC is switched-off by comparing V_3 with an internal reference. Voltage at Pin 3 is used for overload point compensation.
4	Ground
5	Output : push-pull output for charge and discharge of the gate capacitance of the power MOS transistor.
6	Supply voltage : Supply voltage input. From it are derived a stable internal reference voltage (V_{REF}) and the switching threshold V_{6A}, V_{6E}, $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage detector. if $V_6 > V_{6E}$ the V_{REF} is switched on and switched off when $V_6 < V_{6A}$. In addition the logic is only enable for $V_{6\,min} < V_6 < V_{6\,max}$.
7	Soft-start : input for soft-start and integration network. Start-up will begin with short pulses by connecting a capacitor between Pin 7 to ground. This capacitor together with a resistor connected between Pin 7 and error amplifier output also as acts an integrator network for regulation.
8	Zero detector : Input for the oscillator feedback. After starting oscillator, every zero transit of the feedback voltage (falling edge) triggers an output pulse at Pin 5. The trigger threshold is at typically - 50mV

4605-01.TBL

BLOCK DIAGRAM



4605-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Pin	Value	Unit
V_1			1	-0.3, +3	V
V_2			2	-0.3	V
V_3	Supply Voltage		3	-0.3	V
V_4			4	-0.3	V
V_6			6	-0.3, +20	V
V_7			7	-0.3	V
I_1			1	3	mA
I_2			2	3	mA
I_3			3	3	mA
I_4	Supply Current	$t_p \leq 50\mu s$, $V \leq 0.1$	4	- 1.5	A
I_5		$t_p \leq 50\mu s$, $V \leq 0.1$	5	-0.5, +1.5	A
I_6		$t_p \leq 50\mu s$, $V \leq 0.1$	6	0.5	A
I_7			7	3	mA
I_8			8	-3, +3	mA
T_j	Junction Temperature			+125	°C
T_{stg}	Storage Temperature			-40, +125	°C

4605-02 TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	100	°C/W
$R_{th(j-c)}$	Junction-case Thermal Resistance	70	°C/W
T_{amb}	Ambient Temperature	-20, +85	°C

4605-03 TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 10V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
START-UP HYSTERESIS						
I_{6E0}	Start-up Current Drain	$V_6 = V_{6E}$		0.6	0.8	mA
V_{6E}	Switch-on Voltage		11	12	13	V
V_{6A}	Switch-off Voltage		4.5	5	5.5	V
I_{6E1}	Switch-on Current	$V_6 = V_{6E}$		11		mA
I_{6A1}	Switch-off Current	$V_6 = V_{6A}$		10		mA
VOLTAGE CLAMP (V_6 = 10V, IC Switched off)						
$V_{2(Max.)}$	At Pin 2 ($V_6 < V_{6E}$)	I_2 = 1mA	5.6	6.6	9	V
$V_{3(Max.)}$	At Pin 3 ($V_6 < V_{6E}$)	I_3 = 1mA	5.6	6.6	9	V
CONTROL RANGE						
V_{1R}	Control Input Voltage		390	410	430	mV
$-V_R$	Voltage Gain of the Control Circuit in the Control Range	$V_R = d(V_{2S} - V_{2B})/dV_1$ f = 1kHz		43		dB
PRIMARY CURRENT SIMULATION VOLTAGE						
V_{2B}	Basic Value		0.955	1.00	1.03	V
OVERLOAD RANGE AND SHORT CIRCUIT OPERATION						
V_{2O}	Peak Value in the Range of Secondary Overload	$V_1 = V_{1R}$ - 10mV	2.8	2.95	3.1	V
DV_2	Maximum Ramp Amplitude	$V_{2O} - V_{2B}$	1.82	1.95	2.08	V
V_{2S}	Peak Value in the Range of Secondary Short Circuit Operation	$V_1 = 0$	2.3	2.5	2.7	V
FOLDBACK POINT CORRECTION						
$-I_2$	Foldback Point Correction Current	V_3 = 3.7V	300	500	650	µA

4605-04 TBL

ELECTRICAL CHARACTERISTICS (V_{CC} = 10V, T_{amb} = 25°C, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GENERALLY VALID DATA (V_6 = 10V) VOLTAGE OF THE ZERO Transition DETECTOR						
V_{8P}	Positive Clamping Voltage	I_8 = 1mA		0.75		V
V_{8N}	Negative Clamping Voltage	I_8 = -1mA		-0.2		V
V_{8S}	Threshold Value		40	50		mV
TUL	Suppression of Transformer Ringing		3	3.8	4.5	µs
$-I_8$	Input Current	V_8 = 0	0		4	µV
PUSH-PULL OUTPUT STAGE SATURATION VOLTAGES						
V_{SatU}	Pin 5 Sourcing	I_5 = -0.1A		1.5	2.0	V
V_{SatU}	Pin 5 Sinking	I_5 = +0.1A		1.0	1.2	V
V_{SatU}	Pin 5 Sinking	I_5 = +0.5A		1.4	1.8	V
OUTPUT SLOW RATE						
$+dV_5/dt$	Rising Edge			70		V/µs
$-dV_5/dt$	Falling Edge			100		V/µs
REDUCTION OF CONTROL VOLTAGE						
$-I_1$	Current to reduce the Control Voltage	V_7 = 1V		50		µA
PROTECTION CIRCUIT						
$V_{6(Min.)}$	Undervoltage Protection for V_6 : Voltage at Pin 5 = $V_{5(Min.)}$ if $V_6 < V_{6(Min.)}$		7.0	7.25	7.5	V
$V_{6(Max.)}$	Overvoltage Protection for V_6 : Voltage at Pin 5 = $V_{5(Min.)}$ if $V_6 > V_{6(Max.)}$		15	16	16.5	V
V_{3A}	Undervoltage Protection for V_{AC} : Voltage at Pin 5 = $V_{5(Min.)}$ if $V_3 < V_{3A}$	V_2 = 0V	970	1005	1040	mV
Oj	Over Temperature : at the given chip temperature the IC will switch V_5 to $V_{5(Min.)}$			150		°C
V_{3Sat}	Voltage at Pin 3 if one of the protection functions was triggered ; (V_3 will be clamped until $V_6 < V_{6A}$)	I_3 = 750µA		0.4	0.8	V
I_6	Current Drain during Burst Operation	$V_3 = V_2$ = 0V		8		mA

4605-05.TBL

FUNCTIONAL DESCRIPTION

In free running fly-back converters, the TDA4605 assumes control of a MOS power transistor and all necessary regulation and monitoring functions.

The serial circuit of power transistor and primary winding of the flyback transformer is connected to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer and during the switch-off period it is fed to te load via the secondary winding. By varing the switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations.

The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle begins as soon as the energy stored in the transformer has been totally delivered to the secondary side.

In different load ranges, the SMPS will behave as follows :

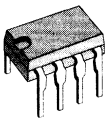
- **No-Load Operation :** The power supply unit oscillates in non continuous mode at a typical frequency of 20 to 40kHz. Depending upon the transformer winding and the regulated voltage divider, the output voltage can be slightly above the nominal value.
- **Normal Operation :** Starting from typ. 200kHz, the switching frequency falls with increasing load and decreasing AC voltage. The duty cycle depends primarily on the AC voltage. The output voltage is only slightly load-dependent.
- **Overload Point :** Maximum output power is available at this point of the output characteristics
- **Overload :** The energy transferred per operation cycle is limited at the top. Therefore, the output voltage will fall with secondary oveloading.

SGS-THOMSON MICROELECTRONICS

TEA2018A

CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP TO 0.5 A
- CURRENT LIMITATION
- TRANSFORMER DEMAGNETIZATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (< 1.6 mA)
- THERMAL PROTECTION



DIP8
(Plastic Package)

ORDER CODE : TEA2018A

DESCRIPTION

The TEA2018A is an 8-pin DIP low-cost integrated circuit designed for the control of switch mode power supplies.

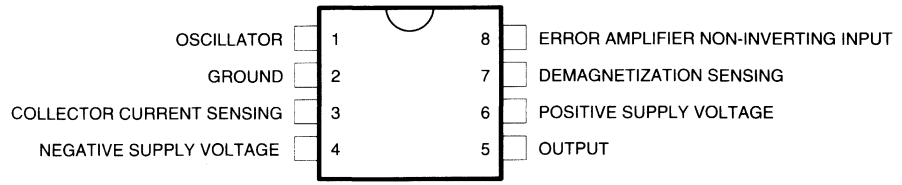
Due to its current mode regulation, the TEA2018A facilitates design of power supplies with following features :

- High stability regulation loop
- Automatic input voltage feed-forward in discontinuous mode fly-back
- Automatic pulse-by-pulse current limitation

Typical applications : Video Display Units, TV sets, typewriters, microcomputers and industrial applications

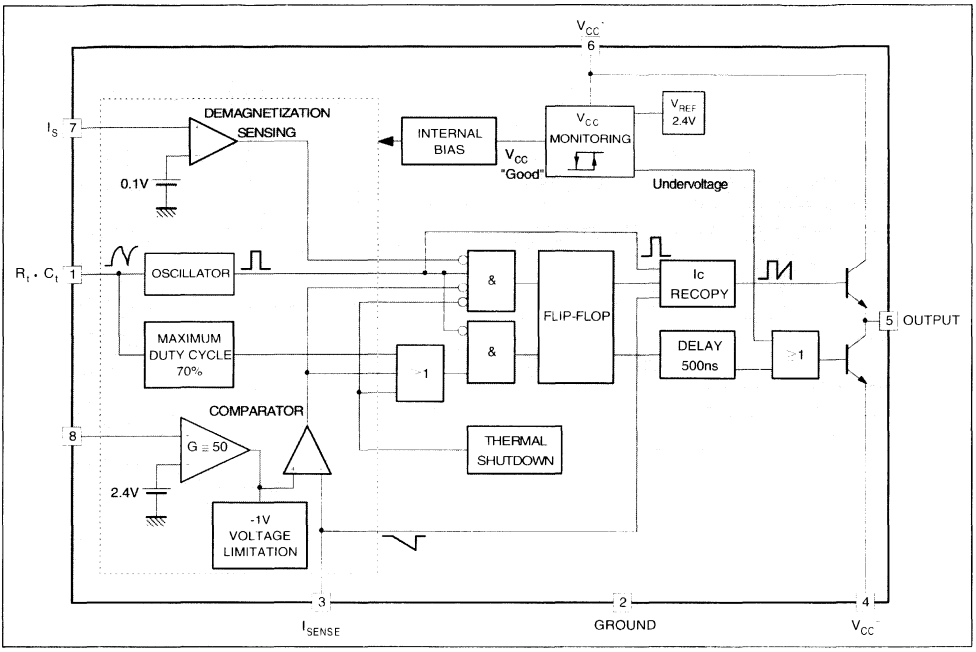
Where synchronization is required, use the TEA2019. For more details, see application note AN406/0591

PIN CONNECTIONS



2018A-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}+	Positive Supply Voltage	15	V
V_{CC}-	Negative Supply Voltage	-5	V
I_O(peak)	Peak Output Current (duty cycle < 5%)	±1	A
I_I	Input Current (Pin 3)	±5	mA
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Ambient Temperature Range	-20, +70	°C
T_{stg}	Storage Temperature Range	-40, +150	°C

2018A-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	80	°C/W

2018A-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, potentials referenced to ground (unless otherwise specified) (see test circuit)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}+	Positive Supply Voltage	6.6	8	15	V
V_{CC}-	Negative Supply Voltage	-1	-3	-5	V
$V_{CC(start)}$	Minimum Positive Supply Voltage required for starting (V_{CC}+ rising)		6	6.6	V
$V_{CC(stop)}$	Minimum Positive Voltage below wich device stops operating (V_{CC}+ falling)	4.2	4.9	5.6	V

2018A-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, potentials referenced to ground (unless otherwise specified) (see test circuit)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔV_{CC+}	Hysteresis on V_{CC+} Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Stand-by Supply Current before starting ($V_{CC+} < V_{CC(start)}$)		1	1.6	mA
$V_{th(IC)}$	Current Limitation Threshold Voltage (Pin 3)	-1100	-1000	-880	mV
$R_{(IC)}$	Collector Current Sensing Input Resistance		1000		Ω
$V_{7(th)}$	Demagnetization Sensing Threshold	75	100	125	mV
I_S	Demagnetization Sensing Input Current (Pin 7 = 0V)		1		µA
τ_{max}	Maximum Duty Cycle	60	70		%
A_V	Error Amplifier Gain		50		
I_{I+}	Error Amplifier Input Current (non-inverting input)		2		µA
V_{REF}	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
t_{OSC}	Oscillator Free-running Period (R = 59kΩ, C = 1.2nF)	44	48	52	µs
$\frac{\Delta f_{OSC}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V_{CC+} = +8V)		0.05		%/°C
$\frac{\Delta f_{OSC}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V_{CC+} (+8V < V_{CC+} < +14V)		0.5		%/V
$t_{on(min)}$	Minimum Conducting Time (C_t = 1nF)		2		µs

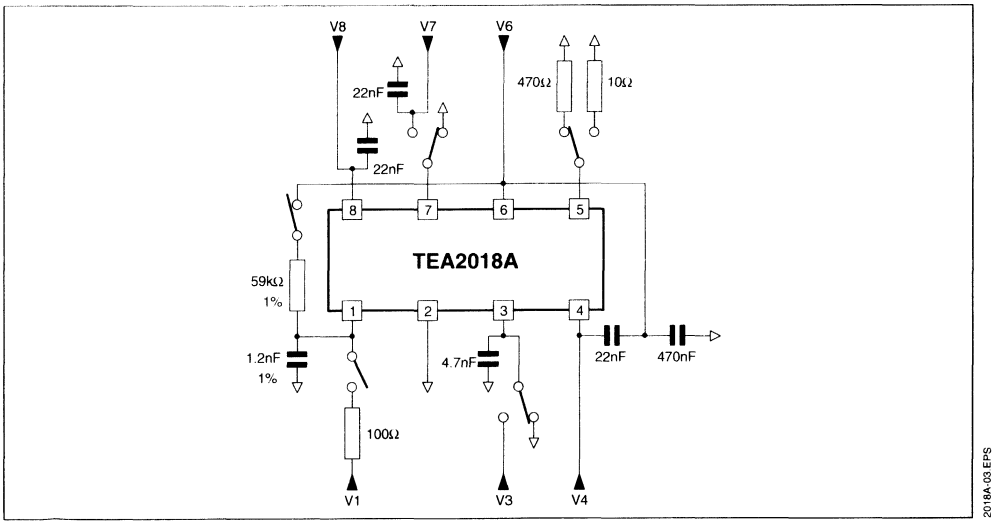
2018A-04.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC+}	Positive Supply Voltage		8		V
V_{CC-}	Negative Supply Voltage		-3		V
I_O	Output Current			0.5	A
f_{oper}	Operating Frequency		30		kHz

2018A-05.TBL

TEST CIRCUIT



2018A-03.EPS

GENERAL DESCRIPTION

(see application note AN-086)

Operating Principles (Figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator sawtooth which acts as clock signal. The period T_{osc} is given by : $T_{osc} \cong 0.66\ C_t\ (R_t + 200)$ (T_{osc} in seconds, C_t in Farad, R_t in Ω)

The end of the conduction time is determined by a signal issued from comparing the following signals :

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor,
b) the output of the error amplifier.

Base Drive

- Fast turn-on : On each period, a current pulse ensures fast transistor switch-on.
  This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.
- Proportional base drive : In order to save power, the positive base current after the starting pulse becomes an image of the collector current.
  The ratio $\frac{I_C}{I_B}$ is programmed as follows Figure 2) :

$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

- Efficient and fast switch-off : When the positive base drive is removed, 1ms (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

Safety Functions

- Overload & short-circuit protection : When the voltage applied to pin 3 exceeds the current limitation threshold voltage [$V_{th}(I_C)$], the output flip-flop is reset and the transistor is turned off. The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 3 at the maximum allowable collector current.
- Demagnetization sensing : This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized. When not used, pin 7 must be grounded.
- $t_{on(max)}$: Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70 % of the period.
- $t_{on(min)}$: A minimum conducting time is ensured during each period (see Figure 2)
- Supply voltage monitoring : The TEA2018A will stop operating if V_{CC}^+ on pin 6 falls below the threshold level $V_{CC(stop)}$

TEST CIRCUIT

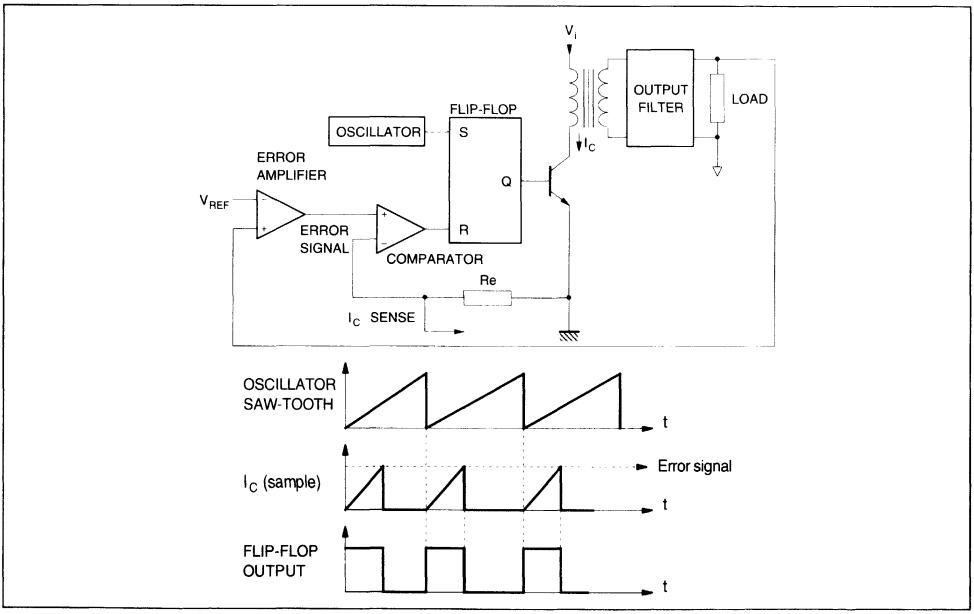
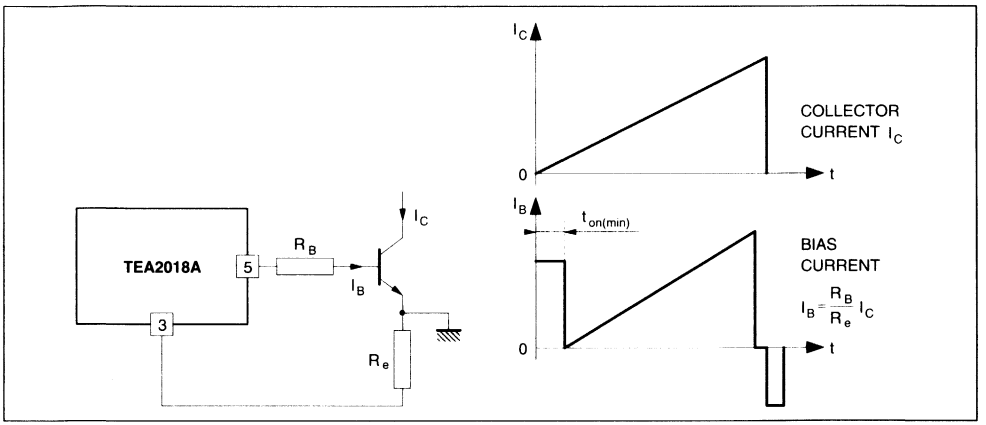
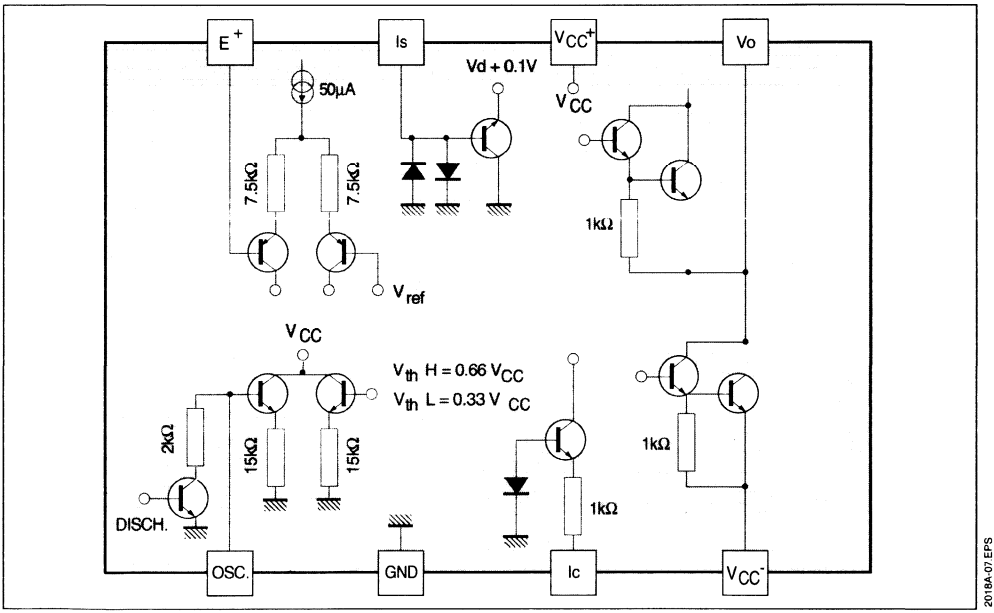


Figure 2



SCHEMATICS OF INPUTS AND OUTPUTS



Starting Process (Figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.

This current charges the power supply voltage capacitor of the device.

No output pulses are available before the voltage on pin 6 has reached the threshold level [$V_{CC(start)}$, V_{CC} rising].

During this time the TEA2018A draws only 1 mA (typically). When the voltage on pin 6 reaches this threshold, base drive pulses appear.

The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1 V (typically) (ΔV_{CC}) is implemented to avoid the device from stopping.

Figure 3 : Normal Start-up Sequence

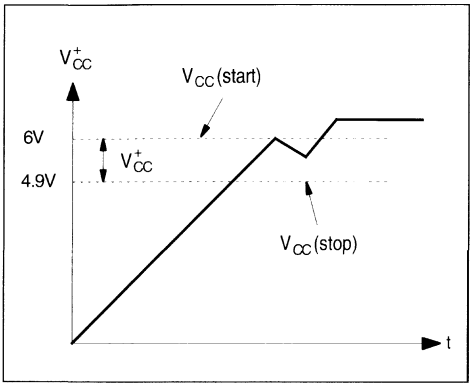
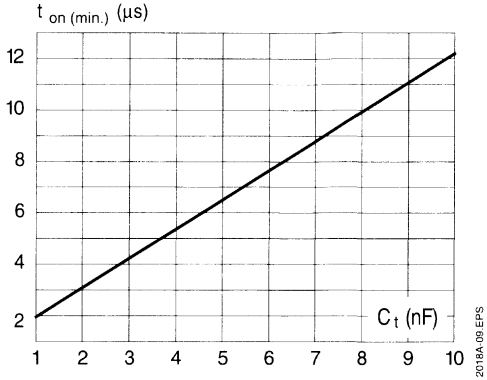
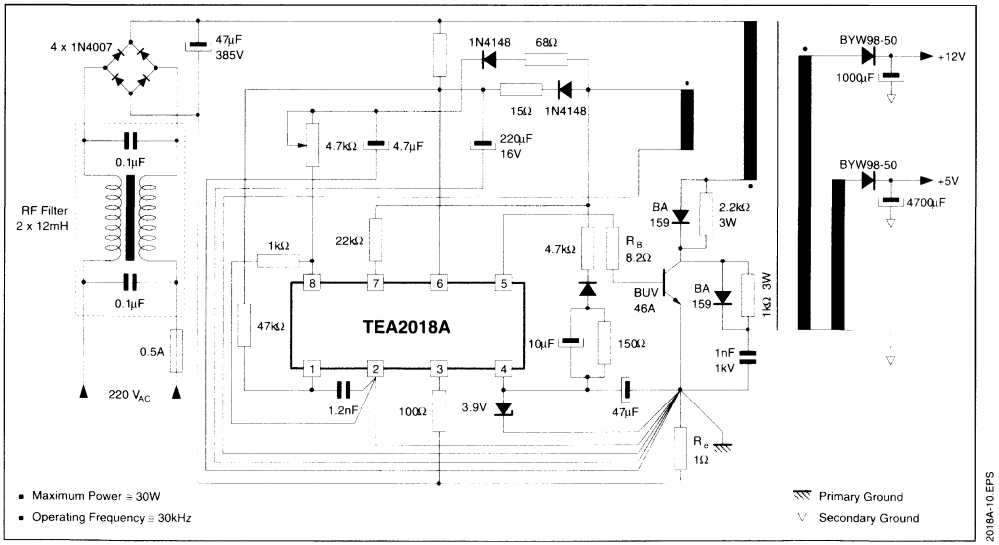


Figure 4 : $t_{ON\,(min.)}$ versus C_t



TYPICAL APPLICATION



SGS-THOMSON MICROELECTRONICS

TEA2019

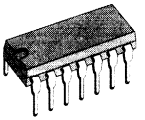
CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP TO 0.5A
- CURRENT LIMITATION
- TRANSFORMER DEMAGNETIZATION AND POWER TRANSISTOR SATURATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (1.6mA)
- SYNCHRONIZATION CAPABILITY WITH INTERNAL PLL
- THERMAL PROTECTION

Due to its current mode regulation, the TEA2019 facilitates design of power supplies with following features :

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications. For more details, see application note AN406/0591.



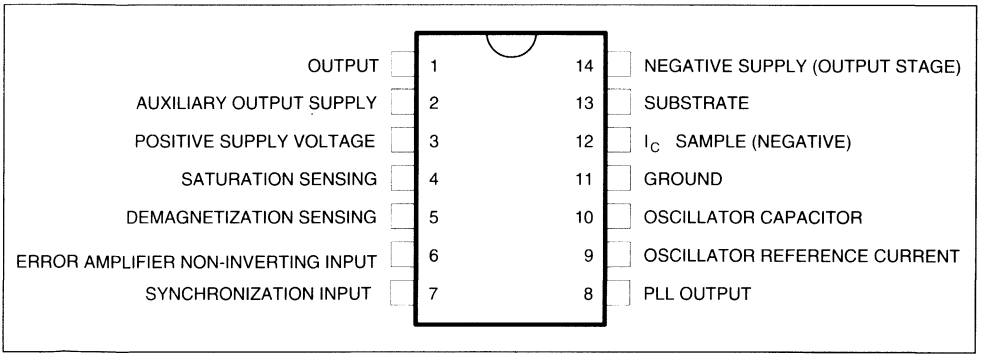
DIP 14
(Plastic package)

ORDER CODE : TEA2019

DESCRIPTION

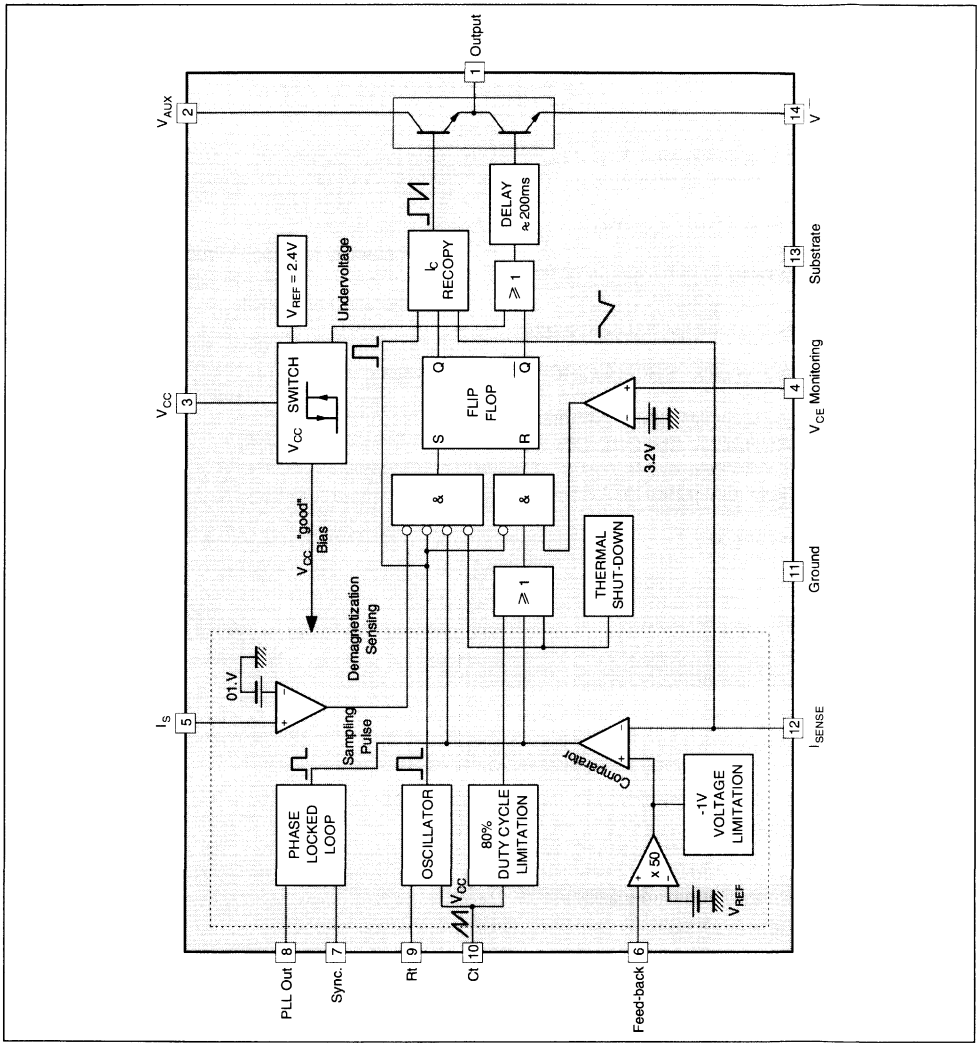
The TEA2019 is an 14-pin DIP low cost integrated circuit designed for the control of switch mode power supplies. It has the same basic functions as the TEA2018A but with synchronization capability by internal PLL. It is particularly suitable for applications where oscillator synchronization is required.

PIN CONNECTIONS



2019-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+_{CC}	Positive Supply Voltage	15	V
$V_{(aux)}$	Auxiliary Output Supply Voltage	15	V
V^-_{CC}	Negative Supply Voltage	– 5	V
I_O (peak)	Peak Output Current (duty cycle < 5%)	± 1	A
I_I	Input Current Pins 4-5	± 5	mA
T_j	Junction Temperature	150	°C
T_{oper}	Operating Ambient Temperature Range	– 20, + 70	°C
T_{stg}	Storage Temperature Range	– 40, + 150	°C

2019-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	80	°C/W

2019-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, potentials referenced to ground (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+_{CC}	Positive Supply Voltage	6.6	8	15	V
V_{CC}	Negative Supply Voltage	–1	–3	–5	V
$V_{CC(start)}$	Minimum positive supply voltage required for starting (V^+_{CC} rising)		6	6.6	V
$V_{CC(stop)}$	Minimum positive voltage below which device stops operating (V^+_{CC} falling)	4.2	4.9	5.6	V
$\Delta\ V^+_{CC}$	Hysteresis on V^+_{CC} Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Standby Supply Current Before Starting [$V^+_{CC} < V_{CC(start)}$]		1	1.6	mA
$V_{th\ (Ic)}$	Current Limitation Threshold Voltage (pin 12)	–1100	–1000	–880	mV
$R_{(Ic)}$	Collector Current Sensing Input Resistance		1000		Ω
I_S	Demagnetization Sensing Threshold	75	100	125	mV
	Demagnetization Sensing Input Current (pin 5 grounded)		1		µA
τ_{max}	Maximum Duty Cycle	70	80		%
A_V	Error Amplifier Gain		50		
I^+_I	Error Amplifier Input Current (non-inverting input) (pin 6)		2		µA
$V_{(REF)}$	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{(REF)}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
T_{OSC}	Oscillator Free-running Period (R = 59kΩ, C = 1.5nF)	60	65	70	µs
$\frac{\Delta f_{OSC}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V^+_{CC} = + 8V)		0.05		%/°C
$\frac{\Delta f_{OSC}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V^+_{CC} (+ 8V < V^+_{CC} < + 14V)		0.5		%/V
$t_{on(min)}$	Minimum Conducting Time (C_t = 1nF)		2		µs

2019-03.TBL

SYNCHRONIZATION INPUT (pin 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{7pp}	Peak to Peak Sawtooth Voltage		0.5	2.5	V
$R_{(7)}$	Input Impedance		20		kΩ

2019-04.TBL

PLL CHARACTERISTICS (see Test Circuit)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Frequency Sensitivity			100		Hz/µA
ΔT	Capture Range (T_{OSC} = 64µs Typ.)	T_{OSC} - $T_{SYN\ min}$	5.5	8		µs
		$T_{SYN\ max}$ - T_{OSC}	4.5	8		µs

2019-05.TBL

SATURATION SENSING (pin 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{(4)}$	Input Threshold		3.2		V
$I_{(4)}$	Input Current (V_4 > 3.2V)	50			µA
	Input Internal Resistance		1		kΩ

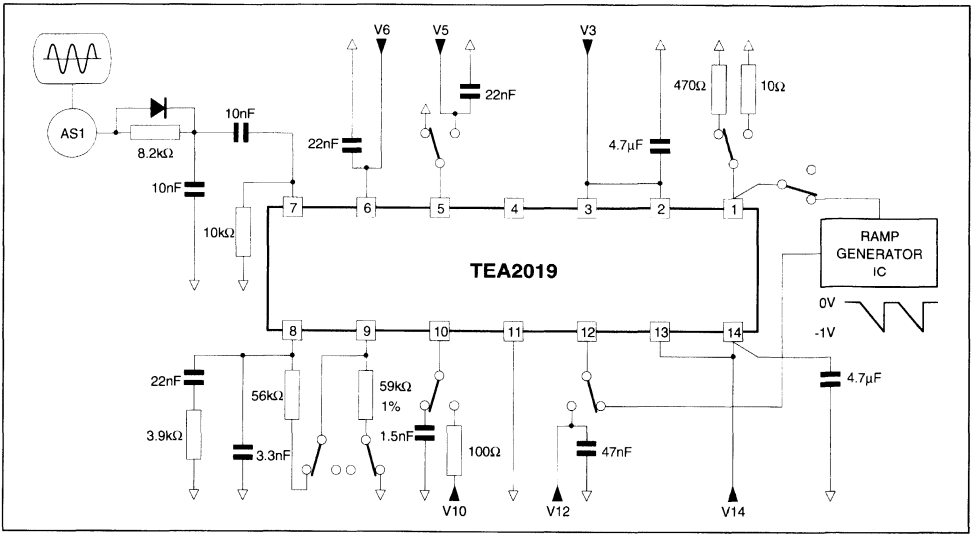
2019-06.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+_{CC}	Positive Supply Voltage		8		V
V_{CC}	Negative Supply Voltage		3		V
I_O	Output Current			0.5	A
F_{oper}	Operating Frequency		30		kHz

2019-07.TBL

TYPICAL CIRCUIT



GENERAL DESCRIPTION
(see application note AN406/0591)

OPERATING PRINCIPLES (Figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator saw-tooth which acts as clock signal. The period T_{osc} is given by :

$T_{osc} \approx 0.69\ C_t\ (R_t + 2000)$

(T_{osc} in seconds, C_t in Farad, R_t in Ω)

The end of the conduction time is determined by a signal issued from comparing the following signals.

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor.
b) the output of the error amplifier.

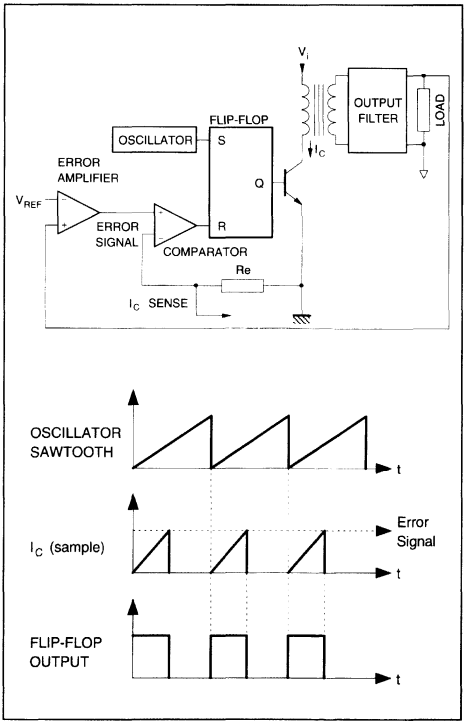
BASE DRIVE

- Fast turn-on
  On each period, a current pulse ensures fast transistor switch-on.
  This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.
- Proportional base drive
  In order to save power, the positive base current after the starting pulse becomes an image of the collector current.

The ratio $\frac{I_C}{I_B}$ is programmed as follows (Figure 2).

$$\frac{I_C}{I_B} = \frac{R_B}{R_E}$$

Figure 1 : Current Mode Control



- Efficient and fast switch-off
  When the positive base drive is removed, 1s (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

SAFETY FUNCTIONS

- Overload & short-circuit protection
  When the voltage applied to pin 12 exceeds the current limitation thershold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.

  The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 12 at the maximum allowable collector current.

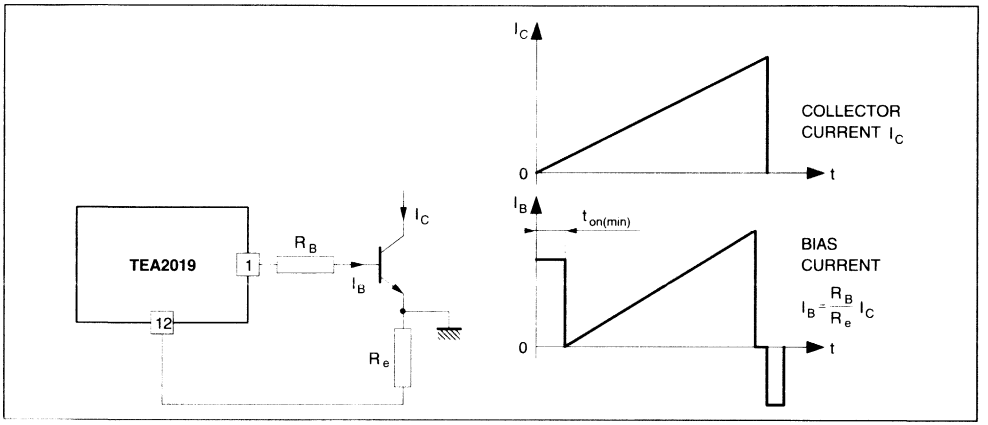
- Demagnetization sensing
  This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.
  When not used, pin 5 must be grounded.

- $t_{on(max)}$
  Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.

- $t_{on(min)}$
  A minimum conducting time is ensured during each period (see Figure 2).

- Supply voltage monitoring
  The TEA2019 will stop operating if V_{CC}+ on Pin 3 falls below the threshold level $V_{CC(stop)}$.

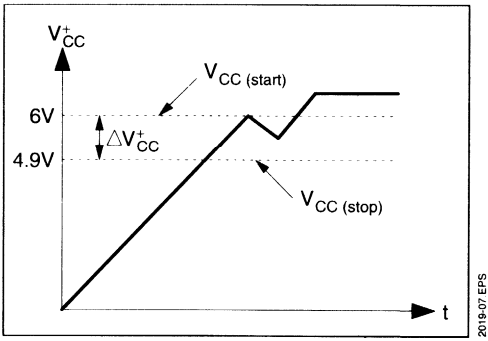
Figure 2



STARTING PROCESS (Figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.
This current charges the power supply storage capacitor of the device.
No output pulses are available before the voltage on pin 3 has reached the threshold level [$V_{CC(start)}$, V^+_{CC} rising].
During this time the TEA2019 draws only 1mA (typically). When the voltage on pin 3 reaches this threshold base drive pulses appear.
The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1V (typically) (ΔV_{CC}) is implemented to avoid the device from stopping.

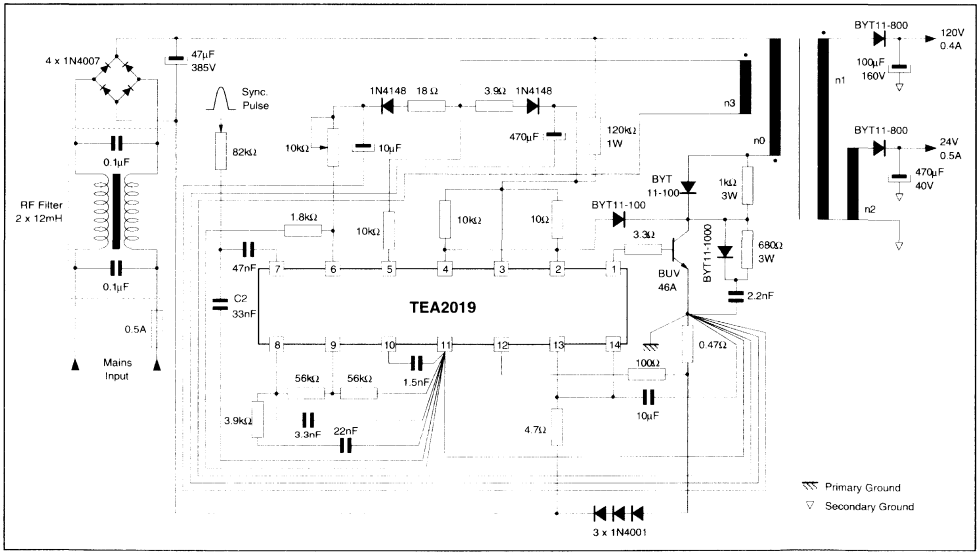
Figure 3 : Normal TEA2019 Start up Sequence



The TEA2019 has some additional capabilities compared to the TEA2018A :

- The oscillator charge current its supplied through an internal current generator, programmed externally - instead of using an external charging resistor. The sawtooth so obtained is linear.
- The oscillator can be synchronized through an internal PLL circuit. This feature provides synchronization between the external sync pulse and the end of the switching transistor current. The sync pulse can be for example the fly-back pulse of a TV horizontal sweep circuit. As indicated in the application diagram, this pulse is applied first to a R.C. network to obtain a low voltage sawtooth and then to pin 7 of the circuit. The PLL output (pin 8) supplies a correction current to pin 9 through an external resistor, so as to maintain the oscillator at the correct frequency (refer to application note AN406/0591 for detailed information).
- In the TEA2019, the power supply of the positive output stage is separated from the main power supply, so that it can be supplied from a lower voltage in order to reduce the I.C. power dissipation.
  For low power applications, the circuit can be normally supplied by connecting pins 2 and 3 together.
- In order to protect the substrate (pin 13) from the parasitic voltage peaks produced by negative output current peaks at pin 14, the substrate (pin 13) is internally separated from the negative supply (pin 14). They must be externally connected together.
- The switching transistor saturation voltage can be monitored at pin 4. To achieve this, a high voltage diode must be connected between the collector of the switching transistor and pin 4. Also a resistor must be connected from pin 4 to V^{+}_{CC} (see application diagram). This arrangement is useful when the chosen value of base current is very low and as a consequence the saturation voltage will be high. In this event, when $V_{CE(sat)}$ increases above 2.5V, the base current is interrupted before the normal end of the period.
  Remark : the TEA2019 can also operate without this protection.

TYPICAL APPLICATION

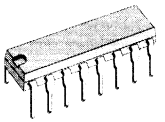


- P_{MAX} = 60W
- Free-running Frequency : 15kHz
- $155V_{RMS} \leq V_{AC} \leq 250V_{RMS}$
- Outputs: 120V ± 3%, 0.4A
  24V ±3%, 0.5A
- V_{CE} Monitoring

TEA2260
TEA2261

SWITCH MODE POWER SUPPLY CONTROLLER

- POSITIVE AND NEGATIVE CURRENT UP TO 1.2A and – 2A
- LOW START-UP CURRENT
- DIRECT DRIVE OF THE POWER TRANSISTOR
- TWO LEVELS TRANSISTOR CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- SOFT-STARTING
- UNDER AND OVERVOLTAGE LOCK-OUT
- AUTOMATIC STAND-BY MODE RECOGNITION
- LARGE POWER RANGE CAPABILITY IN STAND-BY (Burst mode)
- INTERNAL PWM SIGNAL GENERATOR



BATWING DIP 16
(Plastic Package)

ORDER CODES : TEA2260 - TEA2261

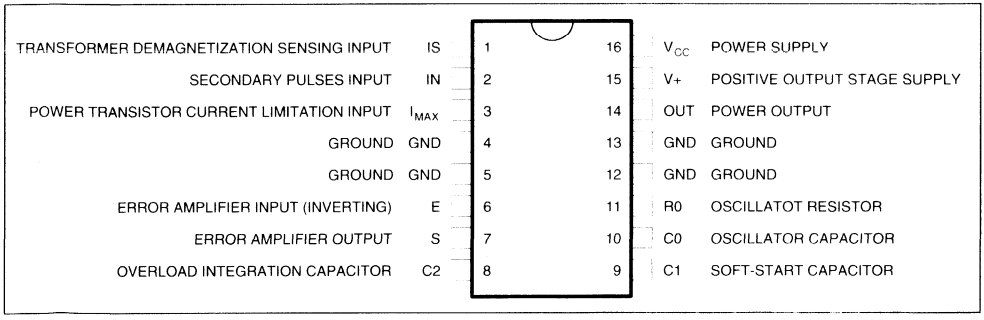
DESCRIPTION

The TEA2260/61 is a monolithic integrated circuit for the use in primary part of an off-line switching mode power supply.

All functions required for SMPS control under normal operating, transient or abnormal conditions are provided.

The capability of working according to the "master-slave" concept, or according to the "primary regulation" mode makes the TEA2260/61 very flexible and easy to use. This is particularly true for TV receivers where the IC provides an attractive and low cost solution (no need of stand-by auxiliary power supply). See application note AN376/0490 for detailed information.

PIN CONNECTIONS



2261-01.EPS

SIMPLIFIED APPLICATION DIAGRAMS

Figure 1 : Master-slave Concept

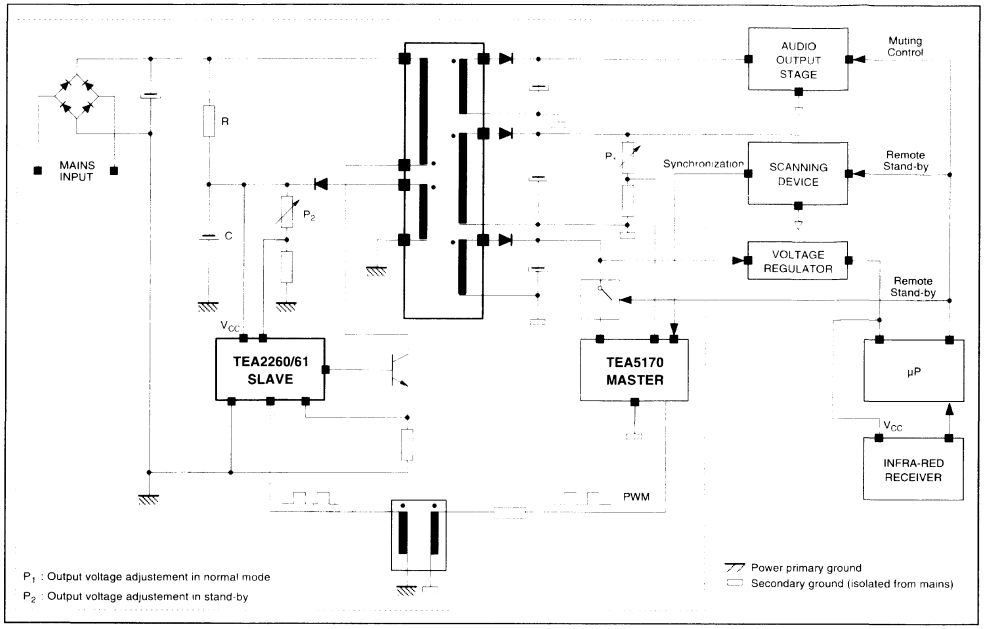
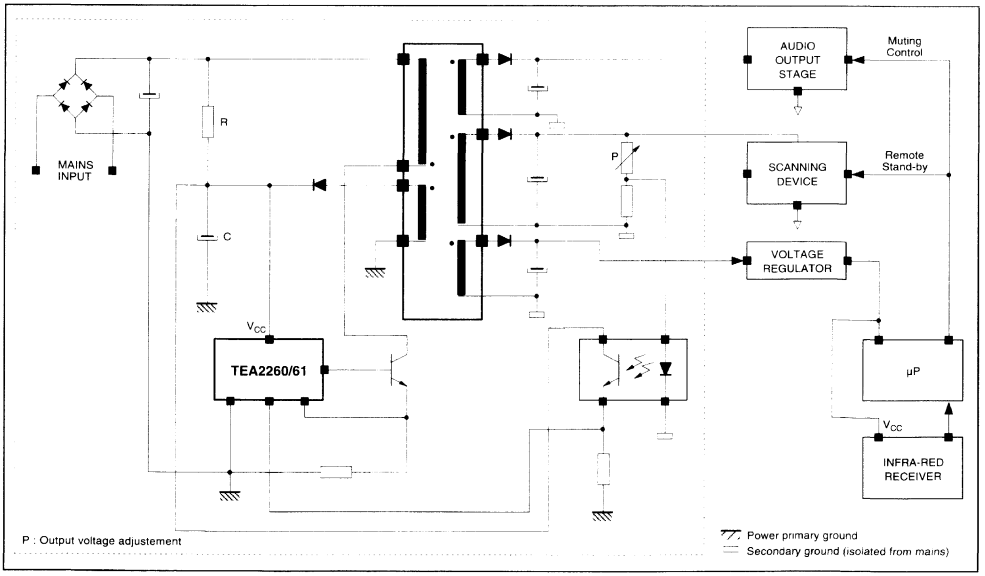
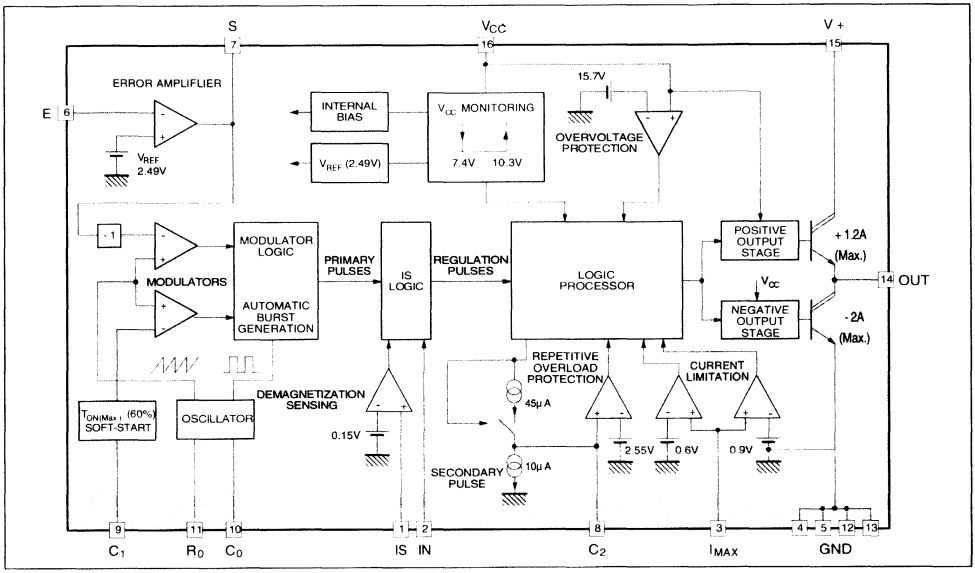


Figure 2 : Secondary Regulation (with optocoupler)



BLOCK DIAGRAM



2261-04.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply	V16-V4, 5, 12, 13	20	V
V+	Output Stage Power Supply	V15-V4, 5, 12, 13	20	V
I_{OUT+}	Positive Output Current (source current)		1.5	A
I_{OUT-}	Negative Output Current (sink current)		2.5	A
T_j	Operating Junction Temperature		150	°C
T_{stg}	Storage Temperature Range		-40, +150	°C

2261-01.TBL

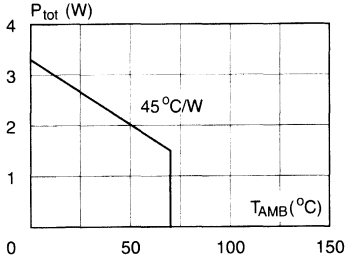
THERMAL DATA

$R_{th\ (j-c)}$	Junction-case Thermal Resistance	11	°C/W
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	45	°C/W

2261-02.TBL

* Soldered on a 35µm, 40cm² board copper area.

MAXIMUM POWER DISSIPATION



2261-05.EPS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	V_{CC} stop	12	V_{CC} max	V
I_{OUT+}	Positive Output Current (source current)			1.2	A
I_{OUT-}	Negative Output Current (sink current)			2.0	A
I_{OUT+}	Average Positive Output Current			0.6	A
I_{OUT-}	Average Negative Output Current			0.6	A
F_{oper}	Operating Frequency	10		100	kHz
V_{IN}	Input Pulses Amplitude (Pin 2)	1.5	2.5	4.5	V
R_{OSC}	Oscillator Resistor Range	20		150	kΩ
C_{OSC}	Oscillator Capacitor Range	0.47		4.7	nF
C1	Soft-starting Capacitor Range	0.047	1		µF
C2	Overload Integration Capacitor	0.047	1		µF
C2/C1	Ratio C2/C1 (C2 must be ≥ C1)	1			
T_{amb}	Operating Ambient Temperature	-20		70	°C

2261-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} =12V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY					
$V_{CC(start)}$	Starting Voltage (V_{CC} increasing)	9.3	10.3	11.3	V
$V_{CC(stop)}$	Stopping Voltage (V_{CC} decreasing)	6.4	7.4	8.4	V
Hyst V_{CC}	Hysteresis ($V_{CC(start)}$ - $V_{CC(Stop)}$)	2.4	2.9		V
$I_{CC(start)}$	Starting Current (V_{CC} = 9V)		0.7	1.4	mA
I_{CC}	Supply Current (V_{CC} = 12V)		7.5	15	mA
$V_{CC(max)}$	Overvoltage Threshold on V_{CC}	15	15.7		V
$I_{CC(over)}$	Supply Current after Overvoltage Detection (V_{CC} = 17V)	26	35	42	mA
OSCILLATOR / PWM SECTION					
$\frac{\text{Delta F}}{F}$	Accuracy (R_{OSC} = 68kΩ, C_{OSC} = 1nF)		10		%
t_{ON} max	Maximum Duty Cycle in Primary Regulation Mode	50	60	70	%
ERROR AMPLIFIER SECTION					
A_{VO}	Open Loop Gain		75		dB
F_{ug}	Unity Gain Frequency		550		kHz
I_{SC}	Short Circuit Output Current (Pin 7 connected to ground)		2		mA
I_{BE}	E Input Bias Current (Pin 6)		0.08		µA
V_{REF}	Internal Voltage Reference (connected to error amplifier input and not directly accessible)	2.34	2.49	2.64	V
INPUT SECTION					
V_{IN}	IN Input Threshold (Pin 2)	0.6	0.85	1.2	V
V_{IS}	IS Input Threshold (Pin 1)		0.15		V
I_{BIN}	IN Input Bias Current		0.3		µA
I_{BIS}	IS Input Bias Current		0.4		µA
CURRENT LIMITATION SECTION					
V_{IM1}	First Current Limitation Threshold	558	600	642	mV
V_{IM2}	Second Current Limitation Threshold	837	900	963	mV
ΔV_{IM}	Thresholds Difference V_{IM2} - V_{IM1}		300		mV
V_{C2}	Lock-out Threshold on Pin C2	2.25	2.55	2.85	V
I_{DC2}	Capacitor C2 Discharge Current		10		µA
I_{CC2}	Capacitor C2 Charge Current		45		µA
$I_{BI(max)}$	Maximum Input Bias Current (Pin 3)		0.2		µA

2261-04.TBL

GENERAL DESCRIPTION

The TEA2260/61 is an off-line switch mode power supply controller. The synchronization function and the specific operation in stand-by mode make it well adapted to video applications such as TV sets, VCRs, monitors, etc...

The TEA2260/61 can be used in two types of architectures :

- Master/slave architecture. In this case, the TEA2260/61 drives the power transistor according to the pulse width modulated signals generated by the secondary located master circuit. A pulse transformer provides the feedback (see Figure 1).
- Conventional architecture with linear feedback signal (feedback sources : optocoupler or transformer winding) (see Figure 2).

Using the TEA2260/61, the stand-by auxiliary power supply, often realized with a small but costly 50Hz transformer, is no longer necessary. The burst mode operation of the TEA2260/61 makes possible the control of very low output power (down to less than 1W) with the main power transformer.

When used in a master/slave architecture, the TEA2260/61 and also the power transistor turn-off can be easily synchronized with the line transformer. The switching noise cannot disturb the picture in this case.

As an S.M.P.S. controller, the TEA2260/61 features the following functions :

- Power supply start-up (with soft-start)
- PWM generator
- Direct power transistor drive (+1.2A, -2.0A)
- Safety functions : pulse by pulse current limitation, output power limitation, over and under voltage lock-out.

S.M.P.S. OPERATING DESCRIPTION

Starting Mode - Stand By Mode

Power for circuit supply is taken from the mains through a high value resistor before starting. As long as V_{CC} of the TEA2260/61 is below V_{CC} start, the quiescent current is very low (typically 0.7mA) and the electrolytic capacitor across V_{CC} is linearly charged. When V_{CC} reaches V_{CC} start (typically 10.3V), the circuit starts, generating output pulses with a soft-starting. Then the SMPS goes into the stand-by mode and the output voltage is a percentage of the nominal output voltage (eg. 80%).

For this the TEA2260/61 contains all the functions required for primary mode regulation : a fixed frequency oscillator, a voltage reference, an error amplifier and a pulse width modulator (PWM).

For transmission of low power with a good efficiency in stand-by, an automatic burst generation system is used, in order to avoid audible noise.

Normal Mode (secondary regulation)

The normal operating of the TV set is obtained by sending to the TEA2260/61 regulation pulses generated by a regulator located in the secondary side of the power supply.

This architecture uses the "Master-slave Concept", advantages of which are now well-known especially the very high efficiency in stand-by mode, and the accurate regulation in normal mode.

Stand-by mode or normal mode are obtained by supplying or not the secondary regulator. This can be ordonnered for exemple by a microprocessor in relation with the remote control unit.

Regulation pulses are applied to the TEA2260/61 through a small pulse-transformer to the IN input (pin 2). This input is sensitive to positive square pulses. The typical threshold of this input is 0.85V.

The frequency of pulses coming from the secondary regulator can be lower or higher than the frequency of the starting oscillator.

The TEA2260/61 has no soft-starting system when it receives pulses from the secondary. The soft-starting has to be located in the secondary regulator. Due to the principle of the primary regulation, pulses generated by the starting system automatically disappear when the voltage delivered by the SMPS increases.

Stand-by Mode - Normal Mode Transition

During the transition there are simultaneously pulses coming from the primary and secondary regulators.

These signals are not synchronized and some care has to be taken to ensure the safety of the switching power transistor.

A very sure and simple way consist in checking the transformer demagnetization state.

- A primary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the secondary regulator.
- A secondary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the primary regulator.

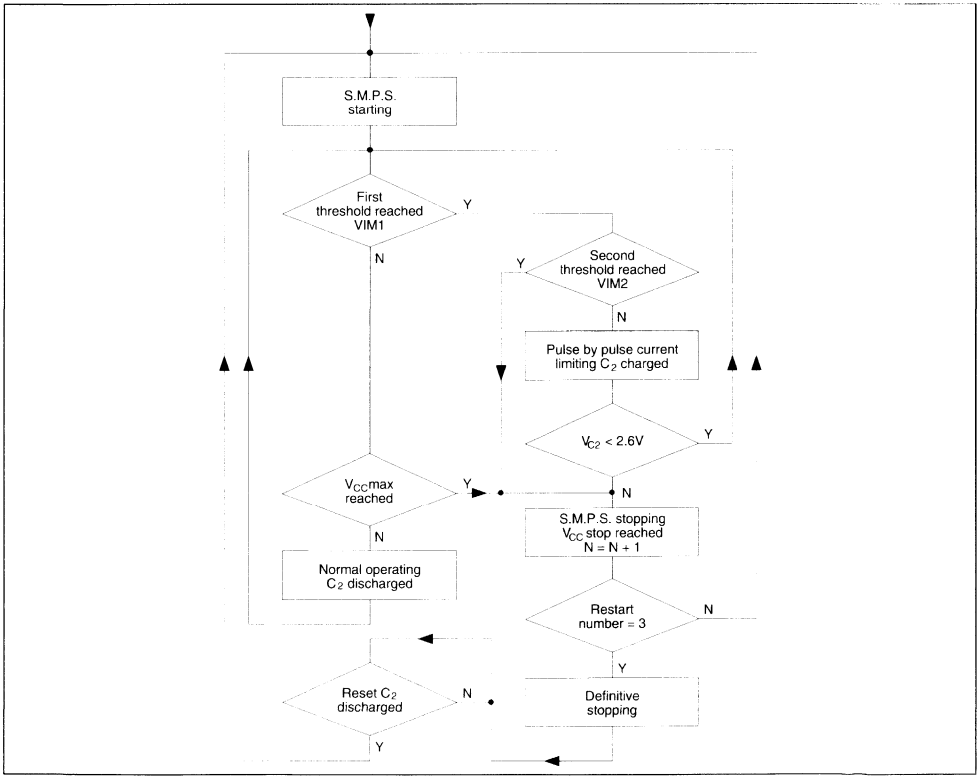
With this arrangement the switching safety area of the power transistor is respected and there is no risk of transformer magnetization.

The magnetization state of the transformer is checked by sensing the voltage across a winding of the transformer (generally the same which supplies the TEA2261). This is made by connecting a resistor between this winding and the demagnetization sensing input of the circuit (pin 1).

SECURITY FUNCTIONS OF THE TEA2260 (see flow-chart below)

- **Undervoltage detection.** This protection works in association with the starting device "V_{CC} switch" (see paragraph Starting-mode - standby mode). If V_{CC} is lower than V_{CC}stop (typically 7.4V) output pulses are inhibited, in order to avoid wrong operation of the power supply or bad power transistor drive.
- **Overvoltage detection.** If V_{CC} exceeds V_{CC}max (typically 15.7V) output pulses are inhibited. Restarting of the power supply is obtained by reducing V_{CC} below V_{CC}stop.
- **Current limitation of the power transistor.** The current is measured by a shunt resistor. A double threshold system is used :
  - When the first threshold (V_{IM1}) is reached, the conduction of the power transistor is stopped until the end of the period : a new conduction signal is needed to obtain conduction again.
  - Furthermore as long as the first threshold is reached (it means during several periods), an external capacitor C_2 is charged. When the voltage across the capacitor reaches V_{C2} (typically 2.55V) the output is inhibited. This is called the "repetitive overload protection". If the overload diseappears before V_{C2} is reached, C_2 is discharged, so transient overloads are tolerated.
  - Second current limitation threshold (V_{IM2}). When this threshold is reached the output of the circuit is immediatly inhibited. This protection is helpfull in case of hard overload for example to avoid the magnetization of the transformer.
- **Restart of the power supply**. After stopping due to V_{C2}, V_{IM2}, V_{CC}Max or V_{CC}stop triggering, restart of the power supply can be obtained by the normal operating of the "V_{CC} switch" but thanks to an integrted counter, if normal restart cannot be obtained after three trials, the circuit is definitively stopped. In this case it is necessary to reduce V_{CC} below approximately 5V to reset the circuit. From a practical point of view, it means that the power supply has to be temporarily disconnected from any power source to get the restart.

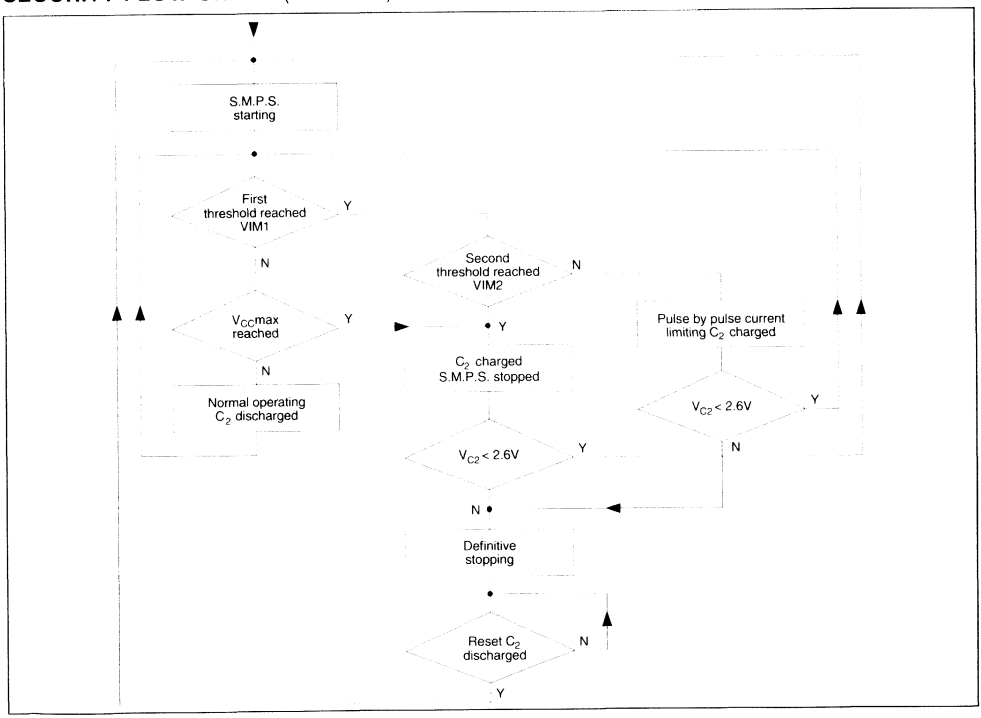
SECURITY FLOW-CHART (TEA2260)



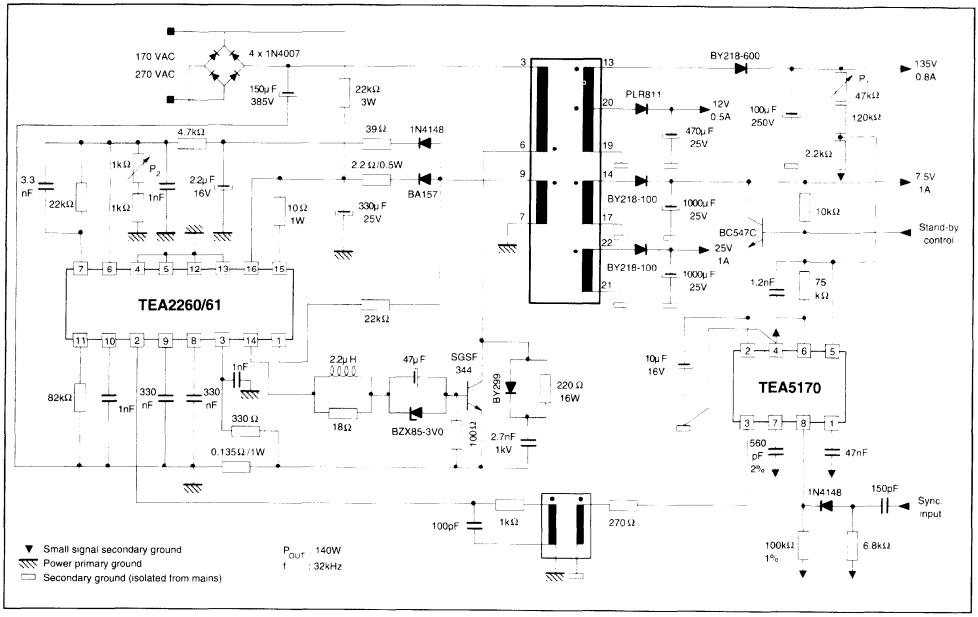
SECURITY FUNCTIONS OF THE TEA2261 (see flow-chart below)

- **Undervoltage detection.** This protection works in association with the starting device "V_{CC} switch" (see paragraph Starting-mode - standby mode). If V_{CC} is lower than V_{CC}stop (typically 7.4V) output pulses are inhibited, in order to avoid wrong operation of the power supply or bad power transistor drive.
- **Overvoltage detection.** If V_{CC} exceeds V_{CC}max (typically 15.7V) output pulses are inhibited and the external capacitor C_2 is charged as long as V_{CC} is higher than V_{CC} stop. Restarting of the power supply is obtained by reducing V_{CC} below V_{CC}stop except if the voltage across C_2 reaches V_{C2} (typically 2.55V) (refer to "Restart of the power supply" paragraph).In this last case, the circuit is definitively stopped.
- **Current limitation of the power transistor.** The current is measured by a shunt resistor. A double threshold system is used :
  - When the first threshold (V_{IM1}) is reached, the conduction of the power transistor is stopped until the end of the period : a new conduction signal is needed to obtain conduction again.
  - Furthermore as long as the first threshold is reached (it means during several periods), an external capacitor C_2 is charged. When the voltage across the capacitor reaches V_{C2} (typically 2.55V) the output is inhibited. This is called the "repetitive overload protection". If the overload diseappears before V_{C2} is reached, C_2 is discharged, so transient overloads are tolerated.
  - Second current limitation threshold (V_{IM2}). When this threshold is reached the output of the circuit is immediatly inhibited. This protection is helpfull in case of hard overload for example to avoid the magnetization of the transformer.
- **Restart of the power supply**. After stopping due to V_{IM2}, V_{CC}Max or V_{CC}stop triggering, restart of the power supply can be obtained by the normal operating of the "V_{CC} switch" V_{CC} switch sequency from V_{CC}stop to V_{CC}start . After stopping due to V_{C2} threshold reaching, the circuit is definitively stopped. In this case it is necessary to reduce V_{CC} below approximately 5V to reset the circuit. From a practical point of view, it means that the power supply has to be temporarily disconnected from any power source to get the restart.

SECURITY FLOW-CHART (TEA2261)



TYPICAL APPLICATION (Master/slavearchitecture)



TV - SET SMPS (with TEA5170)

Input voltage range	170VAC – 270VAC
Input DC voltage range	210VDC – 370VDC
Output power in normal mode	25W < P_O < 140W
Output power in stand by mode	2W < P_O < 45W
Operating frequency	32 kHz
Efficiency at full load	> 80%
Efficiency in stand by mode (P_O = 7W)	> 50%

Short circuit protected
Open load protected
Long duration overload protected
Complete shutdown after repetitive default detection

Load regulation (VDC = 310V)

Output 135V (± 0.18%) ——> (I_{135} : 0.01A to 0.8A ; I_{25} = 1A)
Output 25V (± 2%) ——> (I_{135} : 0.8A ; I_{25} : 0.5A —> 1A)

Line regulation

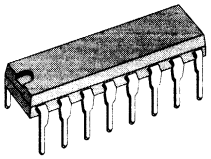
Output 135V (± 0.13%) ——> (210V < V_{DC} < 370V)
Output 25V (± 0.17%) ——> (I_{135} : 0.8A ; I_{25} : 1A)

SGS-THOMSON MICROELECTRONICS

TEA2262

SWITCH MODE POWER SUPPLY CONTROLLER

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1A
- LOW START-UP CURRENT
- DIRECT DRIVE OF THE MOS POWER TRANSISTOR
- TWO LEVELS TRANSISTOR CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- SOFT-STARTING
- UNDER AND OVERVOLTAGE LOCK-OUT
- AUTOMATIC STAND-BY MODE
- LARGE POWER RANGE CAPABILITY IN STAND-BY (Burst mode)
- INTERNAL PWM SIGNAL GENERATOR



BATWING DIP16
(Plastic Package)

ORDER CODE : TEA2262

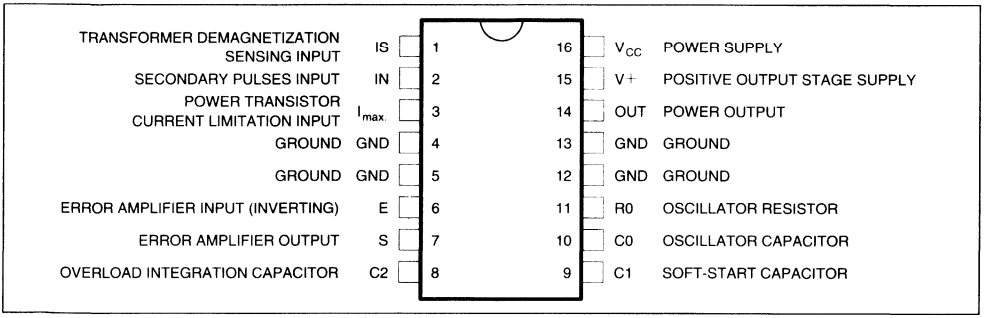
DESCRIPTION

The TEA2262 is a monolithic integrated circuit for the use in primary part of an off-line switching mode power supply using a MOS power transistor.

All functions required for SMPS control under normal operating, transient or abnormal conditions are provided.

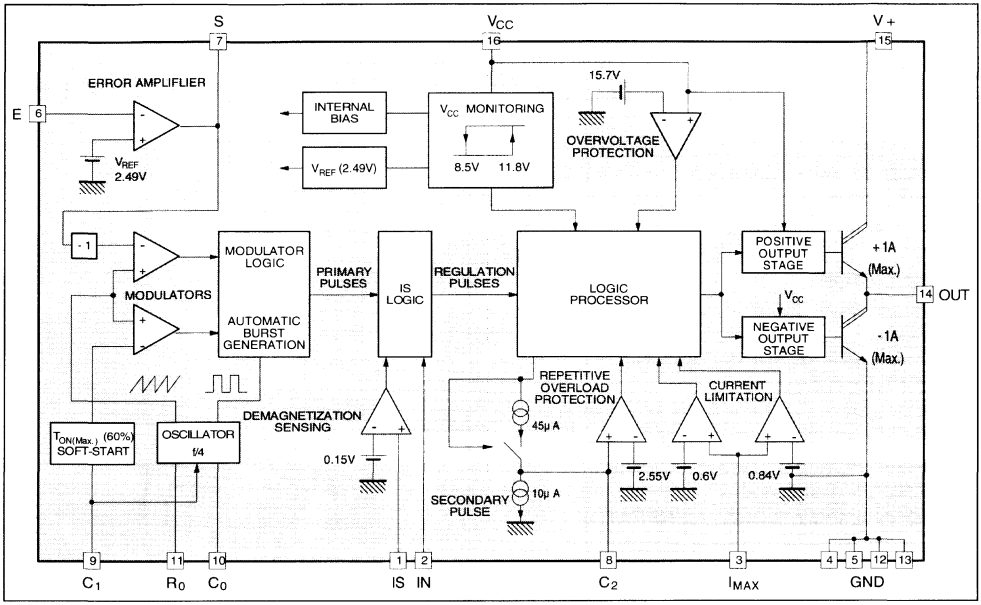
The capability of working according to the "master-slave" concept, or according to the "primary regulation" mode makes the TEA2262 very flexible and easy to use. This is particularly true for TV receivers where the IC provides an attractive and low cost solution (no need of stand-by auxiliary power supply).

PIN CONNECTIONS



2262-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply V16-V4, 5, 12, 13	20	V
V+	Output Stage Power Supply V15-V4, 5, 12, 13	20	V
I_{OUT}+	Positive Output Current (source current)	1.5	A
I_{OUT}-	Negative Output Current (sink current)	1.5	A
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	-40, +150	°C

2262-01.TBL

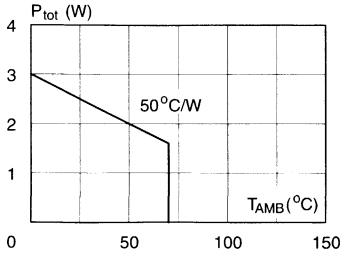
THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	15	°C/W
$R_{th\ (j-a)}$*	Junction-ambient Thermal Resistance	50	°C/W

2262-02.TBL

* Soldered on a 35µm, 40cm^2 board copper area

MAXIMUM POWER DISSIPATION



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	V_{CC} stop	12	V_{CC} max	V
I_{OUT+}	Positive Output Current (source current)			1	A
I_{OUT-}	Negative Output Current (sink current)			1	A
I_{OUT+}	Average Positive Output Current			0.3	A
I_{OUT-}	Average Negative Output Current			0.3	A
F_{oper}	Operating Frequency	10		150	kHz
V_{IN}	Input Pulses Amplitude (Pin 2)	1.5	2.5	4.5	V
R_{OSC}	Oscillator Resistor Range	10		100	kΩ
C_{OSC}	Oscillator Capacitor Range	0.33		4.7	nF
C1	Soft-starting Capacitor Range	0.047	1		µF
C2	Overload Integration Capacitor	0.047	1		µF
C2/C1	Ratio C2/C1 (C2 must be ≥ C1)	1			
T_{amb}	Operating Ambient Temperature	-20		70	°C

2262-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} =12V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
POWER SUPPLY					
$V_{CC(start)}$	Starting Voltage (V_{CC} increasing)	9.5	11.8	13	V
$V_{CC(stop)}$	Stopping Voltage (V_{CC} decreasing)	7	8.5	9.5	V
Hyst V_{CC}	Hysteresis ($V_{CC(start)}$ - $V_{CC(Stop)}$)	2.7	3.3	3.7	V
$I_{CC(start)}$	Starting Current (V_{CC} = 9V)		0.5		mA
I_{CC}	Supply Current (V_{CC} = 12V)		6.5		mA
$V_{CC(max)}$	Overvoltage Threshold on V_{CC}	15	15.7		V
$I_{CC(over)}$	Supply Current after Overvoltage Detection (V_{CC} = 17V)		35		mA
OSCILLATOR / PWM SECTION					
$\frac{\Delta F}{F}$	Accuracy (R_{OSC} = 68kΩ, C_{OSC} = 1nF)		10		%
t_{ON} max	Maximum Duty Cycle in Primary Regulation Mode	50	60	70	%
ERROR AMPLIFIER SECTION					
A_{VO}	Open Loop Gain		75		dB
F_{ug}	Unity Gain Frequency		550		kHz
I_{SC}	Short Circuit Output Current (Pin 7 connected to ground)		2		mA
I_{BE}	E Input Bias Current (Pin 6)		0.08		µA
V_{REF}	Internal Voltage Reference (connected to error amplifier input and not directly accessible)	2.34	2.49	2.64	V
INPUT SECTION					
V_{IN}	IN Input Threshold (Pin 2)	0.6	0.85	1.2	V
V_{IS}	IS Input Threshold (Pin 1)		0.15		V
I_{BIN}	IN Input Bias Current		0.3		µA
I_{BIS}	IS Input Bias Current		0.4		µA
CURRENT LIMITATION SECTION					
V_{IM1}	First Current Limitation Threshold	550	600	650	mV
V_{IM2}	Second Current Limitation Threshold	780	840	900	mV
ΔV_{IM}	Thresholds Difference V_{IM2} - V_{IM1}	190	240	280	mV
V_{C2}	Lock-out Threshold on Pin C2	2.25	2.55	2.85	V
I_{DC2}	Capacitor C2 Discharge Current		10		µA
I_{CC2}	Capacitor C2 Charge Current		45		µA
$I_{BI(max)}$	Maximum Input Bias Current (Pin 3)		0.2		µA

2262-04.TBL

SIMPLIFIED APPLICATION DIAGRAMS

Figure 1 : Master-slave Concept

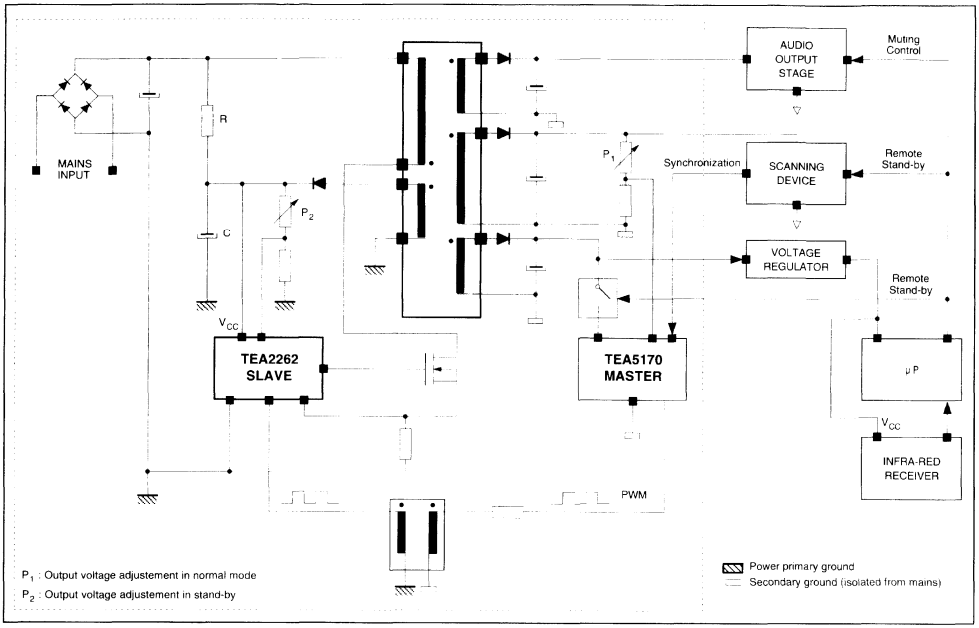
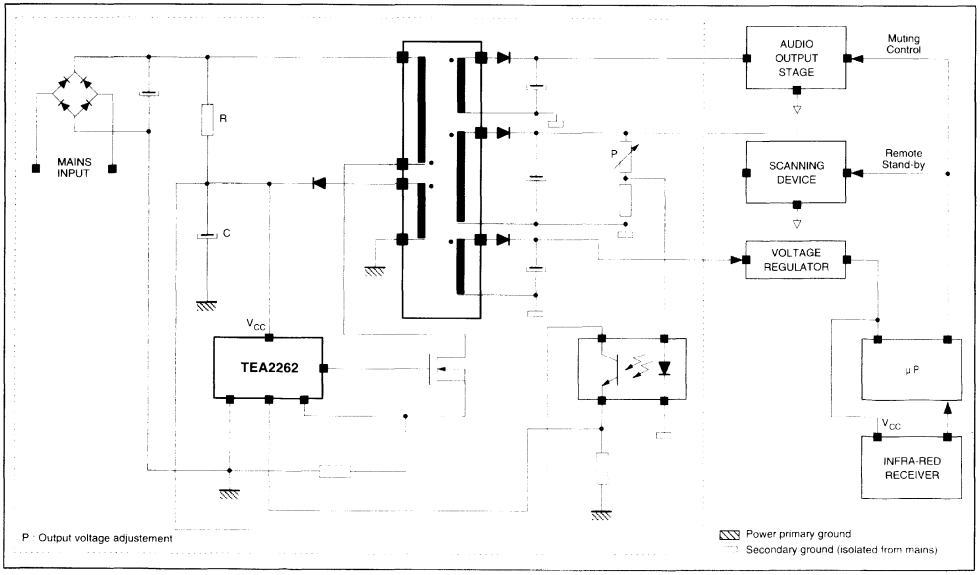


Figure 2 : Secondary Regulation (with optocoupler)



GENERAL DESCRIPTION

The TEA2262 is an off-line switch mode power supply controller. The synchronization function and the specific operation in stand-by mode make it well adapted to video applications such as TV sets, VCRs, monitors, etc...

The TEA2262 can be used in two types of architectures :

- Master/slave architecture. In this case, the TEA2262 drives the power transistor according to the pulse width modulated signals generated by the secondary located master circuit. A pulse transformer provides the feedback (see Figure 1).
- Conventional architecture with linear feedback signal (feedback sources : optocoupler or transformer winding) (see Figure 2).

Using the TEA2262, the stand-by auxiliary power supply, often realized with a small but costly 50Hz transformer, is no longer necessary. The burst mode operation of the TEA2262 makes possible the control of very low output power (down to less than 1W) with the main power transformer.

When used in a master/slave architecture, the TEA2262 and also the power transistor turn-off can be easily synchronized with the line transformer. The switching noise cannot disturb the picture in this case.

As an S.M.P.S. controller, the TEA2262 features the following functions :

- Power supply start-up (with soft-start)
- PWM generator
- Direct power transistor drive (±1A)
- Safety functions : pulse by pulse current limitation, output power limitation, over and under voltage lock-out.

S.M.P.S. OPERATING DESCRIPTION

Starting Mode - Stand By Mode

Power for circuit supply is taken from the mains through a high value resistor before starting. As long as V_{CC} of the TEA2262 is below V_{CC} start, the quiescent current is very low (typically 0.5mA) and the electrolytic capacitor across V_{CC} is linearly charged. When V_{CC} reaches V_{CC} start (typically 11.8V), the circuit starts, generating output pulses with a soft-starting. Then the SMPS goes into the stand-by mode and the output voltage is a percentage of the nominal output voltage (eg. 80%).

During starting phase, in order to avoid transformer magnetization (specially at high frequency), the frequency oscillator is divided by four.

At switch-on, C_0 charging current is divided by four. It recover its normal value when the voltage on soft-start capacitor reach 2.5V.

The current also recover its standard value when the soft-start capacitor is discharged because of a burst operating mode (starting in stand-by).

In other words, the charging current will become and stay at its normal value, as soon as one of the following events occurs :

- V_{C1} rearch 2.5V
- C_1 is discharged by burst operating mode

For this the TEA2262 contains all the functions required for primary mode regulation : a fixed frequency oscillator, a voltage reference, an error amplifier and a pulse width modulator (PWM).

For transmission of low power with a good efficiency in stand-by, an automatic burst generation system is used, in order to avoid audible noise.

Normal Mode (secondary regulation)

The normal operating of the TV set is obtained by sending to the TEA2262 regulation pulses generated by a regulator located in the secondary side of the power supply (TEA5170 for example).

This architecture uses the "Master-slave Concept", advantages of which are now well-known especially the very high efficiency in stand-by mode, and the accurate regulation in normal mode.

Stand-by mode or normal mode are obtained by supplying or not the secondary regulator. This can be ordonnered for exemple by a microprocessor in relation with the remote control unit.

Regulation pulses are applied to the TEA2262 through a small pulse-transformer to the IN input (pin 2). This input is sensitive to positive square pulses. The typical threshold of this input is 0.85V.

The frequency of pulses coming from the secondary regulator can be lower or higher than the frequency of the starting oscillator.

The TEA2262 has no soft-starting system when it receives pulses from the secondary. The soft-starting has to be located in the secondary regulator.

Due to the principle of the primary regulation, pulses generated by the starting system automatically disappear when the voltage delivered by the SMPS increases.

Stand-by Mode - Normal Mode Transition

During the transition there are simultaneously pulses coming from the primary and secondary regulators.

These signals are not synchronized and some care has to be taken to ensure the safety of the switching power transistor.

A very sure and simple way consist in checking the transformer demagnetization state.

- A primary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the secondary regulator.
- A secondary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the primary regulator.

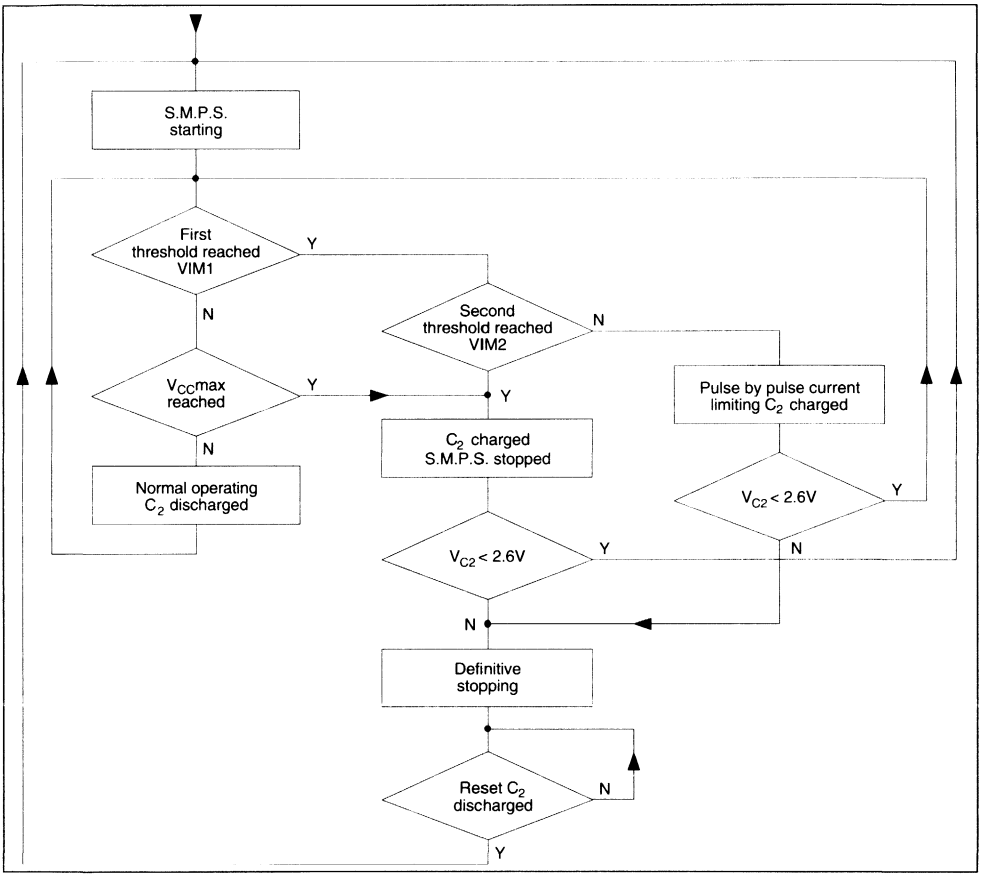
With this arrangement the switching safety area of the power transistor is respected and there is no risk of transformer magnetization.

The magnetization state of the transformer is checked by sensing the voltage across a winding of the transformer (generally the same which supplies the TEA2262). This is made by connecting a resistor between this winding and the demagnetization sensing input of the circuit (pin 1).

SECURITY FUNCTIONS (see flow-chart below)

- **Undervoltage detection.** This protection works in association with the starting device "V_{CC} switch" (see paragraph Starting-mode - standby mode). If V_{CC} is lower than V_{CC}stop (typically 8.5V) output pulses are inhibited, in order to avoid wrong operation of the power supply or bad power transistor drive.
- **Overvoltage detection.** If V_{CC} exceeds V_{CC}max (typically 15.7V) output pulses are inhibited and the external capacitor C_2 is charged as long as V_{CC} is higher than V_{CC} stop. Restarting of the power supply is obtained by reducing V_{CC} below V_{CC}stop except if the voltage across C_2 reaches V_{C2} (typically 2.55V) (refer to "Restart of the power supply" paragraph).In this last case, the circuit is definitively stopped.
- **Current limitation of the power transistor.** The current is measured by a shunt resistor. A double threshold system is used :
  - When the first threshold (V_{IM1}) is reached, the conduction of the power transistor is stopped until the end of the period : a new conduction signal is needed to obtain conduction again.
  - Furthermore as long as the first threshold is reached (it means during several periods), an external capacitor C_2 is charged. When the voltage across the capacitor reaches V_{C2} (typically 2.55V) the output is inhibited. This is called the "repetitive overload protection". If the overload diseappears before V_{C2} is reached, C_2 is discharged, so transient overloads are tolerated.
  - Second current limitation threshold (V_{IM2}). When this threshold is reached the output of the circuit is immediatly inhibited. This protection is helpfull in case of hard overload for example to avoid the magnetization of the transformer.
- **Restart of the power supply**. After stopping due to V_{IM2}, V_{CC}Max or V_{CC}stop triggering, restart of the power supply can be obtained by the normal operating of the "V_{CC} switch" V_{CC} switch sequency from V_{CC}stop to V_{CC}start . After stopping due to V_{C2} threshold reaching, the circuit is definitively stopped. In this case it is necessary to reduce V_{CC} below approximately 5V to reset the circuit. From a practical point of view, it means that the power supply has to be temporarily disconnected from any power source to get the restart.

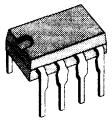
SECURITY FLOW-CHART



TEA5170

SWITCH MODE POWER SUPPLY SECONDARY CIRCUIT

- INTERNAL PWM SIGNAL GENERATOR
- POWER SUPPLY WIDE RANGE 4.5V – 14.5V
- SOFT START
- REFERENCE VOLTAGE 2V ± 5%
- WIDE FREQUENCY RANGE 250kHz
- MINIMUM OUTPUT PULSE WIDTH 500nS
- MAXIMUM PRESET DUTY CYCLE
- SYNCHRONIZATION WINDOW
- OUTPUT SWITCH
- UNDERVOLTAGE LOCKOUT
- FREQUENCY RANGE WITH SYNCHRONIZATION 64kHz



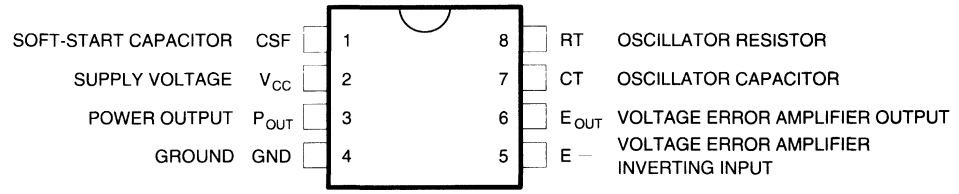
DIP8
(Plastic Package)

ORDER CODE : TEA5170

DESCRIPTION

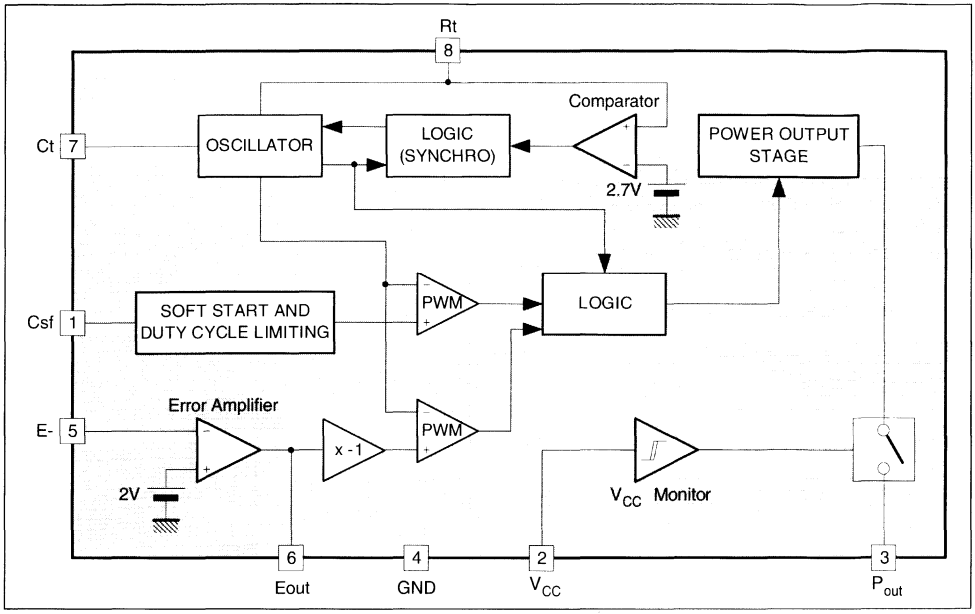
The TEA5170 is designed to work in the secondary part of an off-line SMPS, sending pulses to the slaved TEA2164 or TEA2260/61 which are located on the primary side of the main transformer. An accurate regulated voltage is obtained by duty cycle control. The TEA5170 can be externally synchronized by higher or lower frequency signal, then it could be used in applications like TV set ones. For more details, refer to application note AN408/0591.

PIN CONNECTIONS



5170-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	– 40, + 150	°C

5170-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	90	°C/W

5170-02.TBL

RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	5		14	V
RT	Timing Resistor	47		180	kΩ
CT	Timing Capacitor	0.12		1.8	nF
Fosc	Oscillator Frequency	12		250	kHz
Fsy	Synchro Frequency	12		64	kHz
T_{amb}	Operating Ambient Temperature	– 20		70	°C
VRT	Voltage on Pin RT (8)			7	Volt
VCT	Current on Pin CT (1)			100	µA
ISOURCE	Output Current		30	60	mA

5170-03.TBL

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OSCILLATOR						
TA	Free Period	RT = 100kΩ ± 0% CT = 1.2nF ± 0%, Vcc = 12V	60.40	65.60	70.80	µS
TB		RT = 100kΩ ± 0% CT = 560pF ± 0%, Vcc = 12V	29.18	31.70	34.22	µS
ΔF_{OSC} (T)	Frequency drift due to ambient temperature variation from 0°C to 70°C $\frac{F_{OSC}(70°C) - F_{OSC}(0°C)}{70°C \times F_{OSC}(25°C)}$	RT = 100kΩ ± 0% CT = 1.2nF ± 0%, Vcc = 12V		0.01		%/°C
ΔF_{OSC} (V_{CC})	Frequency drift due to V_{CC} variation from 5V to 12V $\frac{F_{OSC}(12V) - F_{OSC}(5V)}{7V \times F_{OSC}(12V)}$	RT = 100kΩ ± 0% CT = 1.2nF ± 0%		0.07		%/V
ERROR VOLTAGE AMPLIFIER (V_{CC} = 12V)						
Ibias	Input Bias Current	Ein = 2V	0	0.2	1	µA
Gvol	Voltage Gain			80		dB
GB	Gain Bandwidth			2		MHz
	Slew Rate			2		V/µs
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Voltage Reference	Using the voltage error amplifier as a follower	1.9	2	2.1	V
ΔV_{REF} (V_{CC})	Line Regulation $\frac{V_{REF}(12V) - V_{REF}(5V)}{7V}$	V_{CC} = 5V to 12V	– 3	0.4	3	mV/V
ΔV_{REF} (T)	V_{REF} drift with temperature $\frac{V_{REF}(70°C) - V_{REF}(0°C)}{70°C}$	T_A = 0°C to 70°C		0.2		mV/°
$T_{ON\ MIN}$						
$T_{ONMIN\ A}$	Minimum Duty Cycle	Ct = 1.2nF ± 0% Rt = 100kΩ ± 0%	1.77	2.53	3.29	µs
$T_{ONMIN\ B}$	Minimum Duty Cycle	Ct = 560pf ± 0% Rt = 100kΩ ± 0%	1.04	1.49	1.94	µs
POWER OUTPUT STAGE						
V_{POUTH}	Output High Level	I_{load} = 1mA	6.3	6.9	7.5	V
V_{POUTL}	Output Low Level	I_{load} = – 1mA	0.5	0.8	1.1	V
I_{SINK}	Sink Current	V_{POUT} = 3V	30	60	190	mA
I_{SOURCE}	Source Current	V_{POUT} = 3V	30	110	190	mA
SYNCHRONISATION						
$F_{trig\ Max}$	Maximum Synchro Frequency		64			kHz
V_{trig}	Synchro Triggering Threshold			2.7	3	V
T_{trigp}	Synchro Triggering Pulse Width	at VRT = 2.7Volt (fig 5)	800			nS
Wtrig +	Positive Triggering Window $\frac{T_{trig+} - T_O}{T_O}$	CT = 1.2nF ± 0% RT = 100kΩ ± 0%	25	35	40	%
Wtrig –	Negative Triggering Window $\frac{T_O - T_{trig-}}{T_O}$	CT = 1.2nF ± 0% RT = 100kΩ ± 0%	9	29	42	%
SOFT START						
I_{csf}	*Csf Load Current	V_{csf} = 1V	2.5	3.7	6	µA
Donmax	Maximum Duty Cycle	V_{cs} > 2.5V, V_{CC} = 12V CT = 1.2nf ± 0% RT = 100kΩ ± 0%	60	78	95	%

*Csf is a high impedance capacitor

5170-04 TBL

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12V, unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} MONITOR						
V_{START}	Turn-on Threshold		3.60	4	4.40	V
V_{HYST}	Hysteresis Voltage		100			mV
V_{STOP}	Turn-off Threshold		3.50			V
TOTAL DEVICE						
I_{CC}	Supply Current	RT = 100kΩ ± 0%, CT = 1.2nf ± 0% No Load on Pin 3, V_{CC} = 12V	7	12	25	mA

5170-05.TBL

GENERAL DESCRIPTION

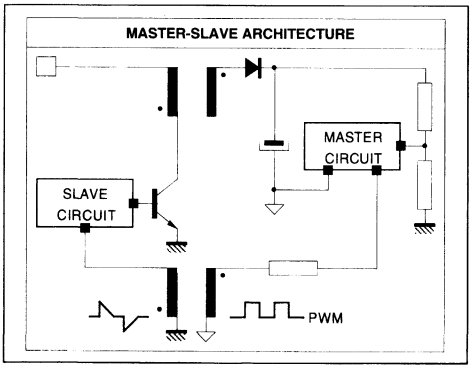
The TEA5170 takes place in the secondary part of an isolated off-line SMPS. During normal mode operation, it sends pulses to the slave circuit located in the primary side (TEA2164, TEA2260/61) through a pulse transformer to achieve a very precisely regulated voltage by duty cycle control.

The main blocs of the circuit are :
- an error voltage amplifier
- an RC oscillator
- an output stage
- a V_{CC} monitor
- a voltage reference bloc
- a pulse width modulator
- two logic blocs
- a soft start and Duty cycle limiting bloc

PRINCIPLE OF OPERATION

The TEA5170 sends pulses continuously to the slave circuit in order to insure a proper behaviour of the primary side.
- According to this, the output duty cycle is varying between $D_{ON\ (min.)}$ (0.05) and $D_{ON\ (max.)}$ (0.75) : then even in case of open load, pulses are still sent to the slave circuit.

Figure 1 : Basic Concept

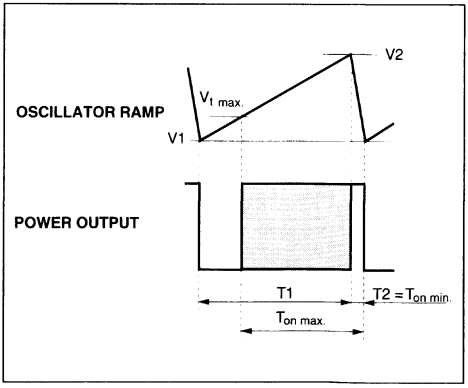


5170-03.EPS

ASYNCHRONIZED MODE (Figure 2)

The regulated voltage image is compared to 2V vol-tage reference. The error voltage amplifier output and the RC oscillator voltage ramp are applied to the internal Pulse Width Modulator Inputs.
The PWM logic Output is connected to a logic bloc which behaves like a RS latch, sets by the PWM output and resets when Ct downloading occurs. Finally, the push-pull output bloc delivers square wave signal whom output leading edge occurs during Ct uploading time, and output trailing edge at Ct downloading time end. The duty cycle is limited to 75% of oscillator period as maximum value and to Ct downloading time/oscillator period as minimum value (Figure 2).

Figure 2

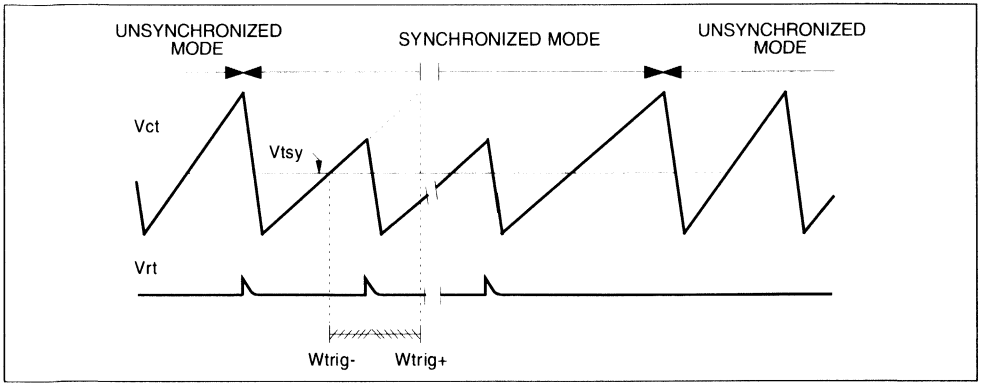


5170-04.EPS

SYNCHRONIZED MODE (see Figure 3)

The TEA5170 will enter the Synchronized Mode when it receives one pulse through Rt during Ct discharge.
At that time Ct charging current will be multiplied by 0.75 and period will increase up to To x 1.26.
A pulse occuring during the synchro window, commands the Ct downloading. If none, the TEA5170 will return to normal mode at the end of the period.

Figure 3



Remark : In case of an application between TEA5170 and TEA2164, to optimize the synchronization windows of these circuits, the following relations have to be used : $T_m = \frac{T_{SYNC}}{1.06} T_e = \frac{T_m}{1.223}$ with T_e : Free period of the TEA2164 oscillator, and T_m : Free period of the TEA5170 oscillator.

BLOCK DESCRIPTION

The error voltage amplifier inverting-input and output are accessible to use different feed-back network and allowing parasitic filtering network. The non-inverting input is internaly connected to 2V reference voltage.

The RC oscillator is designed to work at high frequency (up to 250kHz). R_T sets the capacitor charging current $Io = 2/R_T$.

The capacitor C_T is loaded from $V_1 \approx 1V$ to $V_2 = 2V$ during $T1 = \frac{C_T R_T}{1.985}$ and then down loaded through an integrated resistor $R_2 \approx 1k\Omega$ during $T_2 = 1300\ C_T$

The ramp is used to limit the duty cycle. Then the maximum duty cycle is

$$DONMAX = \frac{1}{T1 + T2} (0.73\ T1 + T2)$$

The output level is V_{CC} independant when V_{CC} is over 8V.

The V_{CC} monitoring switches the circuit on when V_{CC} is over 4V and switches it off when under 3.8V. This function insures a proper starting procedure (made by the primary side circuit).

SYNCHRONIZATION

(see Figures 4 and 5)

Figure 4 : Triggering Schematic

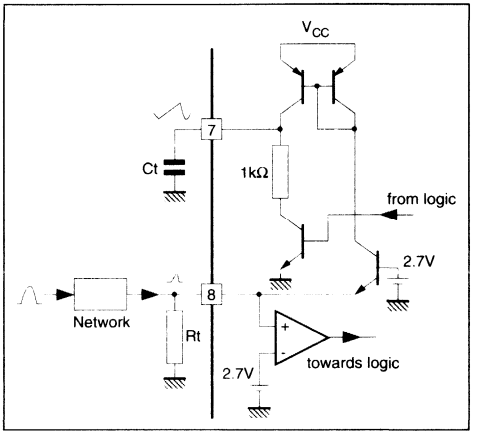
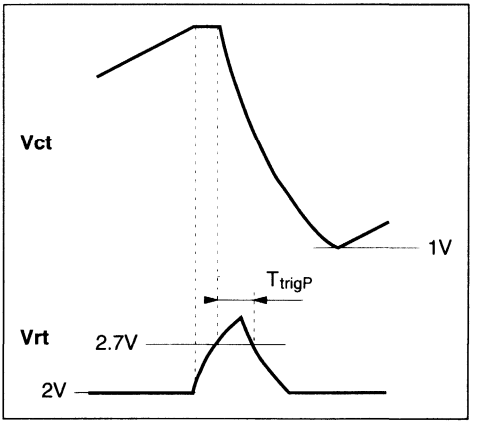


Figure 5 : Typical Waveforms



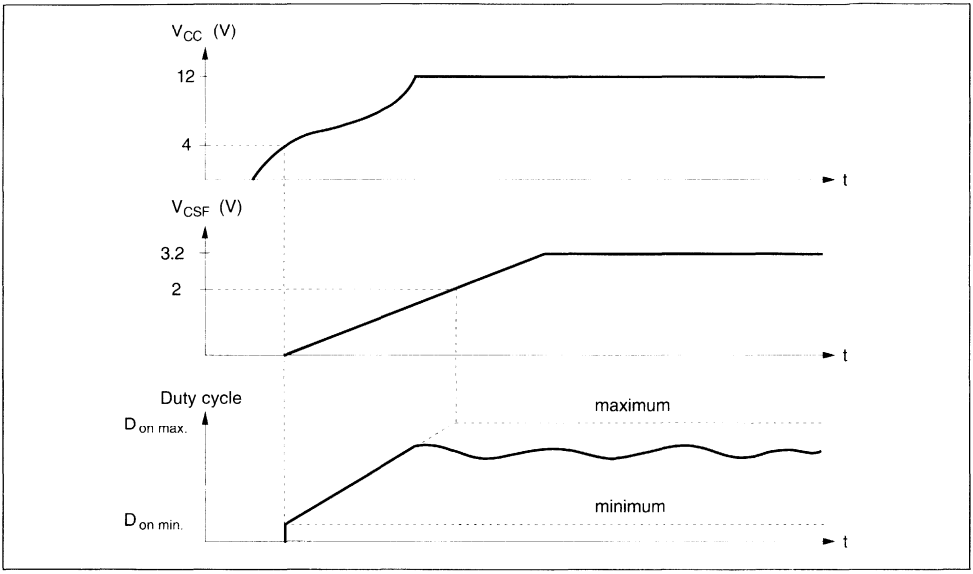
STARTING

When V_{CC} is under 4V, output pulses are not allowed and the slave circuit keeps its own mode. When V_{CC} is going over 4V, output pulses are sent via the pulse transformer (or an optical device) to the slave circuit which is synchronizing and entering the slaved mode. Output pulses can be shut down only if V_{CC} goes below 3.8 Volt.

SOFT START

Using Csf, it is possible to make a soft start sequence. When V_{CC} grows from 0V to 4V, voltage on Csf equals 0V. When V_{CC} is higher than 4V, Csf is loaded by a 3.7µA current, then TonMAX (Vcsf) will vary linearly from Tonmin to Tonmax according to Csfst bias.
When V_{CC} will go low (3.8 Volt threshold), Csf will be downloaded by an internal transistor.

Figure 6 : Soft-Start Sequence



POWER OUTPUT STAGE

Figure 7 : Electrical Schematic

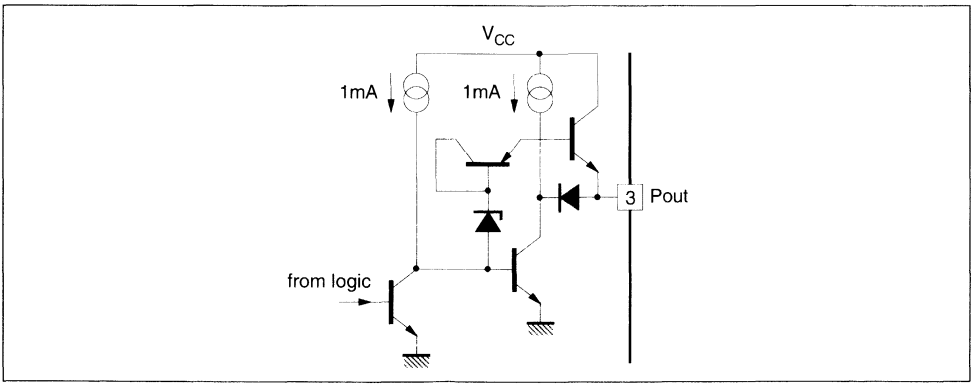


Figure 8

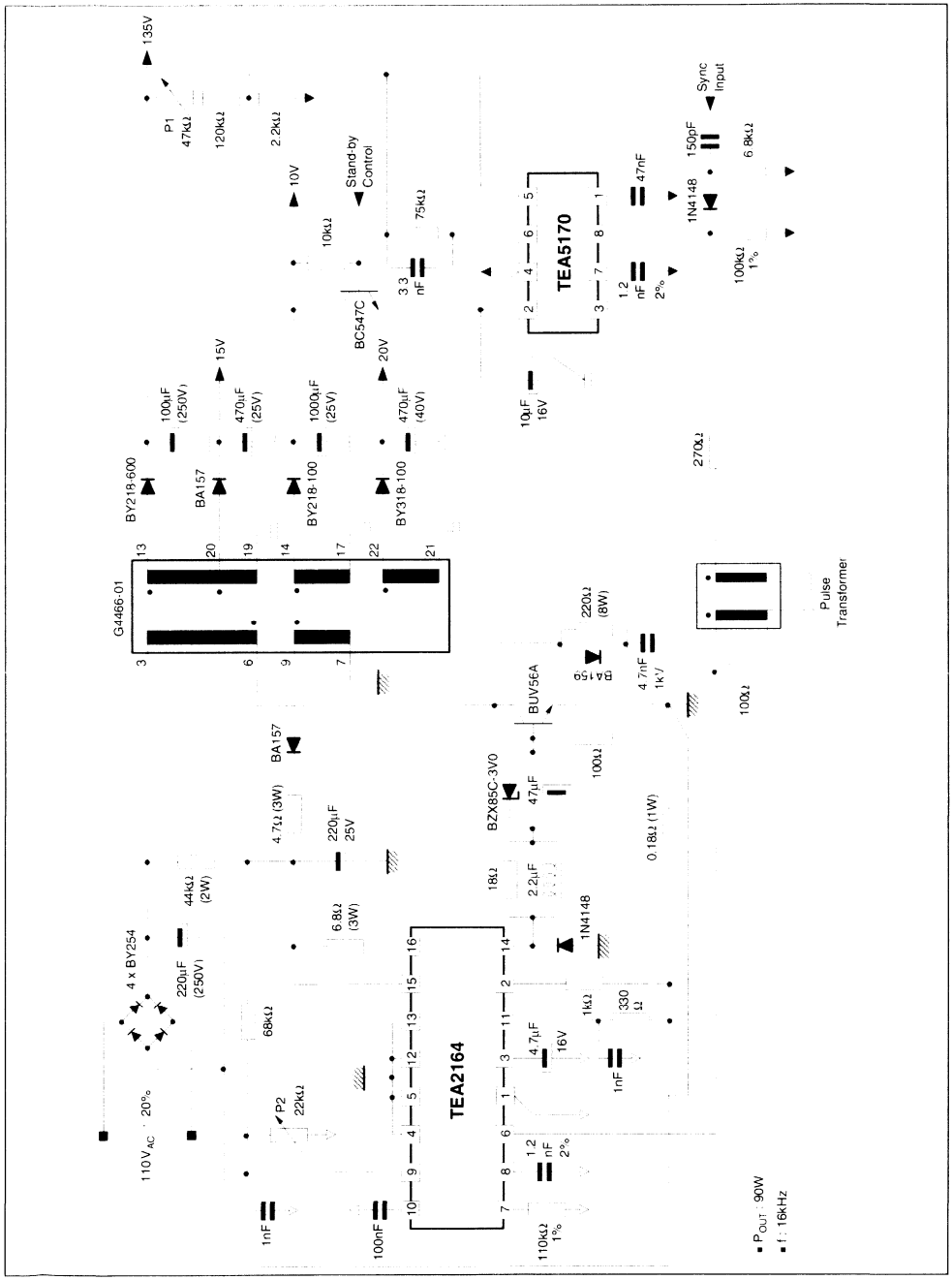
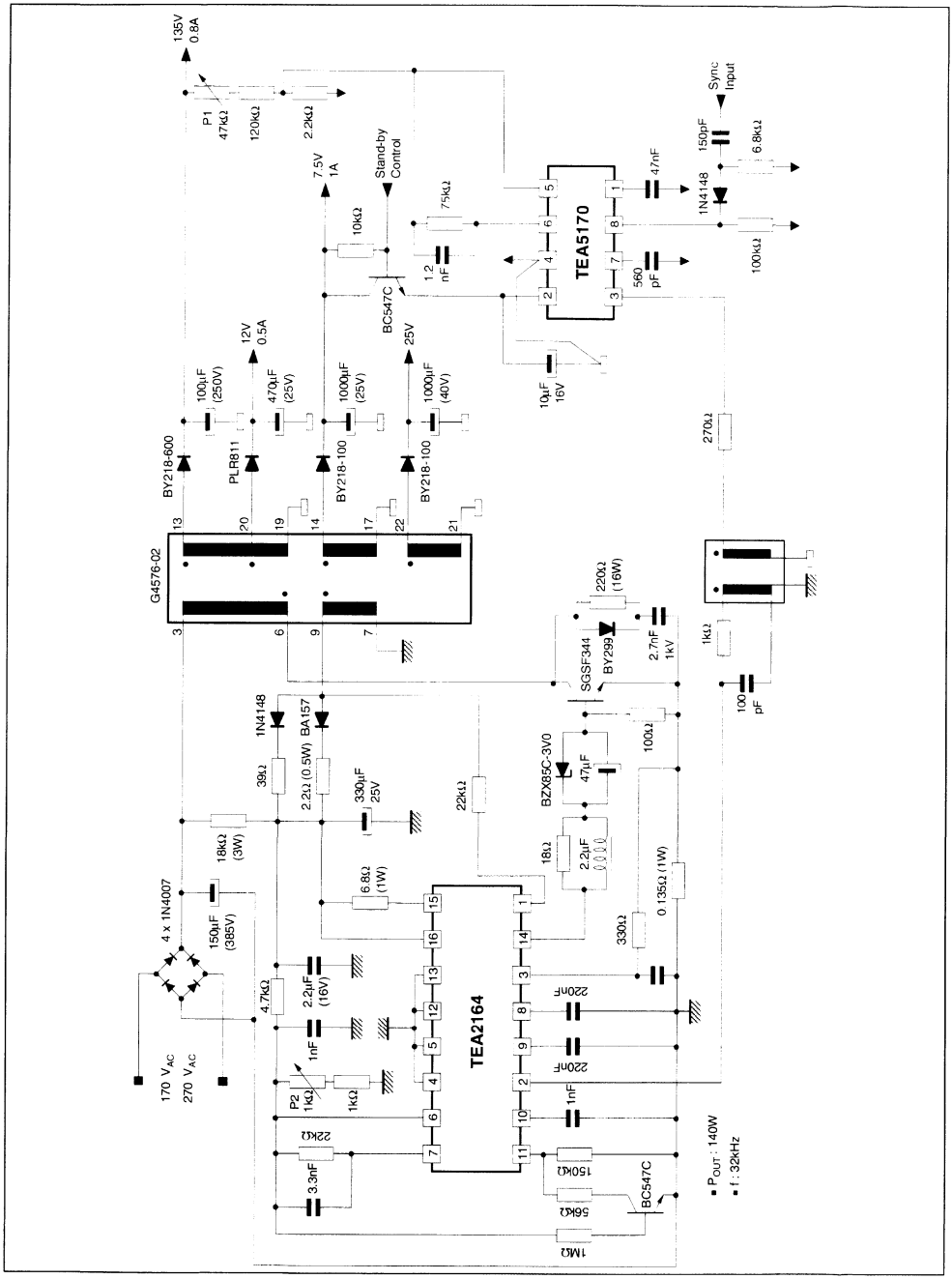

TEA2164
TEA5170
G4466-01
BY219-600
BA157
BY218-100
BY318-100
BUV56A
BZX85C-3V0
BC547C
1N4148
4 x BY254
110V AC ± 20%
P1
47kΩ
P2
22kΩ
120kΩ
2.2kΩ
10kΩ
75kΩ
68kΩ
44kΩ (2W)
220µF (250V)
100µF (250V)
470µF (25V)
1000µF (25V)
470µF (40V)
10µF 16V
4.7Ω (3W)
6.8Ω (3W)
220µF 25V
18Ω
2.2µF
47µF
100Ω
0.18Ω (1W)
220Ω (8W)
4.7nF 1kV
270Ω
100Ω
4.7µF 16V
1kΩ
330 Ω
1nF
1.2 nF 2%
110kΩ 1%
100nF
3.3 nF
1.2 nF 2%
47nF
150pF
6.8kΩ
100kΩ 1%
Sync Input
Pulse Transformer
Stand-by Control
10V
15V
20V
135V
P_{OUT} : 90W
f : 16kHz
5170-10.EPS

Figure 9



SGS-THOMSON MICROELECTRONICS

GRAPHIC CIRCUITS

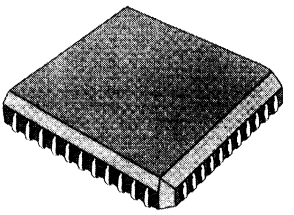
SGS-THOMSON MICROELECTRONICS

STG 1700

TRUE COLOR PALETTE-DAC WITH 16-BIT PIXEL PORT

For complete specifications please contact your nearest sales office

- Operation up to 135MHz
- 2:1 multiplexing using internal PLL
- Standard VGA and high color operation up to 110MHz
- Synchronous PixMix switching between modes
- Low power sleep mode
- Triple 8-bit DACs with comparators
- External or internal VRef DAC control



PLCC44

DESCRIPTION

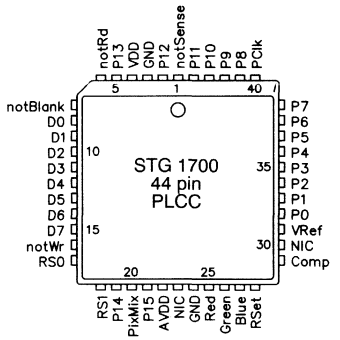
The STG 1700 is a Super VGA compatible Palette-DAC designed for PC systems requiring pixel rates up to 135MHz. It features a 16-bit pixel port and supports a number of different pixel modes which can be grouped into three categories:

- 8-bit pixel port giving standard SVGA and high/true color modes
- 16-bit pixel port giving faster high color/true color operation
- Serializing 16-bit pixel port to give two 8-bit pixels at 2 x PClk frequency

The PixMix capability allows pixel-by-pixel switching between modes.

The STG 1700 includes a 135MHz triple 8-bit video DAC, controlled by either an external 1.235V voltage reference or an on-chip voltage reference. A VGA compatible micro port makes use of "magic access" cycles (repeated accesses to the mask register) to control the extended features.

PIN CONNECTIONS



EXAMPLE MODES AND FREQUENCIES (ALL NON-INTERLACED)

Pixel port mode	Screen resolution	Simultaneous colors	Refresh rate (Hz)	PClk and data frequency (MHz)	Video frequency (MHz)
8-bit pixel port	1280x1024	256	60	110	110
	1024x768	256	80	90	90
	800x600	65K	80	110	55
	640x480	16.7M	80	102	34
16-bit pixel port	1024x768	65K	80	90	90
	800x600	16.7M	80	110	55
Serializing 16-bit pixel port	1280x1024	256	75	67.5	135

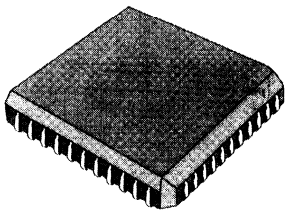
SGS-THOMSON MICROELECTRONICS

STG 1702

ENHANCED TRUE COLOR PALETTE-DAC WITH 16-BIT PIXEL PORT

For complete specifications please contact your nearest sales office

- Enhanced true color performance through new double 24-bit packed pixel mode
- Operation up to 135MHz
- Flexible multiplexing using internal PLL
- Standard VGA and high color operation up to 110MHz
- Synchronous PixMix switching between modes
- Programmable power-down features
- On-chip checksum test
- **RS2** pin allows direct write access to registers



PLCC44

DESCRIPTION

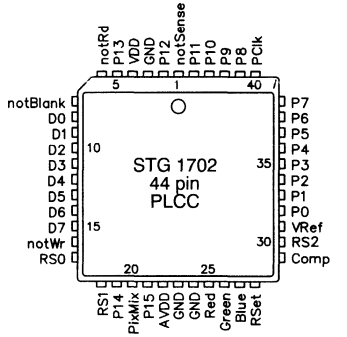
The STG 1702 is a Super VGA compatible Palette-DAC designed for PC systems requiring up to 135MHz pixel rates. Pixel modes supported by the STG 1702 include:

- Serializing 16-bit pixel port providing 135MHz 8-bit and 56MHz 24-bit packed pixel modes using the PLL
- 16-bit pixel port giving faster high color/true color operation up to 110MHz sampling rate
- 8-bit pixel port giving standard SVGA and high/true color modes up to 110MHz sampling rate

The PixMix capability allows pixel-by-pixel switching between modes.

The STG 1702 includes a 135MHz triple 8-bit video DAC, controlled by either an external 1.235V voltage reference or an on-chip voltage reference. A VGA compatible micro port makes use of both the "magic access" sequence and direct **RS2** mapping to control the extended features.

PIN CONNECTIONS



EXAMPLE MODES AND FREQUENCIES (ALL NON-INTERLACED)

Pixel port mode	Screen resolution	Simultaneous colors	Refresh rate (Hz)	PClk and data frequency (MHz)	Video frequency (MHz)
8-bit pixel port	1280x1024	256	60	110	110
	800x600	65K	80	110	55
	640x480	16.7M	80	102	34
16-bit pixel port	1024x768	65K	80	90	90
	800x600	16.7M	80	110	55
Serializing 16-bit pixel port	1280x1024	256	75	67.5	135
	1024x768	16.7M	55	85	56

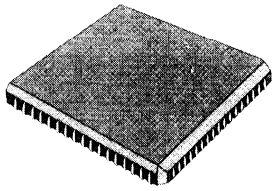
SGS-THOMSON MICROELECTRONICS

STG 1703

DUAL CLOCK SYNTHESIS PALETTE-DAC WITH 16-BIT PIXEL PORT

For complete specifications please contact your nearest sales office

- Fully integrated dual clock synthesizer and 16-bit pixel port true color Palette-DAC
- Two phase-locked loop synthesizers provide independently controlled video and memory clock outputs
- PLLs use an external crystal or a reference clock input
- 16-bit pixel port supports VGA high color and true color standards up to 135MHz
- Programmable power-down features
- On-chip checksum test



PLCC 68

DESCRIPTION

The STG 1703 is a super VGA compatible Palette-DAC with integrated clock synthesizers that can provide the memory and subsystem clock signals for the PC graphics subsystem. The video clock can be one of 2 VGA base frequencies or 14 VESA standard frequencies which can also be reprogrammed through the standard micro port interface.

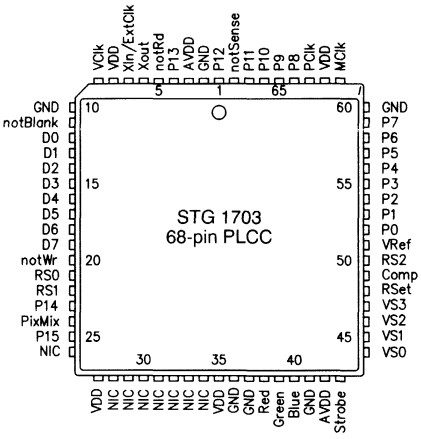
The memory clock output is also user programmable, at frequencies of up to 80MHz.

Pixel modes supported by the STG 1703 include:

- Serializing 16-bit pixel port providing 135MHz 8-bit and 56MHz 24-bit packed pixel modes using an internal PLL
- 16-bit pixel port giving faster high color/true color operation up to 110MHz sampling rate
- 8-bit pixel port giving standard SVGA and high/true color modes up to 110MHz sampling rate

The 68 PLCC pinout is designed to permit easy upgrade from the STG1700/1702 44 pin PLCC.

PIN CONNECTIONS



EXAMPLE MODES AND FREQUENCIES (ALL NON-INTERLACED)

Pixel port mode	Screen resolution	Simultaneous colors	Refresh rate (Hz)	PClk and data frequency (MHz)	Video frequency (MHz)
8-bit pixel port	1280×1024	256	60	110	110
	800×600	65K	80	110	55
	640×480	16.7M	80	102	34
16-bit pixel port	1024×768	65K	80	90	90
	800×600	16.7M	80	110	55
Serializing 16-bit pixel port	1280×1024	256	75	67.5	135
	1024×768	16.7M	55	85	56

SGS-THOMSON MICROELECTRONICS

STV9410

CRT AND LCD SEMI-GRAPHIC DISPLAY PROCESSOR

PRELIMINARY DATA

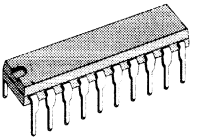
- CMOS SINGLE CHIP CRT AND LCD DISPLAY PROCESSOR
- BUILT IN 6 KBYTE RAM
- 25 ROWS OR MORE OF 40 CHARACTERS
- CRT MODE :
  - ANALOG Y LUMINANCE OUTPUT OF 4-BIT DAC
  - R,G,B DIGITAL COLOR OUTPUTS
  - FAST BLANKING OUTPUT FOR VIDEO SWITCH COMMAND
  - SYNCHRONIZATION INPUT AND OUTPUT
  - MASTER AND SLAVE SYNCHRONIZATION MODES
- LCD MODE :
  - 8 GREY LEVELS
  - 4 BIT DATA WITH CLOCK OUTPUT
  - 3 OUTPUTS FOR LCD DRIVERS SYNCHRONIZATION
  - CONTRAST ANALOG COMMAND WITH DAC OUTPUT
- 128 ALPHANUMERIC CODES AND 128 SEMI-GRAPHIC CODES IN INTERNAL ROM
- PARALLEL ATTRIBUTE THANKS TO 2 BYTE CODES
- 128 ALPHANUMERIC AND 96 SEMI-GRAPHIC USER DEFINABLE CODES DOWN-LOADABLE IN RAM
- 3-WIRE ASYNCHRONOUS SERIAL MCU INTERFACE
- SQUARE WAVE OR LOGICAL PROGRAMMABLE OUTPUT
- FULLY PROGRAMMABLE WITH 7 16-BIT CONTROL REGISTERS
- 24-PIN SO OR 20-PIN DIP PACKAGE

DESCRIPTION

STV9410 controller is a VLSI CMOS Display Processor. Time base generator, display control & refresh logic, interface for transparent MCU memory access, ROM character sets, memory to store display data & page codes and control registers are gathered on a single chip component packed in a short 20 DIP or SO plastic package.

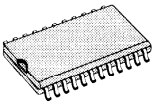
Using its 3-wire serial interface, working in both read and write mode to program 7 control registers and to access internal RAM, STV9410 is a highly flexible processor.

The STV9410 provides the user an easy to use and cost effective solution to display alphanumeric and semigraphic Information on CRT and LCD screens.



DIP20
(Plastic Package)

ORDER CODE : STV9410P

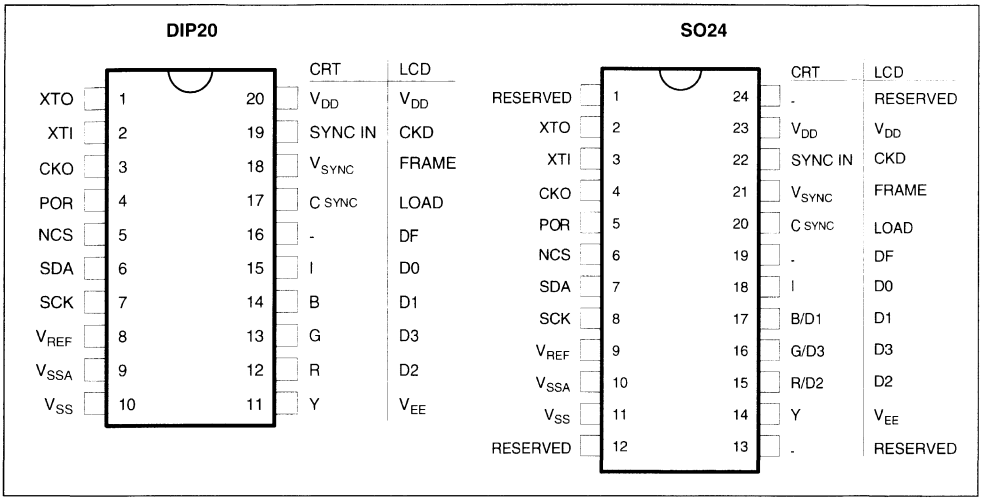


SO24
(Plastic Micropackage)

ORDER CODE : STV9410D

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS



PIN DESCRIPTION

Symbol	Pin n°		I/O	Description
	DIP20	SO24		
CRT MODE				
-	-	1	-	Reserved
XTO	1	2	O	Crystal oscillator output
XTI	2	3	I	Crystal oscillator or clock input
CKO	3	4	O	Clock output
POR	4	5	O	Programmable output port
NCS	5	6	I	Serial interface selection
SDA	6	7	I/O	Serial data input/output
SCK	7	8	I	Serial interface clock input
V_{REF}	8	9	I	Reset input and ref supply of Y DAC
V_{SSA}	9	10	S	Ref ground of Y DAC
V_{SS}	10	11	S	Ground
-	-	12	-	Reserved
-	-	13	-	Reserved
Y	11	14	O	Luminance output
R	12	15	O	Red output
G	13	16	O	Green output
B	14	17	O	Blue output
I	15	18	O	Fast blanking output
-	16	19	O	Reserved
C_{SYNC}	17	20	O	Composite synchro output
V_{SYNC}	18	21	O	Vertical synchro output
SYNC IN	19	22	I/O	Synchro input
V_{DD}	20	23	S	+5v power supply
-	-	24	-	Reserved

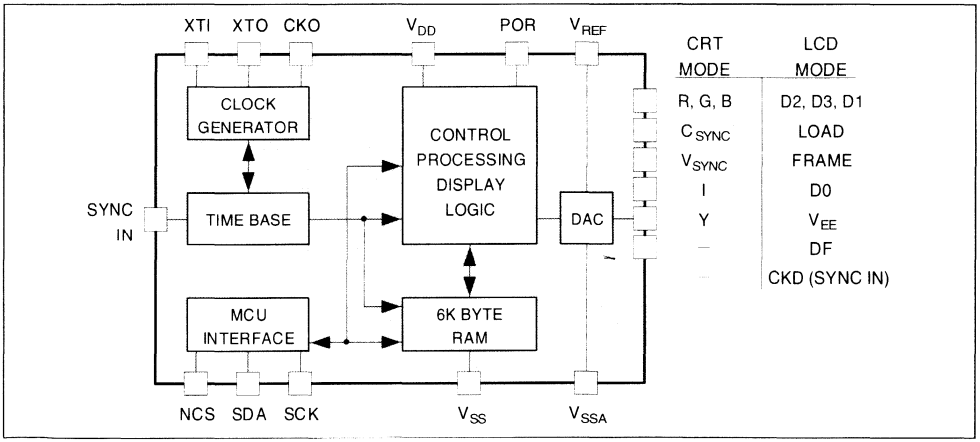
9410V-01.TBL

PIN DESCRIPTION (continued)

Symbol	Pin n°		I/O	Description
	DIP20	SO24		
LCD MODE				
-	-	1	-	Reserved
XTO	1	2	O	Crystal oscillator output
XTI	2	3	I	Crystal oscillator or clock input
CKO	3	4	O	Clock output
POR	4	5	O	Programmable output port
NCS	5	6	I	Serial interface selection
SDA	6	7	I/O	Serial data input/output
SCK	7	8	I	Serial interface clock input
V_{REF}	8	9	I	Reset input and ref supply of Y DAC
V_{SSA}	9	10	S	Ref ground of Y DAC
V_{SS}	10	11	S	Ground
-	-	12	-	Reserved
-	-	13	-	Reserved
V_{EE}	11	14	O	Constrast adjustment
D2	12	15	O	D2 Data output
D3	13	16	O	D3 Data output
D1	14	17	O	D1 Data output
D0	15	18	O	D0 Data output
DF	16	19	O	LCD polarity output
LOAD	17	20	O	Load output (line)
FRAME	18	21	O	Frame output
CKD	19	22	I/O	Data Clock
V_{DD}	20	23	S	+5v power supply
-	-	24	-	Reserved

9410V-02 TBL

BLOCK DIAGRAM



9410V-03 EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage	-0.3, +7.0	V
V_{IN}*	Input Voltage	-0.3, +7.0	V
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-40, +125	°C
P_{tot}	Power Dissipation	300	mW

9410V-03.TBL

* with respect to V_{SS}

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_a = 0 to + 70°C, fxtal = 8 to 10MHz, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.75	5.0	5.25	V
I_{DD}	Supply current *	-	-	50	mA
INPUTS					
NCS, SDA, SCK, SYNC IN, XTI					
V_{IL}	Input low voltage	0	-	0.8	V
V_{IH}	Input high voltage (except XTI)	2	-	V_{DD}	V
I_{IL}	Input leakage current (except XTI) (0 < V_{IN} < V_{DD})	-10	-	+10	µA
C_{IN}	Input capacitance (except XTI)	-	TBD	-	pF
V_{REF}					
V_{rh}	Voltage reference of DAC	1.5	-	V_{DD}	V
V_{rst}	Reset level on V_{REF}	0	-	0.4	V
R_{IN}	V_{REF} to V_{SSA} internal resistance	0.4	-	1.0	kΩ
V_{SSA}	Reference level of DAC	0	-	V_{DD}	V
OUTPUTS					
SDA, C_{SYNC}, V_{SYNC}, R, G, B, I, SYNC IN, DF, XTO, CKO, POR					
V_{OL}	Output low voltage (I_{OL} = 1.6mA)	0	-	0.4	V
V_{OH}	Output high voltage (I_{OH} = - 0.1mA)	0.8 V_{DD}	-	V_{DD}	V
Y					
	Output voltage (V_{REF}=5V, V_{SSA}=0, I_{OUT}=0)				
L_I	Integral linearity	-	-	0.25	V
L_D	Differential linearity	-	-	0.1	V
Z_{OUT}	Output impedance	-	-	0.5	kΩ
T_p	Propagation time at V_{OUT} 90% of V_{FINAL}, C_L=20pF, I_{OUT}=0, V_{REF}=5V, V_{SSA}=0V	-	-	80	ns

9410V-04.TBL

* no load on outputs

TIMINGS

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_a = 0 to + 70°C, fxtal = 8 to 10MHz,
V_{IL} = 0.8V, V_{IH} = 2V, V_{OL} = 0.4V, V_{OH} = 2.4V, C_L = 50pF, unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
SERIAL INTERFACE NCS, SCK, SDA (Figure 1)					
T_{csl}	NCS low to SCK falling edge	0			ns
T_{sch}	SCK pulse width high	80			ns
T_{scl}	SCK pulse width low	80			ns
f_{SCK}	Serial Clock Frequency			4	MHz
T_{sds}	Set up time of SDA on SCK rising edge	20			ns
T_{sdh}	Hold time of SDA after SCK rising edge	20			ns
T_{sdv}	Access time in read mode		50		ns
T_{sdx}	Hold data in read mode	0			ns
T_{sdz}	Serial interface disable time		50		ns
T_{read}	Delay before Valid Data	2			µs
OSCILLATOR INPUT (XTI) (Figure 1)					
T_{wh}	Clock high level	30			ns
T_{wl}	Clock low level	30			ns
F_{clk}	Clock frequency	8		10	MHz
RESET (V_{REF})					
T_{res}	Reset Low level pulse	2			µs
OUTPUT SIGNALS SDA, C_{SYNC}, V_{SYNC}, R, G, B, I, SYNC IN, DF, XTO, CKO, POR (Figure 2)					
T_{ph}, T_{pl}	Propagation time C_L = 30 pF C_L = 100 pF			50 100	ns ns
T_{skew}	Skew between R, G, B, I signals			30	ns

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_a = 0 to + 70°C, fxtal = 8 to 10MHz,
V_{OL} = 0.2V_{DD}, V_{OH} = 0.8V_{DD}, C_L = 100pF, unless otherwise specified)

LCD INTERFACE D0, D1, D2, D3, CKD, LOAD, DF, FRAME (Figure 3)					
t_{CYC}	CKD Shift Clock Period	4 x Pxtal			ns
t_{CH}	CKD Clock High	150			ns
t_{CL}	CKD Clock Low	150			ns
t_{WLD}	Load Pulse Width	150			ns
t_{SU}	Data Set-up Time	150			ns
t_{DH}	Data Hold Time	150			ns
t_{DF}	DF Delay from Load			100	ns
t_{SUF}	Frame Set-up before Load	150			ns

9410V-05.TBL

Figure 1 : Microcontroller Interface Timings

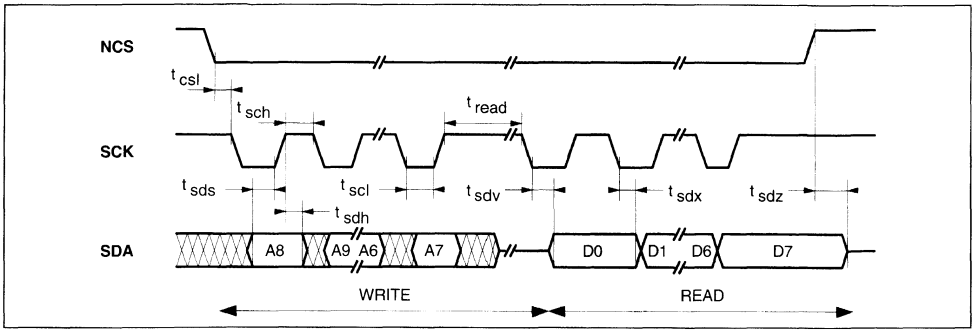


Figure 2 : Output Signals Delay versus Clock

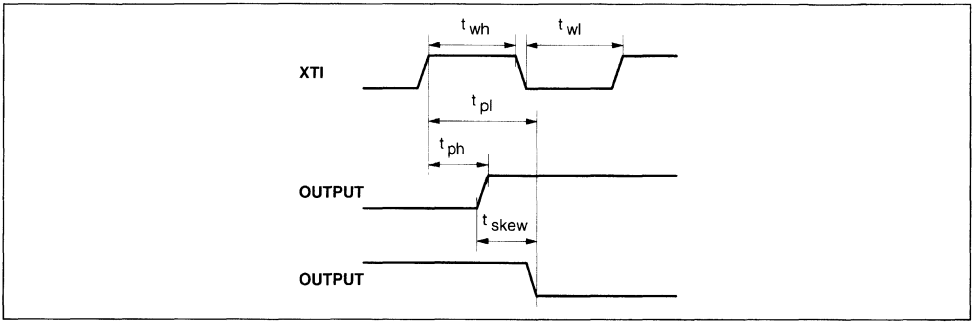
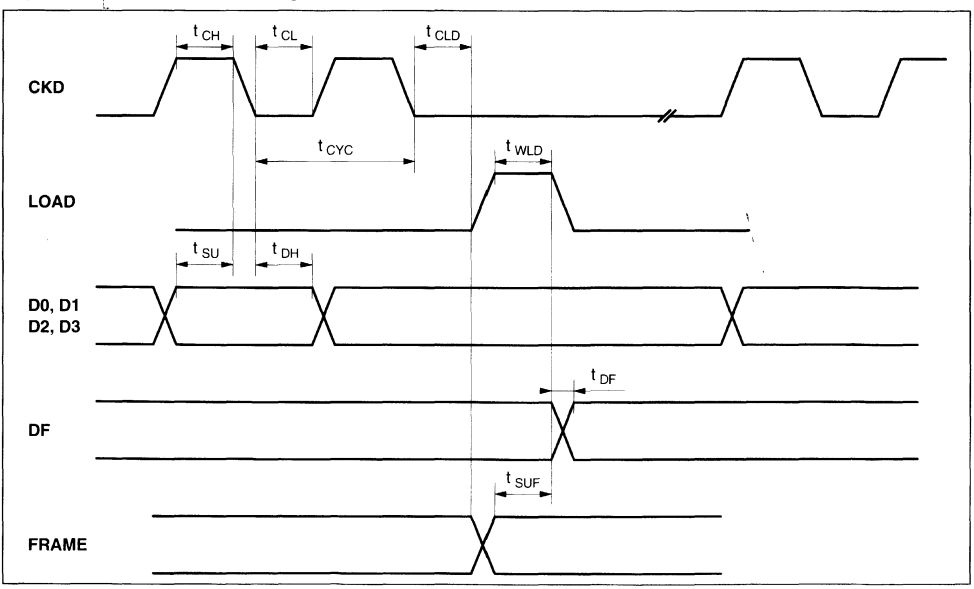


Figure 3 : LCD Interface Timings



2. FUNCTIONAL DESCRIPTION

STV9410 display processor operation is controlled by a host microcomputer via a 3-wire serial bus. It is fully programmable through seven internal read/write registers and performs all the display functions either for CRT screen or LCD passive matrix by generating pixels from data stored in its internal memory. In addition, the host can have straightforward access to the on-chip 6 Kbytes RAM, even during the display operation.

The following functions are integrated in the STV9410 :

- Crystal oscillator,
- Programmable timing generator,
- Microcomputer 3-wire serial interface,
- ROM character generator including 128 alphanumeric and 128 semigraphic character sets,
- 6 Kbytes on chip RAM to store character codes, user definable character sets, and any host microcomputer data,

and in CRT mode :

Y output driven by a 4-bit DAC

Programmable master or slave synchro interface

- R, G, B, I outputs

in LCD mode :

- LCD interface for passive multiplexed matrix
- 7 grey levels plus black

2.1 SERIAL INTERFACE

This 3-wire serial interface can be used with any microcomputer. Data transfer is supported by hardware peripherals like SPI or UART and can be emulated with standard I/O port using software routine (see application note).

NCS input enables transfer on high to low transition and transfer stays enabled as long as NCS input remains at logical low level. NCS input disables transfer as soon as low to high transition occurs, whatever transfer state is, and transfer remains disabled as long as NCS input remains at logical high level.

SCK input receives serial clock; it must be high at the beginning of the transfer; data is sampled on rising edge of SCK.

SDA input (in write mode) receives data which must be stable at least t_{sds} before and at least t_{sdh} after SCK rising edge. In read mode, SDA receives address and read command (R/W bit) and then it switches from input state to output state to send data (see Data transfer and Application Note).

Data Transfer in Write Mode

The host MCU writes data into STV9410 registers or memory. The MCU sends first MSB address with R/W bit clear, it sends secondly LSB address followed by data byte. STV9410, then, internally increments received address, ready to store a second data byte if needed, and so on, as long as NCS remains low (see Figure 4). LSB bytes are sent first.

Data Transfer in Read Mode

The host MCU reads data from STV9410 registers or memory. The MCU sends first MSB address with R/W bit set, it sends secondly LSB address, then SDA pin switches from input state to output state and provides data at SCK MCU clock rate. Notice that a minimum delay is needed before sending the first SCK rising edge to sample the first data bit (at least 2µs). After each data byte STV9410 internally increments address and it sends next data at SCK frequency. SDA remains in output state as long as NCS remains low (see Figure 5).

Address auto-incrementation allows host MCU to use 8, 16, 32-bit data words to optimize transfer rate. LSB bytes are sent first. SCK max speed is 4MHz.

Figure 4 : Serial Interface Write Mode

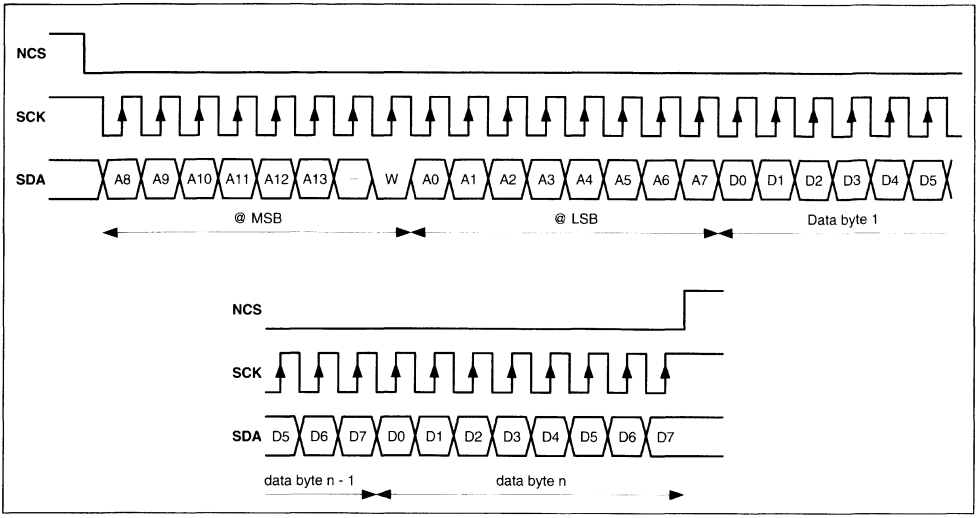
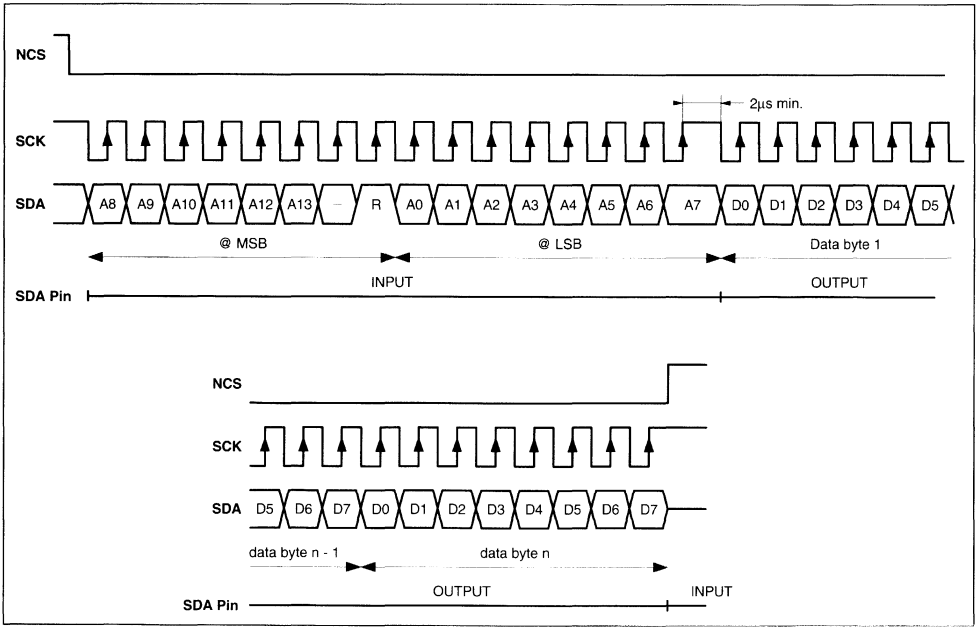
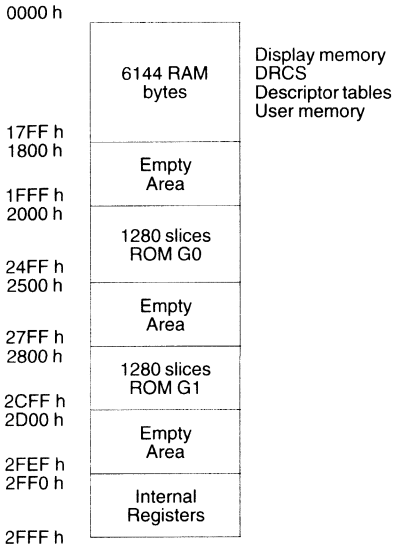


Figure 5 : Serial Interface Read Mode



2.2. ADDRESSING SPACE

STV9410 registers, RAM and ROM are mapped in a 12 kbytes addressing space. The mapping is the following :



2.2.1 Register Set

VERT

2FF1	LCD	ILC	C/H	V/P	VSE	HSE	-	F8
2FF0	F7	F6	F5	F4	F3	F2	F1	F0

LCD : LCD/CRT mode
ILC : Interlaced/non-interlaced
C/H : Composite/horizontal synchro
V/P : Vertical synchro/port
VSE : Vertical synchro enable
HSE : Horizontal synchro enable
F (8:0) : Number of scan line per frame

HORI

2FF3	-	-	-	-	-	MG2	MG1	MG0
2FF2	-	-	L5	L4	L3	L2	L1	L0

MG (2:0): Margin duration
L (5:0) : Line duration

HSYN

2FF5	SU7	SU6	SU5	SU4	SU3	SU2	SU1	SU0
2FF4	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

SU (7:0) : Synchro rising edge position
SD (7:0) : Synchro falling edge position

POR

2FF7	VOE	-	-	-	-	-	TE	PV
2FF6	N7	N6	N5	N4	N3	N2	N1	N0

VOE : Video output enable
TE : Timer enable
PV : Port value
N (7:0) : Square wave period

ADDR

2FF9	-	P12	P11	P10	P9	P8	P7	P6
2FF8	-	G12	G11	G10	-	A12	A11	A10

P (12:6) : Address of first descriptor of page to display
G (12:10) : Graphic character set address
A (12:10) : Alphanumeric character set address

DISP

2FFB	IMG	GMG	RMG	BMG	-	-	-	HIC
2FFA	FLE	CCE	IN1	IN2	BR3	BR2	BR1	BR0

IMG, GMG, RMG, BMG : Margin value of I, G, R, B outputs
HIC : High contrast forces black and white on outputs
FLE : flashing enable
CCE : Conceal enable
IN1, IN0 : Fast blanking mode
BR (3:0) : Luminosity adjustment on Y output

CURS

2FFD	CEN	CBL	CUL	-	C12	C11	C10	C9
2FFC	C8	C7	C6	C5	C4	C3	C2	C1

CEN : Cursor enable
CBL : Cursor blinking
CUL : Cursor underlining
C (12:1) : Cursor address

2.2.2 Descriptor

UNIFORM

MSB	0	RTP	FFB	-	I	C2	C1	C0
LSB	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

RTP : Real time port
FFB : Field flyback
I : Fast blanking
C (2:0) : Strip color (G, R, B)
SL (7:0) : Number of scan line of the strip

CHARACTER

MSB	1	RTP	DE	ZY	C12	C11	C10	C9
LSB	C8	C7	C6	C5	C4	C3	C2	C1

RTP : Real time port
DE : Display enable
ZY : Vertical zoom
C (12:1) : Address of first character to display

2.2.3 Code Format

ALPHANUM

MSB (ODD)	CHARACTER NUMBER							
LSB (EVEN)	0	IV	DW	DH	FL	FC2	FC1	FC0

CHARACTER NUMBER : lower than 80h in ROM
from 80h to FFh in RAM

IV : Inverted video
DW : Double width
DH : Double height
FL : Flashing
FC (2:0) : Foreground color (G, R, B)

GRAPHIC

MSB (ODD)	CHARACTER NUMBER							
LSB (EVEN)	1	BC2	BC1	BC0	FL	FC2	FC1	FC0

CHARACTER NUMBER : lower than 80h in ROM
from 80h to DFh in RAM

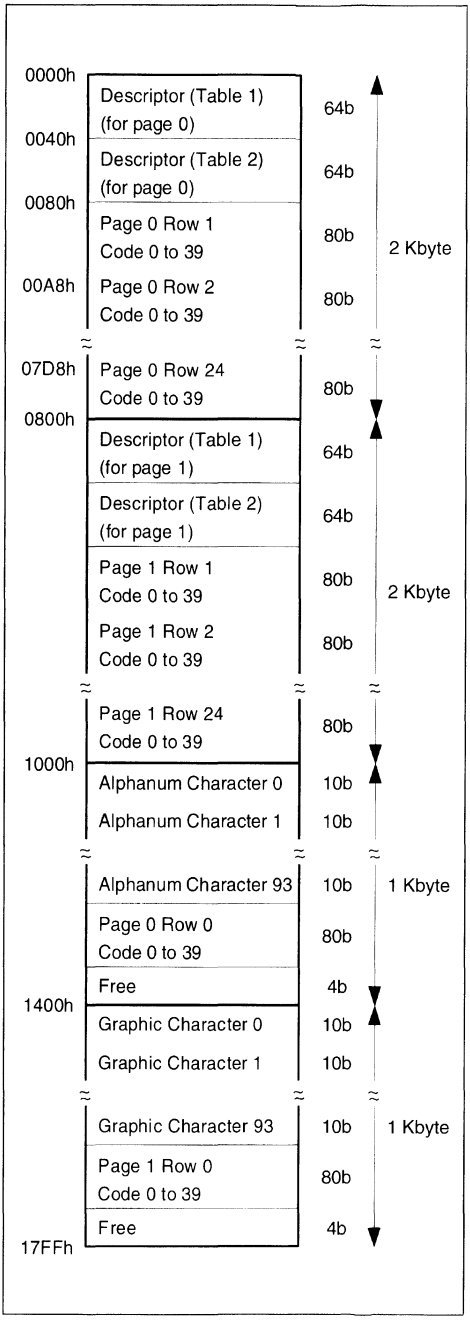
BC (2:0) : Background color (G, R, B)
FL : Flashing
FC (2:0) : Foreground color (G, R, B)

CONTROL

MSB (ODD)	1	1	1	EOL	IF	IB	UL	CC
LSB (EVEN)	1	BC2	BC1	BC0	HG	FC2	FC1	FC0

EOL : End of line
IF, IB : Fast blanking foreground/background
UL : Underline
CC : Conceal
BC (2:0) : Background color (G, R, B)
HG : Hold graphic
FC (2:0) : Foreground color (G, R, B)

2.2.4 Example of RAM Maping



2.3 CLOCK AND TIMING GENERATOR

The whole timing is derived from XTI input frequency which can be an external generator or a crystal signal thanks to XTO/XTI oscillator.This clock is also pixel frequency which can be chosen between 8MHz to 10MHz (pxlck). This clock is available on CKO pin. It should be use for the MCU, saving a crystal in the application.

The active area of a video line is 320 pixels periods long (40 characters of 8 pixels wide). Number of lines per frame, margin width, line duration, leading and trailing edges of horizontal synchronization are fully programmable in CRT mode using VERT, HORI, HSYN registers.

A RESET, can be applied to STV9410 by pulling low V_{REF} pin ($\leq 0.4V$).

On RESET, default values are forced into configuration registers and video outputs are at low level.

All unused bit of registers are always read as "0".

2.3.1 Time Base Registers

Vertical Time Base and Configuration Register (VERT)

Internal address : 2FF1-2FF0 h

RESET value :01-36 h

(@ = RESET default configuration)

2FF1 h	LCD	ILC	C/H	V/P	VSE	HSE	-	F8
@	0	0	0	0	0	0	0	1
2FF0 h	F7	F6	F5	F4	F3	F2	F1	F0
@	0	0	1	1	0	1	1	0

LCD : 1 LCD mode
0 CRT mode @

ILC : 1 Interlaced scanning
0 non-interlaced scanning @

C/H : 1 C_{SYNC} is composite synchro
0 C_{SYNC} is horizontal synchro @

V/P : 1 V_{SYNC} is vertical synchro
0 V_{SYNC} is RTP bit of current descriptor @

VSE : 1 enable vertical synchro with SYNC IN
0 disable @

HSE : 1 enable horizontal synchro with SYNC IN
0 disable @

F (8:0) : scan line number per frame (@ 312)

Figure 6 : Vert Register Scan Lines Programmation

2FF1							2FF0									Nb of Scan Lines	LSB HEXA
LCD	ILC	C/H	V/P	VSE	HSE	-	F8	F7	F6	F5	F4	F3	F2	F1	F0	F(0:8) + 2	
X	X	X	X	X	X	-	0	0	0	0	0	0	0	0	0	Not allowed	-
							0	0	0	0	0	0	0	0	1	3	01
							0	0	0	0	0	1	1	1	0	16	0E
							0	0	0	1	1	1	1	1	0	64	3E
							0	0	1	1	0	0	0	1	0	100	62
							0	0	1	1	1	0	1	1	0	120	76
							0	1	1	1	0	1	1	1	0	240	EE
							0	1	1	1	1	1	0	0	0	250	F8
							1	0	0	0	0	0	1	0	0	262	04
							1	0	0	0	0	0	1	0	1	263	05
							1	0	0	1	1	0	1	0	0	310	34
							1	0	0	1	1	0	1	1	0	312	36
							1	0	0	1	1	0	1	1	1	313	37
							1	0	0	1	1	1	1	1	0	320	3E
							1	1	1	0	1	1	1	1	0	480	DE
							1	1	1	1	1	1	1	1	0	512	FE
							1	1	1	1	1	1	1	1	1	513	FF

F[8:0] = Scan Line Number - 2

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Margin and Horizontal Time Base Register (HORI)

Internal address : 2FF3-2FF2 h
RESET value :03-3F h
(@ = RESET default configuration)

2FF3	-	-	-	-	-	MG2	MG1	MG0
@	0	0	0	0	0	0	1	1
2FF2	-	-	L5	L4	L3	L2	L1	L0
@	0	0	1	1	1	1	1	1

MG(2:0) : Left and right margin duration (@ = 4µs)

$$MG = \left(\frac{\text{Margin Duration}}{8\ \text{pxlck}}\right) - 1$$

L(5:0) : Line duration (@= 64µs)

$$L = \left(\frac{\text{Line Duration}}{8\ \text{pxlck}}\right) - 1$$

Horizontal Synchronization Register (HSYN)

Internal address : 2FF5-2FF4 h
RESET value :E6-DC h
(@ = RESET default configuration)

2FF5	SU7	SU6	SU5	SU4	SU3	SU2	SU1	SU0
@	1	1	1	0	0	1	1	0
2FF4	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
@	1	1	0	1	0	1	0	0

SU(7:0) : SYNC rising edge position (@ = 57.75µs)

$$SU = \left(\frac{\text{Rise Edge Position}}{2\ \text{pxlck}}\right) - 1$$

SD(7:0) : SYNC falling edge position (@= 53.25µs)

$$SD = \left(\frac{\text{Falling Edge Position}}{2\ \text{pxlck}}\right) - 1$$

Figure 7 : HSYN Register Synchro Pulse Programmation

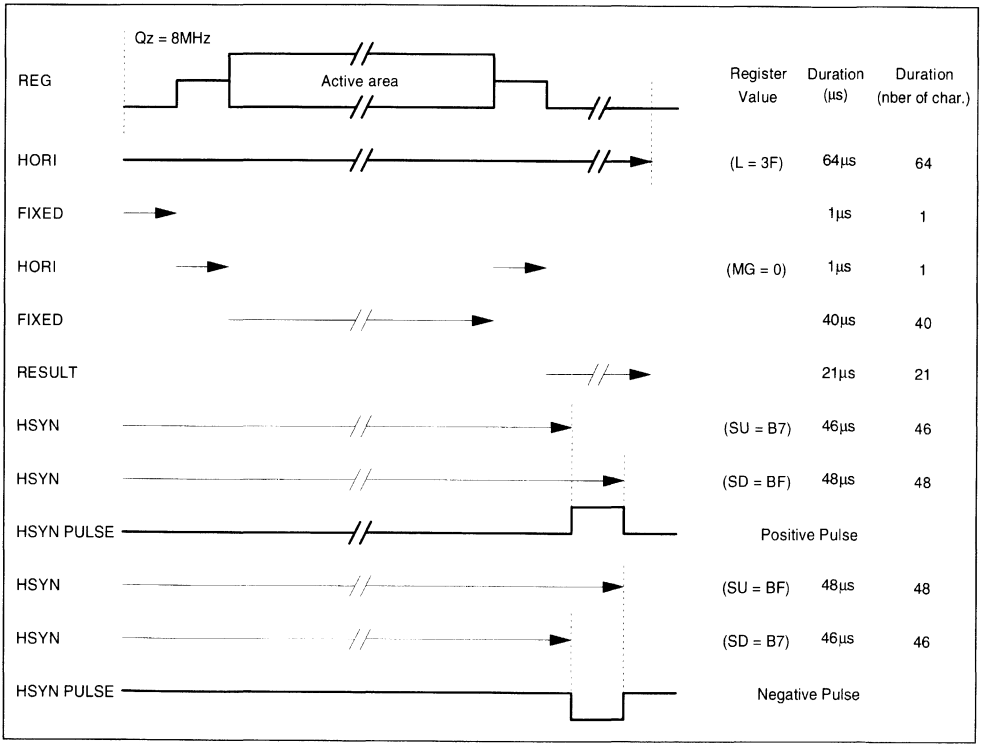
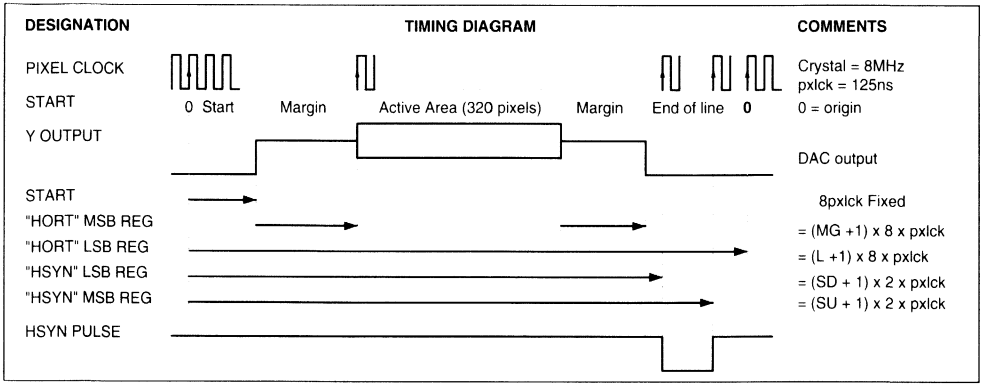


Figure 8 : Horizontal Synchronization Timing



Video Validation and Port Register (PORT)
Internal address : 2FF7-2FF6 h
RESET value :00-00 h
(@ = RESET default configuration)

2FF7	VOE	-	-	-	-	-	TE	PV
@	0	0	0	0	0	0	0	0
2FF6	N7	N6	N5	N4	N3	N2	N1	N0
@	0	0	0	0	0	0	0	0

VOE : Video Output Enable
1 enable synchro & video outputs
0 disable synchro & video outputs @
(@ Output Y, C_{SYNC}, V_{SYNC}, R, G, B, I, POR, and DF are grounded, Input SYNC IN is high impedance)

TE : Timer Enable
1 POR provides a square wave signal with a period of 16 x N(7:0) x pxlck
0 POR output is PV bit @

PV : Port Value
POR output value if TE=0 (@=0)

N(7:0) : Square wave period on POR if TE=1 (@=0)

BEWARE

The programmation of VERT, HORI, HSYN registers must be consistent. To get a proper work of the controller, the following conditions must, in any mode (CRT or LCD), be fulfiled :

- $SU \neq SD$
- $\frac{SU+1}{4} < L$ and $\frac{SD+1}{4} < L$
- $2(MG+1) + 40 \leq L$

Line period is :
- $P_L = [L(5:0) + 1] \times 8$ pxlck
- In LCD, MG(2:0) can be 0, then minimum Line Period is $P_{L\,(min.)} = 43 \times 8$ pxlck

Frame period is :
- $P_F = [F(8:0) + 2] \times P_L$
- In LCD, using a 240 lines matrix, F(8:0) = 238, then minimum frame is :
  $P_{F\,(min.)} = 240 \times 43 \times 8$ pxclk

Pixel period is :
- $Pxclk = \frac{P_{Frame}}{[F(8:0)+2][L(5:0)+1] \times 8}$
- In LCD, using a 240 lines matrix, and MG(2:0) = 0, $Pxclk = \frac{P_{Frame}}{240 \times 43 \times 8}$

Interlaced mode conditions :
- $\frac{SU+1}{4}$ and $\frac{SD+1}{4} < L$
- $\frac{SU+1}{4}$ and $\frac{SD+1}{4} > (MG+1) + 42$

2.3.2. CRT Mode

In CRT mode, the Vsync signal appears at the first two lines of the first strip of the descriptor list. It is recommended to provide an uniform blanked (with FFB bit) strip as first descriptor. The scan line number of this strip have to be equal or higher than scan line number of the vertical blanking Interval.

Master Mode

This mode is selected by writing VSE and HSE bit of VERT register with logical value "0".

Non-interlaced mode is selected by writing ILC bit of VERT register with logical value "0".

Horizontal or composite synchronization signal is output on C_{SYNC} pin, Vertical synchronization signal is output on V_{SYNC} pin.

Signal waveforms are described in Figure 9.

Interlaced mode is selected by writing ILC bit of VERT register with logical value "1".
Even frame is identical to non-interlaced frame. V_{SYNC} PULSE is low during second half of last line of previous Odd frame and during the two first lines of current Even frame.
Odd frame is one scan line more than Even frame. V_{SYNC} PULSE is low during the two first lines and up to first half of the third line of current Odd frame. Half line corresponds to 17th character position. Signals waveforms are described in Figure 10.

Slave Mode

This mode is activated by writing VSE and/or HSE bit of VERT register with logical value "1". Then SYNC IN input signal is sampled according to procedure described below.

Vertical Synchronization

SYNC IN signal may be either a vertical synchronization or a composite synchronization. It is sampled on first pixel of each scan line active area. As soon as SYNC IN signal low level is detected, vertical time base counter F(8:0) of VERT register is reset without any modification of other time base registers.

Horizontal Synchronization

SYNC IN is sampled one pxlck before and one pxlck after internal horizontal pulse transition. If falling edge is not found, one pixel period is added to internal line duration. Using a line frequency locked clock applied on XTI, internal scan line becomes phase locked after few scan line periods at programmed value (see Figure 11).

2.3.3 LCD Mode

LCD mode only works as a master mode with 320 pixels per line. Internal algorithm allows 8 grey levels on passive LCD matrix. Number of scan line is programmable. In order to get maximum refresh frequency of display, margin and line duration must be reduced to miminum. Interlaced mode and external synchronization are not allowed. The 1st line of the first descriptor in the description list correspond to the first line of the LCD display. Y output provides a programmable voltage usable to adjust contrast of LCD display. To reduce supply current consumption, when Y output is unused, V_{SSA} must not be connected to ground, and V_{REF} pin works as a reset pin. Notice that SYNC IN Pin provides (CKD) data clock signal.

2.4 POR OUTPUT

POR is a standard I/O pin programmable at logical level "1" or "0". It can also provide a programmable square wave signal of period
P = 16 x N(7:0) x pxlck ($0 \leq N \leq 255$).

It can drive a capacitive buzzer (see application diagram at page 22).

RESET value of PORT is "0".

Figure 9 : ODD and EVEN Synchronization Pulses in Non-interlaced Mode

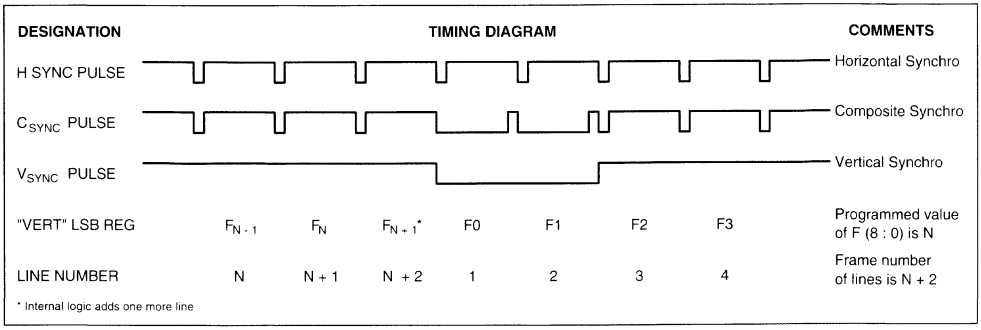


Figure 10 : Interlaced Mode Synchronization Pulses

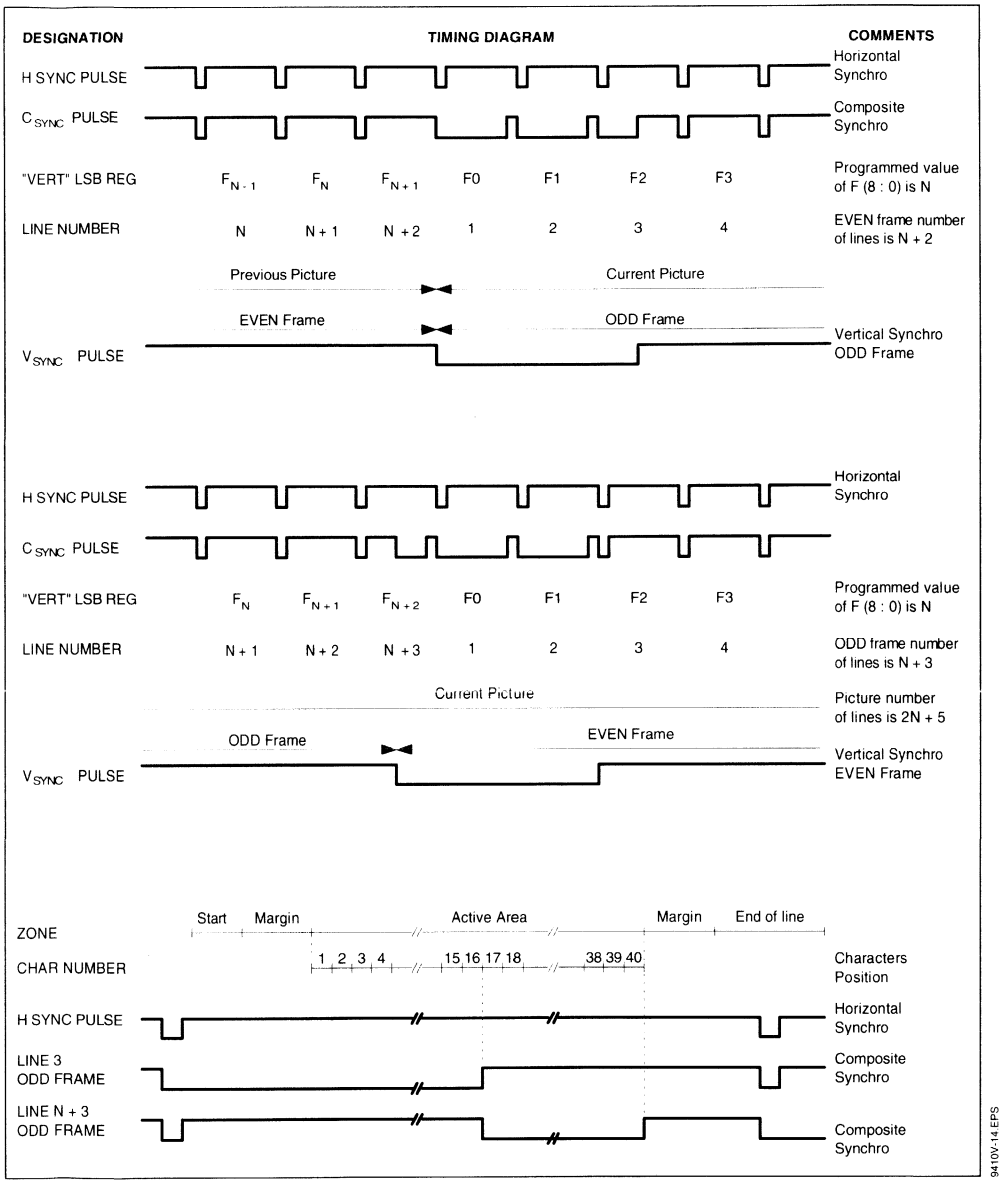
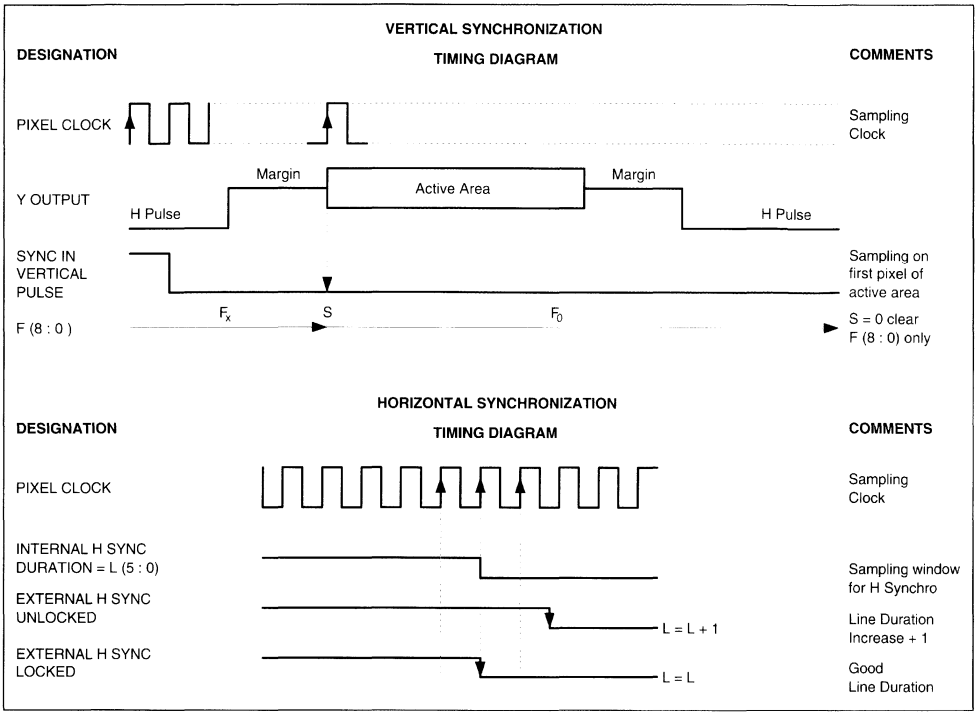


Figure 11 : Synchronization on SYNC IN External Signal



3. INTERNAL REGISTER DESCRIPTION

STV9410 is programmable with 7 registers of 16 bit each. These registers can also be programmed in byte mode. Not significant bit must be cleared in order to be compatible with next generation products.

3.1 TIME BASE REGISTERS

Registers VERT, HORI, HSYN and PORT are described in chapter 2.3

3.2 ADDRESS REGISTER (ADDR)

Internal address : 2FF9-2FF8 h

RESET value :00-00 h
(@ = RESET default configuration)

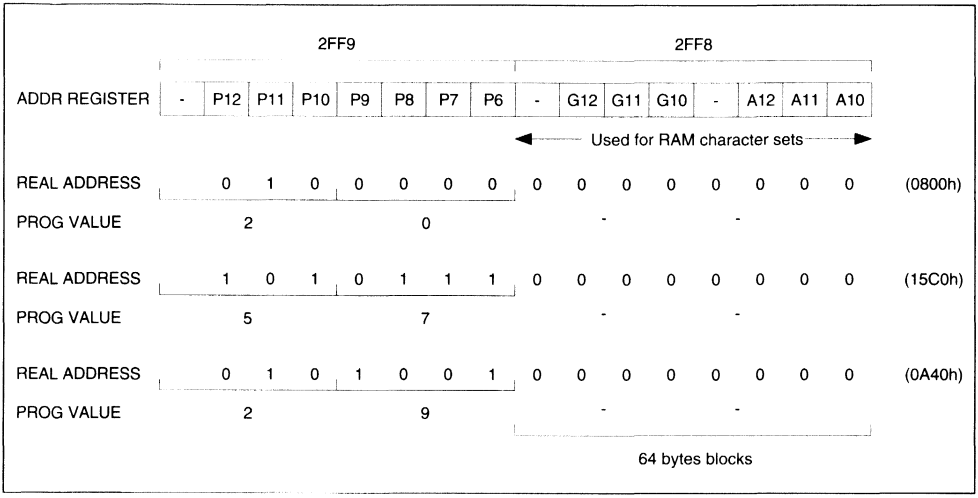
2FF9 h	-	P12	P11	P10	P9	P8	P7	P6
@	0	0	0	0	0	0	0	0

2FF8 h	-	G12	G11	G10	-	A12	A11	A10
@	0	0	0	0	0	0	0	0

P(12:6) : Page first descriptor address, P(5:0)=0 @
G(12:10) : Graphic character set MSB address, G(9:0)=0 @
A(12:10) : Alphanumeric character set MSB address, A(9:0)=0 @

NB : as addresses are in RAM area, address bit 13 is reset to "0"

Figure 12 : ADDR Register and Descriptor List Address



3.3 DISPLAY REGISTER (DISP)

Internal address : 2FFB-2FFA h

RESET value :00-00 h
(@ = RESET default configuration)

2FFB	IMC	GMG	RMG	BMG	-	-	-	HIC
@	0	0	0	0	0	0	0	0

2FFA	FLE	CCE	IN1	IN0	BR3	BR2	BR1	BR0
@	0	0	0	0	0	0	0	0

IMG, GMG, RMG, BMG : Margin value of I,G,R,B outputs and background color and insertion default attribute of next alphanumeric character. In case of graphic characters only I is default attribute.

HIC : Forces alphanumeric characters background black (R, G, B = 0), and foreground white (R, G, B = 1) for maximum contrast, 0 = disable @

FLE : Flashing enable, 0 = disable @

CCE : Conceal enable, 0 = disable @

IN1,IN0 : Insertion attribute mode selection. Mode selects value of I output during active area of scan line in CRT mode; I output value (during margin) is programmed with HORI register; during uniform strip I output value is set according to strip descriptor.
During active time slot :

- 0 0 : I output gets value of current code I attribute (margin attribute or control character attribute) @
- 0 1 : I is set ("1")
- 1 0 : I output gets value of current code I attribute if I=0 R,G,B are reset to "0"
- 0 1 : Reserved mode

BR(3:0) : This value is combined with pixel value to drive Y DAC in CRT mode :
Y= 4xG + 2xR + B + BR(2:0) + 3x(R or G or B) (logical or)
R, G, B, I, Y, = 0 during line flyback.

Black level is output with R, G, B = "0".
White level is output with R, G, B = "1".

During frame flyback, R, G, B, I, Y provides signal according to uniform strip descriptor FFB bit state (see chapter 4.2.1)
During LCD mode BR(3:0) drives continuously Y DAC. Notice that only bit 0 to 2 of BR are used in CRT mode.

3.4. CURSOR REGISTER (CURS)

Internal address : 2FFD-2FFC h

RESET value : 00-00 h
(@= RESET default configuration)

2FFD	CEN	CBL	CUL	-	C12	C11	C10	C9
@	0	0	0	0	0	0	0	0

2FFC	C8	C7	C6	C5	C4	C3	C2	C1
@	0	0	0	0	0	0	0	0

CEN : Cursor enable, 0 = disable @

CBL : 0 cursor blinking off, character blinking attribute unchanged @
1 cursor blinking on, blinking is mixed with character blinking attribute. Blinking frequency is around 1Hz and duty cycle 50%

CUL : 0 character underline attribut is complemented on cursor position @
1 character color is complemented on cursor position

C(12:1) : Cursor address (not a screen position)

4. DISPLAY CONTROL

4.1 SCREEN DESCRIPTION

A screen is composed of successive scan lines gathered in one or several strips. Each strip is defined by a descriptor stored in memory. A list of descriptor allows screen composition, different screens can be defined in memory (see application note and Figures 13, 14.).

Two kinds of strip are available :

- **Uniform color strip**

  Applications :
  - vertical front and back porch
  - vertical synchro
  - border lines

  Parameters :
  - number of scan lines
  - color

- **Character strip**

  Characters and attributes are defined by a succession of codes stored in memory; thanks to the character code, a memory address is calculated and used to get the character pattern.

  Parameters :
  - address of the first code
  - size, display enable

Figure 13 : Programmation of Number of Scan Lines - Vertical Register VERT (2FF0/2FF1) and Descriptor List

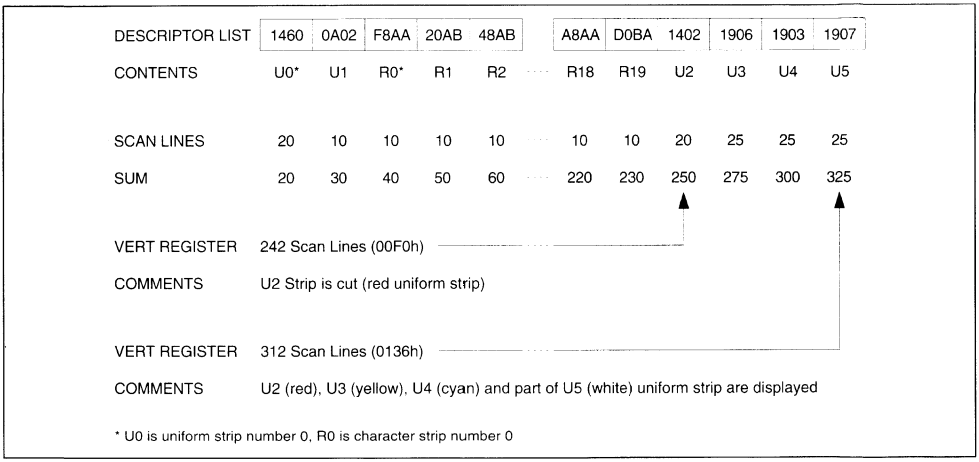
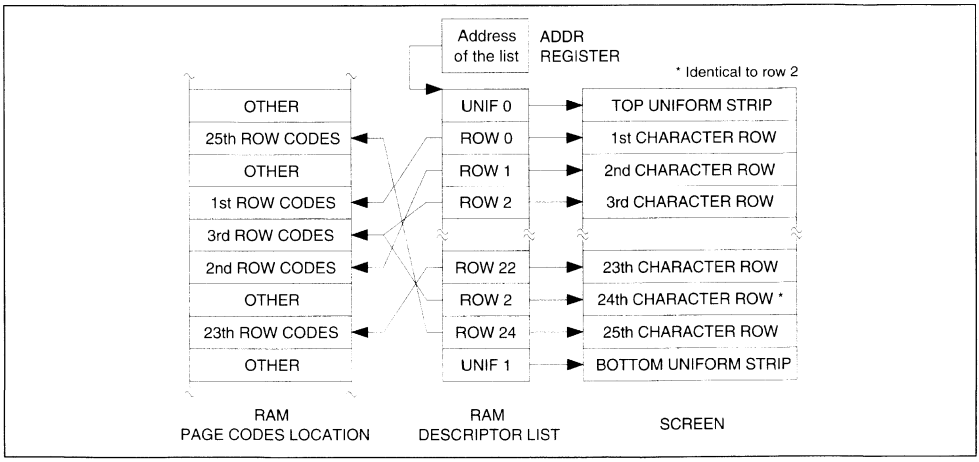


Figure 14 : Relation between Screen Location/Descriptor Pointer/RAM Page Codes



4.2. STRIP DESCRIPTOR

Each strip is defined by 2 bytes.
During the vertical retrace, an internal descriptor address counter is initialised with the value P(12:0) of ADDR register; on the trailing edge of vertical synchro, the first strip descriptor is loaded into the display controller; if it is an uniform strip, selected color is displayed during the corresponding number of scan lines; if it is a character strip, left margin followed by text, followed by right margin are displayed during 10 scan lines ; the next descriptor is then read, and the same process is repeated until the last scan line, this information being given by the vertical timing generator.

4.2.1 Uniform Strip

0	RTP	FFB	-	I	C2	C1	C0
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

RTP : Real Time Port
RTP bit value is output on V_{SYNC} when V/P bit of VERT register is "0", along the complete duration of the strip scan line. Not used in LCD mode.

FFB : Field Flyback
0 R, G, B, I and Y outputs are defined by corresponding bit of DISP for margin and C(2:0) and I for active area
1 R, G, B, I and Y outputs are cleared during Field Flyback, whatever other parameters are.

I : 0 Fast Blanking Disable
1 Fast Blanking Enable

C(2:0) : G, R, B, value during the active area of the strip (320 pixels)

SL(7:0) : Number of scan lines of the strip, minimal value is 1.

4.2.2. Character Strip

1	RTP	DE	ZY	C12	C11	C10	C9
C8	C7	C6	C5	C4	C3	C2	C1

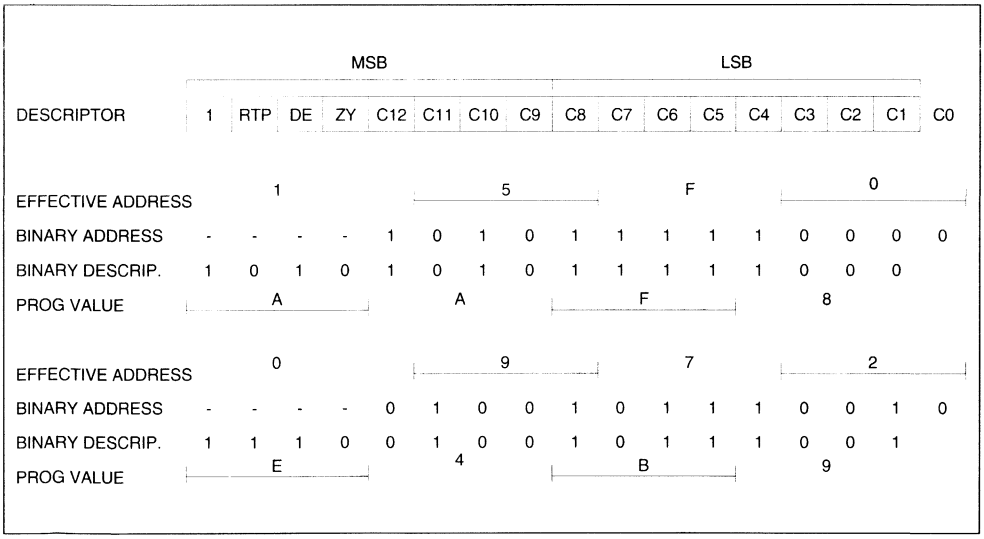
RTP : Real Time Port
RTP bit value is output on V_{SYNC} when V/P bit of VERT register "0", along the complete duration of the strip line, during the whole strip.

DE : Display Enable
0 display off, the strip is displayed with margin attributes IMG, GMG, RMG, BMG bit of DISP register,
1 display on, the strip works as selected.

ZY : Vertical Zoom
0 normal display mode
1 all scan line are doubled, providing a vertical zoom effect

C(12:1) : Address of the first code to display

Figure 15 : Character Strip Descriptor - First Character Address Selection



5. CHARACTER CODE FORMAT

Each character is defined with a two bytes code; the first is at an even address, the second is at the following odd address. Some attributes are parallel, other keep the last explicit value.
STV9410 uses 3 different types of codes.

5.1 ALPHANUMERIC CHARACTERS
(256 patterns)

The background color is not defined by the code; it takes the same value as the previous character or it has the value of the margin color at the beginning of each row.
The character pattern lies in ROM if CHARACTER NUMBER is lower than 80h, (ALPHANUMERIC CHARACTER SET is shown in TABLE 3),else it is User Defined Character in RAM (DRCS).

ODD	CHARACTER NUMBER							
EVEN	0	IV	DW	DH	FL	FC2	FC1	FC0

CHARACTER NUMBER : ROM or RAM character set code
IV : Inverted video if set.
DW : Double character width if set, code must be repeated for the right part of the character.
DH : Double character height if set, code must be repeated for the bottom part of the character. The first DH attribute encountered in a vertical column is always interpreted as a top part.
FL : Flashing, inverted phase if IV is set.
FC(2:0) : Foreground color (Green, Red, Blue).

5.2. GRAPHIC CHARACTERS (224 patterns)

IV, DW, DH, UL take the value "0"
CHARACTER NUMBER must be lower than E0h.
The character pattern lies in ROM if CHARACTER NUMBER is lower than 80h, (STANDARD MOSAIC character set is shown in Table 4), else it is an User Defined Character in RAM (DRCS).

ODD	CHARACTER NUMBER							
EVEN	1	BC2	BC1	BC0	FL	FC2	FC1	FC0

CHARACTER NUMBER : ROM or RAM character set code
BC(2:0) : Background color (Green, Red, Blue).
FL : Flashing.
FC(2:0) : Foreground color (Green, Red, Blue).

5.3. CONTROL CHARACTERS (32 codes)

These characters are displayed as foreground color spaces if HG bit is clear. They can change some attributes applying to themselves and to the following string.

ODD	1	1	1	EOL	IF	IB	UL	CC
EVEN	1	BC2	BC1	BC0	HG	FC2	FC1	FC0

EOL : End Of Line
0 normal control code
1 space are displayed until the end of the row, allowing memory space saving
IF,IB : Insert foreground, Insert background attribute.
0 fast blanking disable
1 fast blanking enable
UL : Underlined
0 disable
1 enable
CC : Conceal Character
0 disable
1 enable, character is diplayed as a space.
BC(2:0) : Default background color of next character(s)
HG : Hold Graphics
0 disable, the control character is displayed as a uniform space character with foreground color fixed by FC(2:0)
1 enable, the control character pattern takes the last mosaic value encountered in the row, if any, or is a space.
FC(2:0) : G, R, B foreground value of the control character

At the beginning of each row, those attributes take default values :
- EOL, UL, CC, HG = 0
- IF = 1
- IB = IMG (Margin insert attribute)
- BC(2:0) = GMG, RMG, BMG (Margin color).

Notice that following characters code is reserved for futur use.

ODD	1	1	1	1	X	X	X	1
EVEN	1	X	X	X	X	X	X	X

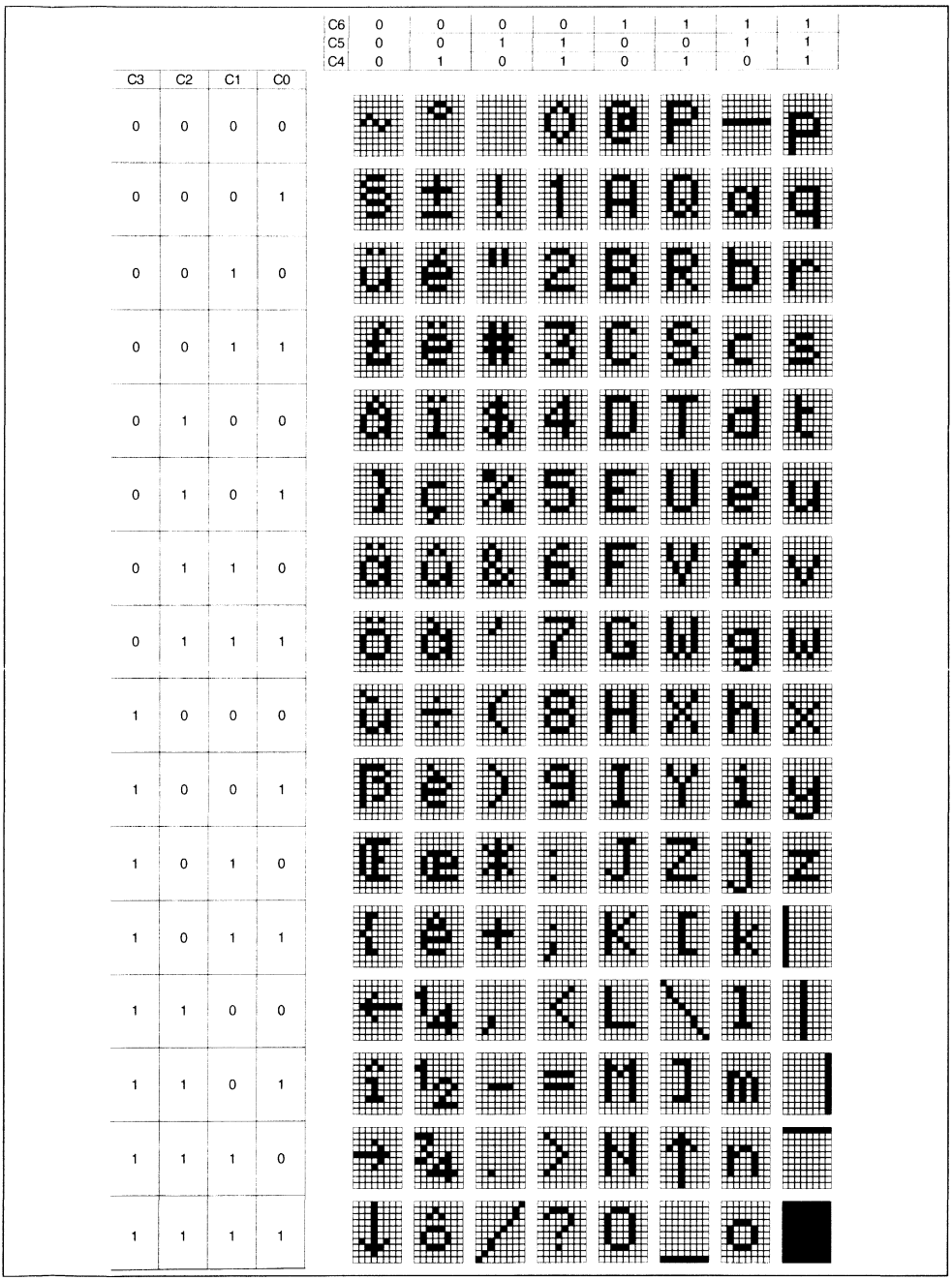
6. CHARACTER GENERATORS

Each pixel is defined with one bit, 1 refers to foreground color, and 0 to background color.

PX7	PX6	PX5	PX4	PX3	PX2	PX1	PX0

PX7 is the leftmost pixel.
Character slice address :
Each character generator contains a succession of patterns arranged as a number of horizontal slices :
- Slice addr = (Set addr) + Char Number x 10 + (slice number)
- Char Number is the number of the character in the set; using DRCS in RAM, the calling code of the character is the number of the character in the set plus 80h.
- Set addr is defined in ADDR register, in RAM for DRCS (see section 3.2), and is 2000h for ALPHANUMERIC ROM, and 2800h for STANDARD MOSAIC ROM.

Table 3 : Go Alphanumeric Character Set 40 Character/Row STV9410



9410V-20.EPS

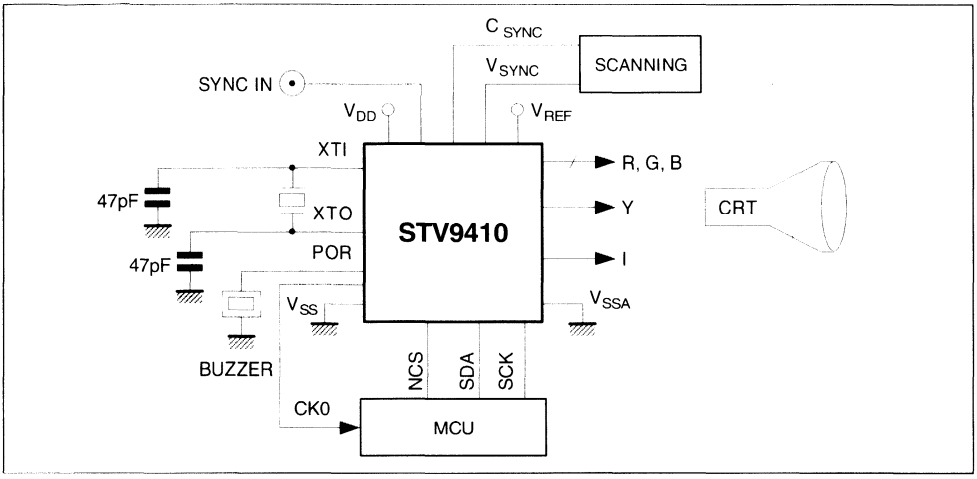
Table 4 : G_1 Semigraphic Character Set

				SEPARATED SEMI-GRAPHIC				MOSAIC SEMI-GRAPHIC			
C6				0	0	0	0	1	1	1	1
C5				0	0	1	1	0	0	1	1
C4				0	1	0	1	0	1	0	1
C3	C2	C1	C0								
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								

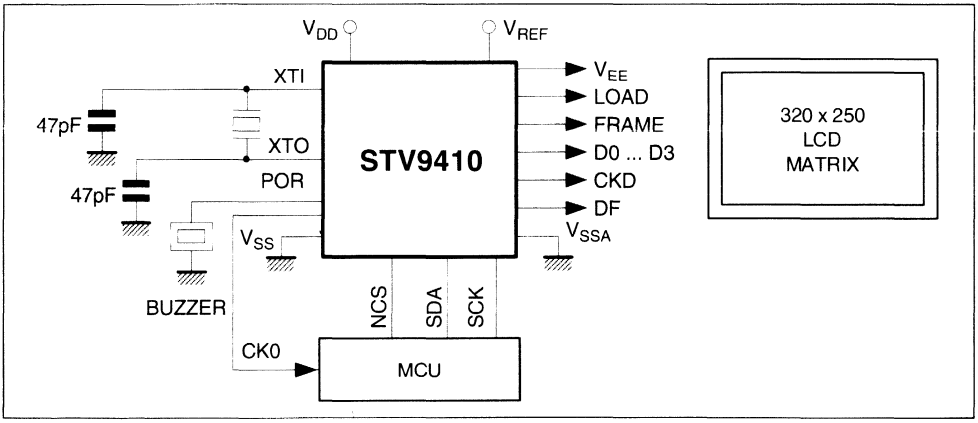
9410V-21.EPS

TYPICAL APPLICATIONS

CRT APPLICATION DIAGRAM



LCD APPLICATION DIAGRAM

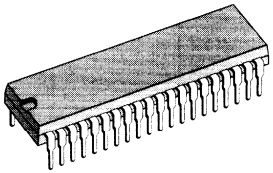


SGS-THOMSON MICROELECTRONICS

TS9347

SINGLE CHIP SEMI–GRAPHIC DISPLAY PROCESSOR

- SINGLE CHIP LOW-COST CRT CONTROLLER
- UP TO 60 Hz SCREEN REFRESH RATE
- 32 KBYTE DEDICATED MEMORY ADDRESSING SPACE
- 2 SCREEN FORMATS :
  25 ROWS OF 40 CHARACTERS
  25 ROWS OF 80 CHARACTERS
- ON-CHIP 154 ALPHANUMERIC AND 128 SEMIGRAPHIC CHARACTER GENERATOR
- EASY EXTENSION OF USER DEFINED ALPHANUMERIC OR SEMI-GRAPHIC SETS (>1K characters)
- 40 CHARACTERS/ROW ATTRIBUTES : FOREGROUND AND BACKGROUND COLOR, DOUBLE HEIGHT, DOUBLE WIDTH, BLINKING, CONCEAL, INSERT
- 80 CHARACTERS/ROW ATTRIBUTES : UNDERLINING, BLINKING, REVERSE, COLOR SELECT
- PROGRAMMABLE ROLL-UP, ROLL-DOWN, UPPER OR LOWER SERVICE ROW
- ON-CHIP R, G, B SHIFT REGISTERS
- ANALOG COMPOSITE LUMINANCE SIGNAL OUTPUT
- VERSATILE I/O CONFIGURATION : VIDEO AND SYNC OR GENERAL PURPOSE I/O PORTS
- ADDRESS/DATA MULTIPLEXED BUS DIRECTLY COMPATIBLE WITH STANDARD MICROCOMPUTERS SUCH A 6801, 6301, 8048, 8051



P
DIP40
(Plastic Package)

DESCRIPTION

A complete display control unit may be implemented with TS9347 and a single standard memory package. This new advanced CRT controller drastically reduces IC cost and PCB area for low-end color or monochrome terminal.

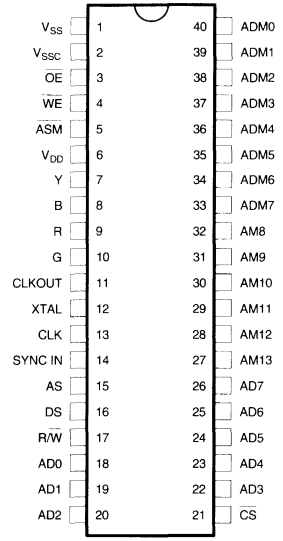
ORDERING INFORMATION

Part Number	Package	Pin Configuration
TS9347CP/1R00	DIP40	1R00
TS9347CP/2R00	DIP40	2R00

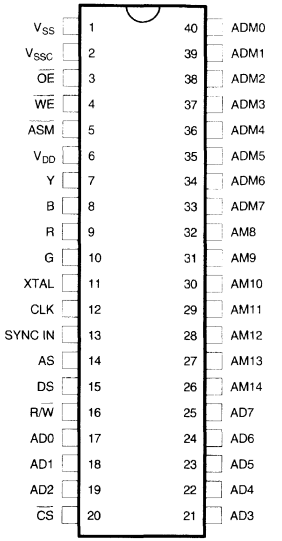
9347-01.TBL

PIN CONNECTIONS

DIP40
TS9347CP/1R00



DIP40
TS9347CP/2R00



9347-01.EPS - 9347-02.EPS

PIN DESCRIPTION (All the input/output pins, XTAL and Y excepted, are TTL compatible)

Name	Pin Type	Function	Description
MICROPROCESSOR INTERFACE			
AD (0:7)	I/O	Multiplexed Address/Data Bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	Address Strobe	The falling egde of this control signal latches the address on the AD (0:7) lines, the state of the Data Strobe (DS) and Chip Select (CS) into the chip.
DS	I	Data Strobe	- When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle (R/W = 1). In write cycle, data present on AD (0:7) lines are strobed by R/W low (see timing diagram 2). - When this input is strobed low by AS, R/W gives the direction of data transfer on AD (0:7) bus. DS high strobes the data to be written during a write cycle (R/W = 0) or enables the output buffers during a read cycle (R/W = 1) (see timing diagram 1).
R/W	I	Read/Write	This input determines whether the internal registers get written or read. A write is active low ("0").
CS	I	Chip Select	The TS9347 is selected when this input is strobed low by AS.
MEMORY INTERFACE			
ADM (0:7)	I/O	Multiplexed Address/Data Bus	Lower 8 bits of memory address appear on the bus when ASM is high. It the becomes the data bus when ASM is low.
AM (8:14)	O	Memory Address/Data Bus	Theses 7 pins provide the high order bits of the memory address.
OE	O	Output Enable	When low, this output selects the memory data output buffers.

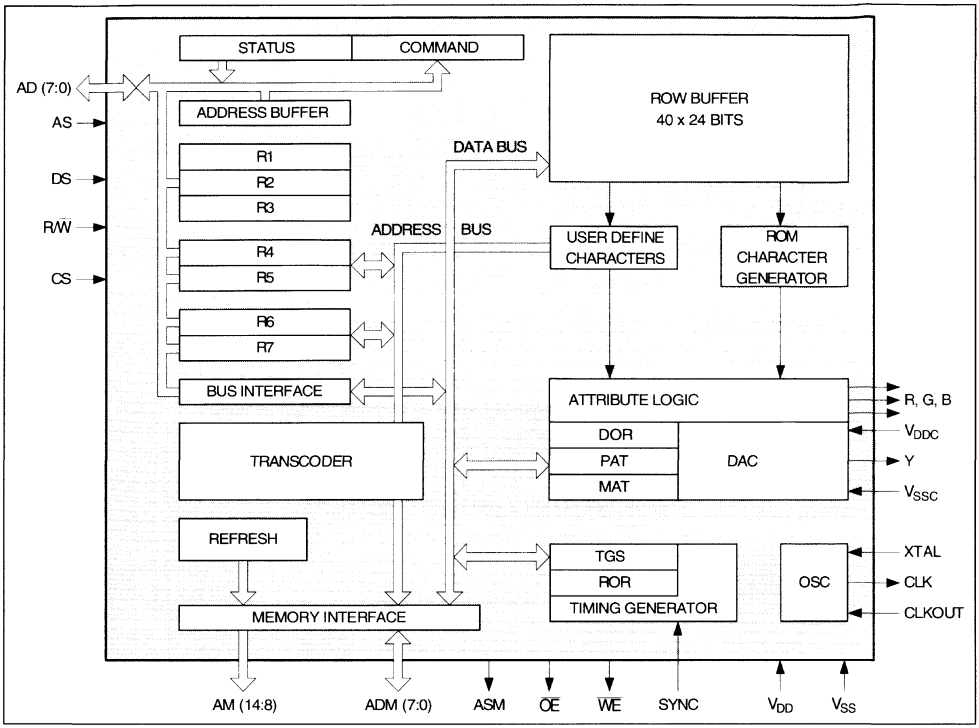
9347-02.TBL

PIN DESCRIPTION (continued)

Name	Pin Type	Function	Description
MEMORY INTERFACE (continued)			
WE	O	Write Enable	This output determines whether the memory gets read or written. A write is active low ("0").
ASM	O	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.
VIDEO INTERFACE			
R	O	Red/ Composite Sync	- When $TGS_5 = 0$, this output delivers the Red component of the video signal. It is low during the H and V blanking intervals. - When $TGS_5 = 1$, this output delivers the composite synchronization signal.
G	O	Gree/Insert/Port1	- When $TGS_4 = TGS_5 = 0$, this output delivers the Green component of the video signal. It is low during the V and H blanking intervals. - When $TGS_4 = 1$, this output delivers the insert attribute. It allows to insert the video signals in another external video for captionning purposes for example. It can also be used as a general purpose attribute or color. - When $TGS_5 = 1$ and TGS4 = 0, this pin is a general purpose output port. Its state is programmed by the value of PAT2.
B	O	Blue/Port2	- When $TGS_5 = 0$, this output delivers the Blue component of the video signal. It is low during the V and H blanking intervals. - When $TGS_5 = 1$, this pin is a general purpose output port programmed by the value of PAT7.
Y	O	Composite Luminance	This analog output delivers the composite luminance signal with 8 different grey levels plus the synchronization level.
Sync	I	Sync. Input/ Input Port	- When $TGS_3 = 1$, this input allows to vertically and, if TGS_2, is set, horizontally synchronize the TS9347 on an external signal. - When $TGS_2 = TGS_3 = 0$, the logic state of this input may be read by the microprocessor, and acts as a general purpose input port. - This input must be grounded if not used.
OTHERS PINS			
CLK XTAL	I/O	Crystal/Clock Input Crystal Output	These pins allow to connect a crystal to generate the input frequency from 12 to 15MHz. If an external signal is used, it must be applied on CLK input, XTAL is left unconnected.
CLK OUT	O	Clock Output	When internal oscillator is used, this pin provides a TTL compatible oscillator output for general operation.
V_{SS}	S	Power Supply	Ground
V_{DD}	S	Power Supply	+5V
V_{SSC} V_{DDC}	S	Power Supply Power Supply	These pins provide separate 0V and 5V power supply for the Y analog converter, allowing easier noise reduction.

9347-03.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	0.3, 7.0	V
V_{IN}*	Input Voltage	0.3, 7.0	V
T_A	Operating Temperature Range	0, +70	°C
T_{stg}	Storage Temperature Range	-55, +150	°C
P_{Dm}	Max. Power Dissipation	0.75	W

9347-04.TBL

* With respect to V_{SS}.

** Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operations (sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

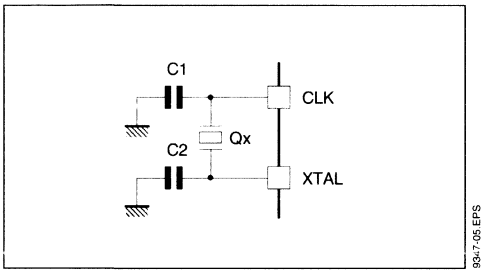
ELECTRICAL OPERATING CHARATERISTICS

V_{CC} = 5.0V ±5%, V_{SS} = 0, T_{amb} = 0 to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{IH}	Input High Voltage CLK (external CLK) Other Inputs	2.2 2	- -	V_{CC} V_{CC}	V -
I_{IN}	Input Leakage Current (execpt CLK)	-	-	10	µA
V_{OH}	Output HIgh Voltage (I_{load} = 500µA)	2.4	-	-	V
V_{OL}	Output Low Voltage I_{load} = 4mA : AD (0:7), ADM (0:7) I_{load} = 1 mA : Other Outputs Except Y	-	-	0.4	V
P_D	Power Dissipation	-	350	500	mW
C_{IN}	Input Capacitance	-	-	15	pF
I_{TSI}	Three State (off state) Input Current	-	-	10	µA
t_{start}	Crystal Oscillator Start Time	-	-	1	ms

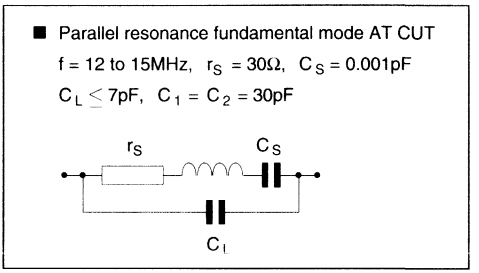
9347-05.TBL

Figure 1 : On Chip Oscillator



93-7-05.EPS

Figure 2 : Typical Crystal Parameters



93-7-06.EPS

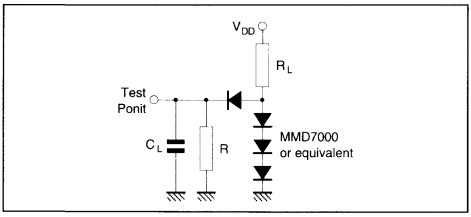
MEMORY INTERFACE

MEMORY INTERFACE CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_{amb} = 0 to +70°C)
Clock : Duty Cycle 40 to 60% ; t_r, t_f < 5ns, V_{IH} = 2.2V
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V, V_{OL} = 0.4V and V_{OH} = 2.4V

Ident. Number	Symbol	Parameter	F_{IN} = 12MHz		F = 1/T		Unit
			Min.	Max.	Mln.	Max.	
1	t_{ELEL}	Memory Cycle Time	500		6T		ns
2	t_D	Output Delay Time from CLK Rising Edge (ASM, OE, WE)	-	60	-	60	ns
3	t_{EHEL}	ASM High Pulse Width	120	-	2T -33	-	ns
4	t_{ELDV}	Memory Access Time from ASM Low	-	250	-	4T -43	ns
5	t_{DA}	Output Delay Time from CLK Rising Edge ADM (0:7), AM (8:14)	-	80	-	80	ns
6	t_{AVEL}	Address SEtup Time to ASM	30	-	T -49	-	ns
7	t_{ELAX}	Address HOld Time from ASM	55	-	T -21	-	ns
8	t_{CLAZ}	Address off Time	-	80	-	80	ns
9	t_{GHDX}	Memory Hold Time	10	-	10	-	ns
10	t_{OZ}	Data off Time from OE	-	60	-	T -19	ns
11	t_{GLDV}	Memory OE Access Time	-	150	-	2T -16	ns
12	t_{QVWL}	Data Setup Time (write cycle)	30	-	T -49	-	ns
13	t_{WHQX}	Data Hold Time (write cycle)	30	-	T -49	-	ns
14	t_{WLWH}	WE Pulse Width	110	-	2T -48	-	ns

9347-06.TBL

Figure 3 : Test Load



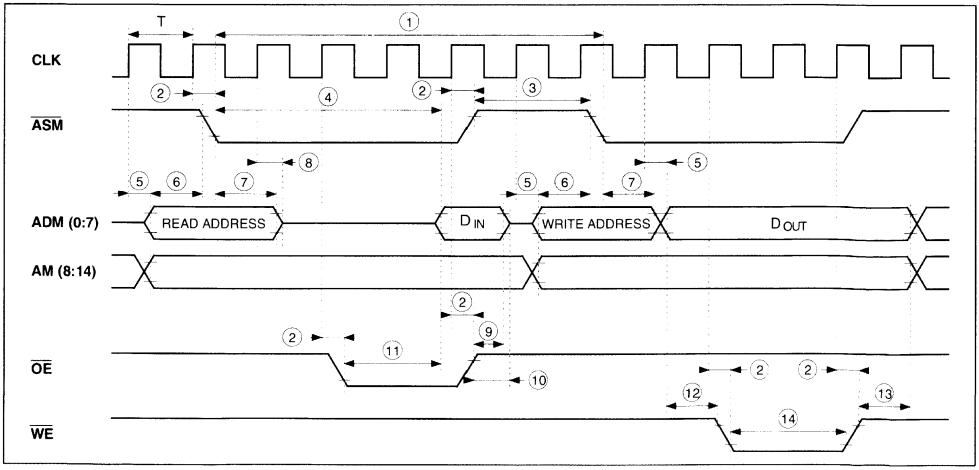
9347-07.EPS

Table 1

Symbol	ADM (0, 7) AD (0, 7)	Other Outputs Except Y
C	100pF	50pF
R_L	1kΩ	3.3kΩ
R	4.7kΩ	4.7kΩ

9347-07.TBL

Figure 4 : Memory Interface Timing Diagram



9347-08.EPS

SGS-THOMSON MICROELECTRONICS

MICROPROCESSOR INTERFACE

TS9347 is MOTEL compatible. It automatically selects the processor type by using AS input to latch to state of the DS input.

No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

TS9347	6801	INTEL Family
	Timing 1	Timing 2
AS	AS	ALE
DS	DS, E, Ø2	$\overline{RD}$
R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$

9347-08.TBL

MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS (AD (0:7), AS, DS, R/$\overline{W}$, $\overline{CS}$)

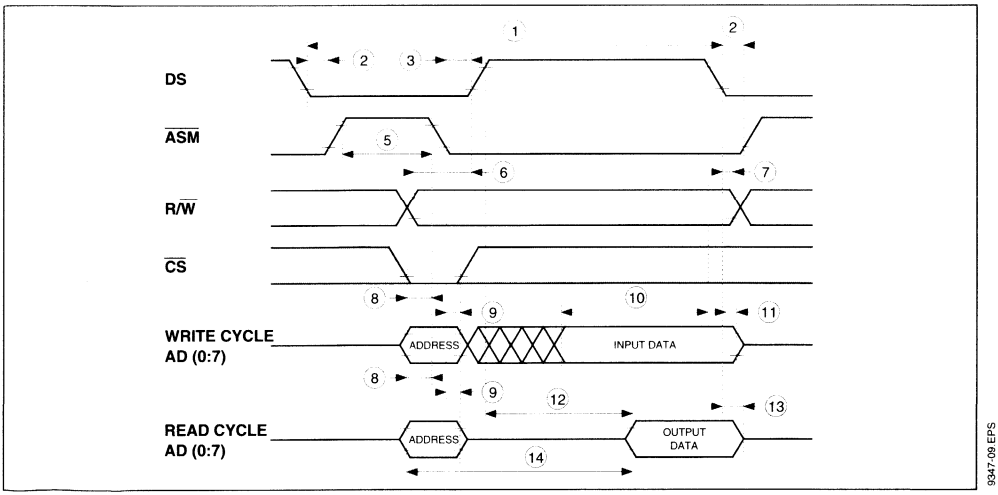
V_{CC} = 5.0 ±5%, T_A = 0 to 70°C, C_L = 100pF on AD (0:7)

Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V on All Inputs ; V_{OL} = 0.4V and V_{OH} = 2.4V on All Outputs.

Ident. Number	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	t_{CYC}	Cycle Time	400	-	-	ns
2	t_{ASD}	DS Low to AS High (timing 1) DS High or R/W High to AS High (timing 2)	26	-	-	ns
3	t_{ASED}	AS Low to DS High (timing 1) AS High or DS Low or R/W Low (timing 2)	30	-	-	ns
4	t_{PWEH}	Write Pulse Width	200	-	-	ns
5	t_{PWASH}	AS Pulse Width	76	-	-	ns
6	t_{RWS}	R/$\overline{W}$ to DS Setup Time (timing 1)	100	-	-	ns
7	t_{RWH}	R/$\overline{W}$ to DS Hold Time (timing 1)	10	-	-	ns
8	t_{ASL}	Address and $\overline{CS}$ Setup Time	20	-	-	ns
9	t_{ASH}	Address and $\overline{CS}$ Hold Time	20	-	-	ns
10	t_{DSW}	Data Setup Time (write cycle)	100	-	-	ns
11	t_{DHW}	Data Hold Time (write cycle)	10	-	-	ns
12	t_{DDR}	Data Access Time from DS (read cycle)	-	-	150	ns
13	t_{DHR}	DS Inactive to High Impedance State Time (read cycle)	10	-	63	ns
14	t_{ACC}	Address to Data Valid Access Time	-	-	300	ns

9347-09.TBL

Figure 5 : Microprocessor Interface Timing Diagram 1 (6801)



9347-09.EPS

Figure 6 : Microprocessor Interface Timing Diagram 2 (INTEL type) - READ CYCLE

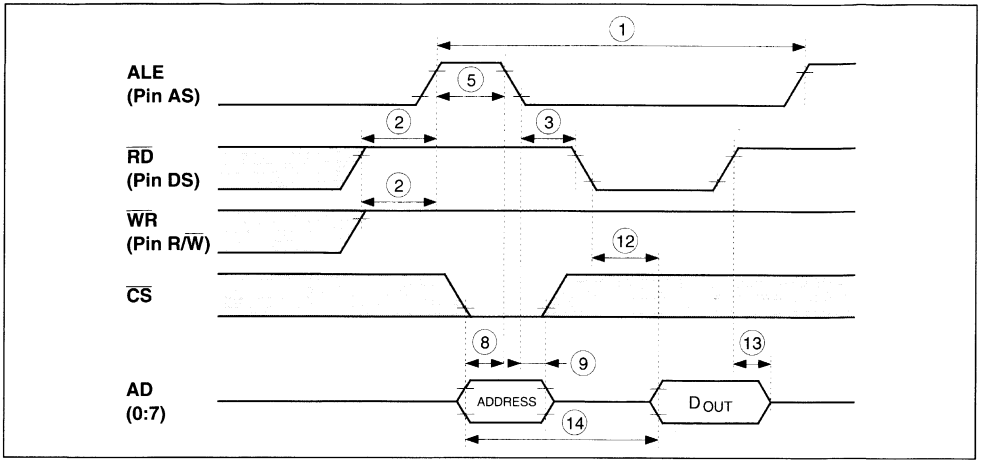
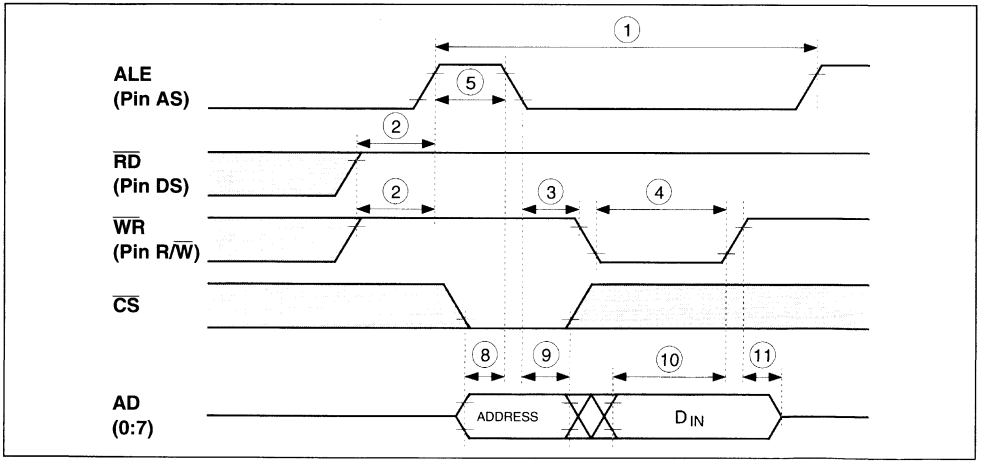


Figure 7 : Microprocessor Interface Timing Diagram 2 (INTEL type) - WRITE CYCLE



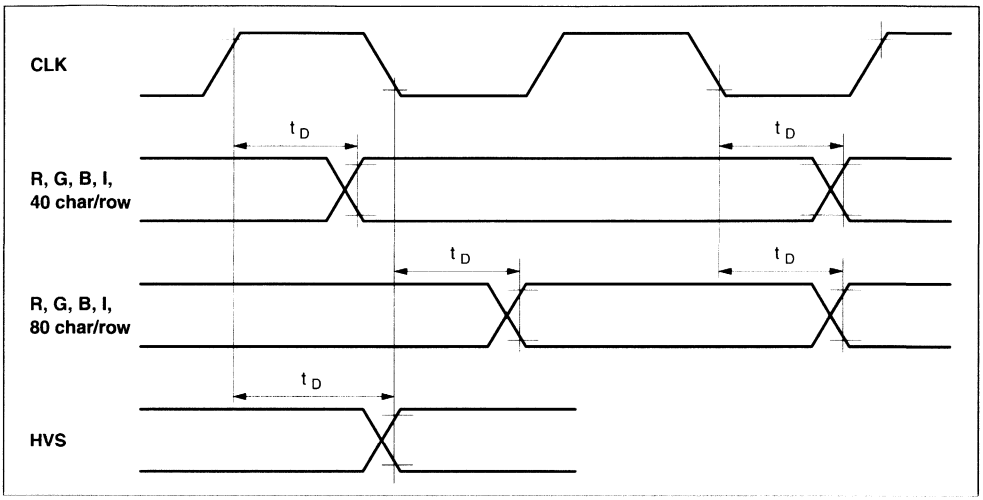
VIDEO INTERFACE R. G. B. I.

V_{CC} = 5.0V ±5%, T_{amb} = 0 to +70°C, CLK Duty Cycle 50%, C_L = 50pF
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2.2V on CLK Inputs
V_{OL} = 0.4V and V_{OH} = 2.4V on All Outputs.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_D	Output Delay from CLK Edge	-	-	60	ns

9347-10.TBL

Figure 8



9347-12.EPS

INPUT CLK

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PWCH}	CLK High Pulse Width	25	-	-	ns
t_{PWCL}	CLK Low Pulse Width	25	-	-	ns
t_{rc}, t_{fc}	CLK Rise and Fall Time	-	-	10	ns
t_{WCOH}	CLKOUT High Pulse Width	20	-	-	ns
t_{WCOL}	CLKOUT Low Pulse Width	20	-	-	ns
t_{rco}, t_{fco}	CLKOUT Rise and Fall Time	-	-	20	ns

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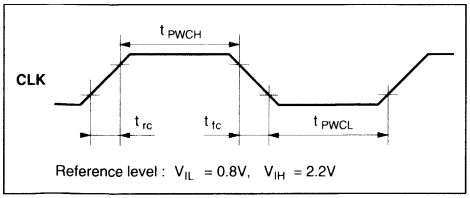
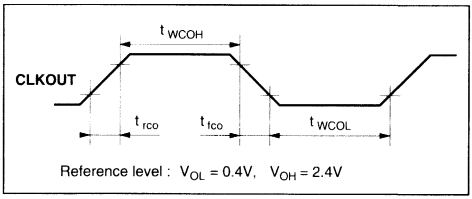
Figure 9 : Case of External CLK Generation



9347-13.EPS

Figure 10 : Case of Internal Oscillator (f_{IN} = 12MHz)



9347-14.EPS

Y OUTPUT : Composite Luminance.

REFERENCE LEVEL

$V_{DDC} = V_{DD} = 5V$, $V_{SSC} = V_{SS} = 0V$

G	R	B	Signal	Level (V)
0	0	0	SYNC	0.06
0	0	0	BLACK	0.50
0	0	1	BLUE	0.80
0	1	0	RED	0.92
0	1	1	MAGENTA	1.03
1	0	0	GREEN	1.15
1	0	1	CYAN	1.26
1	1	0	YELLOW	1.38
1	1	1	WHITE	1.50

9347-12.TBL

ELECTRICAL SPECIFICATION

Over Full Temperature Range : $V_{DDC} = V_{DD} = 5V$ (see note 1)
$V_{SSC} = V_{SS} = 0V$, $C_L = 20pF$, $R_L > 100k\Omega$ to V_{SS} or V_{DD}

Parameter	Min.	Typ.	Max.	Unit
Monotonicity		Guaranteed		
Output Level Dispersion	-	10	50	mV
Propagation Delay (clock edge to 50% output)	-	-	60	ns
Rise and Fall Time (10 - 90%)	-	-	30	ns
Output Static Impedance	-	-	600	Ω

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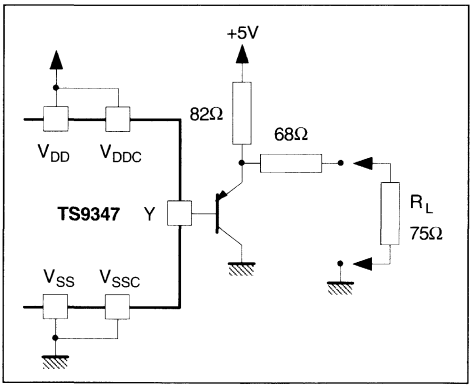
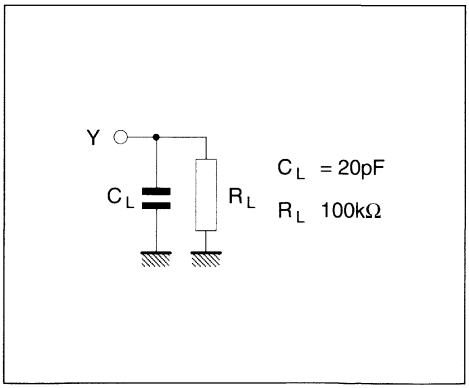
Note : 1. The DAC is a 9 output potentiometric divider : therefore, each voltage variation on V_{DDC} is repercuted on the output with the same relative value with respect to V_{SSC}.

Figure 11 : Typical Application



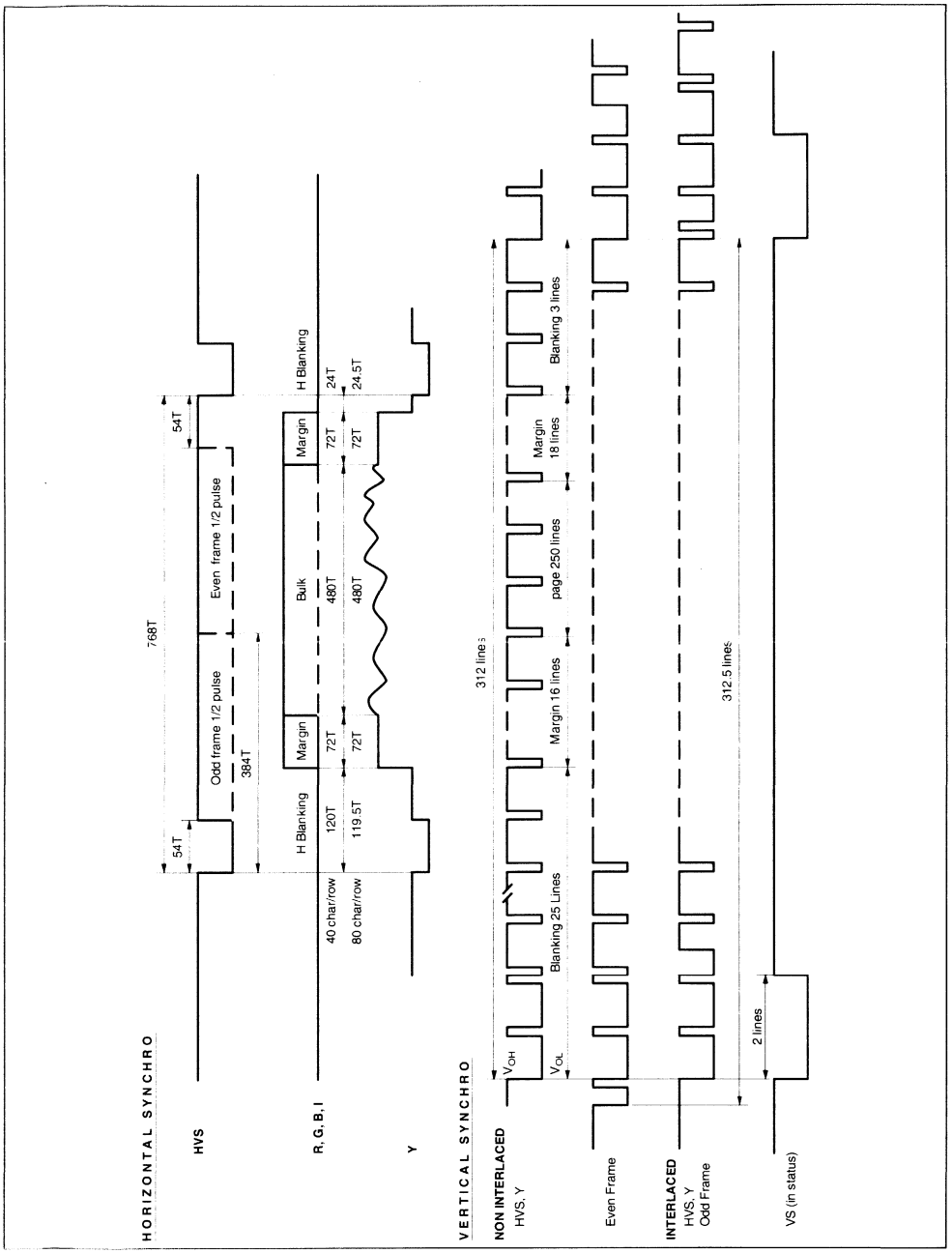
9347-15.EPS

Figure 12 : Test Condition



9347-16.EPS

Figure 13 : Vertical and Horizontal Synchronization Outputs ($T \frac{1}{f_{CLK}}$)



FUNCTIONAL DESCRIPTION

The TS9347 is a low cost, semigraphic, CRT controller.

The TS9347 displays up to 25 rows of 40 characters or 25 rows of 80 characters, including either an upper or lower service row.

The on-chip character generator provides a standard, 5 x 7, character set and standard semigraphic sets.

More user definable (8x10) alphanumeric or semigraphic sets may be mapped in the 32 K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

Microprocessor Interface

The TS9347 provides an 8-bit, address/data multiplexed, microprocessor interface.

It is directly compatible with popular (6801, 8048, 8051, 8085....) microprocessors.

Registers

The microprocessor directly accesses 8 registers :
- R0 : Command/status register
- R1 : R2, R3 : Data registers
- R4, R5, R6, R7 : Each of these register pairs points into the private memory.

Through these registers, the microprocessor indirectly accesses the private memory and 5 more registers :
- ROR, DOR : Base address of displayed page memory and of user external character generators.
- PAT, MAT, TGS : Used to select the I/O configuration, the page attributes and format, and to program the timing generator options.

Private Memory

The user may partition the 32 K x 8 private memory addressing space between :
- pages of character codes (2 K x 8 or 3 K x 8),
- external character generators,
- general purpose user area.

Many types of memory components are suitable :
- ROM, DRAM or SRAM,
- 2 K x 8, 8 K x 8, 16 K x 4, 32 K x 8 organization,
- Modest 400ns cycle time and 240ns access time is required.

40 Characters per Row : Character Code Formats and Attributes

Once the 40 characters per row format has been selected, one character code format out of two must be chosen :
- 24-bit format
  All the attributes are provided in parallel.
- 16-bit format :
  Some parallel attributes, others are latched.

The 16-bit fixed format is compatible with EF9345 CRT controller.
Character attributes provided :
- Back ground and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- 11 x 100 user definable character generator in memory.

80 Characters per Row Format : Character Code Format and Attributes

Two character code formats are provided :
- Long (12 bits) with 4 parallel attributes :
  Blinking, Underlining, Reverse, Color select
- Short (8 bits) : no attributes.

Timing Generator

The whole timing is derived from a 12 to 15MHz on chip oscillator.

The RGB outputs are shifted at 8 to 10MHz for the 40 character/row format and at 12 to 15MHz for the 80 character/row.

The timing generator allows different display modes :
- Interlaced or not
- Master or slave synchronization.

Video Output

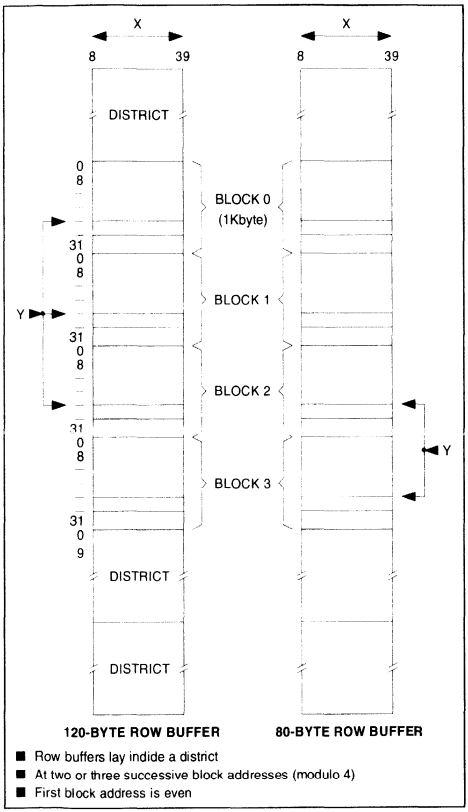
The video output is always available as a composite luminance signal on the analog output Y ; the logic R, V, B, Syncout and Insert components may be selected on the RGB output pins.

MEMORY ORGANIZATION

Logical and Physical Addressing

The physical 32 Kbyte addressing space is logically partitioned by the TS9347 into 40-byte buffers (Figure 15). More precisely, a logical address is given by an X, Y, Z triplet where :
- X = (0 to 39) points to a byte inside a buffer,
- Y = (0,8 to 31) points to a buffer a 1 Kbyte block,
- Z = (0 to 31) points to a block.

Figure 14 : Memory Row Buffer



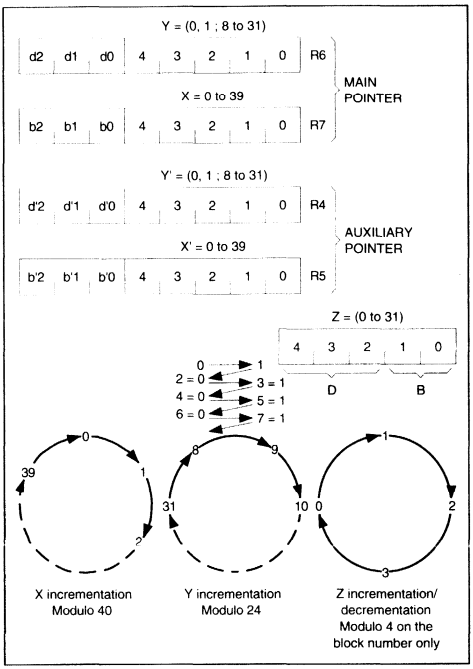
Pointers

Each X, Y, and Z component of a logical address is binary encoded and packed in two 8-bit registers. Such a register pair is a pointer (Figure 15). TS9347 contains two pointers :
- R6, R7 : main pointer
- R4, R5 : auxiliary pointer.

Both pointers have the same format. R7 (resp. R5) holds the X component and the two LSB's of the Z component. R6 (resp R4) holds the Y component and the three MSB's of the Z component. This package induce a partitionning of Z in 8 districts of 4 blocks each.

Logical to physical translation is performed on chip following Figure 16 scheme.

Figure 15 : Pointer Auto Incrementation



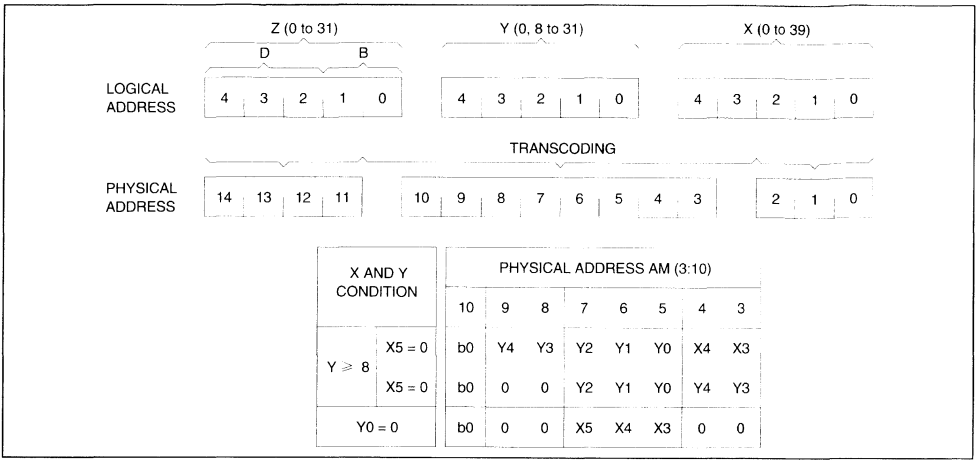
Data Structures in Memory

A page is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row buffer (Figure 14). The buffers belonging to a row buffer must meet the following requirements :
- they have the same Y address,
- they have the same district number,
- they lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.

A Page is a set of successive row buffers :
- with the same format,
- with the same district number,
- with the same block address of first buffer. This block address must be even.
- lying at successive (modulo 24) Y addresses.

Figure 16 : Logical to Physical Address Transcoding Performed on-chip



Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer or row buffer structure. See Figure 15 for pointer incrementation implied by these data structures.

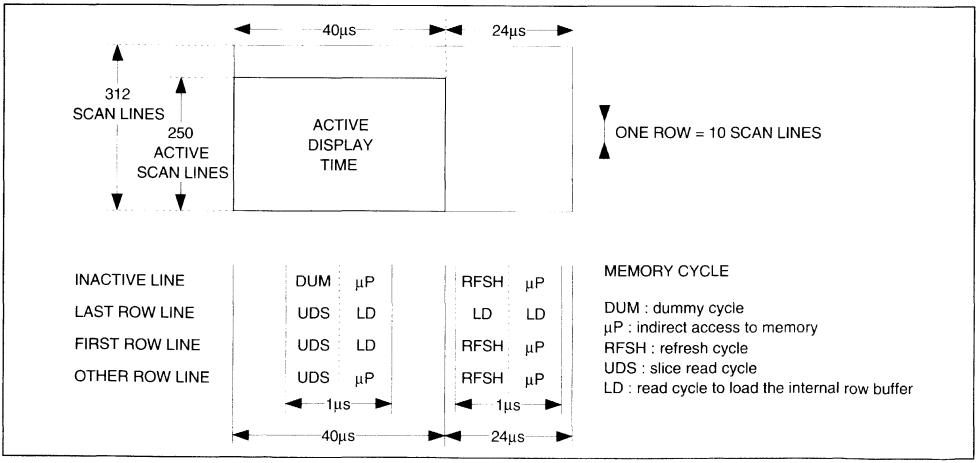
Memory Time Sharing (see Figure 17)

The memory interface provides a 500ns cycle time at f_{IN} = 12MHz. That it to say a 2 Mbyte/s memory bandwidth is shared between :

- reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- reading user defined characters slices from memory (1 byte each µs),
- indirect microprocessor read or write operation,
- refresh cycles to allow DRAM use, with no overhead.

A fixed allocation sheme implements the sharing. During these lines, no microprocessor access is provided for 104µs ; this holds too when no user defined character slices are addressed.

Figure 17 : Memory Cycle Allocation (12MHz operation).



Notes :
1. Dumming cycles are read cycles at dummy addresses.
2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM (0:7) cycle through its 256 states in less than 1ms.
3. The microprocessor may indirectly access the memory once every µs, except during the first and the last line of a row, when the internal buffer must be reloaded.

SCREEN FORMAT AND ATTRIBUTES OUTPUTS CONFIGURATION

The screen format and attributes are programmed through 5 indirectly accessible registers : ROR, TGS, PAT, MAT, and DOR. IND command allows accessing to these registers. TGS is also used to select the timing generator options (see Figures 18a and 18b).

Row And Character Code Format : TGS (6:7)

Two row formats and 4 character code formats are available but cannot be mixed in a given screen.

Timing Generator And Configuration Options : TGS (1:5)

TGS1 = 0 : noninterlaced mode, 312 lines/frame.
TGS1 = 1 : interlaced mode, 312.5 lines/frame.
TGS (2,3) : input synchronization configuration.

The SYNC input may be interpreted as a synchronization signal or as a general purpose input port, which state can be read by the microprocessor in the status register (bit 2). Alternatively, the vertical synchronization output from the timing generator can be read in the same register.
The composite incoming SYNC IN signal is separated into two internal signals :
- Vertical Synchronization In (VSI)
- Horizontal Synchronization In (HSI)

TGS3 = 1 enables VSI to reset the internal line count : SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 0 to 1, the line count is reset at the end of the current line.

TGS3 = TGS2 = 1 enables HSI to control an internal digital PLL : HSI and on-chip generated H. SYNC OUT are considered as in phase if their leading edges match at plus or minus 1 clock period. When they are out of phase, the line period is lenghtened by 1 clock period (80 ns at 12 MHz).
Screen Format Table resumes the different combinations.

TGS (4,5) : output configuration
Three output pins may be configured to output either video signals or general purpose output ports. The Screen Format Table summarizes the possible configurations, with the following definitions :

R, V, B : Red, Green and Blue Video components
I : Insert signal
HVS : Composite H and V synchro output
P1, P2 : General purpose output ports

PAT2 gives the value of P1, PAT7 gives the value of P2 : a logical "1" will cause a "high" on the corresponding output, while a "0" results in a "low".

Figure 18a : Screen Format Table

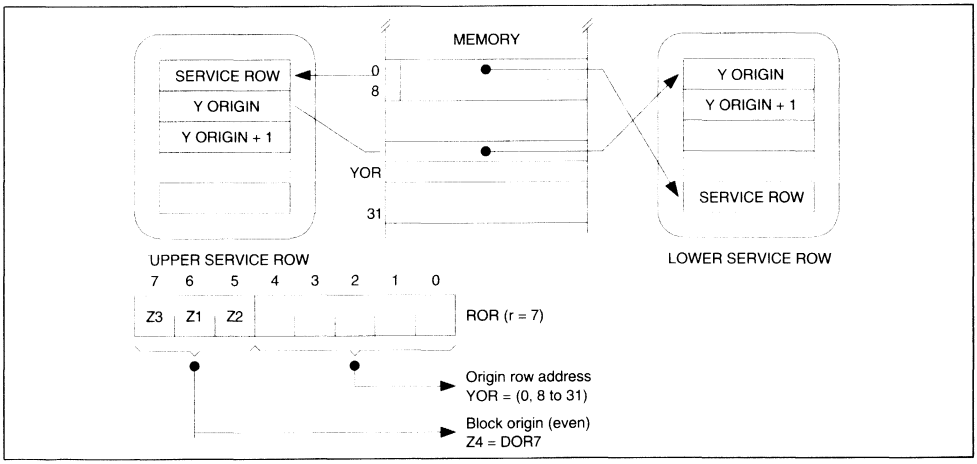
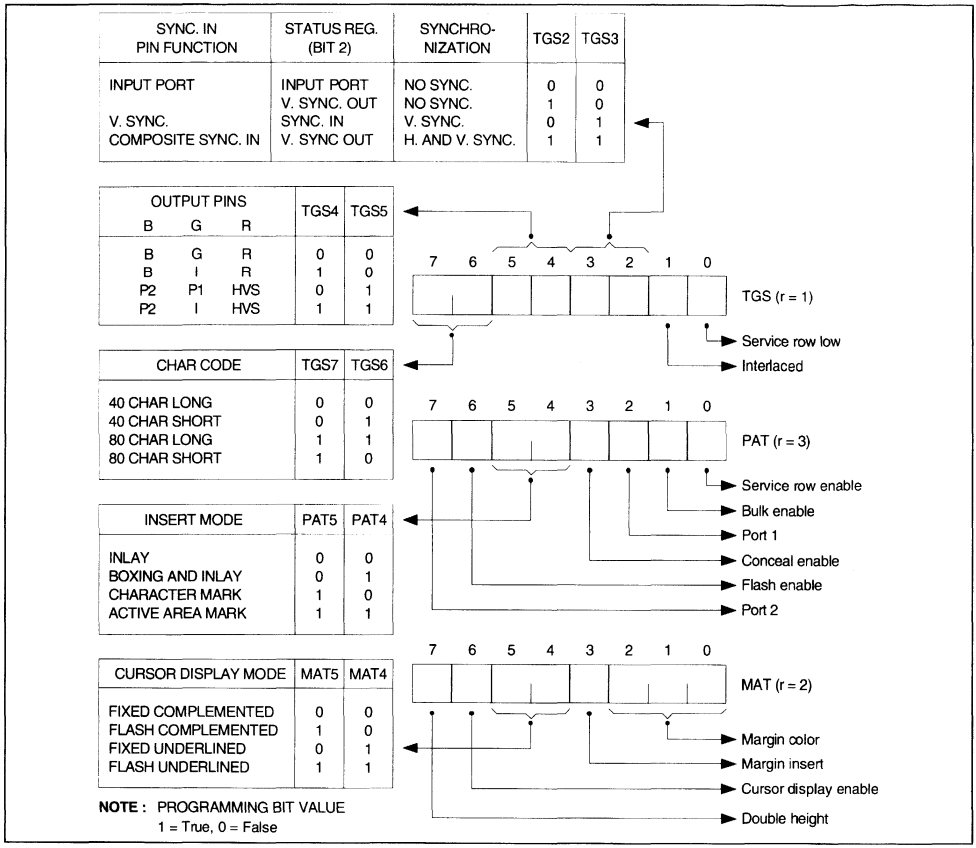


Figure 18b : Screen Format Table



Screen Partition, Page Pointer ROR (see top of the Screen Format Table)

The screen is partitioned in three areas :
- The margin
- The service row
- The bulk or remaining rows

MAT (0:3) declares the color of the margin and the value IM of its insert attribute.

DOR7 and ROR register point to the page to be displayed : DOR7 gives the MSB of the Z address, ROR (7:5) three next bits, the LSB is implicitly Z0 = 0 (the page block address must be even). YOR (= ROR (4:0)) gives the first row to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

Service Row : TGS0 ; PAT0

The 10 scan line service row can be displayed at the top or the bottom of the screen, depending on the value of TGS0. The service row is fetched from the origin block at Y = 0 ; it does not roll ; it may be disabled by PAT0 = 0 ; it is then displayed as a margin extension.

Bulk : PAT1 ; MAT7

The bulk is displayed for 240 scan lines. Each row buffer is usually displayed for 10 scan lines. However, MAT7 = 1 doubles this figure : then every character appears in double height (double height characters are quadrupled).
PAT1 = 0 disables the bulk. When disabled, the corresponding scan lines are displayed as a margin extension.

Cursor : MAT (4:6)

To be displayed with the cursor attribute, a character must be pointed by the main pointer (R6, R7) and MAT6 must be set. The cursor attributes are given by MAT (4,5) :
- Complementation :
  The R, G, B or each pixel is logically negated : R, G, B → $\overline{R}$, $\overline{G}$, $\overline{B}$
- Underline :
  The underline attribute is negated
- Flash :
  The character is periodically displayed with, then without the cursor attribute (50%/50% ≈ 1 Hz).

Flash Enable (PAT 6) **- Conceal Enable** (PAT3)

Any character flashing attribute is a "don't care" when PAT6= 0. When PAT6 = 1, a character flashes if its flashing attributes is set. It is then periodically displayed as a space (50%/50% ≈ 0.5Hz).
PAT3 is a 'don't care" for 80 char./row formats.
When any 40 char./row format is in use :
- if PAT3 = 0, the conceal attribute of any character is a "don't care"
- if PAT3 = 1, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

Insert Modes : PAT (4:5)

These modes make sense only if the insert signal I is available on the G pin, that is to say when TGS4 = 1.
During retrace, margin and extended margin periods, the I signal outputs the value of the insert margin attribute : I = IM = MAT3.
During active line period, the I output is controlled by the insert mode, and I1 and I2, the insert attributes of each characters. The I output may have several uses : (See Figure ???).
- As a margin/active area signal in the Active Area Mark mode
- As a character per character marker signal in the Character Mark mode
- As a video mixing signal in the other modes, provided that the TS9347 has been vertically and horizontally synchronized with an external video source : the I output allows mixing TS9347 video output (I = 1) and external video signal (I = 0). This mixing may occur for the complete character window (Boxing mode) or only for the foreground pixels (Inlay mode).

Video Output during Active Periods

Insert Mode	I1	I2	Char. Levels Pixels	I	Video Output	Comments
Active Area Mark	-	-	-	1	Unchanged	
Character Mark	0	-	-	0	Unchanged	
	1	-	-	1	Unchanged	
Inlay	0	-	-	0	Black	Non insert
	1	-	Background	0	Black	
	1	-	Foreground	1	Unchanged	Inlaid
Boxing and Inlay	0	-	-	0	Black	Non inserted
	1	0	-	1	Unchanged	Boxed
	1	1	Background	0	Black	
	1	1	Foreground	1	Unchanged	Inlaid

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40 Char/row Character Codes

To display pages in 40 character per row format, one out of two character code formats must be selected :

- Long (24 bits) code : all parallel attributes.
- Short (16 bits) code : mix of parallel and latched attributes.

Short codes are translated into long codes by the TS9347 during the internal row buffer loading process. The choise of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

Long Codes

This is the basic 40 char/row code. Each 8 pixel x 10 lines character window on the screen is associated with a 3-byte code in memory, namely the C, B, and A bytes (Figure 19). A row on the screen is associated with a 120 byte row buffer in memory.

3-BYTE CODE STRUCTURE

1. C7 is a don't care. up to 128 characters may be addressed in each set. each user definable set holds only 100 characters : C-byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B (3:7) give the type and the set number of the character.
3. When I2, U, L are not programmable, the default value of these attributes is 0.
4. Character code byte a defines a two color set giving directly (Table 3) the two values (B1, G1, R1) and (B0, G0, R0) respectively affected to the 1's and the 0's of the character pattern. the negative attribute, when set, exchanges the two values.

Figure 19 : 40 Character Long Codes

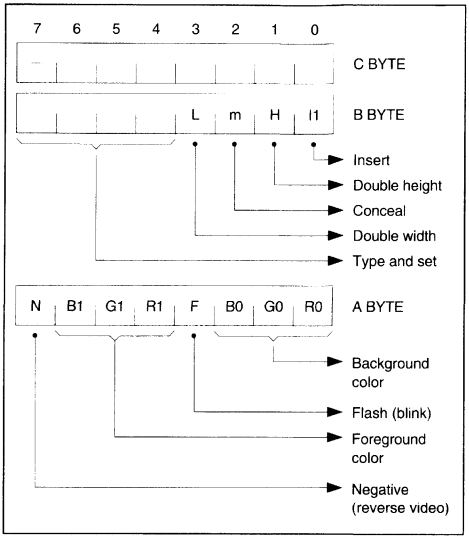

Table 2

Type and Set B (3:7)					Number of Character Per Set	Set Name	Set Type	Cell Location
B7	B6	B5	B4	B3	C (0:6)			
0	I2	1	0	L	128 STANDARD MOSAIC	G10	SEMI GRAPH	ON CHIP ROM
	I2	1	1	L	32 COMPLEMENT. CELLS	GOE		
	I2	0	U	L	128 ALPHANUMERICS	G0	ALPHA	
1	0	0	U	L	100 ALPHA UDS	G'0		EXTERNAL RAM
	0	1	0	L	100 SEMI-GRAPHICS UDS	G'10	SEMI GRAPH	
			1	L	100 SEMI-GRAPHICS UDS	G'11		
	1	X	X	X	800 SEMI-GRAPHICS UDS	Q0:7		

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L = Double width U = Underlined

Notes:
1. Double height, double width : a correct operation assumes that the same character code had been repeated in the page memory (Twice for double height or double width, four times for double size).
2. Double height : each slice of the character is repeated : twice to get a 8 x 20 pattern. However for the alphanumeric characters, scheme is slightly different : the upper slice (SN = 0) is tripled, the next (SN = 1 to 8) are doubled, and the last (SN = 9) is displayed only once.

Table 3 : Coloring a Character

B	G	R	Color Value
0	0	0	BLACK
0	0	1	RED
0	1	0	GREEN
0	1	1	YELLOW
1	0	0	BLUE
1	0	1	MAGENTA
1	1	0	CYAN
1	1	1	WHITE

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Table 4 : Shifting a Slice

7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0

Shift Direction : LSB First
1 = Foreground
0 = Background

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Short Codes

These 16-bit codes achieve memory saving whith some penalties :

- Q0 to Q7 and GOE cannot be reached.
- Some attributes are latched and can be changed only while displaying a space (delimitor code).

They are fully compatible with EF9345 (binary code and display interpretation) if the I2 attribute is given the value 0.

Figure 22 gives the short to long translation process which occurs for each row - while loading the internal row buffer - before display.

HANDLING SHORT AND LONG CODES

The TLM, TLA, TSM, and TSA, commands allow an easy X, Y random or an X sequential access to/from the microprocessor from/to a memory row buffer (see Figures 20 and 21).

User Defined Character Generator In Memory : DOR REGISTER

With 40 char./row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus, a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (Figure 23).

The cells of one given character set should be layed in one block.

Up to 100 character cells may be addressed in each set.

The location in memory, where to fetch the sets in use, are declared by DOR register (Figure 24).

For each type of set, it gives the MSB(s) of the Z block address. TS9347 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. SN is derived from the scan line rank in the row and the double height status.

Figure 20 : Long Codes in Memory Triple Row Buffer

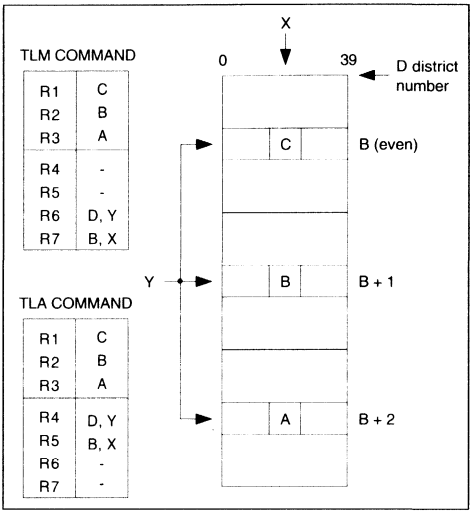

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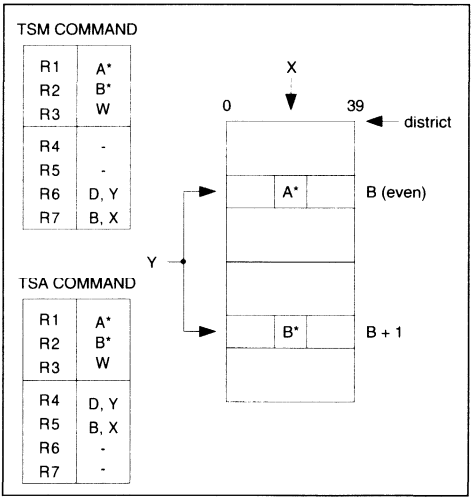
Figure 21 : Short Codes in Memory Double Row Buffer



9347-26.EPS

Figure 22 : Fixed Short Code to Fixed Long Code Translation

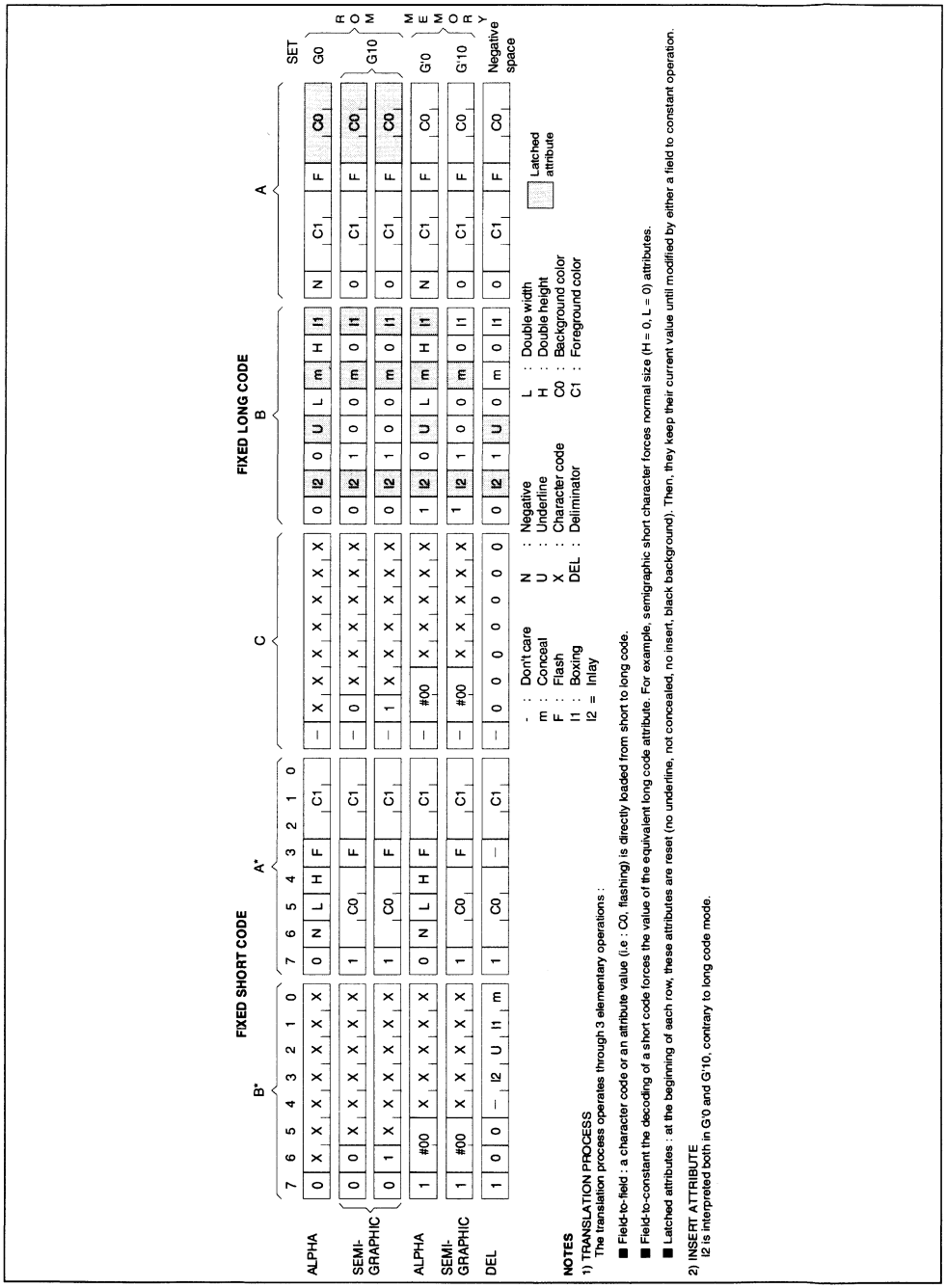


Figure 23 : Packing Uds Cells in Memory

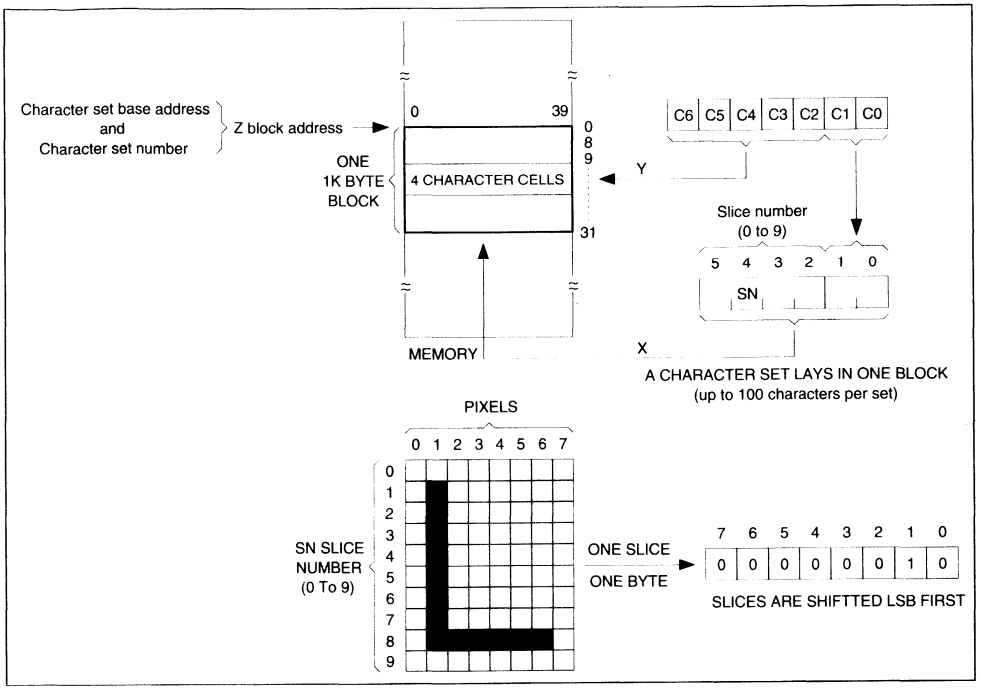
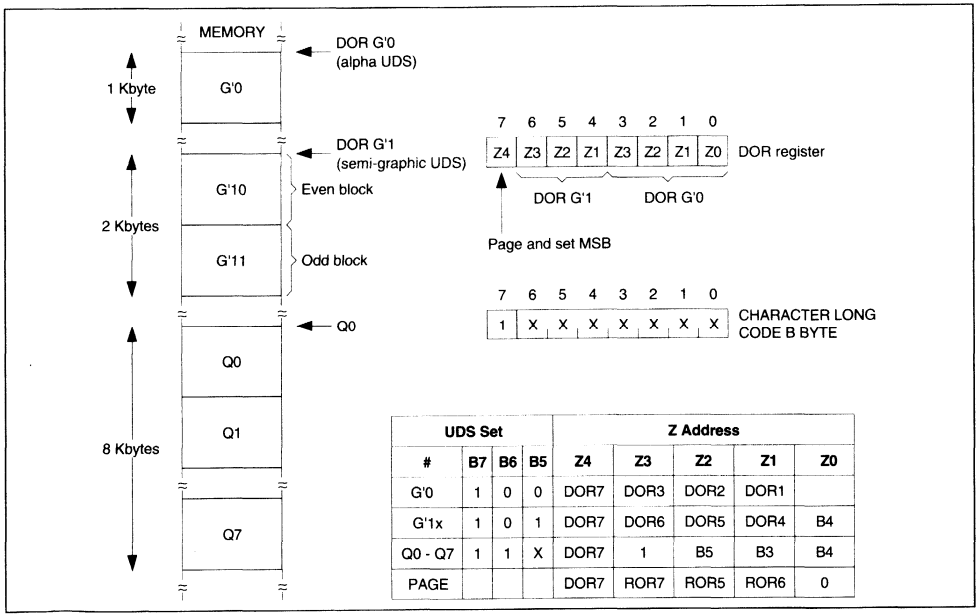


Figure 24 : UDS Fetch to Display



UDS Set				Z Address				
#	B7	B6	B5	Z4	Z3	Z2	Z1	Z0
G'0	1	0	0	DOR7	DOR3	DOR2	DOR1	
G'1x	1	0	1	DOR7	DOR6	DOR5	DOR4	B4
Q0 - Q7	1	1	X	DOR7	1	B5	B3	B4
PAGE				DOR7	ROR7	ROR5	ROR6	0

Loading User Defined Character Set

Before loading a character set into RAM, the user must

- Assign a name to the set :
  G'_0, G'_{10}, G'_{11}, or Q_{0-7}
- Assign a character number to each character belonging to this set. Character numbers range from 0 to 3 and 32 to 127.
  It is binary coded into 7 bits C (0.6) - C (0.6) will be loaded later into a C byte character code in order to display the character.
- A pointer to a character slice in memory is then manufactured from
  the character number C (0.6),
  the slice number SN (0.3),
  the bloc number assigned to the set Z (0.4)

Note : Different sets may be mixed in the same block, as long as the character have different code numbers.

Figure 25 : Accessing a Character Slice in Memory

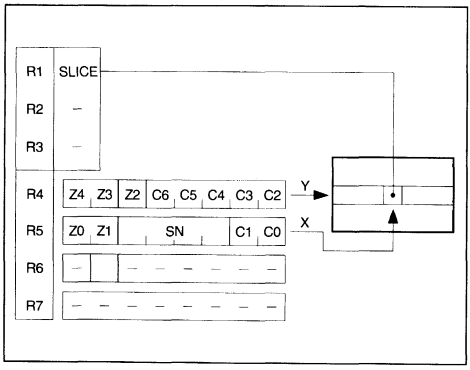


Figure 25 shows how to proceed with the auxiliary pointer and the TBM and TBA commands.

Note : The main pointer may be also used. When sequentially accessing slices of a given character, auto incrementation is helpless.

On-chip Character Generator

- G0 and GOE are common to 40 and 80 char./row modes (Figure 26 and Figure 36).
- G10 is the standard mosaïc set for videotex (Figure 27).
- GOE cannot be reached from the 16 bit short codes (Figure 28).

Displaying the Attributes

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :
   - Underline or underline cursor : foreground forced on the last slice (SN = 9).
   - Flash : background periodically forced on the whole window (≈ 0.5 Hz). The phase depends on the negative attribute.
   - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
   - Negative : exchange the background and foreground color values when set.
   - Coloring.
3. Basic pixel shift frequency : f_{CLK} x 2/3 = 8 to 10MHz

Figure 26 : G_O Alphanumeric Character Set in 40 Character/Row Mode–TS9347.

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

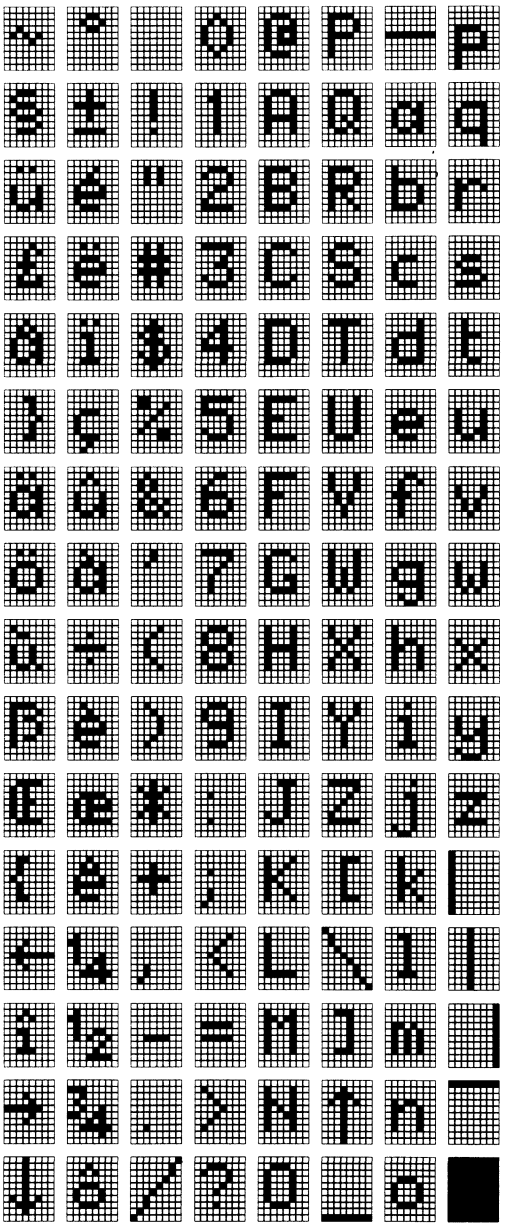


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Figure 27 : G_{10} Semigraphic Character Set.

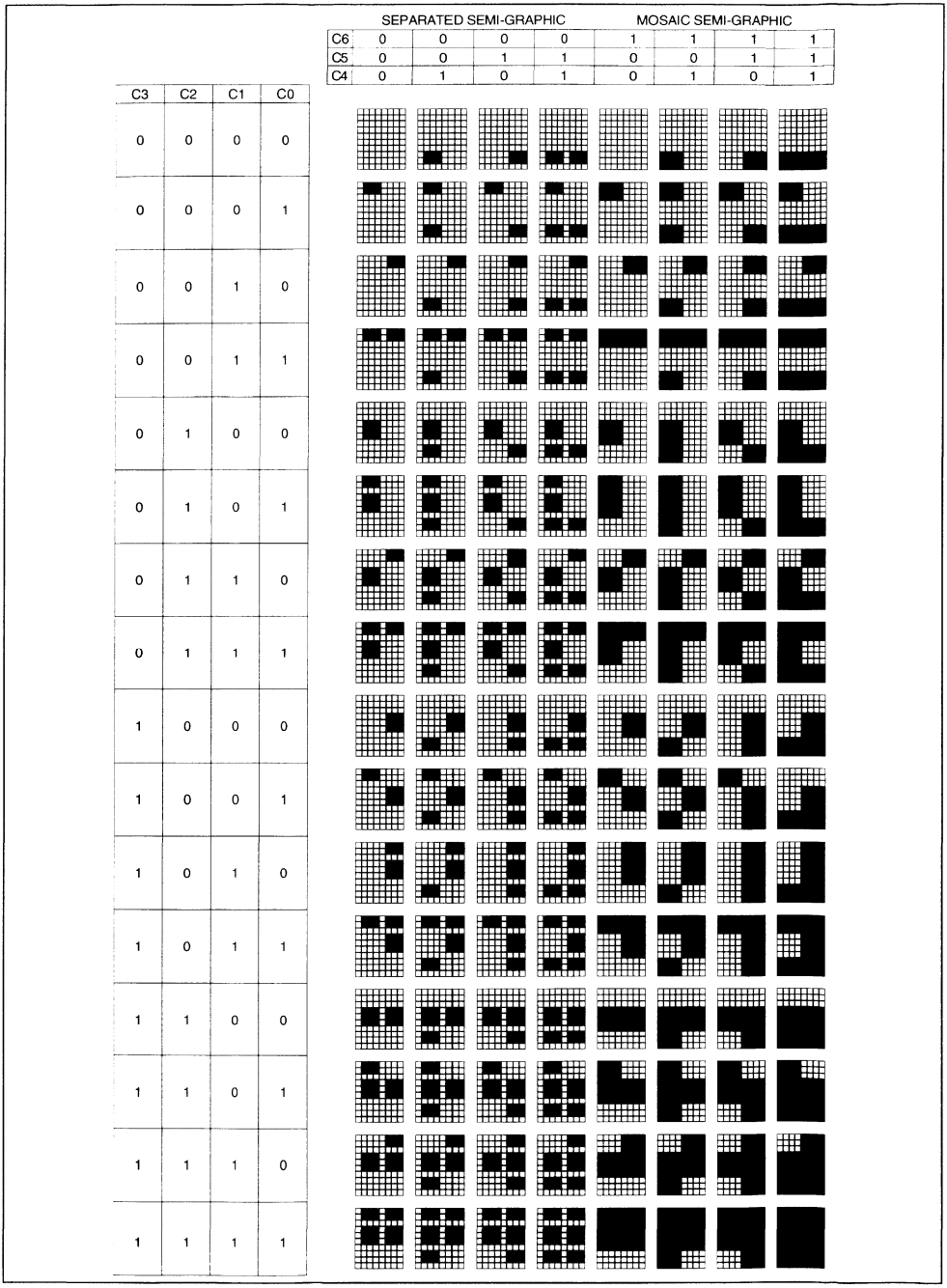
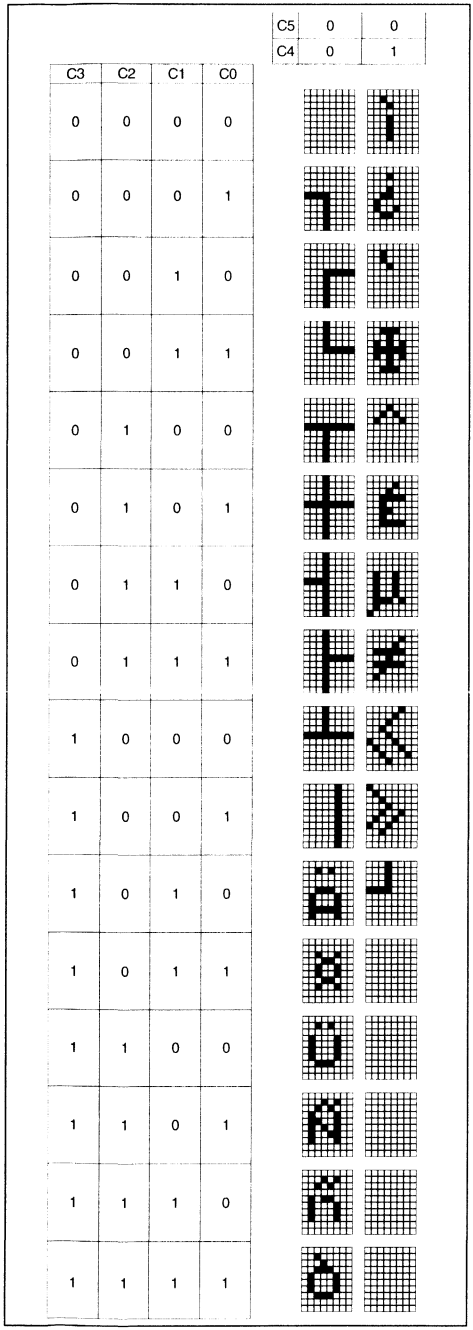


Figure 28 : GOE Extension Character Set



80 CHAR / ROW CHARACTER CODES

To display pages in 80 character per row format, one of two character code formats must be selected :

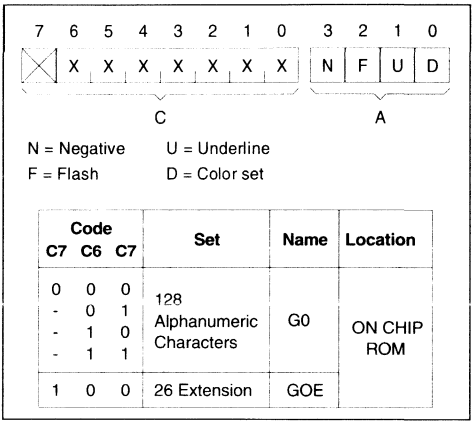
- Long (12 bits) code : 4 parallel attributes
- Short (8 bits) code : no attribute.

Both formats address the on-chip G_0 and GOE sets (154 characters 6 x 10) sets. None allows UDS addressing.

Long Codes

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (Figure 29).

Figure 29 : 80 Char/Row Character Code



Code C7	C6	C7	Set	Name	Location
0	0	0	128 Alphanumeric Characters	G0	ON CHIP ROM
-	0	1			
-	1	0			
-	1	1			
1	0	0	26 Extension	GOE	

Short Codes

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble positive, not underlined, not flashing.

Packing The Codes In Memory

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (Figure 30). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

Access To The Codes In Memory

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A

nibble is repeated in the R3 register (Figure 31). Dedicated auto-incrementation is also performed when required.
KRS command does a similar job the short codes (Figure 32).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (Figure 33). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

Figure 30 : 80 Char / Row Code Packing

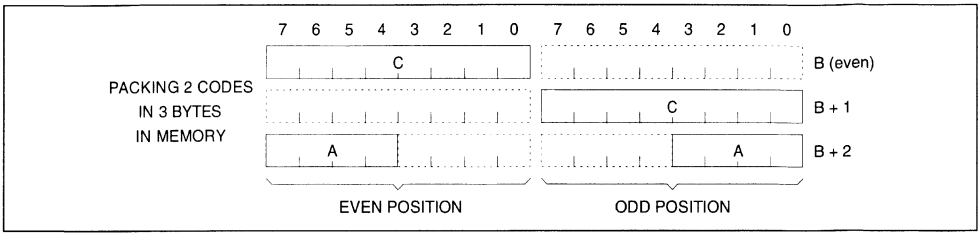


Figure 31 : KRL Command : Sequential Access to Long Codes

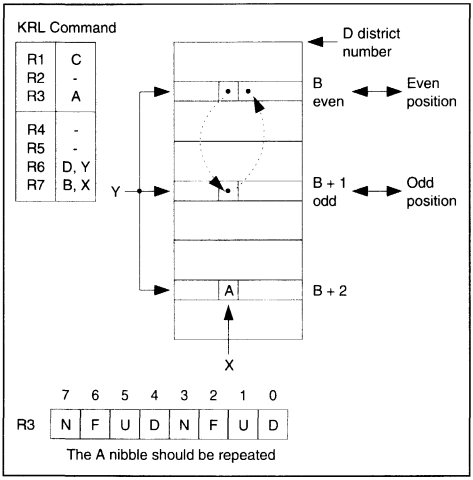


Figure 32 : KRS Command Sequential Access to Short Codes

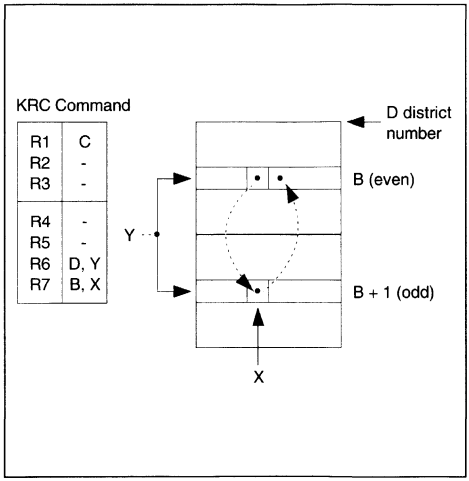
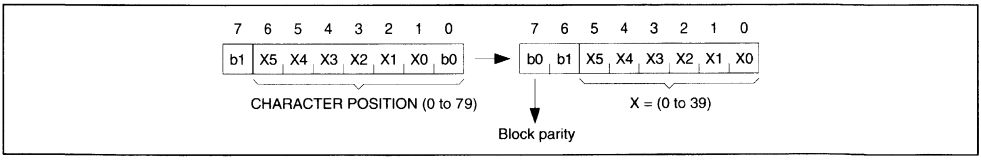


Figure 33 : Transcoding an Horizontal Screen Location into a R7 Pointer



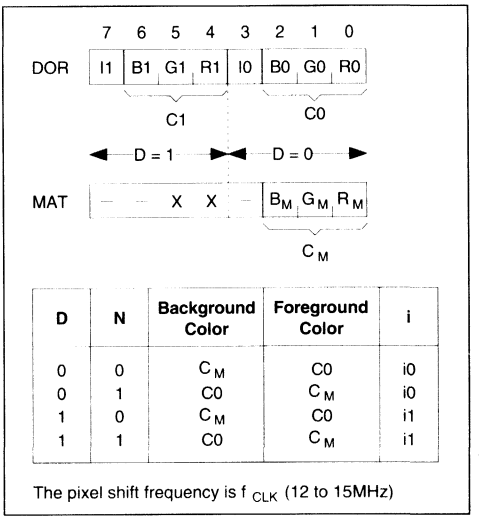
Displaying The Attributes : DOR REGISTER (see Figure 34)

Short code character are not flashing, not underlined and "positive".

The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (SN = 9).
- Flash : background is periodically (0.5Hz - 50%) forced on all the window. The phase depends on the negative attribute.
- Color select : a "positive" character is displayed with a background color same as the margin color. The foreground color is selected in DOR register by the D attribute.
- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : The D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section).

Figure 34



D	N	Background Color	Foreground Color	i
0	0	C_M	C0	i0
0	1	C0	C_M	i0
1	0	C_M	C0	i1
1	1	C0	C_M	i1

The pixel shift frequency is f_{CLK} (12 to 15MHz)

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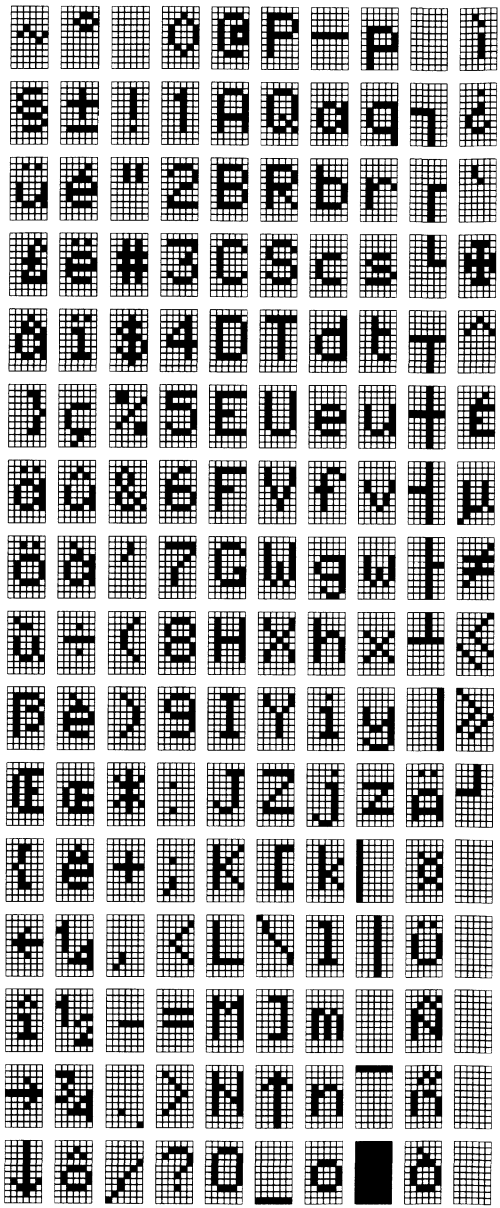
Figure 35 : G_{OE} Alphanumeric Character Set in 80 Character/Row Mode - TS9347

C7	0	0	0	0	0	0	0	0	1	1
C6	0	0	0	0	1	1	1	1	0	0
C5	0	0	1	1	0	0	1	1	0	0
C4	0	1	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



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MICROPROCESSOR ACCESS COMMANDS

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :
- to/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- to/from the dedicated memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

Address Phase

The falling edge of AS latches the AD (0.7) bus state and $\overline{CS}$ signal into the temporary A address register (Figure 36).
- A (0:2) = i
  This register index designates one out of 8 direct access registers R_i.
- A3 = XQR
  This is the execution request bit.
- A (4:7) = ASN
  This is the Auto-Selection Nibble.
- A8 = $\overline{LCS}$
  This is the latched value of $\overline{CS}$ input pin.

TS9347 is selected when the following condition is met : ASN = 2 (Hexa) and $\overline{LCS}$ = 0.

Therefore, TS9347 is mapped in the hexadecimal microprocessor addressing space from XX20 to XX2F, where XX is up to the user. When TS9347 is not selected, its AD bus pins float and no register can be modified (see Figure 37)

Data Phase - Registers

When TS9347 is selected and while AS input is low, the R_i register is accessed.
R0 designates a write-only COMMAND register or a read-only STATUS register.
R1 to R7 hold the arguments of a command. They are read/write registers.
R1, R2, R3 are used to transfer the data.
R4, R5 hold the Auxiliary Pointer (AP).
R6, R7 hold the Main pointer (MP).
(See Figure 36).

Command Register

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see COMMAND TABLE).

Type

There are 3 groups of command :
- The IND command which gives access to on-chip resources,
- The character code transfer commands,
- The general purpose commands.

Parameters

R/$\overline{W}$: Direction
  1 : to DATA registers (R1, R2, R3)
  0 : from DATA registers.

r : Internal resource index (see Figure 38)

i : Auto-incrementation
  1 : with post auto-incrementation
  0 : without auto-incrementation.

p : Pointer select
  1 : auxiliary pointer
  0 : main pointer

s, $\overline{s}$: Source, destination select
  01 : source : MP ; destination : AP
  10 : source : AP ; destination : MP

$\overline{a}$, a : Stop condition
  01 : stop at end of buffer
  10 : no stop.

Figure 36 : Direct Access Registers

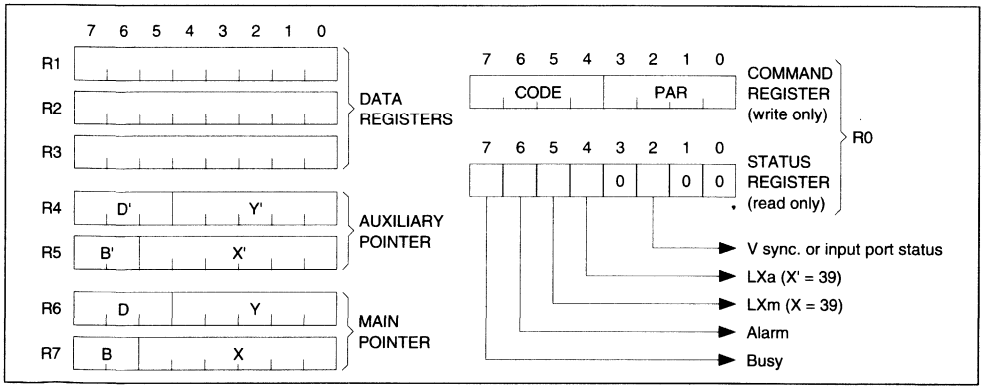


Figure 37

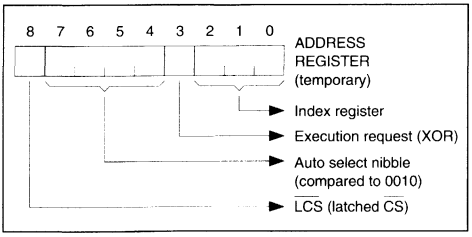
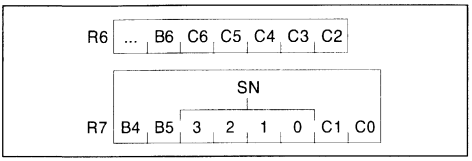


Figure 38 : Indirect on–chip Ressource Access



STATUS REGISTER

This is a read-only, direct access register.

S7 : BUSY — BUSY is set at the beginning of any command execution. It is reset at completion.

S6, S5, S4 : AI, LX_m, LX_a — LX_m or LX_a is set when respectively the main pointer or the auxiliary pointer holds X = 39 before a possible incrementation. The alarm bit S6 is set when LX_m or LX_a is set and an incrementation is performed after access.

S2 : Gives the vertical synchronization signal state, or the input port value. This is maskable by the VRM command. In this case, its values is 0.

S3 = S1 = S0 = 0 Not used.

S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.

Notes on Command Execution

1. The execution of any command starts at the trailing edge of DS when (and only when) :
   - TS9347 has been selected,
   - XQR has been set,

   at the previous AS falling edge.
   This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.
2. At power on, the busy state is undeterminated. It is recommanded to load first a NOP command with XQR = 1 before any effective command.
3. While Busy is set, the current command is under execution. Register access is then restricted.
   Register access with XQR = 0
   - Read STATUS is effective.
   - Write COMMAND or any other register access are ineffective.

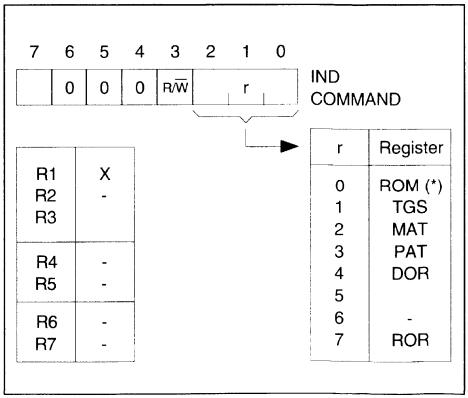
   That is to say, the microprocessor reads undertermined values and may not modify a register.
   Register access with XQR = 1
   - Read STATUS or write COMMAND are effective,
   - Access to other registers is ineffective.

   However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).
4. Execution suspension
   The execution of any command (except VRM, VSM) is suspended during the last and first scan line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 208 memory cycle period. This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND Command (see Figure 38)

This command transfers one byte between R1 and an internal resource. The r parameter designates on on-chip indirect register.

Figure 39



* **Note :** A slice in 40C only can be read from the internal character generator. The slice address must be initialized in R6, R7.

Character Code Access : TLM, TLA, TSM, TSA,KRL, KRS

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory.

TLM, TLA transfers 24 bits with Main/Auxiliary Pointer
TSM, TSA transfers 16 bits with Main/Auxiliary Pointer
KRL transfers 12 bits with Main Pointer
KRS transfers 8 bits with Main Pointer

Code packing, pointer and data structures are explained in the corresponding character code section.
When auto-incrementation is enabled, MP or AP is automatically updated after access so as to point to the next location.
This location corresponds to the next right position on screen. When last position (X = 39) is accessed, LX_m is set. When last position is accessed with auto-incrementation, alarm is also set. MP or AP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

General Purpose Access to a Byte : TBM, TBA

This command uses either MP or AP pointer.
When MP is in use, an overflow yields to a Y incrementation.

Move Buffer Commands : MVB, MVD, MVT

These are memory to memory commands which use R1 as working register.
MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word an 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter a = 1, the process stops when either source or destination buffer end is reached. If the parameter a = 0, the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

Miscellaneous Command : INY, VRM and VSM

INY command increments Y in MP.
VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor from the status register. After power on, the mask state is undetermined.

REGISTER - MAP

Figure 40a

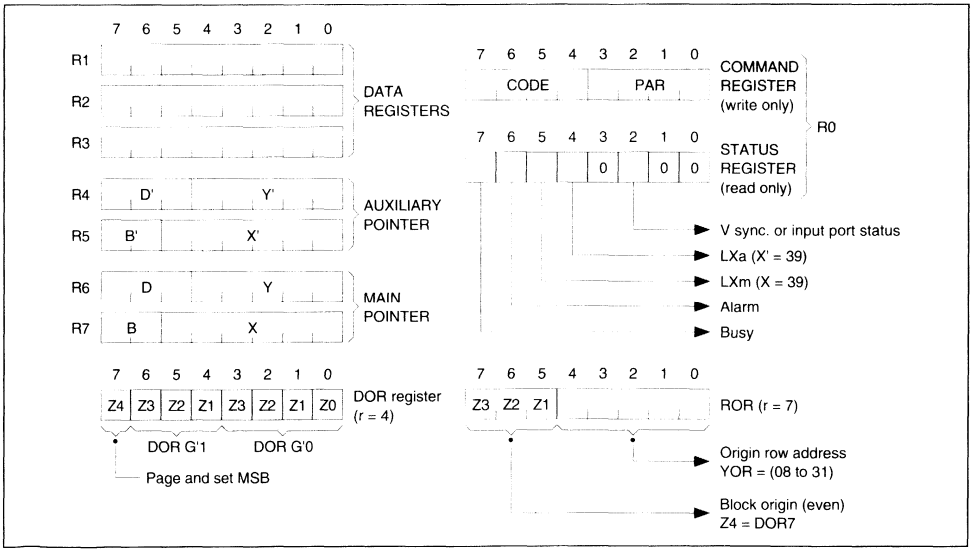


Figure 40b

SYNC. IN PIN FUNCTION	STATUS REG. (BIT 2)	SYNCHRO-NIZATION	TGS2	TGS3
INPUT PORT	INPUT PORT	NO SYNC.	0	0
	V. SYNC. OUT	NO SYNC.	1	0
V. SYNC.	SYNC. IN	V. SYNC.	0	1
COMPOSITE SYNC. IN	V. SYNC OUT	H. AND V. SYNC.	1	1

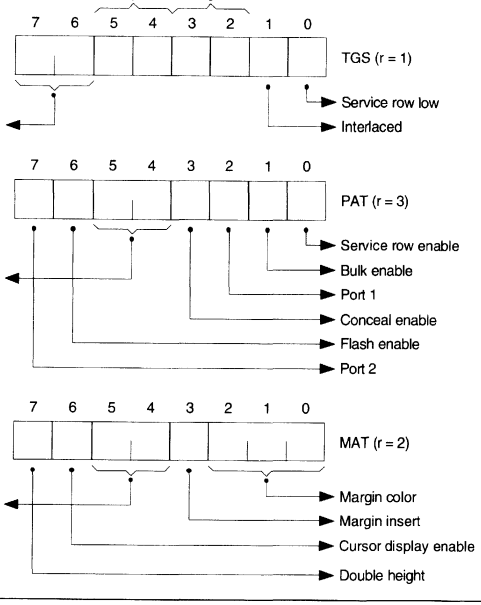
OUTPUT PINS B	G	R	TGS4	TGS5
B	G	R	0	0
B	I	R	1	0
P2	P1	HVS	0	1
P2	I	HVS	1	1

CHAR CODE	TGS7	TGS6
40 CHAR LONG	0	0
40 CHAR SHORT	0	1
80 CHAR LONG	1	1
80 CHAR SHORT	1	0

INSERT MODE	PAT5	PAT4
INLAY	0	0
BOXING AND INLAY	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

CURSOR DISPLAY MODE	MAT5	MAT4
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

NOTE : PROGRAMMING BIT VALUE
1 = True, 0 = False



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COMMAND TABLE

Type	Memo	Code				Parameter				Status			Arguments							Execution Time (1)	
		7	6	5	4	3	2	1	0	Ai	LX_m	LX_a	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R/$\overline{W}$	-	r	-	0	0	0	D	-	-	-	-	MP		2	3.5
40 Characters - 24 Bits	TLM	0	0	0	0	R/$\overline{W}$	0	0	I	X	X	0	C	B	A	-	-	MP		4	7.5
40 Characters - 24 Bits	TLA	0	0	1	0	R/$\overline{W}$	0	1	I	X	0	X	C	B	A	AP		-		4	7.5
40 Characters - 16 Bits	TSM	0	1	1	0	R/$\overline{W}$	0	0	I	X	X	0	A*	B*	-	-	-	MP		3	5.5
40 Characters - 16 Bits	TSA	0	1	1	1	R/$\overline{W}$	0	0	1	X	0	X	A*	B*	-	AP		-		3	5.5
80 Characters - 8 Bits	KRS	0	1	0	0	R/$\overline{W}$	0	0	I	X	X	0	C	-	-	-	-	MP		9	9.5
80 Characters - 12 Bits	KRL	0	1	0	1	R/$\overline{W}$	0	0	I	X	X	0	C	-	A	-	-	MP		12.5	11.5
Byte	TBM	0	0	1	1	R/$\overline{W}$	0	0	I	X	X	0	D	-	-	-	-	MP		4	4.5
Byte	TBA	0	0	1	1	R/$\overline{W}$	1	0	I	X	0	X	D	-	-	AP		-		4	4.5
Move Buffer	MVB	1	1	0	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 4.n	-
Move Double Buffer	MVD	1	1	1	0	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 8.n	-
Move Triple Buffer	MVT	1	1	1	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 12.n	-
Clear Page (4) - 24 Bits	CLL	0	0	0	0	0	1	0	1	X	X	0	C	B	A	-	-	MP		< 4700 (1 K code)	-
Clear Page (4) - 16 Bits	CLS	0	1	1	0	0	1	0	1	X	X	0	A*	B*	-	-	-	MP		< 3500 (1 K code)	-
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	-	-	-	-	-	-	-	1	-
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	X	X	0	-	-	-	-	-	-	-	1	-
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	-	-	-	-	-	Y	-	2	-
No Operation	NOP	1	0	0	1	0	0	0	1	0	0	0	-	-	-	-	-	-	-	1	-

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s, $\overline{s}$: Source, Destination
- 01 : Source = MP, Destination = AP
- 10 : Source = AP, Destination = MP

a, $\overline{a}$: Stop Condition
- 01 : Stop at End of Buffer
- 10 : No Stop

r : Indirect Register Number

\- : Not Affected
W : Used as Working Register
X : Set or Reset Buffer
I : Pointer Incrementation
D : Data
MP : Main Pointer
AP : Auxiliary Pointe

(1) Unit : 12 clock periods (≈ 1µs) without possible suspension

(2) n : Total Number of Words ≤ 40

(3) These commands repeat TLM or KRO with Y incrementation when X overflows. When the last position is reached in a row Y is incremented and the progress starts again on the next row theses command stop only. They can also be used to initialize the page 80 char/row by writing character pairs.

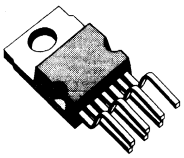
9347-19.TBL

VOLTAGE REGULATORS

TDA8134

5V +12V REGULATOR WITH DISABLE

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

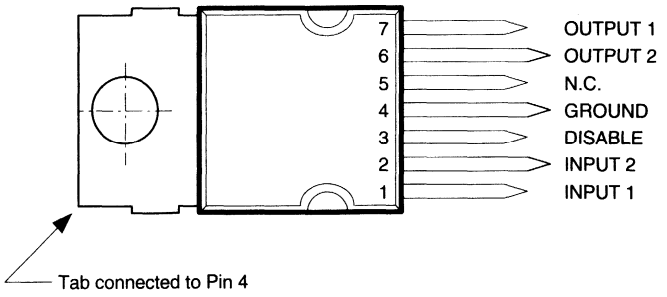
ORDER CODE : TDA8134

DESCRIPTION

The TDA8134 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + 12V at currents up to 600mA.

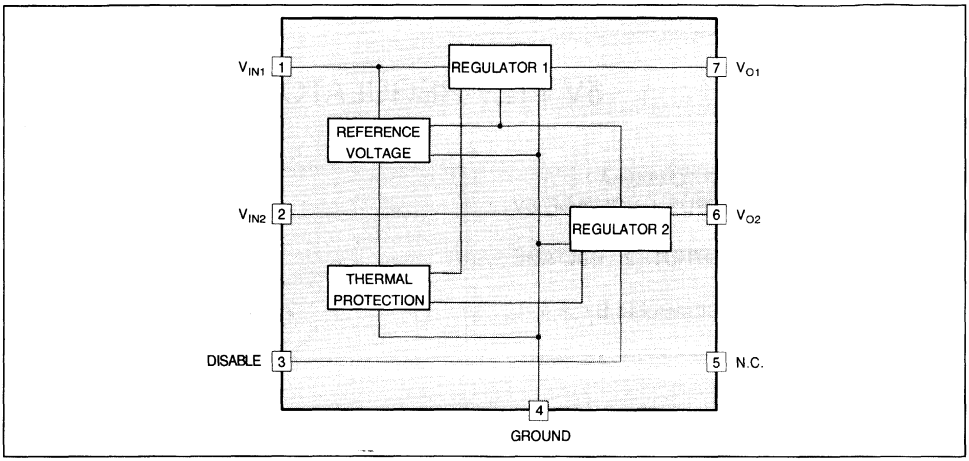
Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



8134-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1, 2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

8134-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W

8134-02.TBL

ELECTRICAL CHARACTERISTICS

(V_{IN1} = 7V ; V_{IN2} = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.9	5	5.1	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0, V_{DIS} = 0 I_{O1} = 10mA, (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	7V < V_{IN1} <14V, I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} <18V, I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} <600mA			100	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} <600mA			240	mV

8134-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = 7V ; V_{IN2} = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} <18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} <18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	–80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = $9V_{DC}$ + $1V_{PP}$ SIN f = 120Hz, I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection2 (see note 1)	V_{IN2} = $16V_{DC}$ + $1V_{PP}$ SIN f = 120Hz, I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	V_{IN1} = V_{IN2} =$14V_{DC}$ I_{O1} = I_{O2} =200mA (see fig. 1)			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

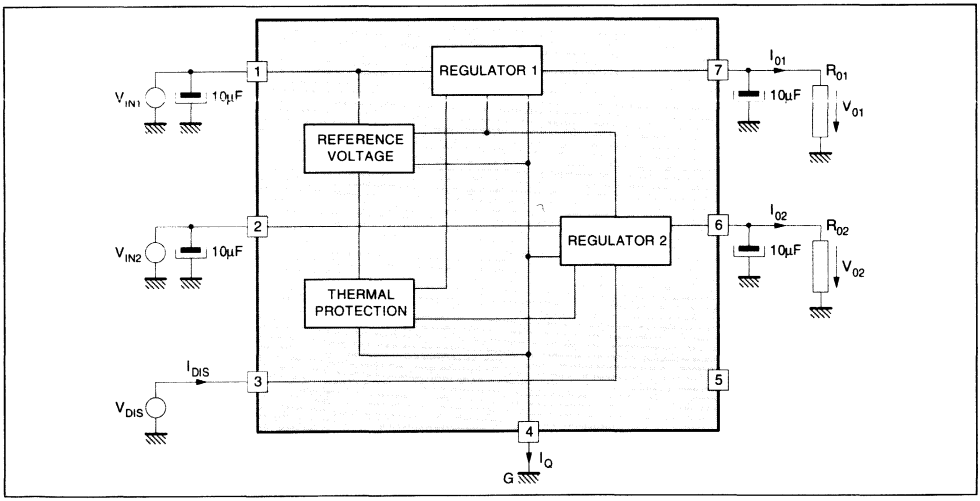
8134-04.TBL

Note 1 : SVR supply voltage rejection :

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
$V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, $1V_{PP}$)
$V_{O\,ac}$ is the peak-peak ripple voltage present at the output

Figure 1 : Test Circuit



8134-03.EPS

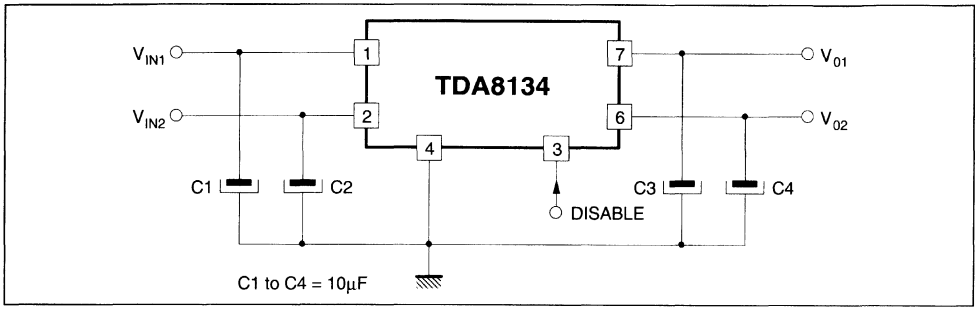
CIRCUIT DESCRIPTION

The TDA8134 is a dual voltage regulator with disable.

The two regulation parts are supplied from one vol-tage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

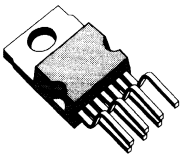
It is possible to switch-off the output voltage 2 (V_{O2}) by appling at Pin 3 (disable input) a low TTL level.

TYPICAL APPLICATION



5V + ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- OUTPUT 2 - VOLTAGE PROGRAMMABLE FROM 5V TO 14V
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

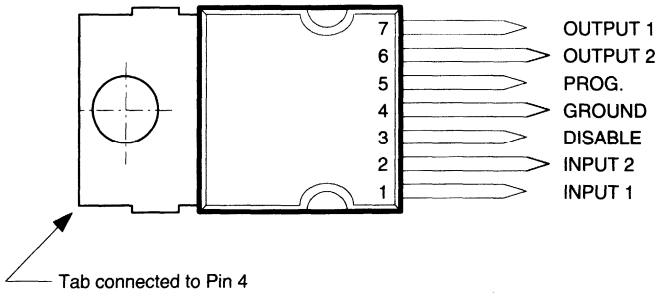
ORDER CODE : TDA8135

DESCRIPTION

The TDA8135 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + adjustable outputs at currents up to 600mA.

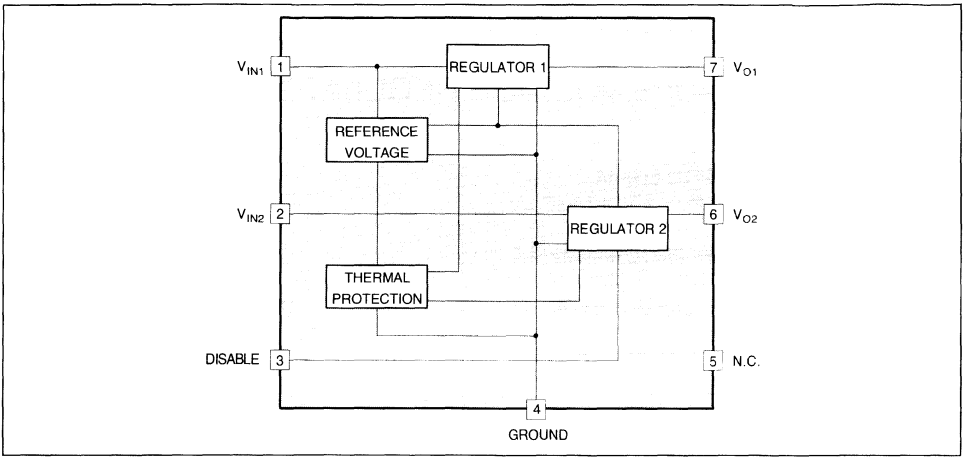
Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



8135-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1, 2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

8135-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W

8135-02.TBL

ELECTRICAL CHARACTERISTICS

(V_{IN1} = 7V ; V_{IN2} = V_{O2} + 2V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.9	5	5.1	V
V_{O2}	Output Voltage at Pin 6	Adustable	5		14	V
I_{Q1}	Quiescent Current	V_{IN2} = 0, V_{DIS} = 0 I_{O1} = 10mA, (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	7V < V_{IN1} <14V, I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation 2	12V < V_{IN2} <20V, I_{O2} = 200mA V_{O2} = 10V			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} <600mA			100	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} <600mA, V_{O2} = 10V			200	mV

8135-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = 7V ; V_{IN2} = V_{O2} + 2V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{O1SC}	Short Circuit Current 1	7V < V_{IN1} <14V			1.3	A
I_{O2SC}	Short Circuit Current 2	V_{O2} + 2V < V_{IN2} <20V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
V_{PROG}	Reference Voltage at Pin 5			2.5		V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	–80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 9V_{DC} + 1V_{PP} SIN f = 120Hz, I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection2 (see note 1)	V_{IN2} = 16V_{DC} + 1V_{PP} SIN f = 120Hz, I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	I_{O1} = I_{O2} =200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

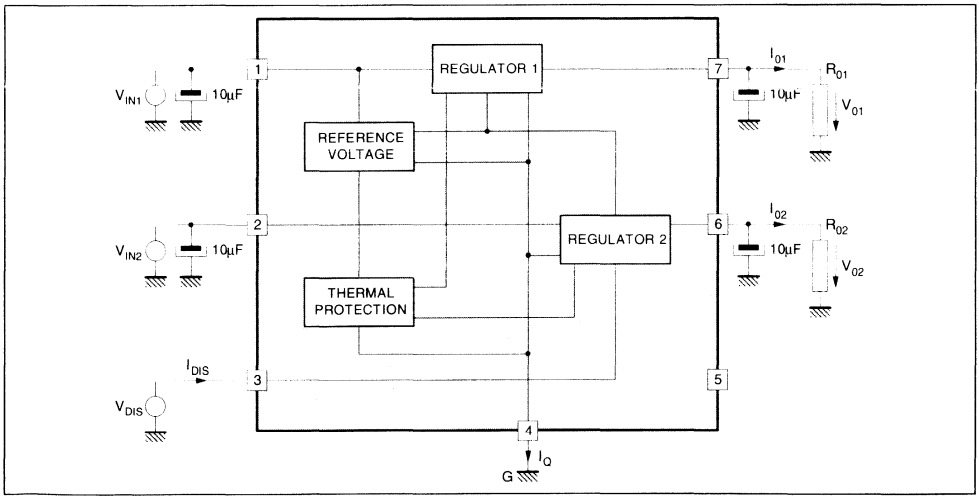
8135-04.TBL

Note 1 : SVR supply voltage rejection :

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
$V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
$V_{O\,ac}$ is the peak-peak ripple voltage present at the output

Figure 1 : Test Circuit



8135-03.EPS

CIRCUIT DESCRIPTION

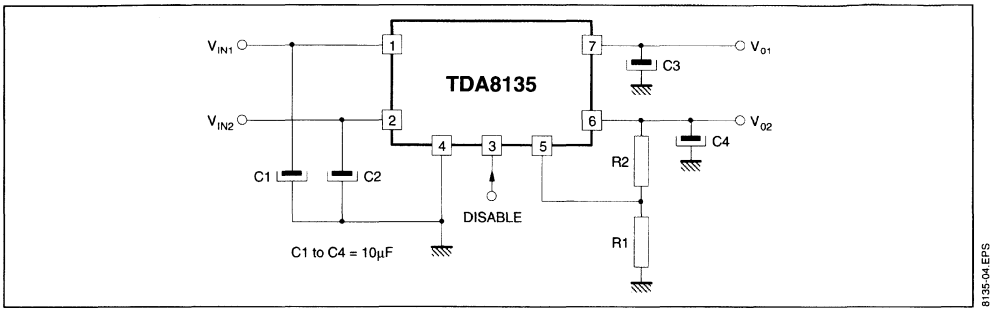
The TDA8135 is a dual voltage regulator with disable.

The two regulation parts are supplied from one vol-tage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

It is possible to switch-off the output voltage 2 (V_{O2}) by appling at Pin 3 (disable input) a low TTL level.

$$V_{02} = V_{PROG} \cdot \frac{R1 + R2}{R1}$$

TYPICAL APPLICATION

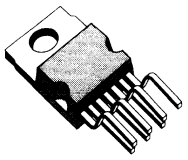


SGS-THOMSON MICROELECTRONICS

TDA8136

DUAL 12V REGULATOR WITH DISABLE

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 12V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT
(Plastic Package)

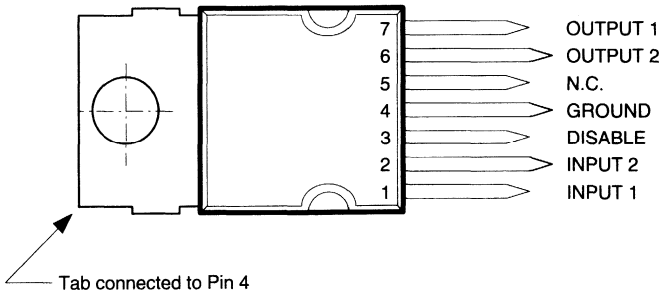
ORDER CODE : TDA8136

DESCRIPTION

The TDA8136 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, both 12V at currents up to 600mA.

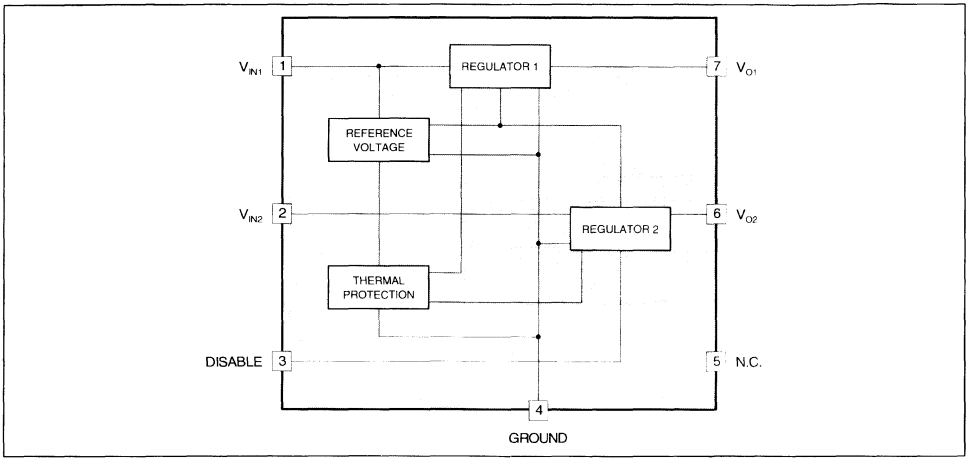
Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

PIN CONNECTIONS



8136-01.EPS

BLOCK DIAGRAM



8136-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1, 2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

8136-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max.	3	°C/W

8136-02.TBL

ELECTRICAL CHARACTERISTICS

($V_{IN1,2}$ = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		11.76	12	12.24	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0, V_{DIS} = 0 I_{O1} = 10mA, (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	14V < V_{IN1} <18V, I_{O1} = 200mA			120	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} <18V, I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} <600mA			240	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} <600mA			240	mV

8136-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN1,2}$ = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} <18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} <18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	–80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 16V_{DC} + 1V_{PP} SIN f = 120Hz, I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection2 (see note 1)	V_{IN2} = 16V_{DC} + 1V_{PP} SIN f = 120Hz, I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	V_{IN1} = V_{IN2} =14V_{DC} I_{O1} = I_{O2} =200mA (see fig. 1)			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

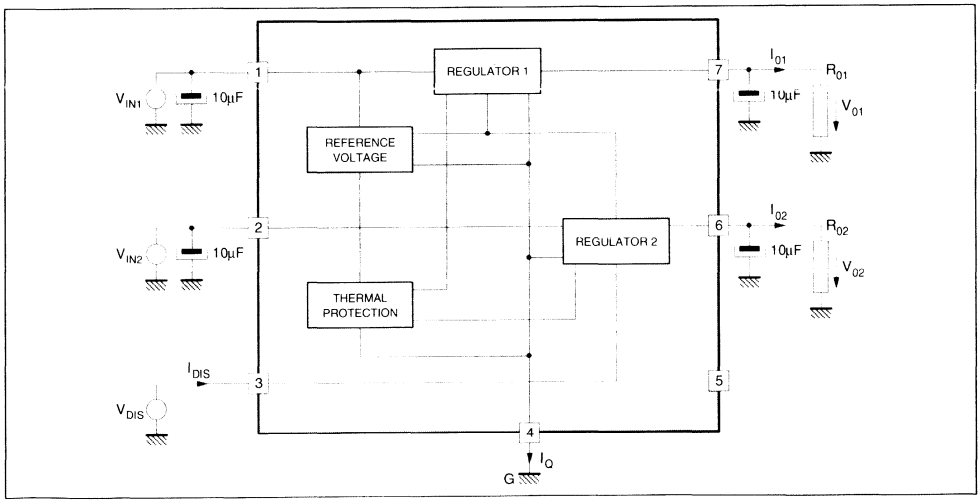
8136-04.TBL

Note 1 : SVR supply voltage rejection :

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
$V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
$V_{O\,ac}$ is the peak-peak ripple voltage present at the output

Figure 1 : Test Circuit



8136-03.EPS

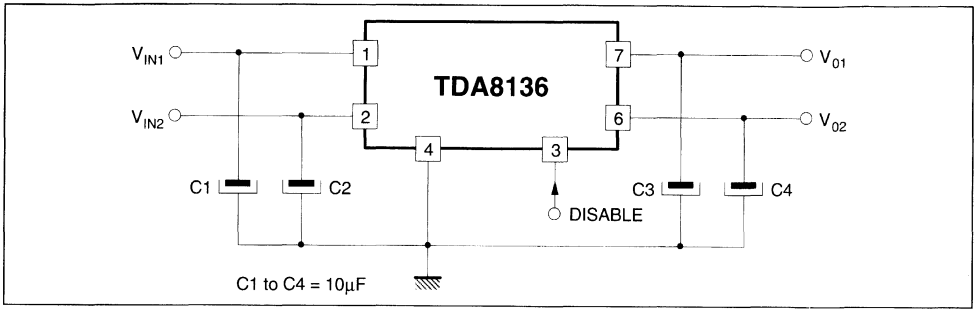
CIRCUIT DESCRIPTION

The TDA8136 is a dual voltage regulator with disable.

The two regulation parts are supplied from one vol-tage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

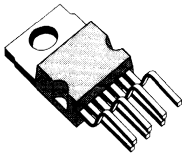
It is possible to switch-off the output voltage 2 (V_{O2}) by appling at Pin 3 (disable input) a low TTL level.

TYPICAL APPLICATION



DUAL 5.1V REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES 5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8137

DESCRIPTION

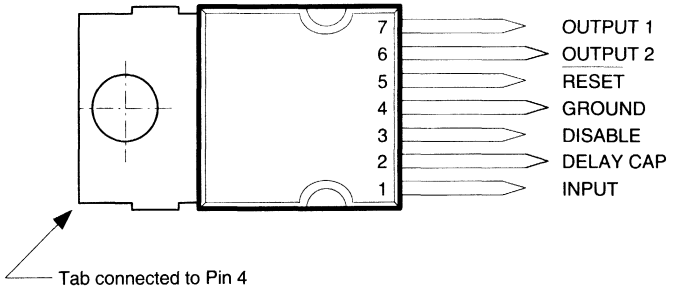
The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

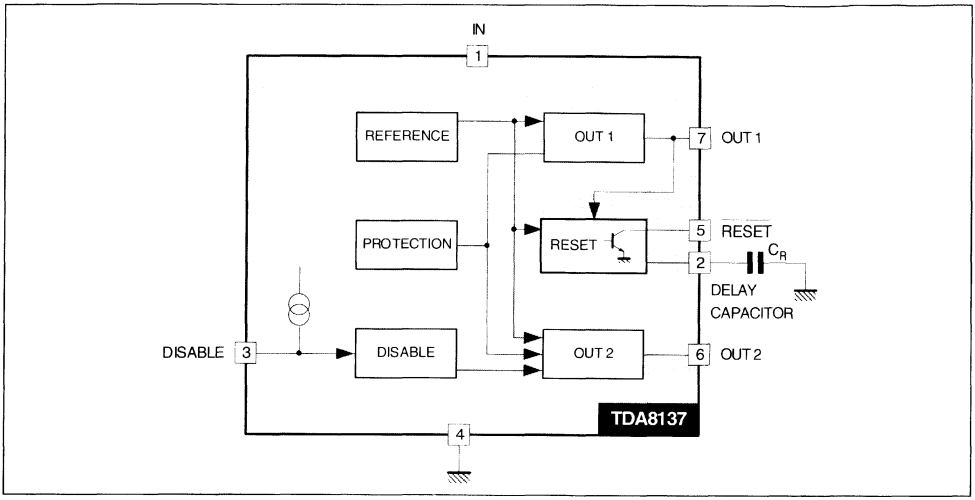
Short circuit and thermal protections are included.

PIN CONNECTION (top view)



8137-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at Pin 5	20	V
$I_{01,\ 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

8137-04.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j\text{-}c)}$	Thermal Resistance Junction-case	Max.	3	°C/W
T_j	Recommended Junction Temperature	Max.	0 to + 150	°C

8137-02.TBL

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{01,\ 2}$	Output Voltage	$I_{01,\ 2}$ = 10mA	5	5.1	5.2	V
		7V < V_{IN} < 14V, 5mA < I_o < 750mA	4.9		5.3	V
$V_{I\ 01,\ 2}$	Dropout Voltage	$I_{01,\ 2}$ = 750mA			1.4	V
		$I_{01,\ 2}$ = 1A			2	V
$\Delta V_{01,\ 2LI}$	Line Regulation	7V < V_{IN} < 14V, $I_{01,\ 2}$ = 200mA			50	mV
$\Delta V_{01,\ 2LO}$	Load Regulation	5mA < $I_{01,\ 2}$ < 0.6A			100	mV
I_Q	Quiescent Current	I_{01} = 10mA, Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K–0.4	K–.25	K–0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see circuit description)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 5	C_e = 100nF (see circuit description)		25		ms
V_{RL}	Saturation Volt. at Pin 5 in Reset Condition	I_5 = 5mA			0.4	V

8137-03.TBL

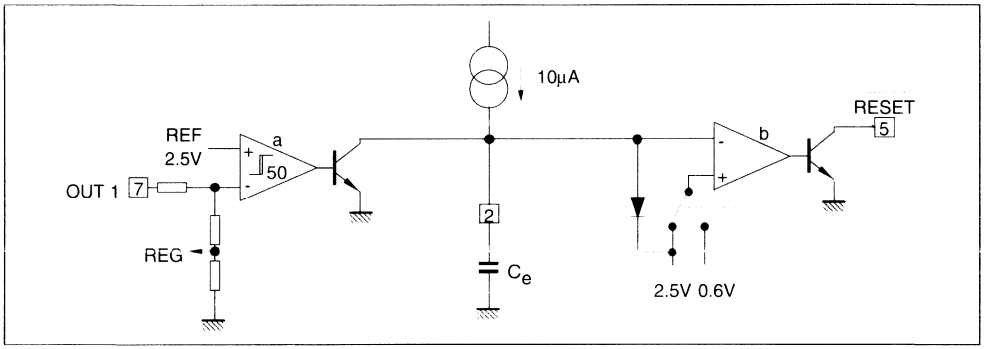
ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$K_{01.2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta V_o \cdot 10^6}{\Delta T \cdot V_O}$ T_j = 0 to + 125°C		100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN} = 7V			1.6	A
		V_{IN} = 16V, (see note 1)			1	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 3	0V < V_{DIS} < 7V	-100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

8137-04.TBL

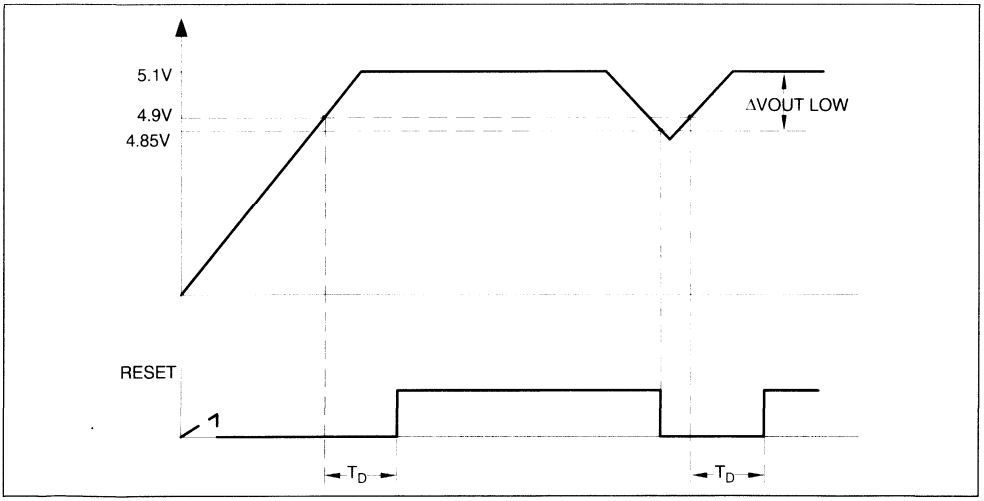
Note 1 : The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.
Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

Figure 1



8137-03.EPS

Figure 2



8137-04.EPS

CIRCUIT DESCRIPTION

The TDA8137 is a dual voltage regulator with Reset and Disable.

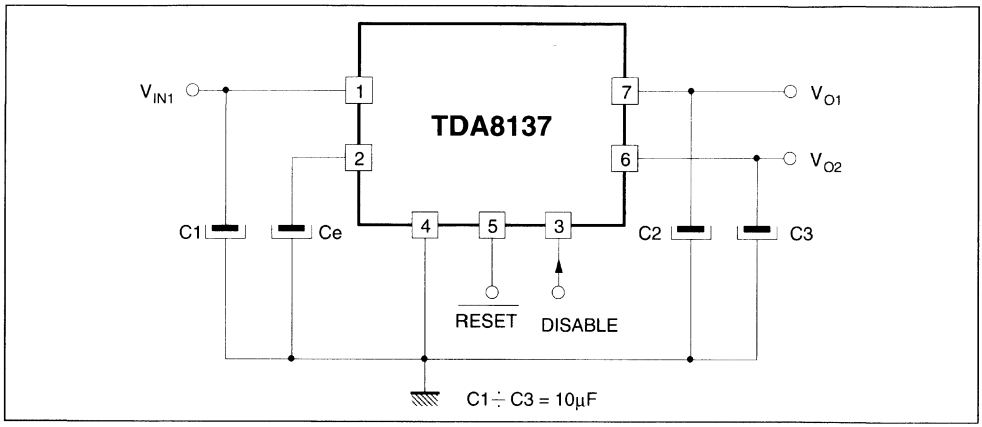
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

The outputs stages have been realized in darlington configuration with a drop typical of 1.2V.

The disable circuit, switches off the output 2 if a voltage lower than 0.8V is applied at pin 3.

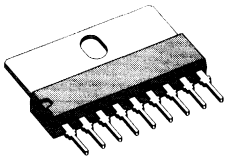
The Reset circuit checks the voltage at the output 1. If this one goes below V_{OUT} - 0.25V (4.85V Typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor Ce and the reset output goes at once low. When the voltage at the OUT 1 rises above V_{OUT} - 0.2V (4.9V Typ.), the voltage V_{Ce} increases linearly to 2.5V corresponding to a delay t_d following the low : $t_d = \frac{Ce \cdot 2.5V}{10\mu A}$ (see figure 2), then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

TYPICAL APPLICATION



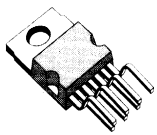
5.1V +12V REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V +/- 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V +/- 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE IN TWO VERSIONS : TDA8138A (DISABLE ONLY), TDA8138B (RESET ONLY)



SIP9
(Plastic Package)

ORDER CODE : TDA8138



HEPTAWAT
(Plastic Package)

ORDER CODE : TDA8138A / TDA8138B

DESCRIPTION

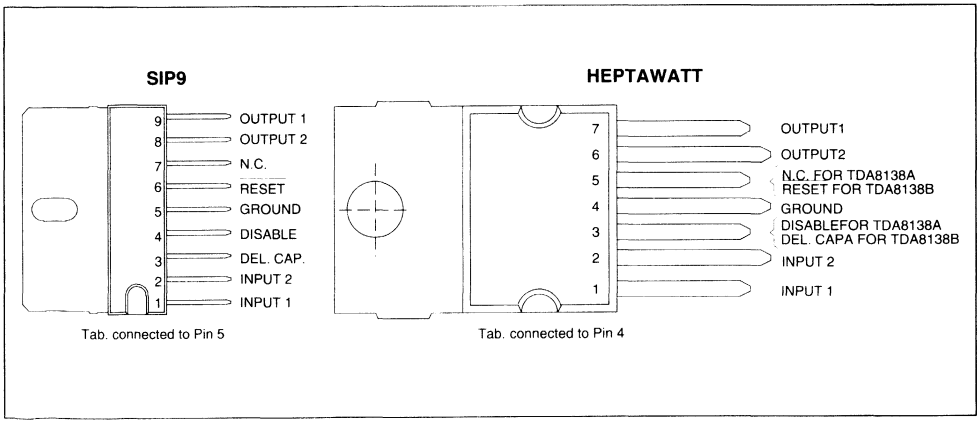
The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value (for TDA8138 and TDA8138B).

Output 2 can be disabled by TTL input (for TDA8138 and TDA8138A).

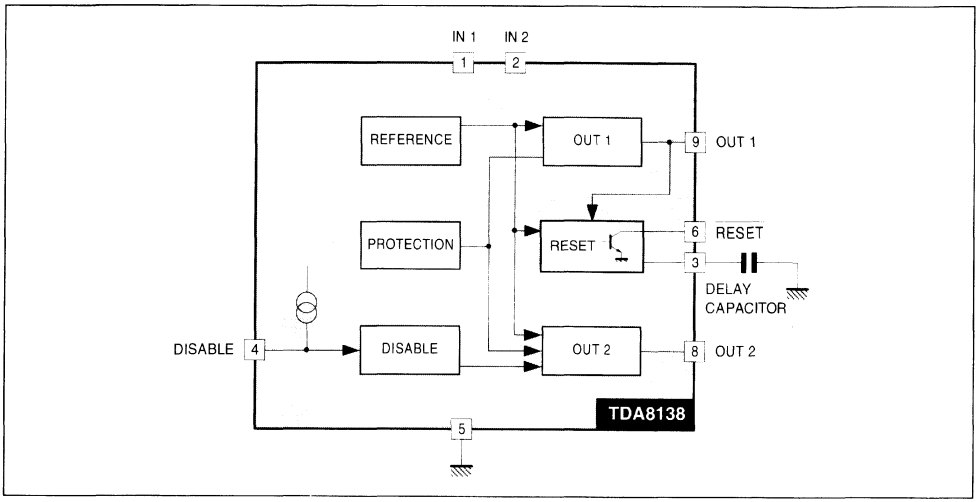
Short circuit and thermal protections are included in all the versions.

PIN CONNECTIONS



8138-01A.EPS - 8138-01B.EPS

BLOCK DIAGRAM (SIP9 package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3 (Heptawatt) or Pin 4 (SIP9)	20	V
V_{RST}	Output Voltage at Pin 6 (SIP9) or Pin 5 (Heptawatt)	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Junction Temperature	0 to +150	°C

8138-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}c)}$	Maximum Thermal Resistance Junction-case for SIP9 Maximum Thermal Resistance Junction-case for Heptawatt	8 3	°C/W °C/W
$R_{th\ (j\text{-}a)}$	Maximum Thermal Resistance Junction-ambient for SIP9	60	°C/W
T_j	Maximum Recommended Junction Temperature	130	°C

8138-02.TBL

ELECTRICAL CHRACTERISTICS (V_{IN1} = 7V, V_{IN2} = 14V, T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	11.76	12	12.24	V
V_{O1}	Output Voltage	7V < V_{IN1} < 14V	4.9		5.3	V
V_{O2}	Output Voltage	14 < V_{IN2} < 18V 5mA < $I_{O1,2}$ < 750mA	11.5		12.5	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA $I_{O1,2}$ = 1A			1.4 2	V V
$V_{O1,2LI}$	Line Regulation	7V < V_{IN1} < 14V 14 < V_{IN2} < 18V $I_{O1,2}$ = 200mA			50 120	mV mV
$V_{O1,2LO}$	Load Regulation	5mA < I_{O1} < 0.6A 5mA < I_{O2} < 0.6A			100 250	mV mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Thrseshold Voltage	K = V_{O1}	K - 0.4	K - 0.25	K - 0.1	V
V_{RTH}	Reset Thrseshold Hysteresis	See circuit description	20	50	75	mV
t_{RD}	Reset Pulse Delay	C_e = 100nF See circuit description		25		ms
V_{RL}	Saturation Voltage in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current in Normal Condition (at Pin 6 for SIP9 or Pin 5 for Heptawatt)	V_5 = 10V			10	µA
$K_{O1,2}$	Output Voltage Thermal Drift	T_j = 0 to 125°C $K_O = \frac{\Delta V_O \cdot 10^6}{\Delta T \cdot V_O}$		100		ppm/°C
$I_{O1,2SC}$	Short Circuit Output Current	V_{IN1} = 7V, V_{IN2} = 14V $V_{IN1,2}$ = 16V (see Note)			1.6 1	A A
V_{DISH}	Disable Voltage High (out 2 active)		2			V
V_{DISL}	Disable Voltage Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0V < V_{DIS} < 7V	-100		2	µA
T_{jsd}	Junction Temperature for Thermal Shut Down			145		°C

8138-03.TBL

Note : Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

CIRCUIT DESCRIPTION

The TDA8138 is a dual voltage regulator with Reset and Disable (TD8138A : Disable only, TDA8138B : Reset only).

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.
Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if Pin 1 is not supplied.

The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at Pin 3 (Heptawatt) or Pin 4 (SIP9)

The Reset circuit checks the voltage at the output 1. If this one goes below V_{OUT} - 0.25V (4.85V typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor C_e and the reset output goes at once Low. When the voltage at the out1 rises above V_{OUT} - 0.2V (4.9V typ.), the voltage V_{Ce} increases linearly to 2.5V corresponding to a delay td following the law : $t_1 = \frac{C_e \cdot 2.5V}{10\mu A}$ (see Figure 2), then the reset output goes high again. To avoid gliches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

Figure 1

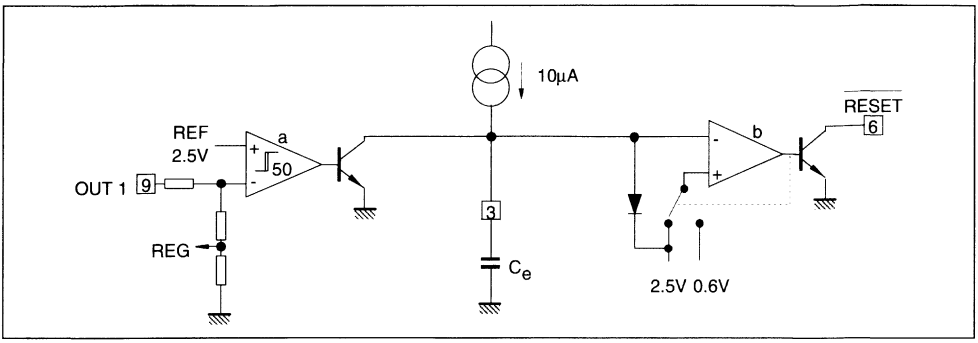
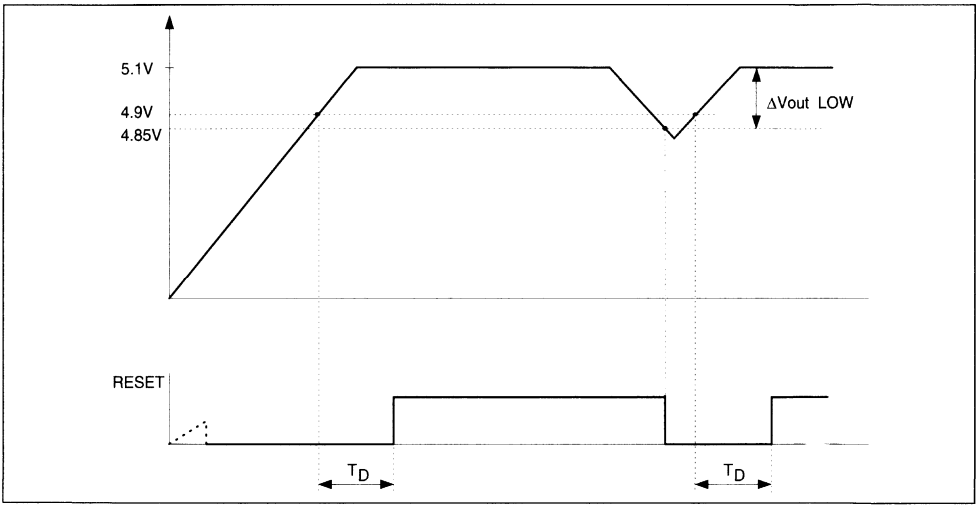
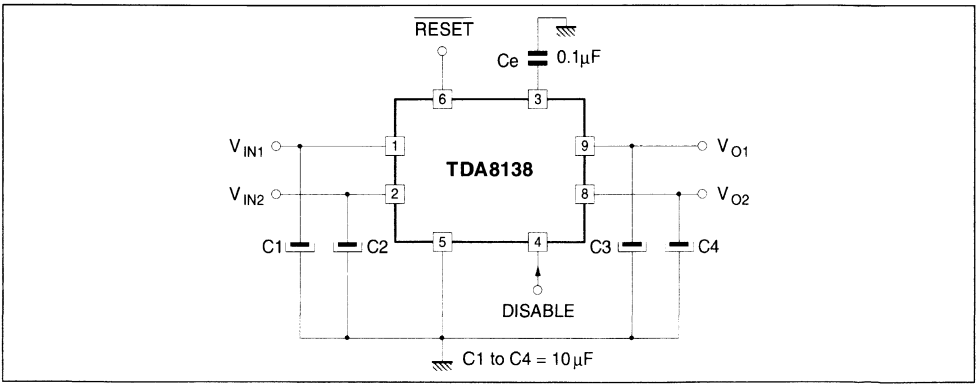


Figure 2



TYPICAL APPLICATION (SIP9 package)

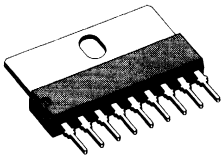


SGS-THOMSON MICROELECTRONICS

TDA8139

5.1V AND ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 750mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- OUTPUT 2 VOLTAGE PROGRAMMABLE FROM 2.8 TO 16V
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



SIP9
(Plastic Package)

ORDER CODE : TDA8139

DESCRIPTION

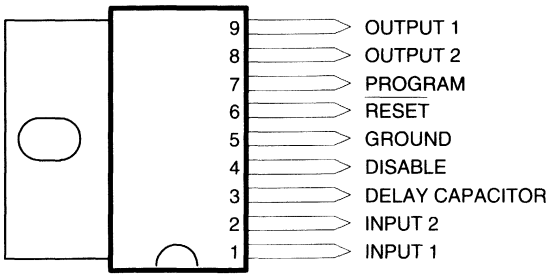
The TDA8139 is a monolithic dual positive voltage regulator designed to provide precision output voltages of 5.1V and adjustable at currents up to 750mA.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

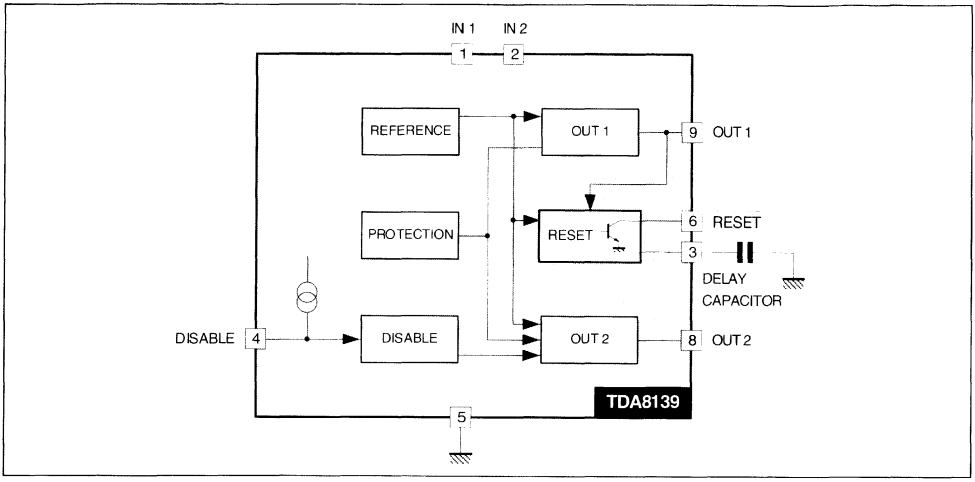
Short circuit and thermal protections are included.

PIN CONNECTIONS



8139-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1, 2	20	V
V_{DIS}	Disable Input Voltage Pin 4	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,\ 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_J	unction Temperature	0 to + 150	°C

8139-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{TH(j\text{-}c)}$	Thermal Resistance Junction-case	Max.	8	°C/W
T_J	Recommended Junction Temperature	Max.	130	°C

8139-02.TBL

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	2.8		16	V
$V_{IO1,\ 2}$	Dropout Voltage	$I_{O1,\ 2}$ = 750mA			1.4	V
V_{O1}	Line Regulation 1	7V < V_{IN1} < 14V, 12V < V_{IN2} < 18V, @ V_{O2} : 10V, $I_{O1,\ 2}$ = 200mA			50	mV
V_{O2}	Line Regulation 2				100	mV
V_{O1}	Load Regulation 1	5mA < $I_{O1,\ 2}$ < 0.6A, @ V_{O2} = 10 V			100	mV
V_{O2}	Load Regulation 2				200	mV
I_Q	Quiescent Current	I_{O1} = 10mA, Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see circuit description)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see circuit description)		25		ms

8139-03.TBL

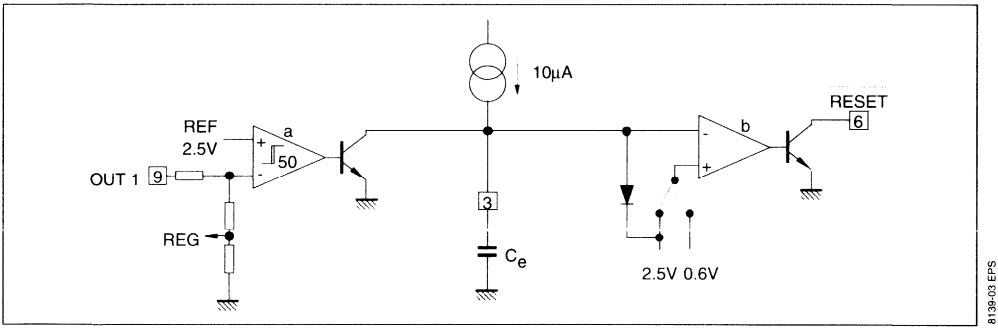
ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 6 in Normal Condition	V_5 = 10V			10	µA
$K_{O1,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta V_o \cdot 10^6}{\Delta T \cdot V_O}$ Tj = 0 to + 125°C		100		ppm/°C
$I_{O1,2\ sc}$	Short Circ. Ouput Current	V_{IN} = 7V			1.6	A
		V_{IN} = 16V, (see note 1)			1	A
V_{DISH}	Disable Volt. at Pin 4 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 4 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 4	0V < V_{DIS} < 7V	-100		2	µA
V_{ref}	Pin 7			2.5		V
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

8139-04 TBL

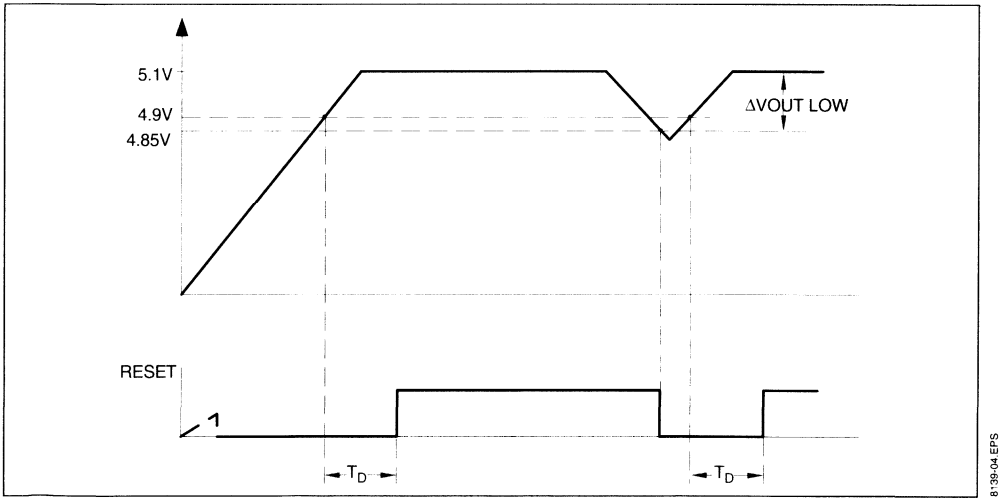
Note 1 : The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, but the thermal protection circuit prevents any excessive temperature.
Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

Figure 1



8139-03 EPS

Figure 2



8139-04 EPS

CIRCUIT DESCRIPTION

The TDA8139 is a dual voltage regulator with Reset and Disable.

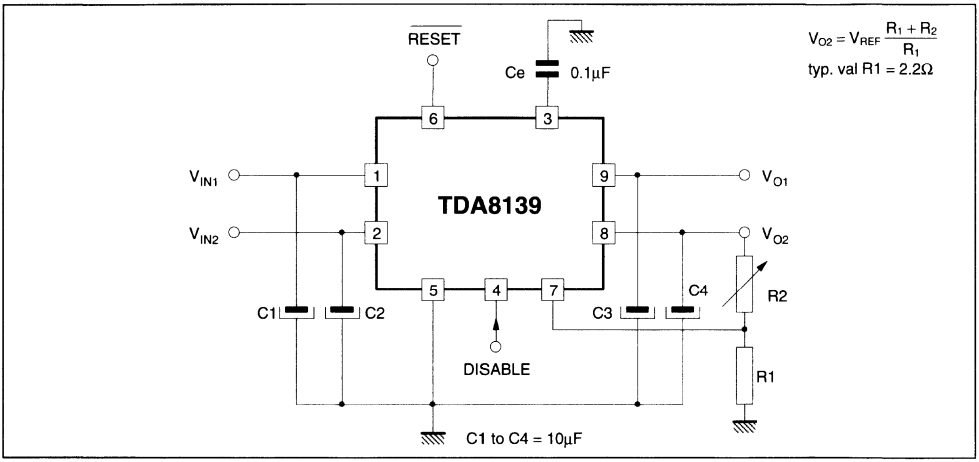
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

The outputs stages have been realized in darlington configuration with a drop typical of 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 4.

The Reset circuit checks the voltage at the output 1. If this one goes below V_{OUT} - 0.25V (4.85V Typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor Ce and the reset output goes at once low. When the voltage at the OUT 1 rises above V_{OUT} -0.2V (4.9V Typ.), the voltage V_{Ce} increases linearly to 2.5V corresponding to a delay t_d following the low : $t_d = \frac{Ce \cdot 2.5V}{10\mu A}$ (see figure 2), then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

TYPICAL APPLICATION

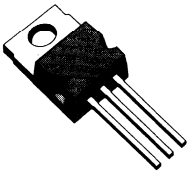


SGS-THOMSON MICROELECTRONICS

TEA7605

LOW-DROP VOLTAGE REGULATOR

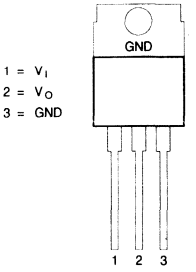
- V_O = 5V ± 4 % (I_O = 5mA)
- $I_{OS} \geq$ 500mA
- $V_I - V_O \leq$ 0.6 V (I_O = 500mA)
- $V_{I\ (surge)} = \pm$ 80V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TO220
(Plastic Package)

ORDER CODE : TEA7605SP

PIN CONNECTIONS



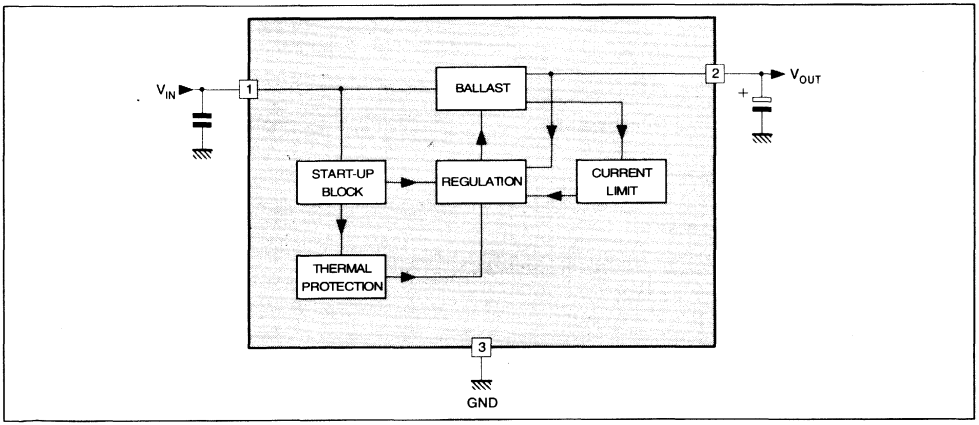
7605-01.EPS

DESCRIPTION

TEA7605 is a low-drop 5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :
- Lowest possible quiescent current (250µA).
- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



7605-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input Voltage - Continuous - τ = 300 ms	 30 80	 V V
$V_{I(R)}$	Reverse Input Voltage - Continuous - τ = 120 ms	 – 18 – 80	 V V
T_J	Operating Junction Temperature	– 45, +150	°C
T_{stg}	Storage Temperature	– 55, +150	°C

7605-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	70	°C/W

7605-02.TBL

ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_I = 14.4V (unless otherwise specified) Output Capacitor = 10µF (see note)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)		4.875	5	5.125	V
V_I	Input Supply Voltage (permanent)				28	V
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA		0.25 10 75	0.4 20 100	mA mA mA
K_{VI}	Line Regulation (V_I = 6 to 26V ; I_O = 5mA)			5	10	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)			40	60	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.18 0.4	 0.6	V V
SVR	Supply Voltage Rejection (I_O = 350mA, f = 120Hz, C_O = 1µF, V_I = 12 ± 5V)			60		dB
I_{OS}	Short-circuit Output Current		0.5	0.7		A

7605-03.TBL

NOTE : Applications Hints

The output capacitor has a direct influence on output voltage stability. A 10 µF capacitor will provide satisfactory results. There is no upper limit on this capacitor value.

If necessary, this value can be reduced down to 1 µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance, 400 mA to < 1 mA).

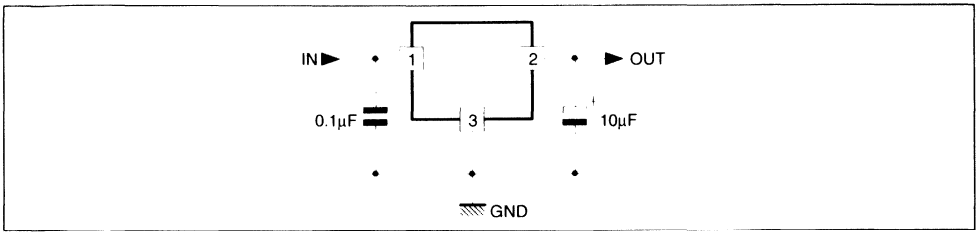
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to +125°C, V_I = 14 .4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_O	Output Voltage (I_O = 5 to 500mA)		4.8	5	5.2	V
$\frac{dV_O}{dt}$	Output Voltage Drift	T_j = – 45 to +25°C T_j = + 25 to +125°C	– 0.4 – 0.6			mV/°C
I_{CC}	Current Consumption	I_O = 0mA I_O = 150mA I_O = 500mA			0.45 25 120	mA mA mA
K_{VI}	Line Regulation (V_I = 6 to 26V, I_O = 5mA)				20	mV
K_{VO}	Load Regulation (I_O = 5 to 500mA)				80	mV
V_I - V_O	Drop-out Voltage	I_O = 150mA I_O = 500mA		0.2	 0.8	V V
I_{OS}	Short-circuit Output Current		0.4			A
I_{OM}	Maximum Output Current		0.5			A

7605-04.TBL

TYPICAL DIAGRAM



AUTOMATIC VOLTAGE SWITCH

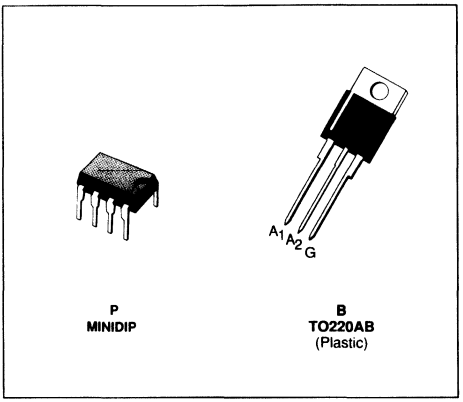
AUTOMATIC VOLTAGE SWITCH (SMPS < 200W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS08CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS08CBI
- V_{DRM} = ± 500 V
- $I_{T(RMS)}$: 5A



P
MINIDIP

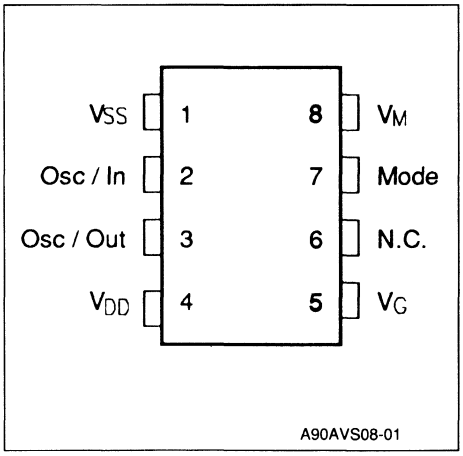
B
TO220AB
(Plastic)

DESCRIPTION

The AVS08 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 200 W. It is composed of 2 devices :

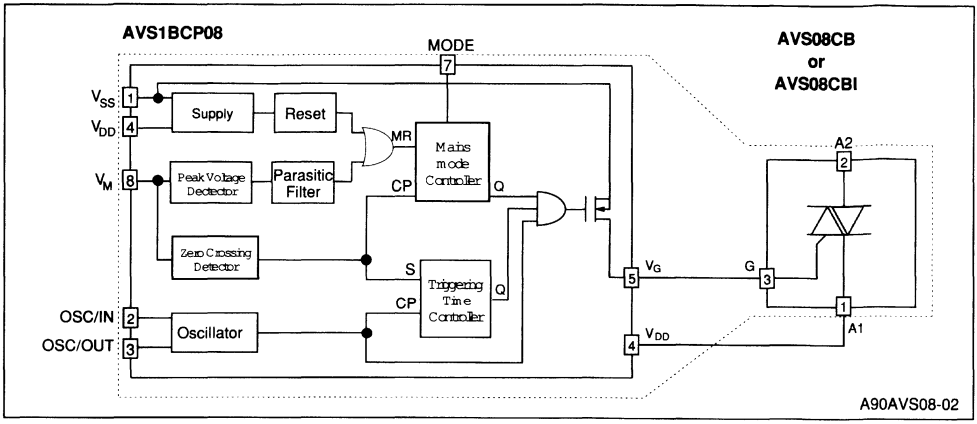
- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



A90AVS08-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1BCP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS08CB / AVS08CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 500	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS08CB	T_C = 100°C	5	A
		AVS08CBI	T_C = 95°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	70 65	A
I^2t	I^2t value		t = 10ms	21	A^2s
di/dt	Critical rate of rise of on-state current (1)		Repetitive f = 50Hz	20	A/µs
			Non Repetitive	100	
T_{stg} T_j	Storage Temperature Junction Temperature Range			- 40 + 125 - 10 + 125	°C

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) T_j = 125°C

THERMAL RESISTANCES

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient		60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	AVS08CB	5.4	°C/W
		AVS08CBI	6.3	
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz)	AVS08CB	4.0	°C/W
		AVS08CBI	4.7	

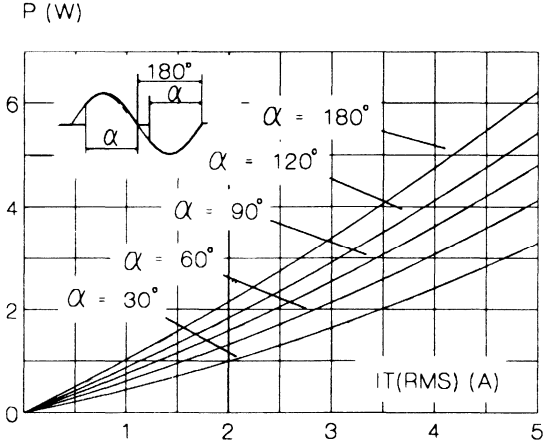
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS08CB / AVS08CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{TM} *	I_{TM} = 7A t_p = 10ms	T_j = 25°C		1.65	V
I_{DRM} *	V_{DRM} rated Gate open	T_j = 25°C		10	µA

* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 :Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).



A90AVS08-03

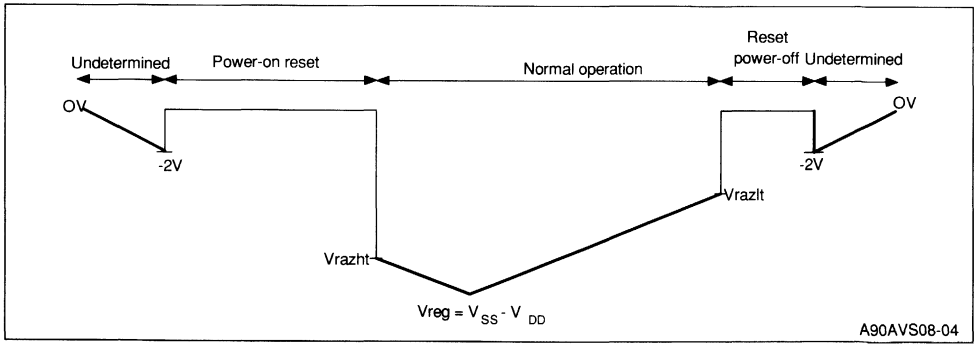
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1BCP08 T_{oper} = 25°C (unless otherwise specified)

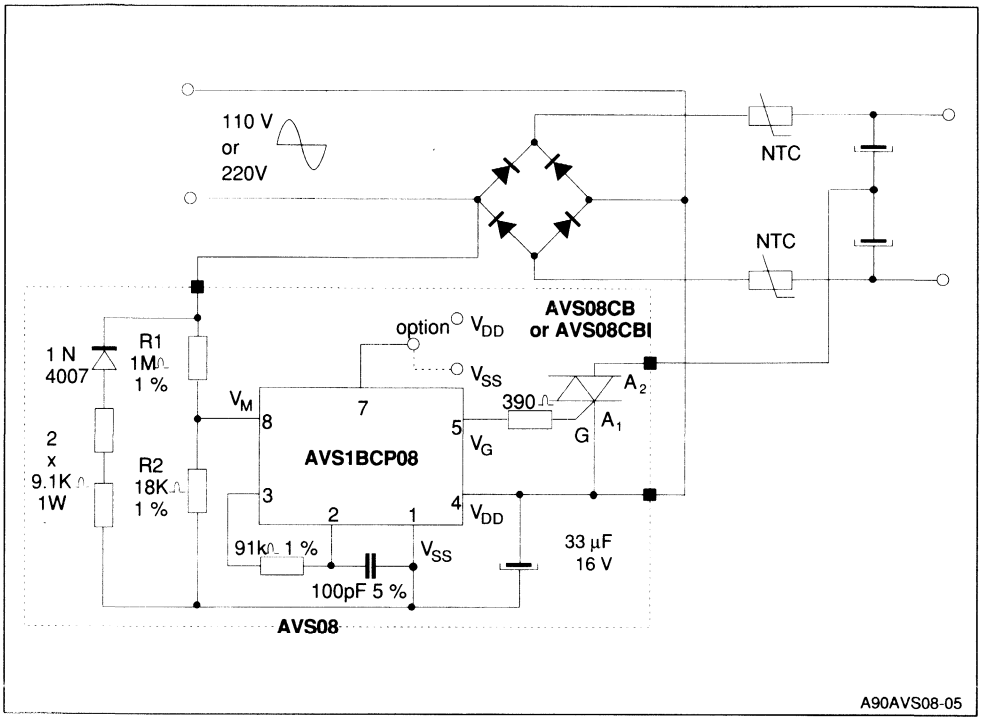
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		25	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			1	mA
F (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	KHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			1 + 50	V µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) : Voltage referred to V_{DD}

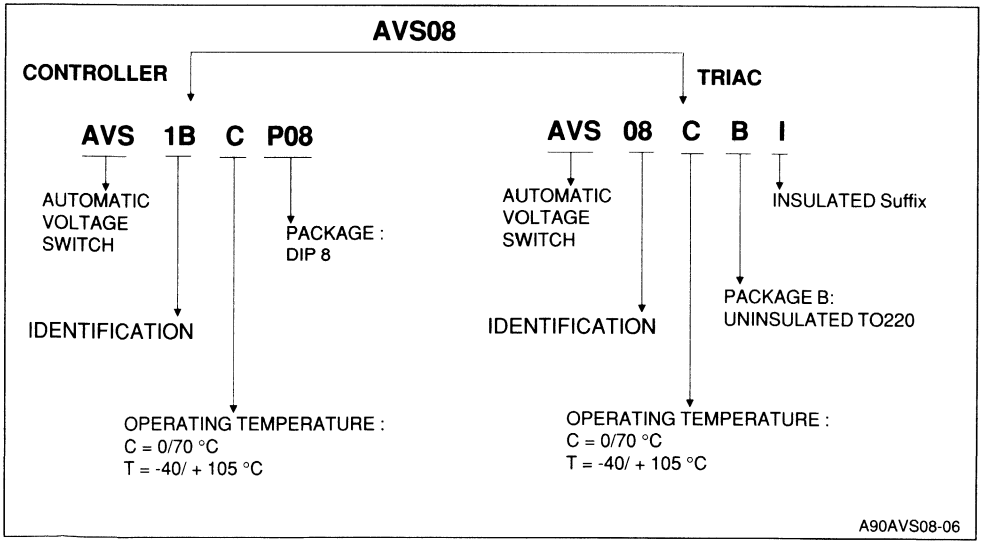
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



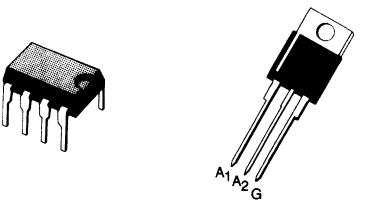
AUTOMATIC VOLTAGE SWITCH (SMPS < 300W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS10CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS10CBI
- V_{DRM} = ± 600V
- $I_{T(RMS)}$: 8A



P
MINIDIP

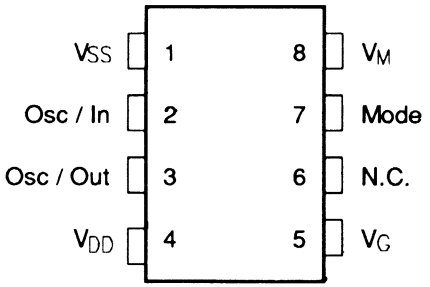
B
TO220AB
(Plastic)

DESCRIPTION

The AVS10 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 300 W. It is composed of 2 devices :

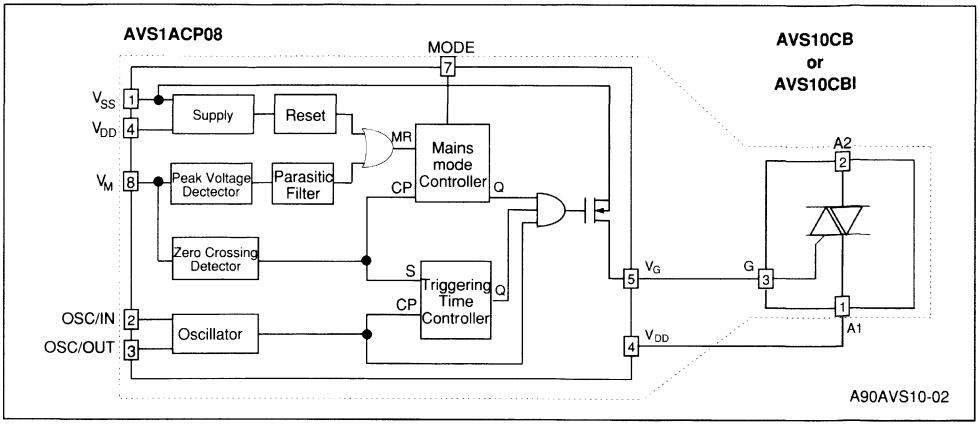
- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage is restored to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



A90AVS10-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS10CB / AVS10CBI T_j = +25°C (unless otherwise specified)

Symbol	Parameter			Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)			± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	AVS10CB	T_C = 80°C	8	A
		AVS10CBI	T_C = 70°C		
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)		t = 8.3ms t = 10ms	85 80	A
I^2t	I^2t value		t = 10ms	32	A^2s
di/dt	Critical rate of rise of on-state current (1)		Repetitive f = 50Hz	20	A/µs
			Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open		T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature			- 40 + 150 0 + 110	°C

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) Tj = 110°C

* For either polarity of electrode A_2 voltage with reference to electrode A_1

THERMAL RESISTANCES

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient		60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	AVS10CB	3.5	°C/W
		AVS10CBI	4.4	
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz)	AVS10CB	2.6	°C/W
		AVS10CBI	3.3	

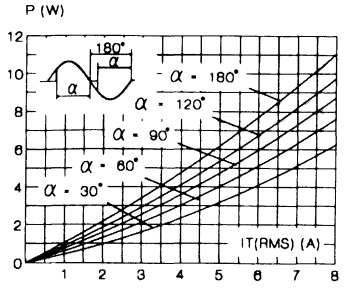
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS10CB / AVS10CBI

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	T_j = 110°C	0.2		V
V_{TM} *	I_{TM} = 11A t_p = 10ms	T_j = 25°C		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	T_j = 25°C		10	µA
		T_j = 110°C		500	

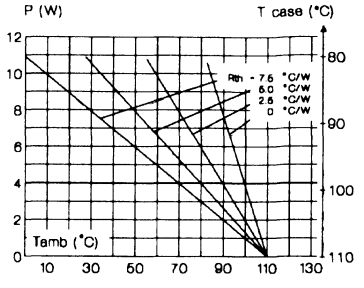
* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 : Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).

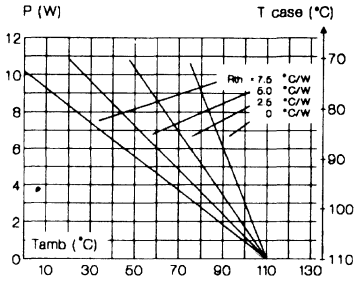


A90AVS10-03

Figure 2 : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heatsink + contact (AVS10CB).

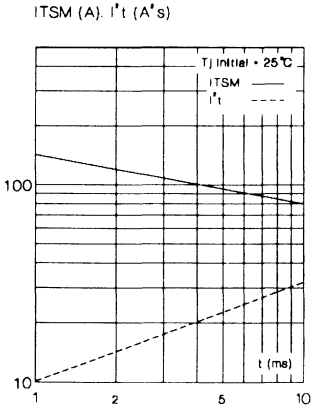


AVS10CB A90AVS10-04



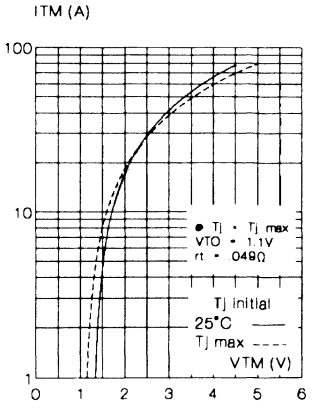
AVS10CBI A90AVS10-05

Figure 3 : Non repetitive surge peak on-state current for a sinusoidal pulse with width : $t \leq 10ms$, and corresponding value of I^2t.



A90AVS10-06

Figure 4 : On-state characteristics (maximum values).



A90AVS10-07

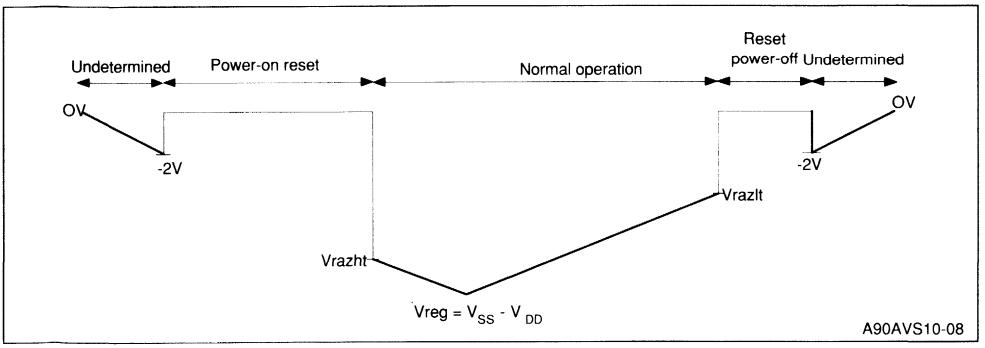
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

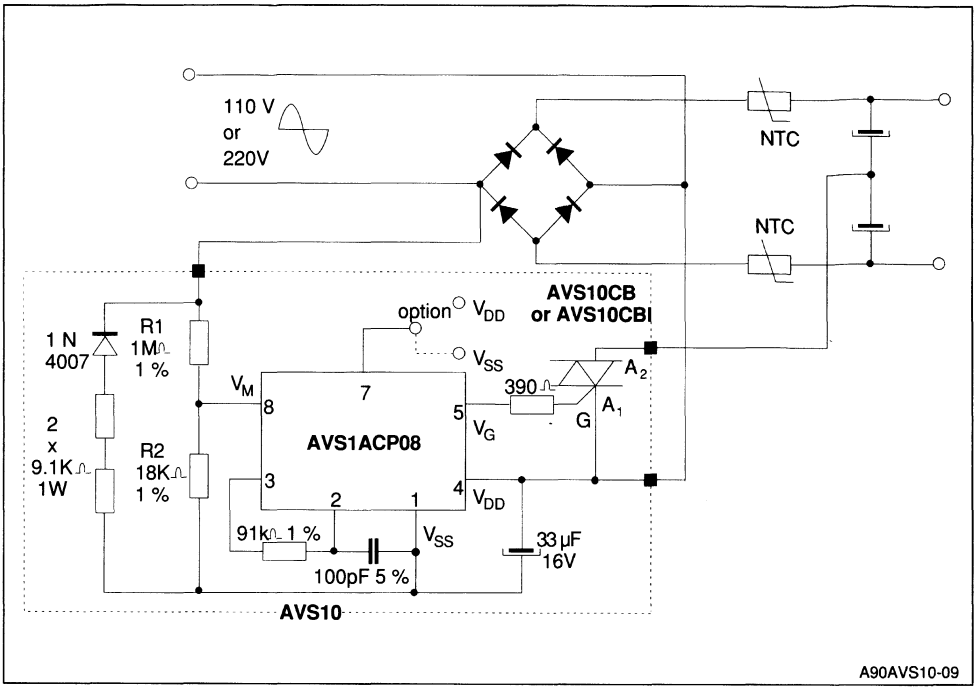
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detectionof 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) : Voltage referred to V_{DD}

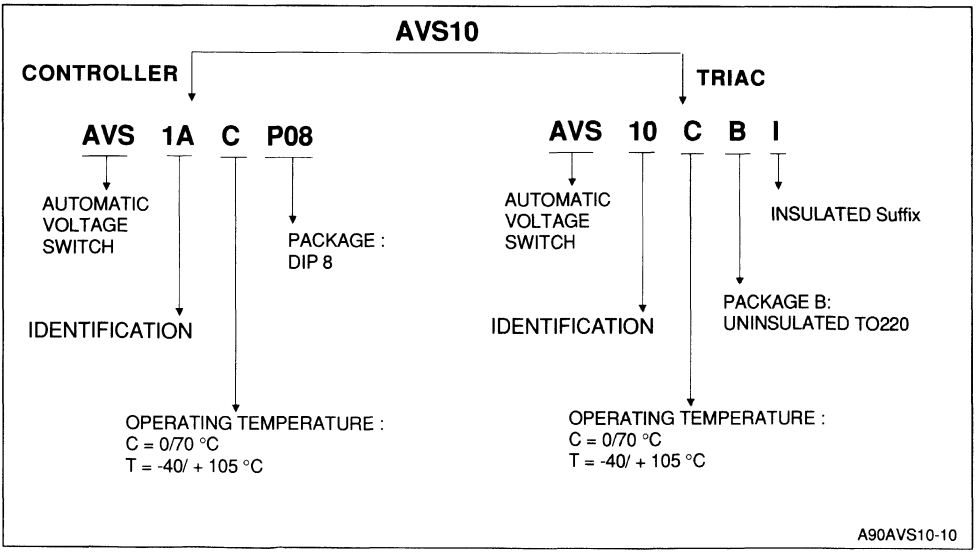
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



SGS-THOMSON MICROELECTRONICS

AVS12

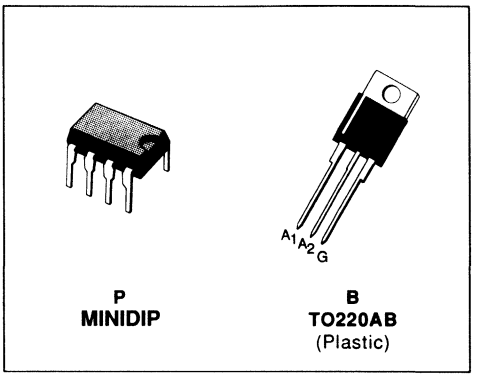
AUTOMATIC VOLTAGE SWITCH (SMPS < 500W)

CONTROLLER

- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIGGERING PULSE TRAIN OF THE TRIAC
- PARASITIC FILTER
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS12CB
- $V_{DRM} = \pm 600V$
- $I_{T(RMS)}$: 12A



P
MINIDIP

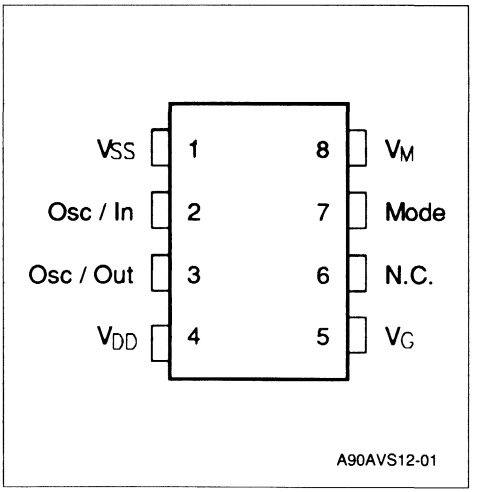
B
TO220AB
(Plastic)

DESCRIPTION

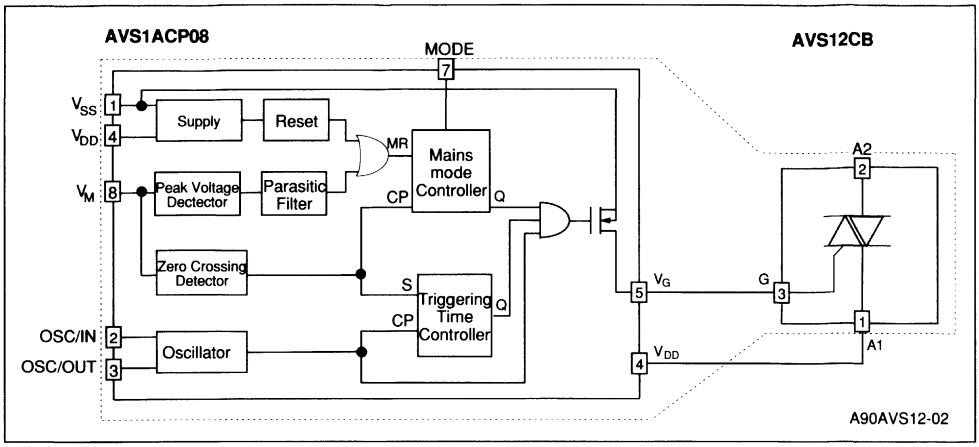
The AVS12 kit is an automatic mains selector (110/220V AC) to be used in SMPS < 500 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option**. If the main power drops from 220V to 110V, the triac control remains locked to the 220V mode and avoids any high voltage spike when the voltage comes back to 220V.
  When connected to V_{DD}, the **mode** input desactivates this **option**.
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against disturbances.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS1ACP08

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C " " T "	0 - 40	+ 70 + 105	°C

TRIAC AVS12CB T_j = 25°C (unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2)		± 600	V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle)	T_C = 70°C	12	A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C)	t = 8.3ms t = 10ms	105 100	A
I^2t	I^2t value	t = 10ms	50	A^2s
di/dt	Critical rate of rise of on-state current (1)	Repetitive f = 50Hz	20	A/µs
		Non Repetitive	100	
dv/dt *	Linear slope up to 0.67 V_{DRM} Gate open	T_j = 110°C	50	V/µs
T_{stg} T_j	Storage Temperature Operating Junction Temperature		- 40 + 150 0 + 110	°C

(1) Gate supply : I_G =100mA – di/dt = 1A/µs
(2) Tj = 110°C

* For either polarity of electrode A_2 voltage with reference to electrode A_1

THERMAL RESISTANCES

TRIAC AVS12CB

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient	60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC	3	°C/W
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f= 50Hz)	2.3	°C/W

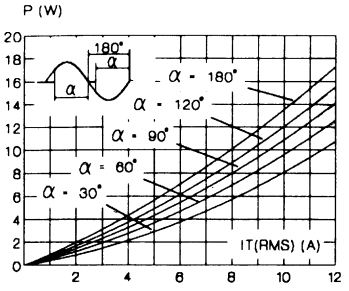
DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS12CB

Symbol	Parameter		Value		Unit
			Min.	Max.	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs	$T_j = 110°C$	0.2		V
V_{TM} *	$I_{TM} = 17A$ tp = 10ms	$T_j = 25°C$		1.75	V
I_{DRM} *	V_{DRM} rated Gate open	$T_j = 25°C$		10	µA
		$T_j = 110°C$		500	

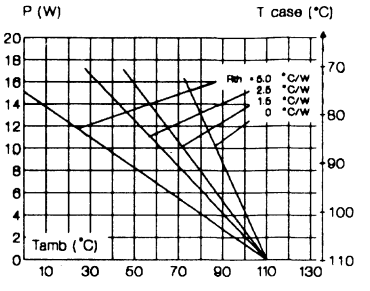
* For either polarity of electrode A_2 voltage with reference to electrode A_1.

Figure 1 : Maximum RMS power dissipation versus RMS on-state current (f = 60Hz).



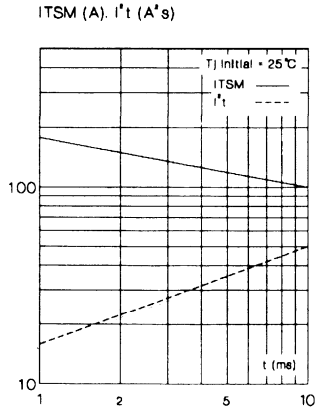
A90AVS12-03

Figure 2 : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heatsink + contact.



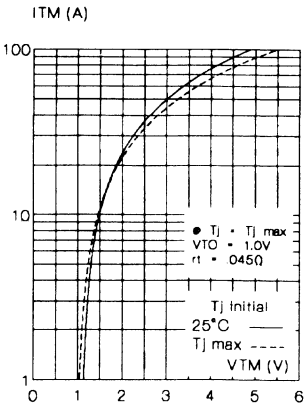
A90AVS12-04

Figure 3 : Non repetitive surge peak on state current for a sinusoidal pulse with width : $t \leq 10ms$, and corresponding value of I^2t.



A90AVS12-05

Figure 4 : On-state characteristics (maximum values).



A90AVS12-06

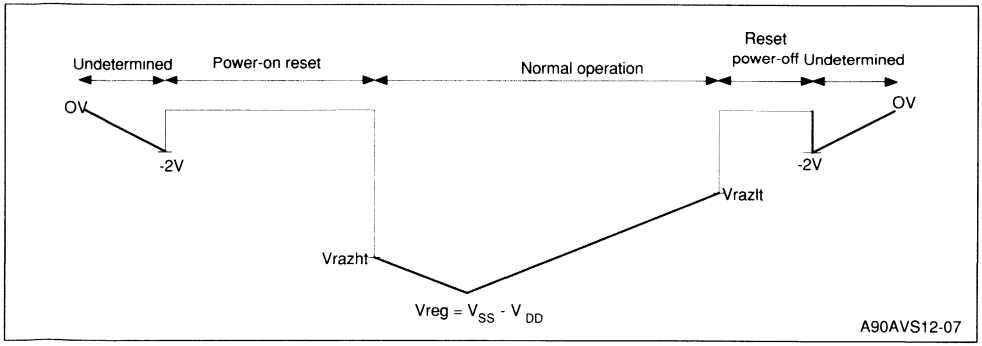
DC GENERAL ELECTRICAL CHARACTERISTICS (continued)

CONTROLLER AVS1ACP08 T_{oper} = 25°C (unless otherwise specified)

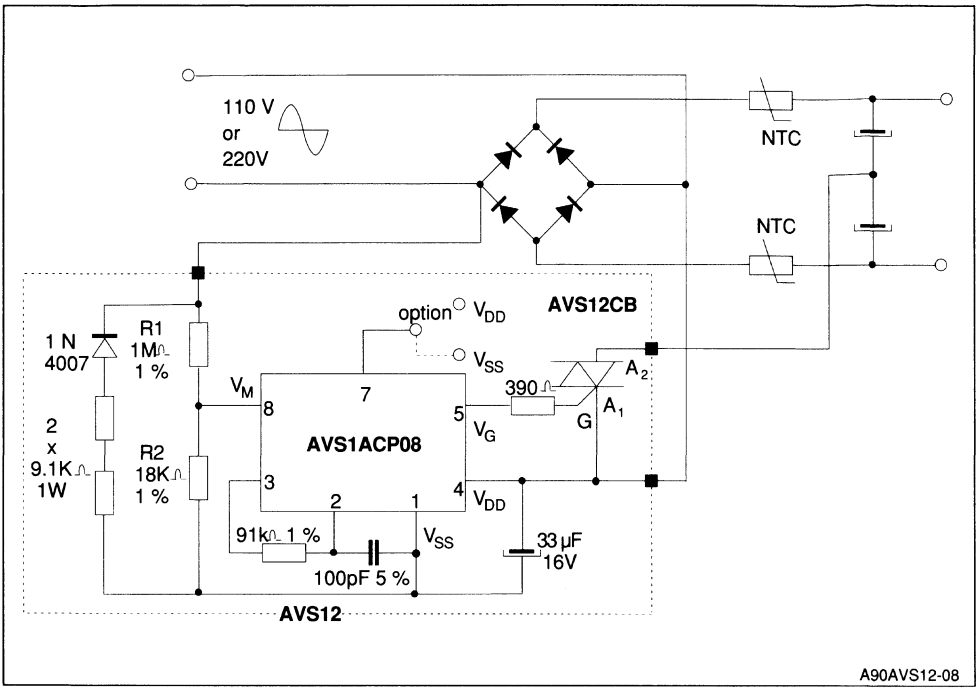
Symbol	Parameter	Value			Unit
		Min	Typ	Max	
V_{SS} (pin 1) (Vreg)	Shunt regulator	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = 9V)	Supply current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent current			0.7	mA
f (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator frequency	42	44	46	kHz
V_M (pin 8) Vth (3)	Peak voltage of detection high-threshold	4.08	4.25	4.42	V
V_M (pin 8) Vh (3)	Peak voltage of detection hysteresis	0.370	0.4	0.420	V
(1) V_M (pin 8) Vth (3)	Zero-crossing detection high-threshold	95	110	125	mV
V_M (pin 8) Vh (3)	Zero-crossing detection hysteresis	20	30	40	mV
(2) Vrazht (4)	Power-on-reset activation threshold		Vreg x 0.89		
(2) Vrazlt (4)	Power-down-reset activation threshold		Vreg x 0.55		
Mode (pin 7)	V_{IL} (4) V_{IH} (4)	0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage current (V_G = V_{DD})			650 + 10	mV µA

NOTES :
(1) : This value gives a typical noise immunity on the zero-crossing detection of 110mV x 1018/18 = 6.20V on the main supply
(2) : See following diagram
(3) : Voltage referred to V_{SS}
(4) : Voltage referred to V_{DD}

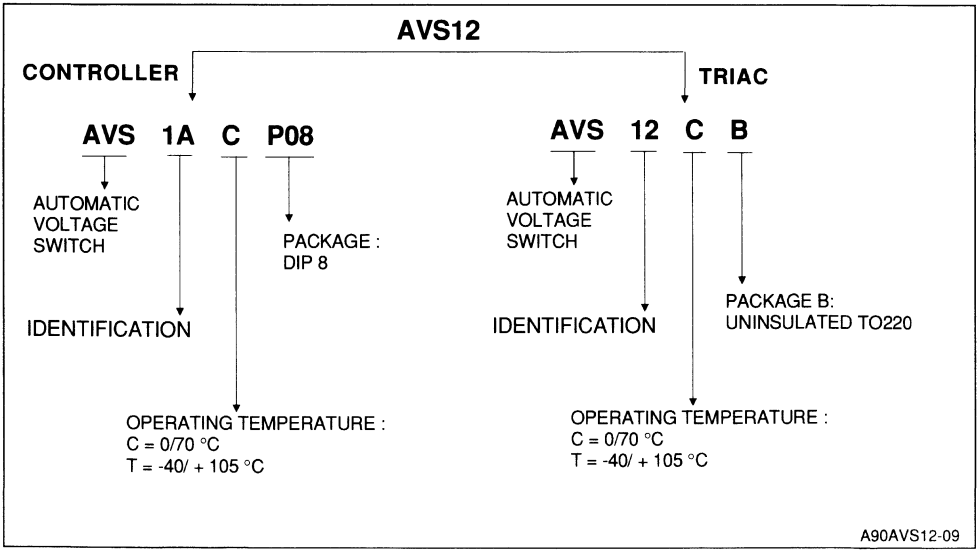
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION



ORDERING INFORMATION



SGS-THOMSON MICROELECTRONICS

AVS20
AVS200

AUTOMATIC VOLTAGE SWITCH (SMPS < 300W)

CONTROLLER

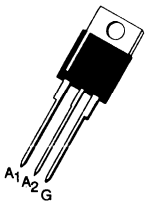
- 50/60Hz FULL COMPATIBILITY
- INTEGRATED VOLTAGE REGULATOR
- TRIAC TRIGGERING BY PULSE TRAIN
- HIGH IMMUNITY TO AC DISTURBANCES (SPIKES, MISSING CYCLE)
- HIGH RELIABILITY ON LINE VOLTAGE DETECTION (PARASITIC FILTER ON SIGNAL INPUT)
- FAST DIGITAL START-UP TIME (< 2 LINE CYCLES)
- LOW POWER CONSUMPTION

TRIAC

- HIGH EFFICIENCY AND SAFETY SWITCHING
- UNINSULATED PACKAGE : AVS10CB/AVS100CB
- INSULATED PACKAGE (2500V_{RMS}) : AVS10CBI
- V_{DRM} = ±600V (AVS10CB), ±800V (AVS100CB)
- $I_{T(RMS)}$: 8A

P
DIP8
(Plastic Package)

ORDER CODE : AVS2ACP08



B
TO220AB
(Plastic Package)

ORDER CODES : AVS10CB-AVS10CBI-AVS100CB

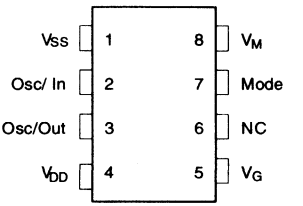
DESCRIPTION

The AVS20 (AVS200) kit is an automatic mains selector (120/230V AC) to be used in SMPS with input power < 300 W. It is composed of 2 devices :

- The **Controller** is optimized for low consumption and high security triggering of the triac. When connected to V_{SS}, the **mode** input activates an additional **option** "the **latched** option". If the main power drops from 230V to 120V, the triac control remains locked to the 230V mode and avoids any high voltage spike when the voltage is restored to 230V.
  When connected to V_{DD}, the **mode** input desactivates this **option** "this is the **follower** option".
- The TRIAC is specially designed for this application. An optimization between sensitivity and dynamic parameters of the triac gate highly reduces the losses of supply resistor and allows excellent immunity against line disturbances.

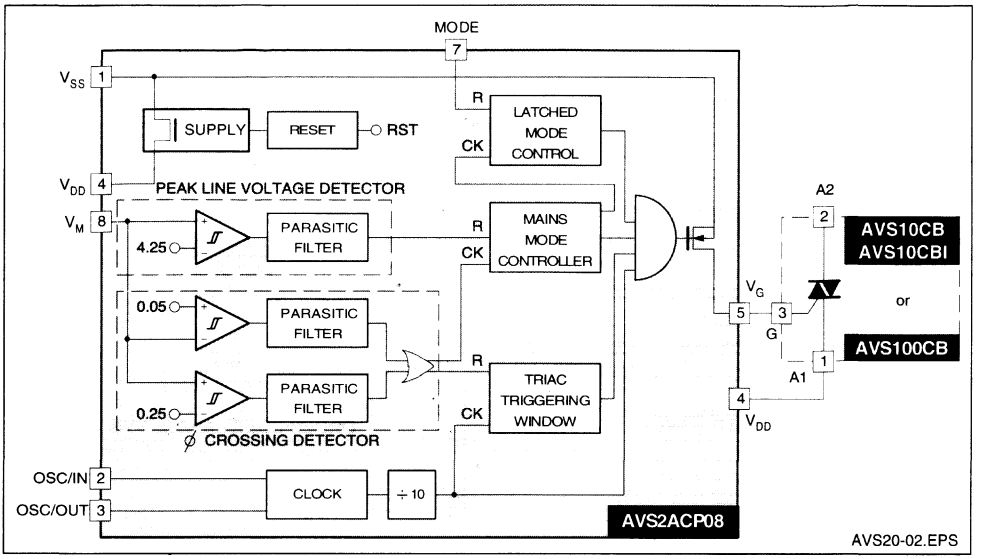
PIN CONNECTIONS

DIP8



AVS20-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CONTROLLER AVS2ACP08

Symbol	Parameter	Min.	Max.	Unit
V_{SS}	Supply voltage	- 12	0.5	V
V_I / V_O	I / O voltage	V_{SS} - 0.5	0.5	V
I_I / I_O	I / O current	- 40	+ 40	mA
T_{stg}	Storage Temperature	- 60	+ 150	°C
T_{oper}	Operating Temperature code " C "	0	+ 70	°C

AVS20-01.TBL

TRIAC AVS10CB / AVS10CBI / AVS100CB T_j = +25°C (unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DRM}	Repetitive peak off-state voltage (2) AVS10 AVS100	 ±600 ±800	 V V
$I_{T(RMS)}$	RMS on-state current (360° conduction angle) T_C = 80°C, AVS10CB/AVS100CB T_C = 70°C, AVS10CBI	 8 8	 A A
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25°C) t = 8.3ms t = 10ms	 85 80	 A A
I^2t	I^2t value (t = 10ms)	32	A^2s
di/dt	Critical rate of rise of on-state current (1) Repetitive f = 50Hz Non Repetitive	 20 100	 A/µs A/µs
dv/dt (3)	Linear slope up to 400V (Gate open) (T_j = 70°C) AVS10 AVS100	 75 150	 V/µs V/µs
T_{stg}	Storage Temperature	-40, +150	°C
T_j	Operating Junction Temperature	0, +110	°C

AVS20-02.TBL

(1) Gate supply : I_G = 100mA – di/dt = 1A/µs
(2) T_j = 110°C
(3) For either polarity of electrode A_2 voltage with reference to electrode A_1

THERMAL RESISTANCES

TRIAC AVS10CB / AVS10CBI / AVS100CB

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction-to-ambient	60	°C/W
$R_{th\ (j-c)}$ DC	Junction-to-case for DC AVS10CB / AVS100CB AVS10CBI	 3.5 4.4	 °C/W °C/W
$R_{th\ (j-c)}$ AC	Junction-to-case for 360° conduction angle (f = 50Hz) AVS10CB / AVS100CB AVS10CBI	 2.6 3.3	 °C/W °C/W

AVS20-03.TBL

DC GENERAL ELECTRICAL CHARACTERISTICS

TRIAC AVS10CB / AVS10CBI / AVS100CB

Symbol	Parameter	Min.	Max.	Unit
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3k\Omega$ Pulse duration> 20µs (T_j = 110°C)	0.2		V
V_{TM} (1)	I_{TM} = 11A (t_p = 10ms, T_j = 25°C)		1.75	V
I_{DRM} (1)	V_{DRM} rated Gate open T_j = 25°C AVS10/AVS100 T_j = 110°C AVS10 T_j = 700°C AVS100		 10 500 500	 µA µA µA

AVS20-04.TBL

CONTROLLER AVS2ACP08 T_{oper} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
MAIN CHARACTERISTICS					
V_{SS} (pin 1) (Vreg)	Shunt Regulator Voltage	- 10	- 9	- 8	V
I_{SS} (pin 1) (Vreg) (@ V_{SS} = -9V)	Supply Current	0.4		30	mA
I_{SS} (pin 1) (@ triac gate non connected)	Quiescent Current		0.6	0.7	mA
F (pin 3) (@ R = 91kΩ) (C = 100pF)	Oscillator Frequency	42	44	46	kHz
V_{PWRON} (2)	Power-on-reset Threshold		0.89 Vreg		
V_{PWROFF} (2)	Power-off-reset Threshold		4.6		V
Mode (pin 7)	V_{IL} (2) V_{IH} (2)	 0.7 Vreg		0.3 Vreg	
V_G (pin 5)	V_{OL} (I_{VG} = 25mA) Leakage Current ($V_G = V_{DD}$)			650 + 10	mV µA
PEAK LINE VOLTAGE DETECTOR					
V_{SWON} (pin 8)	Low Threshold of Trip Point (switching-on of triac triggering) (3)	3.89	4.05	4.22	V
V_{SWOFF} (pin 8)	High Threshold of Trip Point (switching-off of triac triggering) (3)	4.08	4.25	4.42	V
t_{ON} (pin 5)	Triac Turn-on Delay Time (V_{AC} = 120V)	1		2	Line cycles
ZERO VOLTAGE CROSSING DETECTOR					
V_{0CR}PH (pin8)	High Threshold on Positive AC Side (3)		250		mV
V_{0CR}PL (pin8)	Low Threshold on Positive AC Side (3) (4)		200		mV
V_{0CR}NH (pin8)	High Threshold on Negative AC Side (3)		100		mV
V_{0CR}NL (pin8)	Low Threshold on Negative AC Side (3) (4)		60		mV

AVS20-05.TBL

NOTES :

(1) : For either polarity of electrode A_2 voltage with reference to electrode A_1.

(2) : Voltage referred to V_{DD}.

(3) : Voltage referred to V_{SS}.

(4) : These values give a typical noise immunity on the zero-crossing detection of 100mV x $\frac{1018}{18}$ = 5.65V on the mains supply.

Figure 1: Maximum RMS power dissipation versus RMS on-state current (f=60Hz) (Curves are cut-off $(di/dt)_c$ limitation)

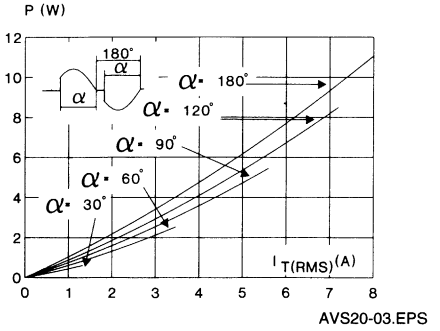


Figure 2a : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heat-sink + contact (AVS10CB/AVS100CB)

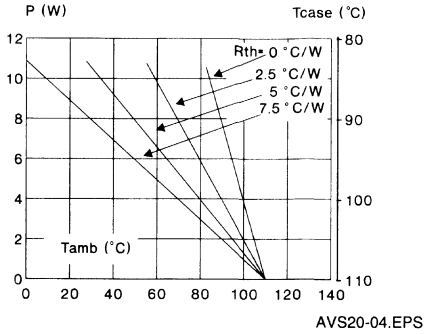
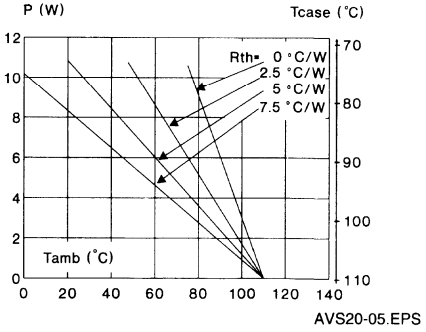


Figure 2b : Correlation between maximum mean power dissipation and maximum allowable temperatures (T_A and T_C) for different thermal resistances heat-sink + contact (AVS10CBI)



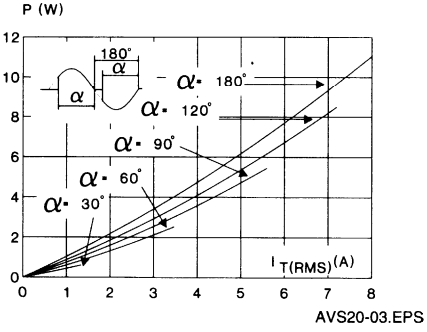


Figure 3 : Non-repetitive surge peak on-state current for a sinusoidal pulse with width : $t \leq 10ms$, and corresponding value of I^2t.

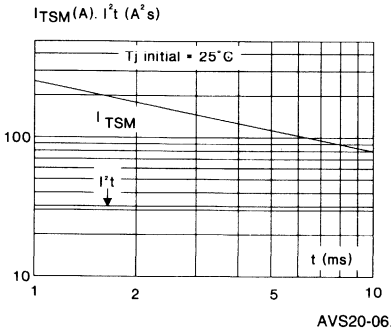
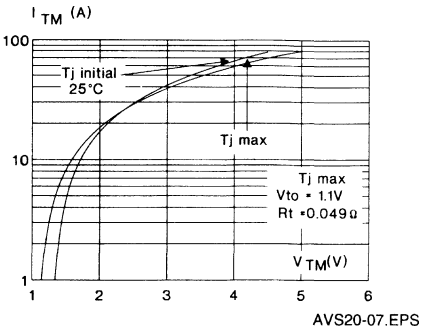
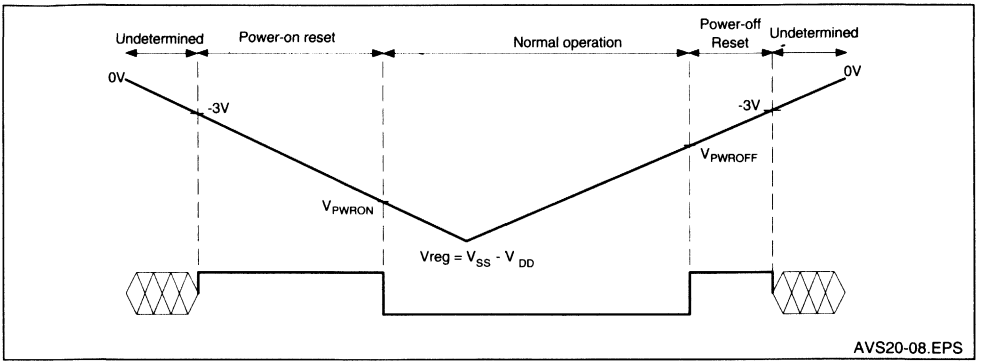


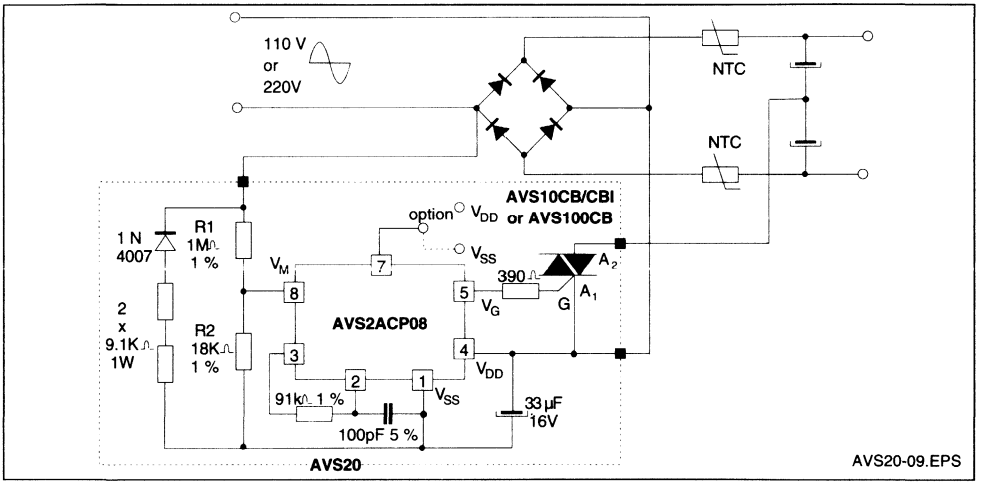
Figure 4 : On-state characteristics (maximum values).



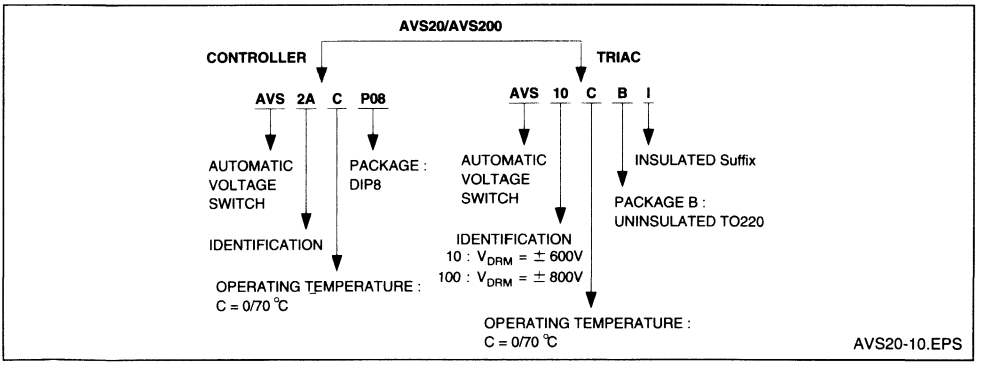
POWER-ON AND POWER-OFF RESET BEHAVIOUR



TYPICAL APPLICATION DIAGRAM

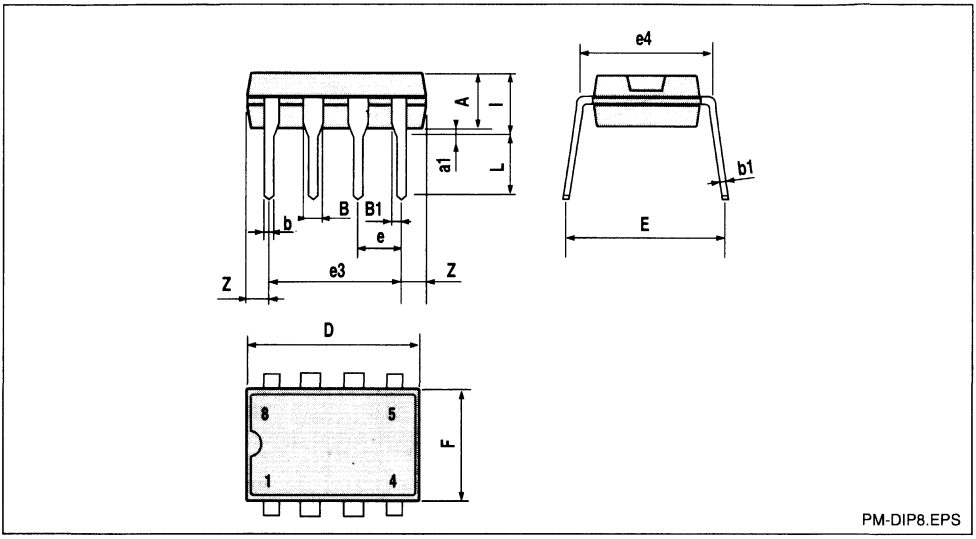


ORDERING INFORMATION



PACKAGE MECHANICAL DATA

CONTROLLER
8 PINS - PLASTIC DIP

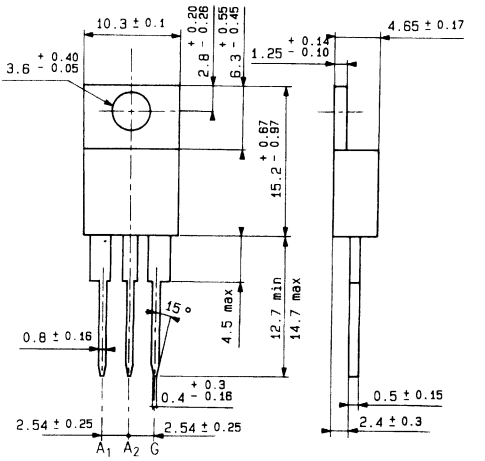


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

TRIAC
3 PINS - PLASTIC TO220AB



PM-TOTRI.IMG

Cooling method : by conduction (method C)
Weight : 2 g

LED DISPLAY DRIVERS

SGS-THOMSON MICROELECTRONICS

M5450
M5451

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

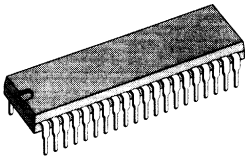
Application Examples :

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

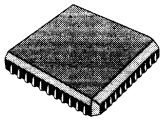
DESCRIPTION

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.



DIP40
(Plastic Package)
ORDER CODE : M5450B7 / M5451B7



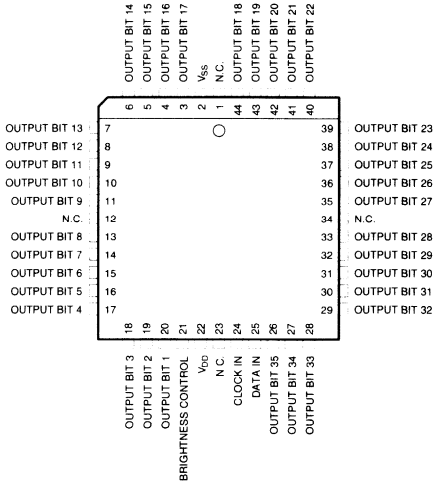
PLCC44
(Plastic Chip Carrier)
ORDER CODE : M5451Q

PIN CONNECTION

DIP40

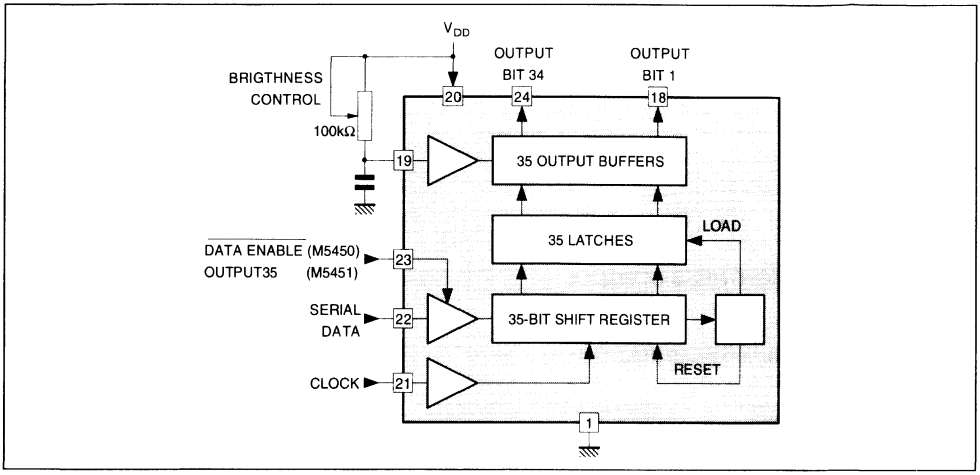
V_{SS}	1	40	OUTPUT BIT 18
OUTPUT BIT 17	2	39	OUTPUT BIT 19
OUTPUT BIT 16	3	38	OUTPUT BIT 20
OUTPUT BIT 15	4	37	OUTPUT BIT 21
OUTPUT BIT 14	5	36	OUTPUT BIT 22
OUTPUT BIT 13	6	35	OUTPUT BIT 23
OUTPUT BIT 12	7	34	OUTPUT BIT 24
OUTPUT BIT 11	8	33	OUTPUT BIT 25
OUTPUT BIT 10	9	32	OUTPUT BIT 26
OUTPUT BIT 9	10	31	OUTPUT BIT 27
OUTPUT BIT 8	11	30	OUTPUT BIT 28
OUTPUT BIT 7	12	29	OUTPUT BIT 29
OUTPUT BIT 6	13	28	OUTPUT BIT 30
OUTPUT BIT 5	14	27	OUTPUT BIT 31
OUTPUT BIT 4	15	26	OUTPUT BIT 32
OUTPUT BIT 3	16	25	OUTPUT BIT 33
OUTPUT BIT 2	17	24	OUTPUT BIT 34
OUTPUT BIT 1	18	23	DATA ENABLE FOR M5450 OUTPUT BIT 35 FOR M5451
BRIGHTNESS CONTROL	19	22	DATA IN
V_{DD}	20	21	CLOCK IN

PLCC44



5450-01.EPS - 5450-02.EPS

BLOCK DIAGRAM (Figure 1)



5450-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 15	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Output Voltage	15	V
I_O	Output Sink Current	40	mA
P_{tot}	Total Package Power Dissipation at 25°C at 85°C	1 560	W mW
T_j	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	– 25 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

5450-01.TBL

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specially designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current LED displays.

A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in figure 1. For the M5450 a DATA ENABLE is used instead of the 35th output. The DATA ENABLE input is a metal option for the M5450.
The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.
Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationship between Data, Clock and DATA ENABLE.

A max clock frequency of 0.5MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.
$T_j = [(V_{OUT})(I_{LED})(\text{No. of segments}) + (V_{DD} \cdot 7mA)](124°C/W) + T_{amb}$

where :
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
124°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	- 0.3 2.2 V_{DD} - 2		0.8 V_{DD} V_{DD}	V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input Current = 750µA, T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0µA Brightness In. = 100µA Brightness In. = 750µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

5450-02.TBL

Notes :
1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40mA.
4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

Figure 2 : Input Data Format

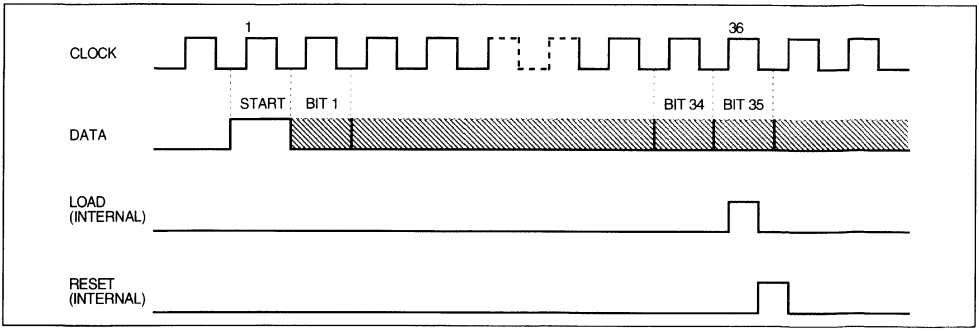


Figure 3

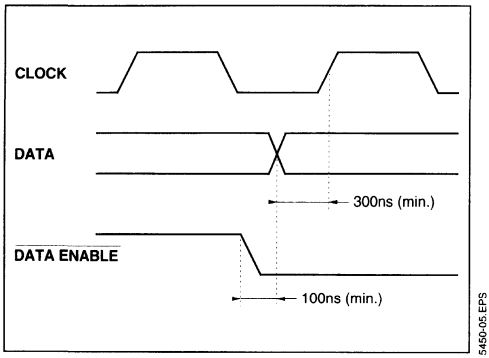


Figure 4

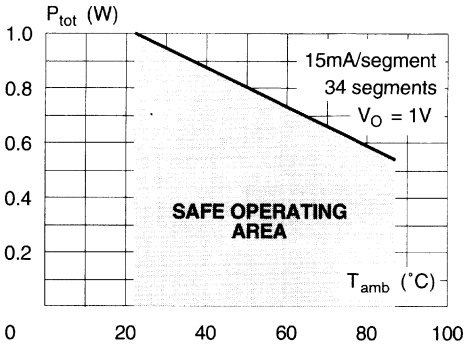


Figure 5

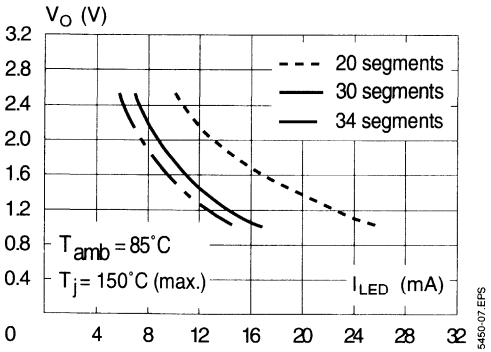
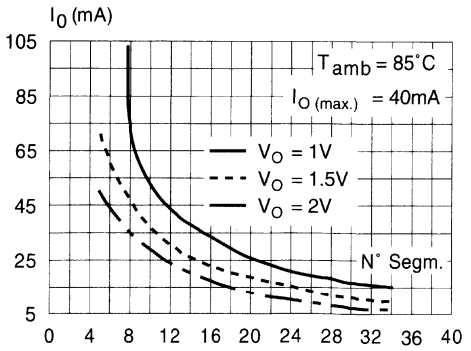
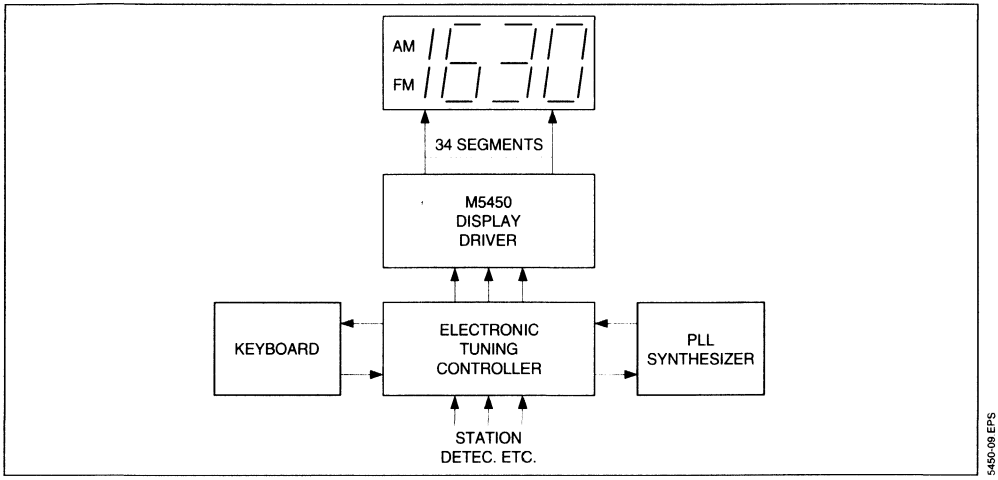


Figure 6

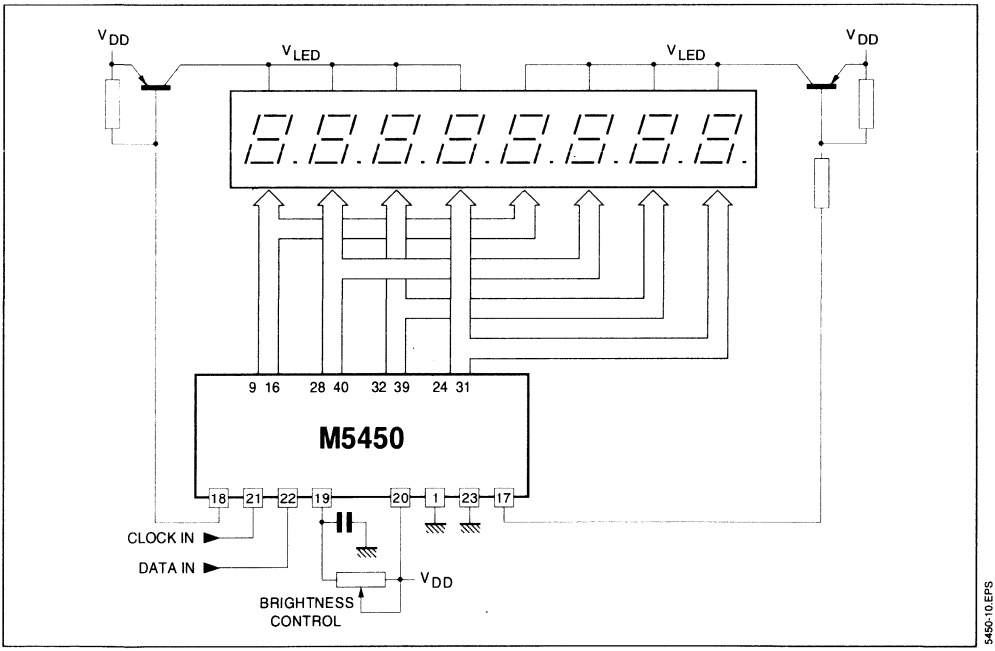


TYPICAL APPLICATIONS

BASIC ELECTRONICALLY TUNED RADIO OR TV SYSTEM



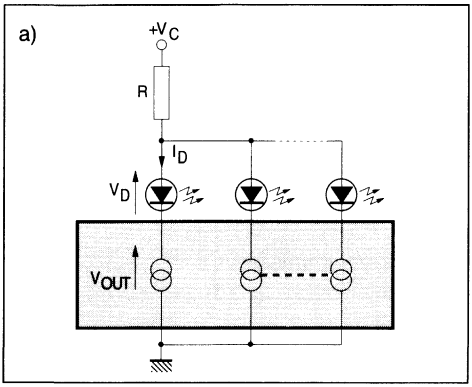
DUPLEXING 8 DIGITS WITH ONE M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a) In the application R must be chosen taking into account the worst operating conditions.



R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

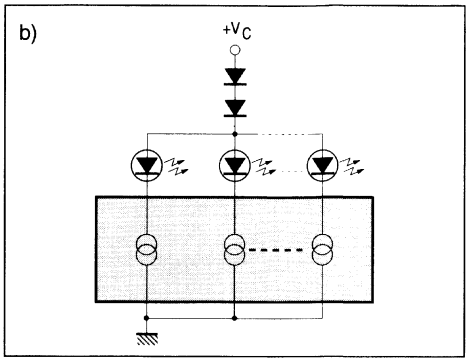
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

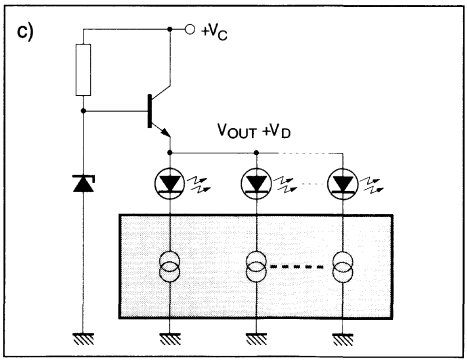
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b) In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.



c) In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



SGS-THOMSON MICROELECTRONICS

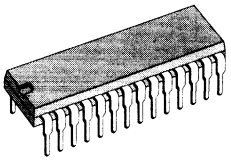
M5480

LED DISPLAY DRIVER

- 3 1/2 DIGIT LED DRIVER (23 segments)
- CURRENT GENERATOR OUTPUTS (no resistors required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS



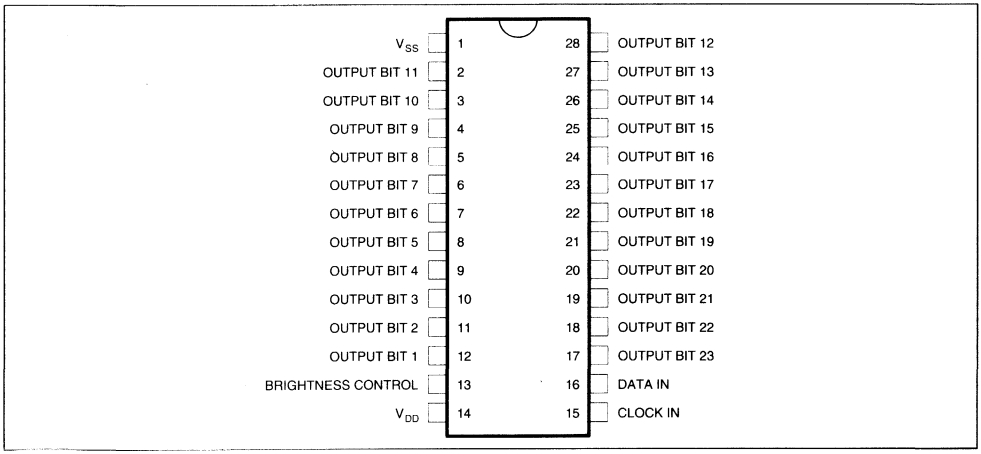
DIP-28
(Plastic Package)

ORDER CODE : M5480B7

DESCRIPTION

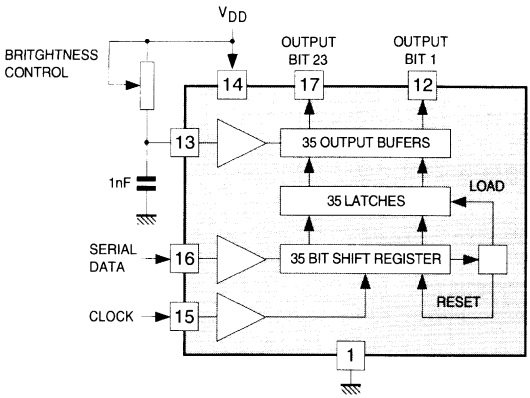
The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3 1/2 digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.
The M5480 is a pin-to-pin replacement of the NS MM 5480.

PIN CONNECTIONS



5480-01.EPS

BLOCK DIAGRAM (Figure 1)



5480-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 to 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	940 490	mW mW
T_j	Junction Temperature		150	°C
T_{oper}	Operating Temperature Range		– 25, + 85	°C
T_{stg}	Storage Temperature Range		– 65, + 150	°C

5480-01.TBL

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	– 0.3 2.2 V_{DD} – 2		0.8 V_{DD} V_{DD}	V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750µA, T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Output Voltage			13.2	18	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

5480-02.TBL

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate 3 1/2 digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

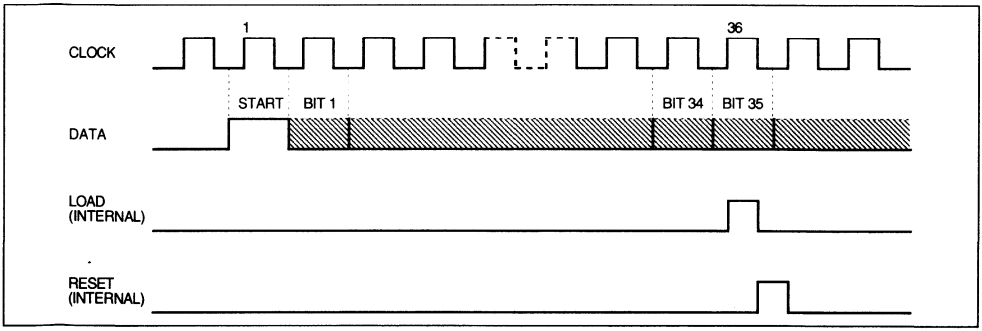
A block diagram is shown in Figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.

There is an internal limiting resistor of 400 Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

Figure 2 : Input Data Format



5480-03.EPS

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5MHz is assumed.

Figure 4 shows the Output Data Format for the M5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

$T_j = [(V_{OUT}) (I_{LED}) (\text{No.of segments}) + V_{DD} . 7 \text{ mA}] (132 \text{ °C/W}) + T_{amb}$

where:
T_j = junction temperature (150 °C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
132 °C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Figure 3

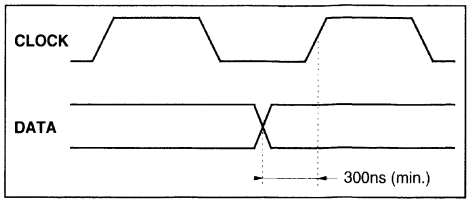


Figure 4 : Serial Data Bus / Outputs Correspondance

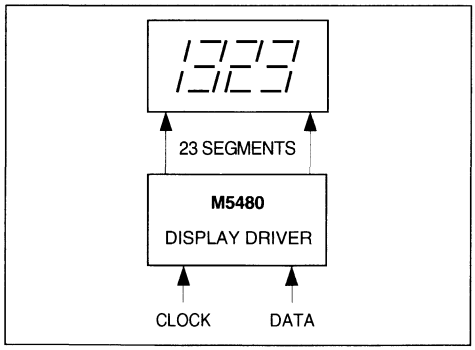
5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	START

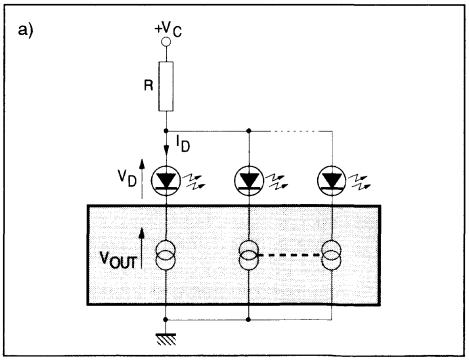
5451	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

5480-03.TBL

TYPICAL APPLICATION

BASIC 3 1/2 Digit Interface.





In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{OUT\,MIN}}{N_{MAX} \cdot I_D}$$

POWER DISSIPATION OF THE IC

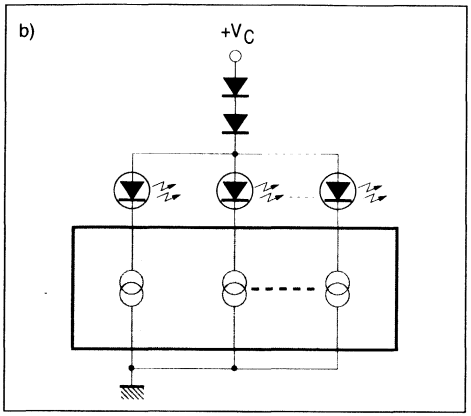
The power dissipation of the IC can be limited using different configurations.

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

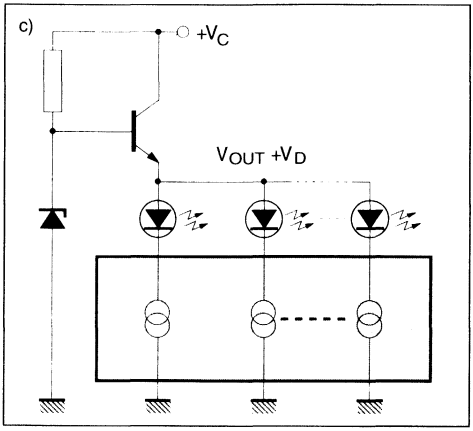
In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.



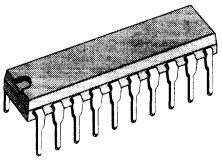
In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (14 segments)
- CURRENT GENERATOR OUTPUTS (no resistor required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications Examples

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS



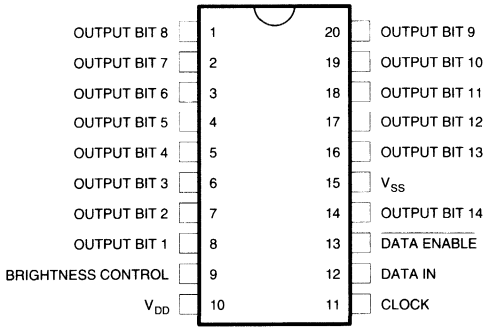
DIP20
(Plastic Package)

ORDER CODE : M5481B7

DESCRIPTION

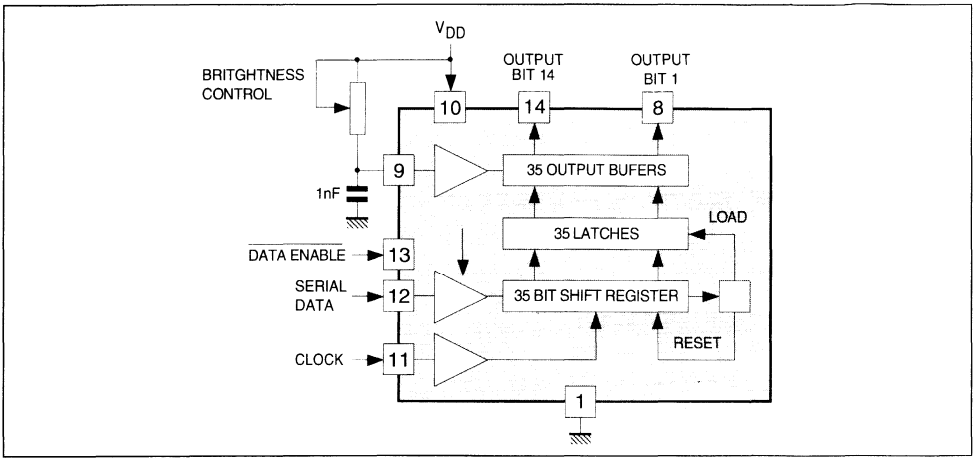
The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit dispaly. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.
The M5481 is a pin-to-pin replacement of the NS MM 5481.

PIN CONNECTIONS



5481-01.EPS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 to 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	1.5 800	W mW
T_j	Junction Temperature		150	°C
T_{oper}	Operating Temperature Range		– 25, + 85	°C
T_{stg}	Storage Temperature Range		– 65, + 150	°C

5481-01.TBL

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 – 0.3 2.2 V_{DD} – 2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

5481-02.TBL

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

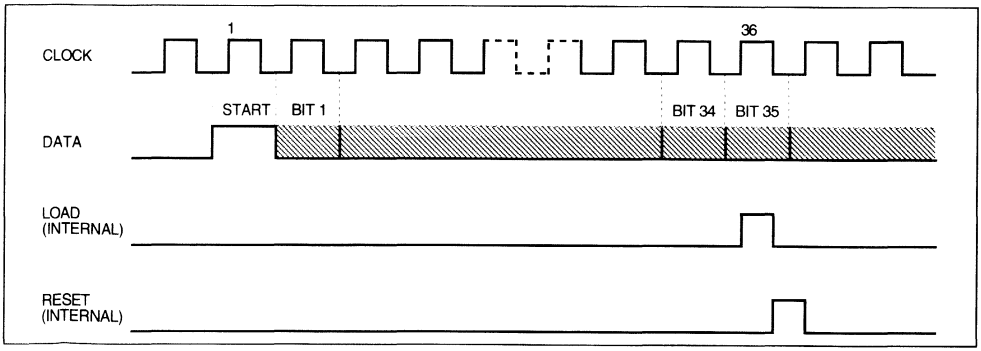
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

These is an internal limiting resistor of 400 Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

Figure 2 : Input Data Format



5481-03.EPS

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and DATA ENABLE.

A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.
$Tj \equiv [(V_{OUT})(I_{LED})(\text{No. of segments}) + V_{DD} . 7\ mA] (80\ °C/W) + T_{amb}$

where:
T_j = junction temperature (150 °C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80 °C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Figure 3

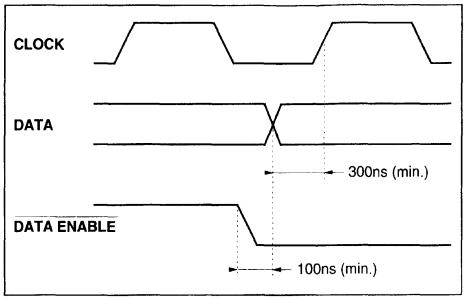


Figure 4 : Serial Bus / Outputs Correspondance

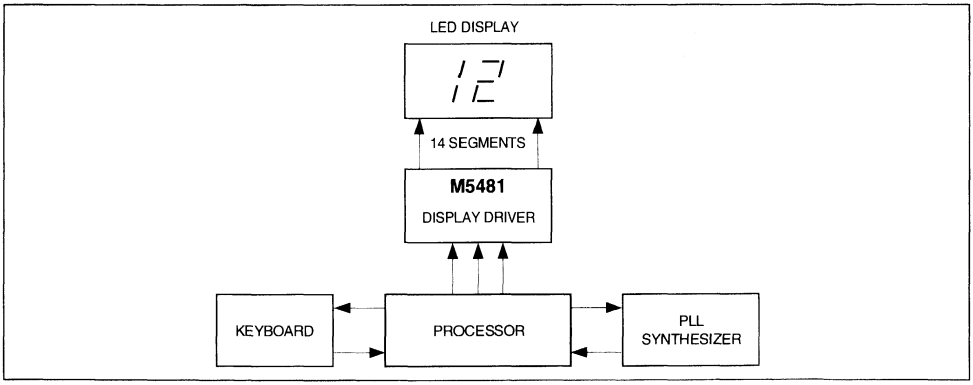
5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	START

5450	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

5481-03.TBL

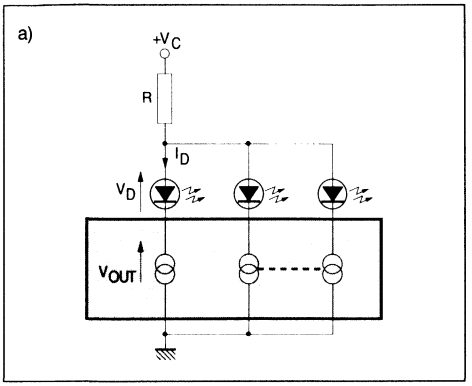
TYPICAL APPLICATION

BASIC electronically tuned TV system.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.



In this application R must be chosen taking into account the worst operating conditions.

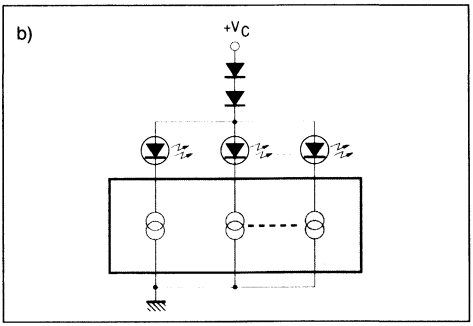
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

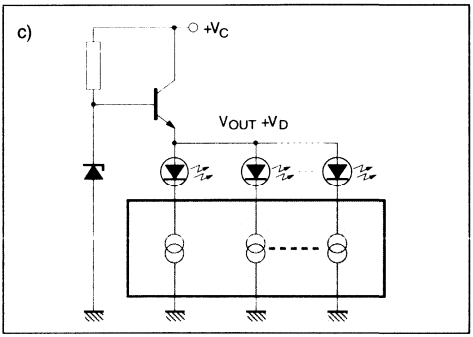
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

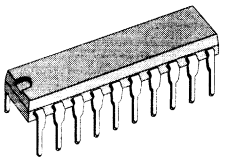
M5482

LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 segments)
- CURRENT GENERATOR OUTPUTS (no resistor required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application Examples

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS



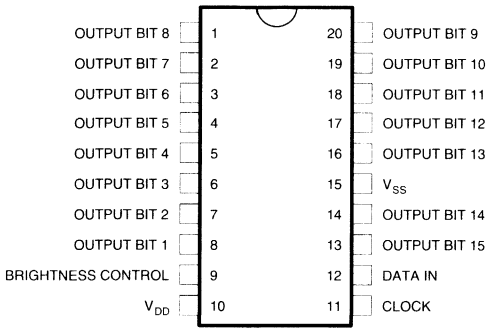
DIP20
(Plastic Package)

ORDER CODE : M5482B7

DESCRIPTION

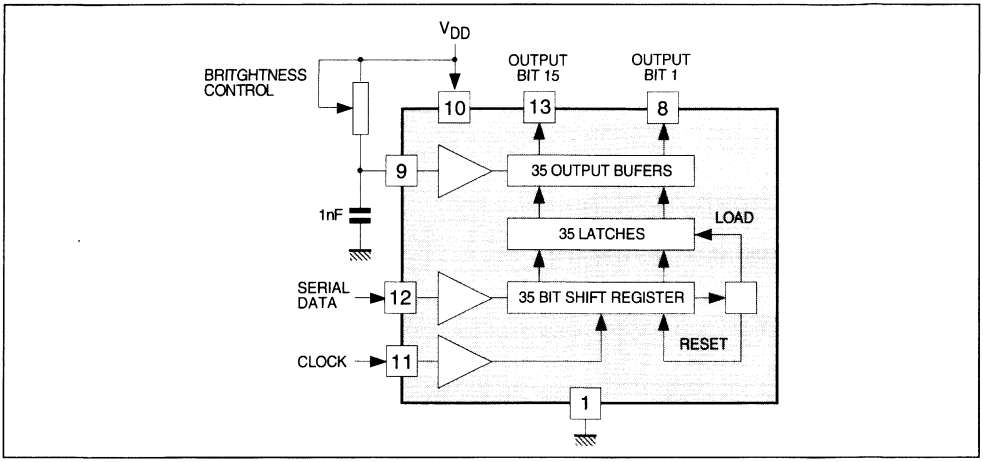
The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5451 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2 V maximum.

PIN CONNECTIONS



5482-01.EPS

BLOCK DIAGRAM



5482-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 to 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	1.5 800	W mW
T_j	Junction Temperature		150	°C
T_{oper}	Operating Temperature Range		– 25, + 85	°C
T_{stg}	Storage Temperature Range		– 65, + 150	°C

5482-01.TBL

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STATIC ELECTRICAL CHARACTERISTICS

(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	 ± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 – 0.3 2.2 V_{DD} – 2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

5482-02.TBL

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

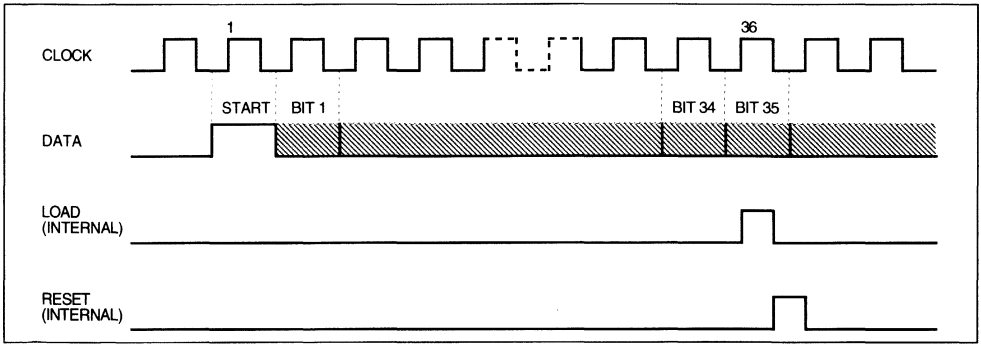
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

Figure 2 : Input Data Format



5482-03.EPS

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.

A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

$T_j \equiv [(V_{OUT})(I_{LED})(\text{no.of segments}) + V_{DD} \cdot 7\ mA]$ (80 °C/W) + T_{amb}

where :

T_j = junction temperature (150 °C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

80 °C/W = thermal coefficient of the package

T_{amb} = ambient temperature

Figure 3

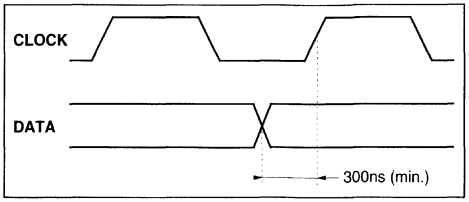


Figure 4 : Serial Data Bus / Outputs Correspondance

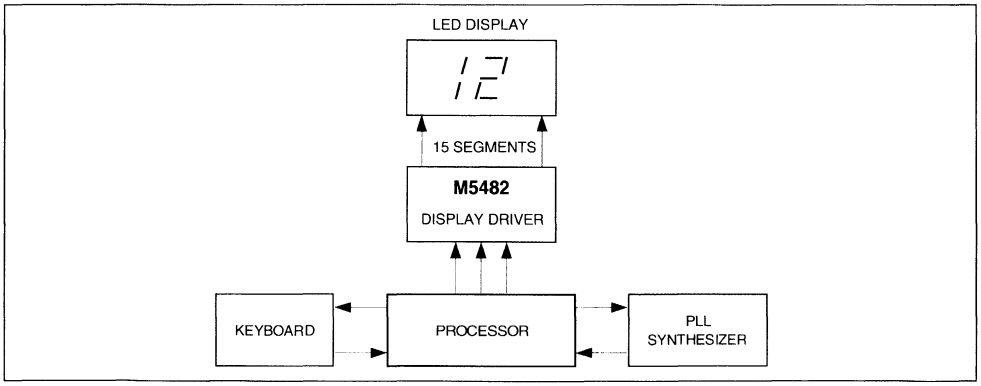
5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	START

5451	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		START
5482	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X		START

5482-03.TBL

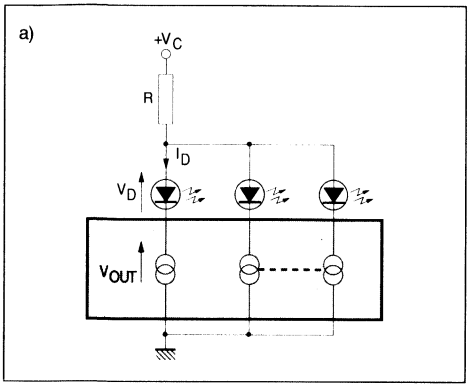
TYPICAL APPLICATION

BASIC electronically tuned TV system.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.



In this application R must be chosen taking into account the worst operating conditions.

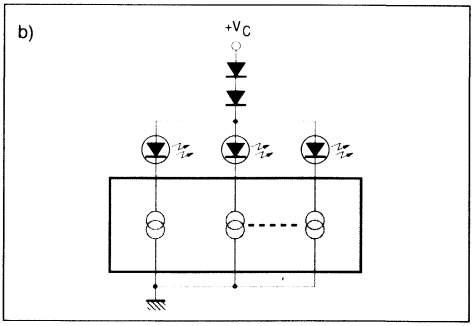
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

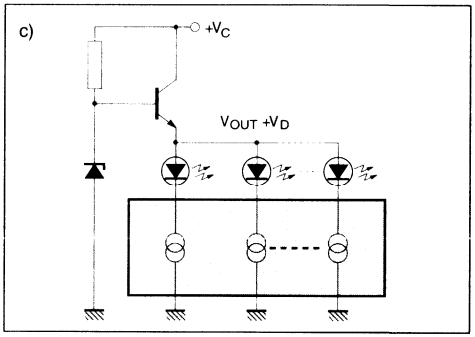
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

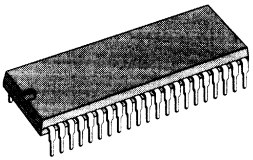
NICAM

SGS-THOMSON MICROELECTRONICS

TDA8204

NICAM DECODER

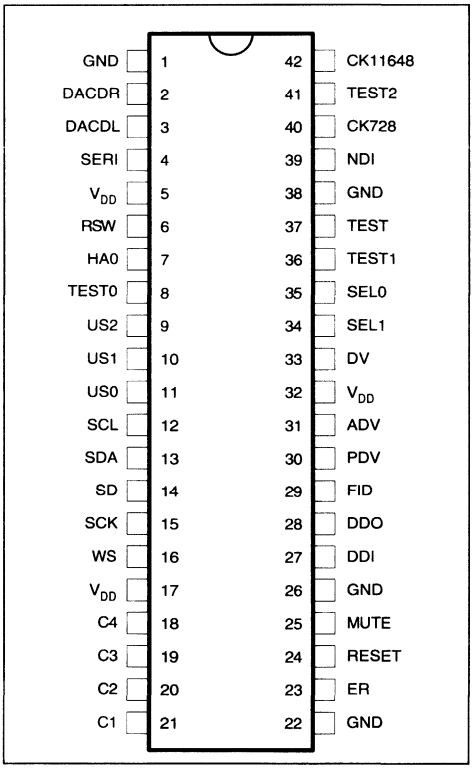
- HIGHLY INTEGRATED TWO-CHIP SOLUTION FOR NICAM DEMODULATION (using TDA8205 QSPK)
- DATA AND SOUND RECOVERY ACCORDING TO EBU SPB 424 SPECIFICATIONS
- I^2S INTERFACE FOR DIGITAL AUDIO PURPOSES (14-bit samples, 32kHz word select clock, 896kHz serial clock)
- 4 TIMES UP SAMPLING DIGITAL FILTER AND NOISE SHAPER
- I^2C INTERFACE FOR MICROCONTROLLER SOFTWARE DRIVE
- PAY TV APPLICATION CAPABILITIES
- AUTOMATIC ERROR MONITORING (programmable error rate limit)



SHRINK 42
(Plastic Package)

ORDER CODE : TDA8204

PIN CONNECTIONS



8204-01.EPS

DESCRIPTION

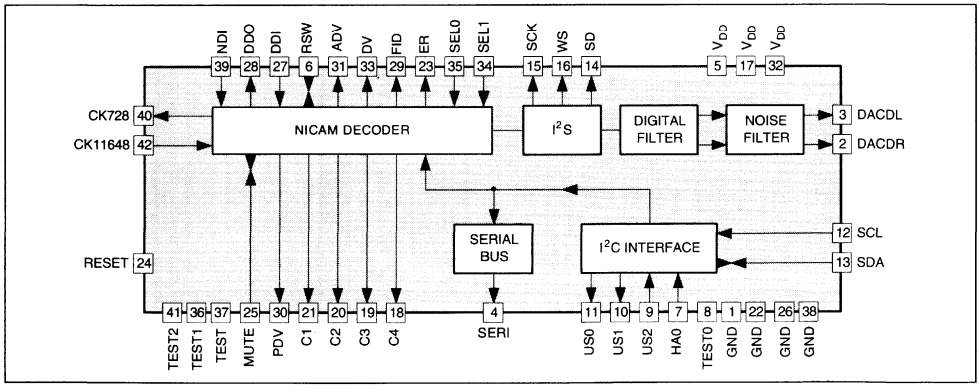
The TDA8204 performs two main functions, first one is NICAM decoding, second one is audio signal recovery (DAC) combined with audio signal switching (Matrix). An I^2S output is provided for digital audio when required and all functions of both the TDA8204 and the TDA8205 are accessed via an on-chip I^2C bus interface. The I^2S interface can be used as an input for converting to analog the D2MAC sound decoded by STV3830.

PIN ASSIGMENT

Pin N°	Pin Name	Function	Pin N°	Pin Name	Function
1	GND	Ground	22	GND	Ground
2	DACDR	PWM Data Output Right	23	ER	Error Monitor Flag Output
3	DACDL	PWM Data Output Left	24	RESET	Reset
4	SERI	Inter Chip Serial Bus Output	25	MUTE	NICAM Mute
5	V_{DD}	+5V Supply	26	GND	Ground
6	RSW	Reserve Sound Switch Status/Control	27	DDI	Descrambled Data Input
7	HA0	Hardware Address Selection	28	DDO	Descrambled Data Output
8	TEST0	To be connected to V_{DD} or GND	29	FID	Frame Identification Flag Output
9	US2	User bit 2 (input)	30	PDV	Parity Data Valid Flag Output
10	US1	User bit 1 (output)	31	ADV	Additional Data Valid Flag Output
11	US0	User bit 0 (output)	32	V_{DD}	+5V Supply
12	SCL	I^2C Bus Clock	33	DV	Data Valid Flag Output
13	SDA	I^2C Bus Data	34	SEL1	Language Selection 1 Input
14	SD	I^2S Bus Data	35	SEL0	Language Selection 0 Input
15	SCK	I^2S Bus Clock	36	TEST1	Not to be connected
16	WS	I^2S Bus Word Select	37	TEST	To be connected to GND
17	V_{DD}	+5V Supply	38	GND	Ground
18	C4	Application Control Bit 4 Flag	39	NDI	NICAM Data Input
19	C3	Application Control Bit 3 Flag	40	CK728	728kHz bit Clock Output
20	C2	Application Control Bit 2 Flag	41	TEST2	Not to be connected
21	C1	Application Control Bit 1 Flag	42	CK11648	11.648MHz bit Clock Input

8204-01.TBL

BLOCK DIAGRAM



8204-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	7	V
P_{tot}	Total Power Dissipation	1.2	W
T_{oper}	Operating Temperature Range	0, + 70	°C
T_{stg}	Storage Temperature Range	- 20, + 150	°C

8204-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}a)}$	Thermal Resistance Juntion-ambient	Max.	67	°C/W

8204-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{DD}	Supply Voltage Range	4.75	5	5.25	V
I_{DD}	Supply Current	30	60	92	mA
OUTPUTS					
DACDR, DACDL, SERI, US1, SCK, WS, C4, ER, DDO, FID, PDV, ADV, DV, CK728					
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	0.7 V_{DD}			V
US0 (open drain)					
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
I_{LK}	High Output Current (leakage)			± 2	µA
CONSTANT CURRENT LED DRIVERS C1, C2, C3					
I_{OL}	Low Output Current (V_{OL} = 0.4V)	- 10			mA
INPUTS					
HA0, US2, RESET, DDI, SEL1, SEL0, TEST, NDI, CK11					
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
BI-DIRECTIONAL					
	RSW, MUTE				
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High OUtput Voltage (I_{OH} = 100µA)	0.7 V_{DD}			V
V_{IL}	Low Input Voltage			0.8	V
	SD				
V_{OL}	Low Output Voltage (I_{OL} = -4mA)			0.4	V
V_{OH}	High Output Voltage (I_{OH} = 4mA)	0.7 V_{DD}			V
V_{IL}	Low Input Voltage			0.8	V
V_{IH}	High Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
I^2C INTERFACE					
	SCL				
V_{IL}	Low Input Voltage	0		1.5	V
V_{IH}	High Input Voltage	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_r, t_f	Input Rise and Fall Times			2	µs
I_{IL}	Input Leakage Current (V_I = 5.5V)			10	µA
C_I	Input Capacitance			7	pF
	SDA				
V_{IL}	Input Low Voltage	0		1.5	V
V_{IH}	Input High Voltage	3		V_{DD}	V
t_r, t_f	Input Rise / Fall Times			2	µs
I_{IL}	Input Leakage Current (V_I = 5.5V with output off)			10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_f	Output Fall Time between 3.0V and 1.0V			200	ns
C_I	Load Capacitance			400	pF

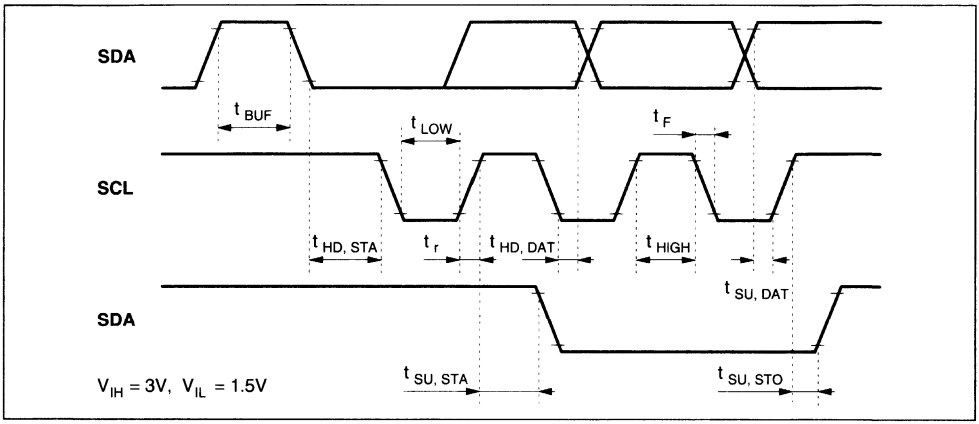
8204-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I^2C BUS TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V)				
t_{LOW} t_{HIGH}	Low Period Clock High Period Clock	4 4			µs µs
t_{SU}, d_{AT}	Data Set-up Time	250			ns
t_{HD}, d_{AT}	Data Hold Time	170			ns
t_{SU}, S_{TO}	Stop Set-up Time from Clock High	4			µs
t_{BUF}	Start Set-up Time following a Stop	4			µs
t_{HD}, S_{TA}	Start Hold Time	4			µs
t_{SU}, S_{TA}	Start Set-up Time following Clock Low to High Transition	4			µs

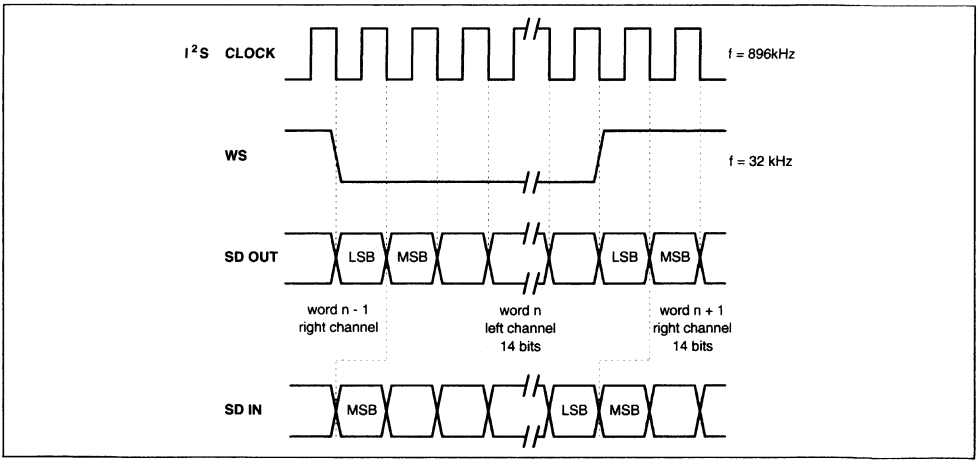
8204-05.TBL

Figure 1 : I^2C Serial Bus Timing



8204-03.EPS

Figure 2 : I^2S Bus Timing Diagram



8204-04.EPS

FUNCTION DESCRIPTION

The TDA8204 is partitioned into 6 major parts shown in the block diagram.
The NICAM Decoder performs data and sound recovery from the signals specified in EBU SPB 424. The expanded digital audio signals (14-bit) are made available at the digital audio interface (I^2S) in a serial multiplex of left and right channels. They are also processed by a 4 times upsampling digital filter and noise shaper which results in a high speed digital data stream at the output pins DACDL/DACDR. This data stream can be applied to the 1-bit D-A convertors contained in the TDA8205.
The TDA8204 is I^2C bus controlled and provides control over the functions of the TDA8205 by means of a serial inter-chip bus.

1 - NICAM Decoder

1.1 - BLOCK DIAGRAM (see Figure 3)

1.2 - DESCRIPTION

NICAM frame alignment requires searching out a frame alignment word (FAW) and a 16 frame sequence conveyed by C0 bit. Because of noise, interferences, errors in the incoming NICAM Data, aliases of the FAW, a robust scheme is implemented. It ensures the decoder will align, and stay aligned, to signals beyond the limit of maximum useable error rate. Thanks to a 511 bit PRBS synchronized by the recovered clock and a modulo 2 adder, original data are recovered. This data stream can be processed externaly for de-encryption in Pay TV applications using descrambled data Pins DDO, DDI.
To allow simultaneous reading and writing of mono/stereo samples, de-interleaved data frames are stored in a 3 page RAM.

The 10-bit input audio samples are expanded to 14-bit using scale factor bits according to NICAM decoding rules. Samples in error by the parity check are replaced by interpolated one or repeated.

Mute is set according to an error counter when the error rate exceeds error rate limit (ERL) and reset when the error rate is below ERL/4.
Application control information (bit C1, C2, C3, C4) is recovered by majority decision logic over 16 frames. the C1, C2, C3 , C4 bits can be read in SR0 register and are set on the C1, C2, C3, C4 pins according to the state of bit 0 (BEA) of the CR2 register.

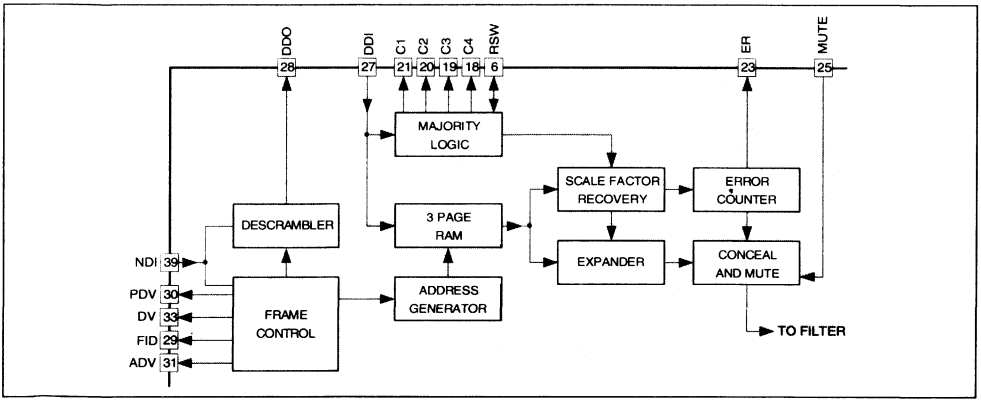
2 - Digital Filter and Noise Shaper

A digital filter performs 4X upsampling in two stages. The main FIR 2x upsampler is followed by a smaller 2x FIR upsampler. Digital upsampling means a much simpler post-DAC reconstruction filter can be used thus saving on external component count and cost.
A noise shaper converts the samples from the digital filter into two high speed serial bitstreams which can be applied to the DACs in the TDA8205.

3 - I^2S Bus

A standard three-wire interface, conforming to the I^2S bus protocol, is provided, allowing connection of an external DAC or DAT interface. Audio samples contain 14-bit, so 16-bit DACs will pad the two LSBs with 0. The word select clock operates at 32kHz and the serial clock at 896kHz.
By setting SDI bit of CR2 to 1, the I^2S interface can receive the D2MAC sound decoded by the STV3840. This prevents duplicating the dual D/A converter.

Figure 3 : NICAM Decoder Block Diagram



4 - Interchip Bus

A one-line serial bus provides interchip communications allowing control of all functions through the single I^2C bus interface.

5 - I^2C Bus

An I^2C bus interface provides access to control and status registers within the two chips to allow control of their functions and monitoring of status. A digital filter is included to improve noise immunity.

5.1 - DATA FLAGS (see Figure 4)

These indicate the status of the descrambled data on the DDO pin. They are inhibited if the decoder is out of alignement.

- FID : Frame alignment word (scrambled)
- PDV : Parity Data Valid. CIB0 and CIB1 overwrite the first 2 bits of FAW
- ADV : 11 additional data bits
- DV : Data valid (mode dependant)

5.2 - DECRYPTION (see Figure 5)

The PRBS generator (used for descrambling) is normally preset to all ones at the start of each frame. However, it is possible to preset it to any value on each frame by means of a code word clock (CWC) and serial code word data (CWD) interface on pins SEL0 and SEL1.

CWD, which is clocked in on the negative going edges of the CWC clock, can be sent anywhere during the frame except when FID = 1. The CWC is asynchronous with respect to the Nicam clock and the CWD will be used on the following frame. During the time FID = 1, the levels on the SEL0, SEL1 pins are read for language selection. Code words for descrambler presetting may be sent in either an 8-bit or 9-bit formats. There are four possibilities :

- if 7 or less clock cycles are counted on CW-clock during a frame, the PRBS generator is preset to all ones ;
- if 8 clock cycles are counted, 8 bits of CW-data are clocked into the shift register, the first bit of the previous transfer now moving to bit 9 position in the shift register. The resulting value is used to preset the PRBS generator on the next frame.
- if 9 clock cycles are counted, the CW-data (which has been clocked into a 9-bit shift register) is used to preset the PRBS generator on the next frame.
- if 10 or more clock cycles are counted, only the first 9 bits of the CW-data are used and loaded into the PRBS generator on the next frame.

Figure 4 : Data Flags

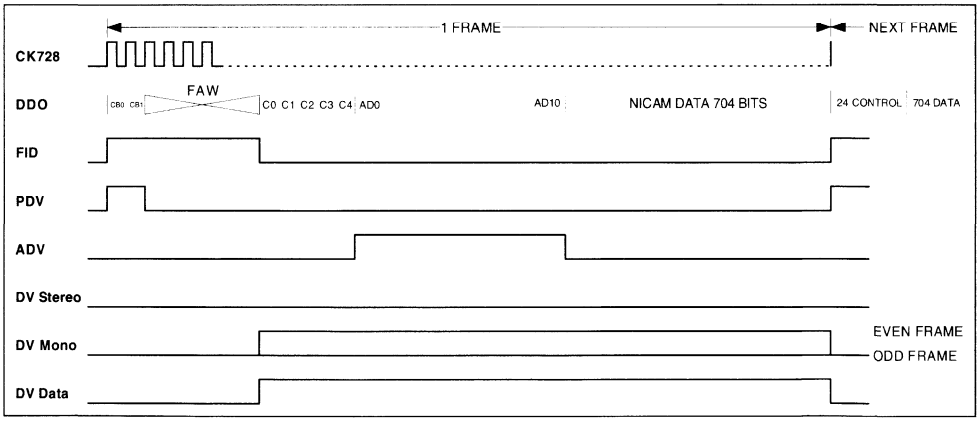
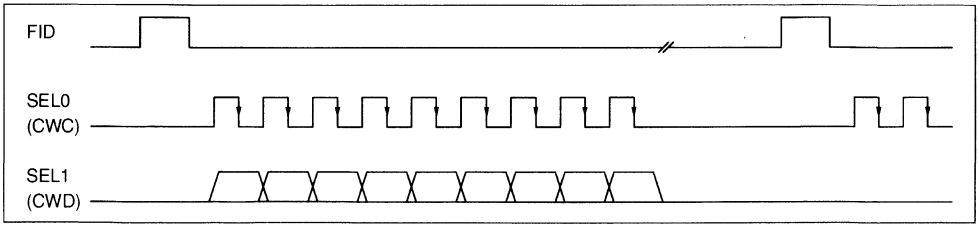


Figure 5 : PRBS Presetter



5.3 - SOFTWARE SPECIFICATION

Software control of IC's is given by programming four registers, one read only status register (SR0) and three read and write control registers (CR1, CR2, CR3).

Transmit format : S = Start, A = Acknowledge
P = stop

S	CHIP ADDRESS	0	A	REG SUB ADDRESS	A	DATA	A	P

Receive format :

S	CHIP ADDRESS	1	A	SR0 DATA	A	CR1 DATA	A	P

Note : All registers are read sequentially; device status and the contents of all registers may be read. The sequence may be terminated by not acknowledging (NOACK) the slave.

Chip address

1	0	1	1	0	1	HAO	R/W
MSB							LSB

HAO : Hardware address selection pin

Register addresses

Reg. Name	Sub Adress								Function
SR0	0	0	0	0	0	0	0	0	NICAM status
CR1	0	0	0	0	0	0	0	1	Matrix and mutes
CR2	0	0	0	0	0	0	1	0	NICAM control
CR3	0	0	0	0	0	0	1	1	Switches

Register contents

SR0 : NICAM status (read only)

US2	C1	C2	C3	C4	MUT	LA2	L/S
US2	0	0	0	1	1	1	1
MSB							LSB

L/S : • If FN1 bit of CR2 is 0, LS bit is loss of frame alignment status
LS =1, FAW is lost
LS = 0 FAW is identified
• If FN1 bit of CR2 is 1, LS bit is selected system status
LS = 1, B/G standard
LS = 0, I standard

LA2 : Loss of sub-frame alignment (1 = loss of alignment)

MUT : NICAM mute (1 = DAC outputs muted)

C4 : Reserve sound flag (1 = FM backup)

C3 : Application control bit 3

C2 : Application control bit 2

C1 : Application control bit 1

US2 : User bit 2 (input)
US2 bit indicates the state of US2 input Pin

CR1 : Matrix and mutes (read and write register)

Q1	Q0	I2	I1	I0	G0	AUM	FRE
0	0	0	0	0	0	0	0
MSB							LSB

Qn : Output select (see tables)

In : Input select (see tables)

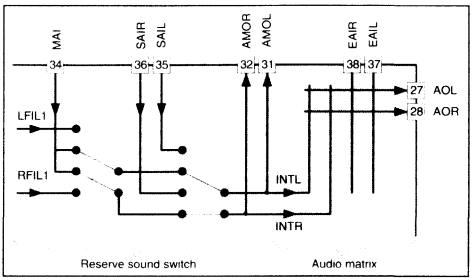
G0 : Auxiliary output gain, 0 = 0dB, 1 = 6dB

AUM : Auxiliary output mute, 0 = no-mute, 1 = muted

FRE : Free run clock VCXO for set up, 0 = normal, 1 = free run
To set crystal series capacitor

Switches and Matrix Description

Figure 6



Output selection

Q1	Q0	Output
0	0	AOL
0	1	AOR

Mute and gain selection

Q0	I2	Mute	Gain
0	0	OFF*	-
0	1	ON*	-
1	0	-	0dB**
1	1	-	+6dB**

* Mute is activated by left channel selection
** Gain is activated by right channel selection

Input selection

I1	I0	Input
0	0	INTL
0	1	INTR
1	0	EAIL
1	1	EAIR

Example of programming

First step : 0 0 1 0 0 X X X
INTL connected to AOL, mute ON on AOL/AOR

Second step : 0 1 0 1 1 X X X
EAIR connected to AOR, gain 0dB on AOL/AOR

Thrird step : 0 0 0 0 0 X X X
INTL connected to AOL, mute OFF on AOL/AOR

The power up default configuration is 0dB and unmute for both channels AOL/R, and INTL connected to AOL, and INTR connected to AOR.

CR2 : NICAM control (read and write register)

SDI	ECT	MAE	FN1	UMT	LA1	LA0	BEA
0	0	0	0	0	0	0	1

MSB LSB

SDI : I^2S direction
0 = Output, 1 = Input
ECT : Bit error rate counting time
0 = 128ms, 1 = 64ms
MAE : Max allowed errors
0 = 511, 1 = 255
FN1 : Set function of bit 0 in SR0, 0 = loss of alignment (status), 1 = system status (I or B/G)
UMT : Un-mute NICAM, 1 = un-mute, 0 = mute
LA1 : Language select 1 (LA1 ⊕ SEL1)
LA0 : Language select 0 (LA0 ⊕ SEL0)
BEA : Set C1-C3 function

ECT	MAE	BER MUTE
0	0	8.9×10^{-3} (1 in 112)
0	1	4.4×10^{-3} (1 in 225)
1	0	1.8×10^{-2} (1 in 56)
1	1	8.9×10^{-3} (1 in 112)

Un-mute at BER/4.

TDA8204 Output (Pin)	BEA	
	0	1
C1 (21)	C1*	Single mono mode
C2 (20)	C2*	Dual mono mode
C3 (19)	C3*	Stereo mode

* Application control bit of NICAM signal

Note : C4 pin remains unchanged. The function of C1-C4 in SR0 remains unchanged.

CR3 : Switches (read and write register)

US1	US0	AUT	IBG	FS1	FS0	X	SYN
0	0	1	0	0	0	0	1

MSB LSB

US1 : User bit 1 (output)
US0 : User bit 0 (output)
AUT : Automatic selection, 1 = enable
IBG : Select system I or B/G, 1 = B/G
FSn : Force switch (see table)
SYN : 1 = synthesiser, 0 = dual VCXO (carrier loop)

FS1	FS0	Selection
0	0	Auto NICAM
0	1	FM-Mono
1	0	FM-Stereo
1	1	NICAM

NICAM STAND-ALONE APPLICATION

The NICAM kit has been designed to be monitored by the I^2C bus; nevertheless stand-alone working capability is offered to the designer for low cost applications.
In order to know the status of the kit in stand-alone mode, consider the contents of the four I^2C registers at power-ON (4 registers : SR0 - CR1 - CR2 - CR3). Hardware configurable pins will be described later.

1 - Power-ON Configuration

SR0 (status)

US2	C1	C2	C3	C4	MUT	LA2	L/S
US2	0	0	0	1	1	1	1

MSB LSB

US2 : Not used in stand-alone
C1 :
C2 : Application control bit status for NICAM signal
C3 :
C4 : Reserve Sound Flag
MUT : DAC outputs muted (demuted as soon as NICAM appears)
LA2 : the subframe alignment is been lost
L/S : FAW status (FN1 of CR2 = 0)

CR1 (R/$\overline{W}$)

Q1	Q0	I2	I1	I0	G0	AUM	FRE
0	0	0	0	0	0	0	0

MSB LSB

Q1 :
Q0 : NICAM sound is sent on all matrix
I2 : outputs and on AMOx pins
I1 :
G0 : Gain = 0dB on AMOx
AUM : AMOx pins un-muted
FRE : VCXO in normal mode

CR2 (R/$\overline{W}$)

SDA	ECT	MAE	FN1	UMT	LA1	LA0	BEA
0	0	0	0	0	0	0	1

MSB LSB

SDA : Normal mode
ECT & MAE : BER = 1/112
FN1 : Bit L/S of SR0 set to alignment loss status
UMT : TDA8204 mute pin 25 to 0
LA1 : Result depending of SEL1
LA0 : Result depending of SEL0
BEA : Beacon decoding mode but all diodes are OFF until a NICAM signal has been found

CR3 (R/$\overline{W}$)

US1	US0	AUT	IBG	FS1	FS0	X	SYN
0	0	1	0	0	0	0	1

MSB LSB

US1 : Not used in stand-by mode
US0 : Not used in stand-by mode
AUT : Automatic standard

IBG : Standard I (don't care)
FSn : Set to Auto NICAM (if NICAM fails, FM mono is selected)
FN2 : Not used
SYN : Synthesizer selected

2 - Hardware Configurable Pins

2.1 - TDA8204 - PIN 6 - (RSW)
- as an output :
  status of the RSW switch
  - 0 = FM mono
  - 1 = NICAM
- as an input :
  - 0 = FM mono (forced)

2.2 - TDA8204 - PINS 34/35 - (SEL0/SEL1)
(see Figure 7)
- to select the language in case of bilingual operation
- selected value is related to LA0 and LA1

As the I^2C bus is not used LA0 and LA1 = 0 (power-ON condition) / SEL0 = Q0, SEL1 = Q1

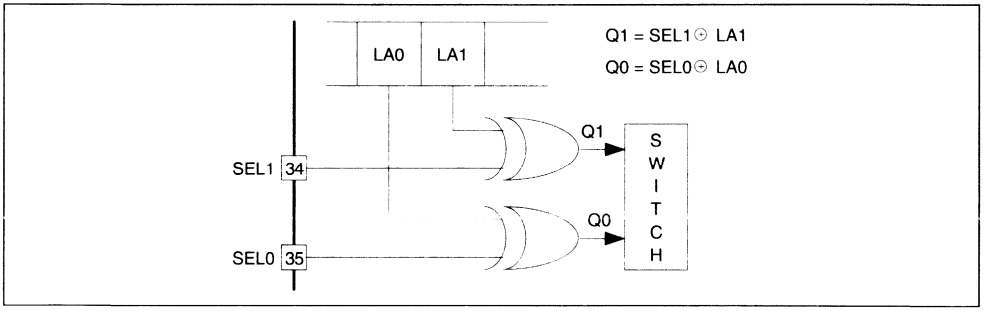
The 4 choices are summarized in the table below.

SEL0	SEL1	DACDL	DACDR
0	0	M1	M2
0	1	M1	M1
1	0	M2	M2
1	1	M2	M1

M1 = Mono 1
M2 = Mono 2

VII - 2.3. TDA8204 - PIN 25 - (MUTE)
- as an output :
  status of the DAC
  - 0 = unmuted
  - 1 = muted
- as an input :
  - 0 = unmute DAC (forced)

Figure 7



APPLICATION DIAGRAMS

Figure 8 : Stand Alone Application (I standard)

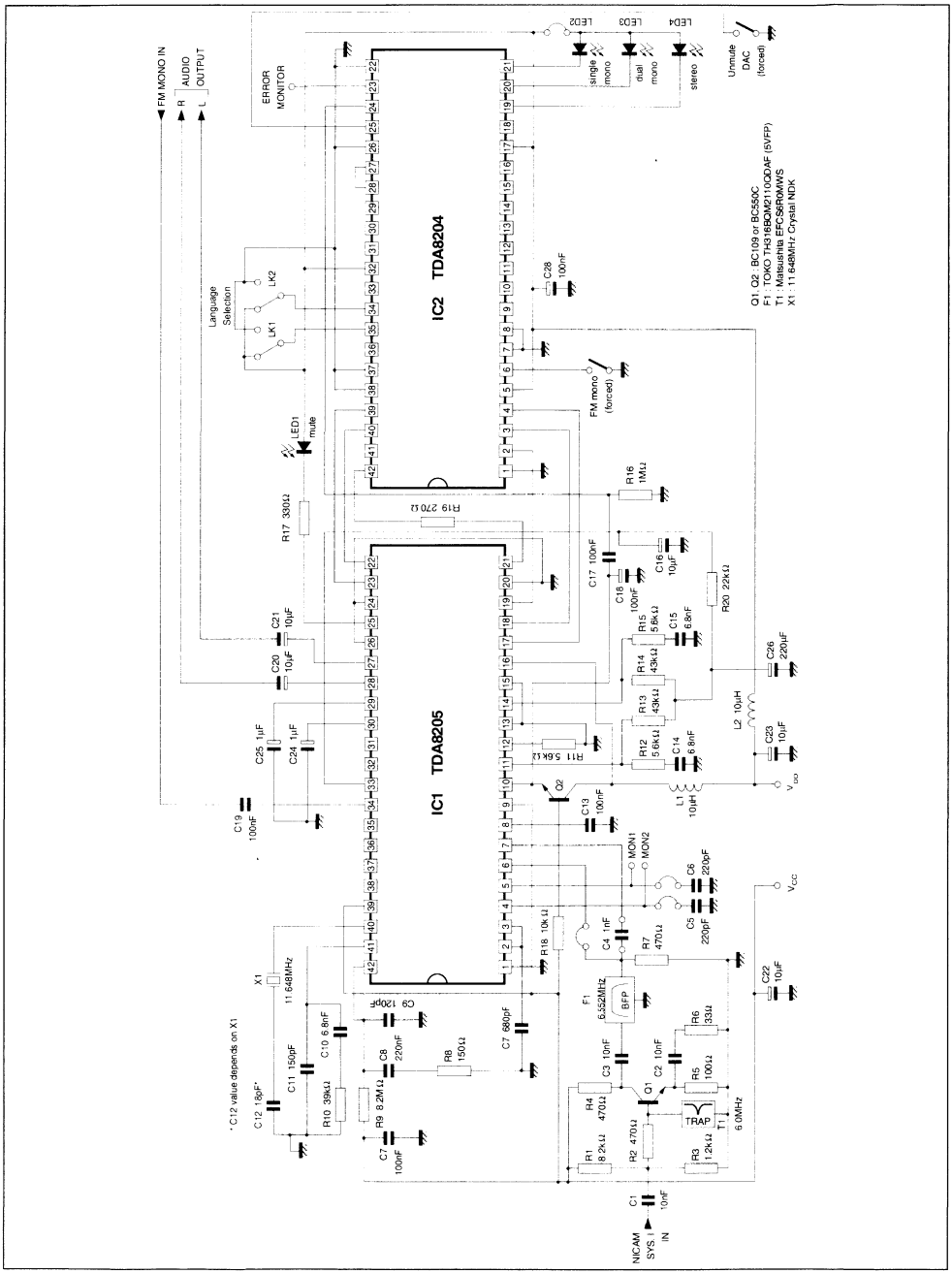
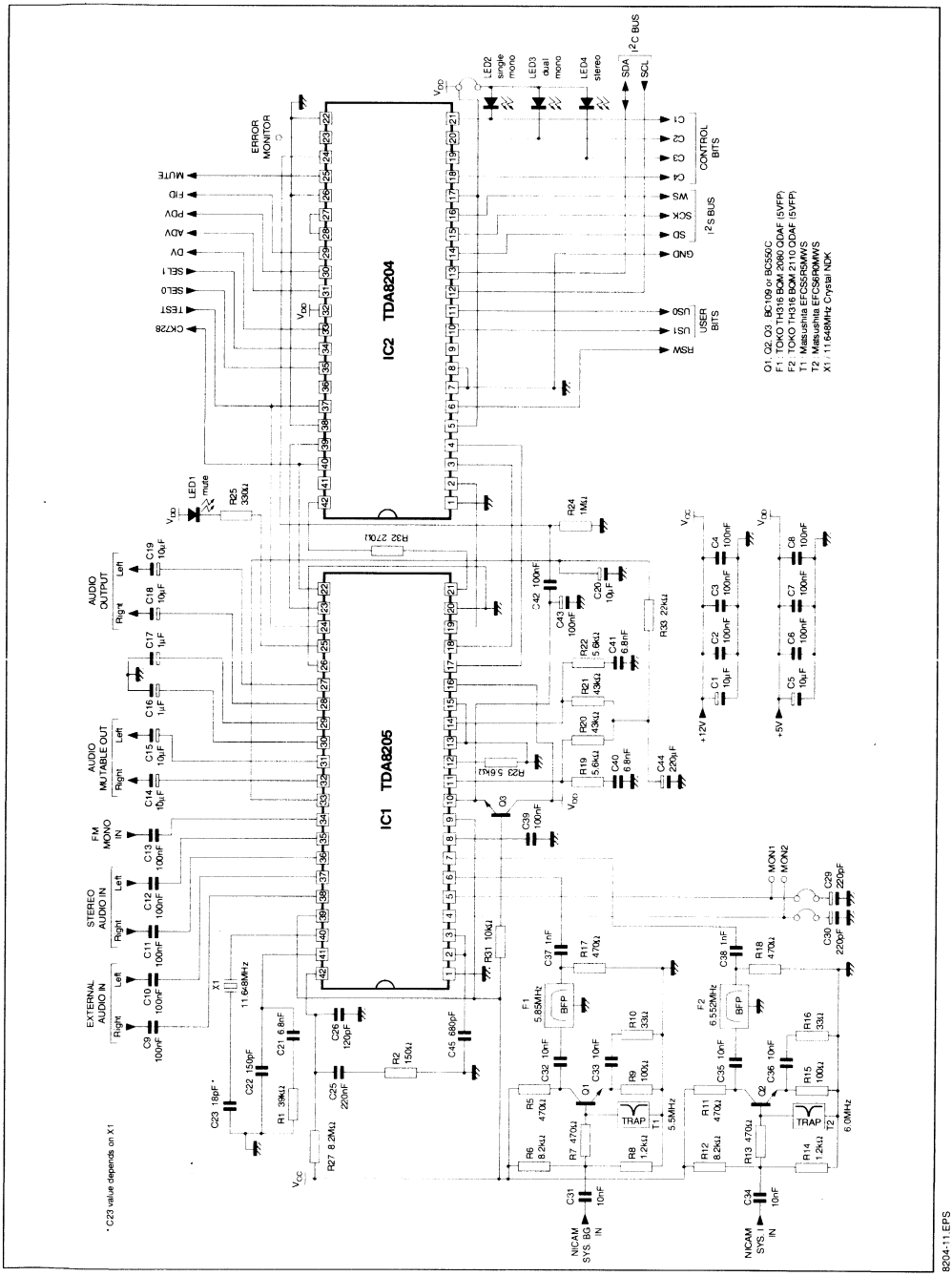


Figure 9 : I²C Bus Controlled Application (I and B/G standard)

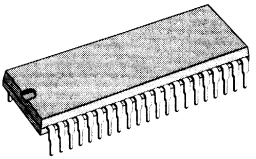


SGS-THOMSON MICROELECTRONICS

TDA8205

NICAM QPSK DEMODULATOR

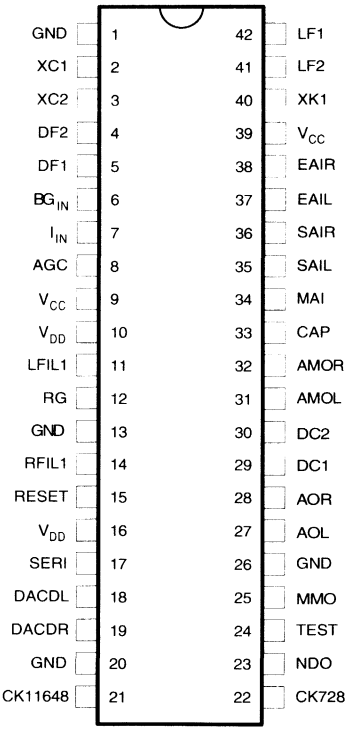
- HIGHLY INTEGRATED TWO CHIP SOLUTION FOR NICAM DEMODULATION (using TDA8204 decoder)
- AUTOMATIC DUAL STANDARD DEMODULATION 6.552MHz FOR I SYSTEM 5.85MHz FOR B/G SYSTEM
- 40dB RANGE AGC
- SINGLE CRYSTAL OPERATION
- NICAM 728 DATA AND CLOCK RECOVERY
- LOW PASS FILTER FOR PWM CODED AUDIO SIGNALS AND J-17 DE-EMPHASIS
- AUTOMATIC FM MONO SELECTION BY RESERVE SOUND SWITCH FUNCTION
- VERSATILE AUDIO SWITCHING MATRIX
- AUTOMATIC MUTE FUNCTION



SHRINK 42
(Plastic Package)

ORDER CODE : TDA8205

PIN CONNECTIONS



8205-01 EPS

DESCRIPTION

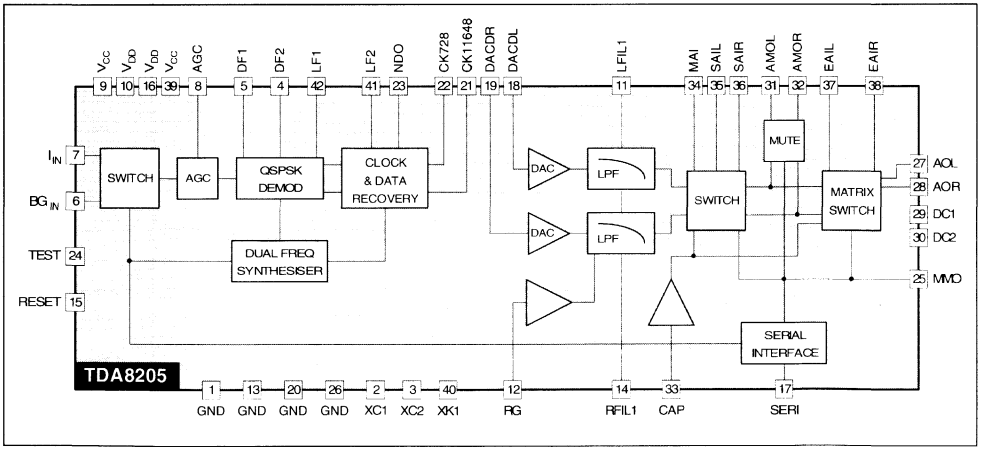
The TDA8205 is essentially divided into two signal processing sections. The first section handles all the NICAM signal acquisition, the QPSK demodulator and clock and data recovery circuits. The key point to note about this section is the dual frequency synthesiser. By use of only one quartz crystal, the IC is able to demodulate QPSK signals from either system I or system B/G in an automatic way. The second section of the TDA8205 manages the analog parts of the twin digital-to-analog converters (DACs) and all filtering and audio switching downstream of the DACs. A simple serial bus from the TDA8204 allows control of the switch functions by the CTV system microcontroller.

PIN ASSIGMENT

Pin No	Pin Name	Function	Pin No	Pin Name	Function
1	GND	Ground	22	CK728	728kHz Clock Intput
2	XC1	Optional Crystal	23	NDO	NICAM Data Output
3	XC2	Optional Crystal	24	TEST	To be connected to GND
4	DF2	Data Filter 2 (eye monitor)	25	MMO	Matrix Mute Out
5	DF1	Data Filter 1 (eye monitor)	26	GND	Ground
6	BG_{IN}	System B/G Input	27	AOL	Audio Output Left
7	I_{IN}	System I Input	28	AOR	Audio Output Right
8	AGC	AGC Filter Capacitor	29	DC1	Decoupling 1
9	V_{CC}	+12V Supply	30	DC2	Decoupling 2
10	V_{DD}	+5V Supply	31	AMOL	Audio Mutable Output Left
11	LFIL1	Left Filter 1 (J-17 De-emphasis)	32	AMOR	Audio Mutable Output Right
12	RG	Gain Setting Resistor for DAC	33	CAP	Decoupling Capacitor
13	GND	Ground	34	MAI	Mono Audio Input
14	RFIL1	Right Filter 1 (J-17 De-emphasis)	35	SAIL	Stereo Audio Input Left
15	RESET	Reset Chip	36	SAIR	Stereo Audio Input Right
16	V_{DD}	+5V Supply	37	EAIL	External Audio Input Left
17	SERI	Interchip Serial Bus Input	38	EAIR	External Audio Input Right
18	DACDL	DAC Data Left Input	39	V_{CC}	+12V Supply
19	DACDR	DAC Data Right Input	40	XK1	11.648MHz Crystal
20	GND	Ground	41	LF2	Loop Filter 2
21	CK11648	11.648MHz Clock Output	42	LF1	Loop Filter 1

9205-01.TBL

BLOCK DIAGRAM



9205-02.EPS

BLOCK DIAGRAM DESCRIPTION

The QPSK signal enters the IC via two inputs after passing through two external bandpass filters at the relevant frequencies of 6.552MHz and 5.85MHz for system I and B/G respectively. The two inputs enter a source selection switch and pass immediately to an AGC block which has a total range of 40dB. The resulting levelled signal passes to the QPSK demodulator which recovers the NICAM 728Kb/s data stream by means of carrier and clock recovery circuits.

Carrier recovery is achieved with a baseband re-modulator which consists of a phase locked loop with a switchable phase detector. This allows it to lock to one of four possible phases of the QPSK

carrier without disruption due to the modulation. Dual frequency operation is made possible by synthesising the carrier reference frequency thus saving the need for two extra crystals. Dual VCXO can also be software selected (SYN bit of CR3 in TDA8204) with external crystal (Pin XC1/XC2) for new standards. Selection between XC1 and XC2 is done with bit "IBG" in CR3 register of TDA8204 (IBG = 0 XC1 selected, IBG = 1 XC2 selected).

The standards switch controls operation of the QSPK demodulator at either 6.552MHz or 5.85MHz. This can be controlled via the I^2C bus or the decoder set into automatic mode in which it determines the standard by alternately trying to lock to the two systems.

On chip low pass filters recover the in-phase and quadrature data channels which are then sliced by comparators. The symbol clock is recovered from this data and used to sample and re-time it. The two data channels are then decoded and serialized to obtain the NICAM-728 data which is then passed on to the NICAM decoder in the TDA8204.

After processing the NICAM into a digital bit-stream in the TDA8204, the data is passed back to the TDA8205 for the analog functions of the DACs to be performed.

Conversion of the pulse width modulated bit streams to analog takes place and is followed by low pass filtering which removes high frequency quantising noise and performs J-17 de-emphasis. The DACs signal level can be adjusted to match the reserve sound signal level.

$1V_{RMS}$ maximum on Pins LFIL1/RFIL1 can be obtained by selection of appropriate resistor on Pin RG.

Once the analog audio has been recovered, certain source switch functions are performed. If the NICAM signal fails and if the reserve sound flag (C4), of SRO register, is set the reserve sound switch automatically selects Mono Audio Input. If the reserve sound flag (C4) is reset, the reserve sound switch will not change and the audio outputs will be muted (DAC outputs muted).

If the NICAM signal only carries data, Mono Audio Input is selected. The reserve sound switch can be forced to select Mono Audio Input via I^2C bus, using Bit FS0 = 1 and FS1 =0 of CR3 Register.

This can be used in the case of NICAM marginal reception. To select Stereo Left and Right Audio Input Bit FS0 = 0 and FS1 = 1 of CR3 Register must be selected. The outputs from this reserve sound switch are available on Audio mutable output left and right, and are internaly connected to the audio matrix.

A simple audio switching matrix is provided internally for flexible control over the audio source and destination selection.

Audio signal left and right coming from the reserve sound switch and the external audio input left and right can be switched to the audio outputs left and right .

DAC and auxiliary audio outputs can be muted. An additional +6dB gain can be applied to raise the output levels to $2V_{RMS}$ maximum. For more information see Software Specification chapter (III.5.3/TDA8204).

The DAC outputs are automatically muted under the following conditions

- loss of frame alignement
- the bit error rate (Ber) is > error rate limit
- NICAM signal is conveying M1 only. The right DAC is muted unless M1 has been selected to be on both DAC outputs.
- NICAM signal is conveying data only.

For test purposes, the DAC outputs can be unmuted by forcing the bi-directional mute Pin 25 of TDA8204 or via I^2C bus.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
V_{DD}	Supply Voltage	7	V
P_{tot}	Total Power Dissipation	1.2	W
T_{oper}	Operating Temperature Range	0, + 70	°C
T_{stg}	Storage Temperature Range	-20, + 150	°C

8205-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-Ambient	Max.	67	°C/W

8205-03.TBL

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, V_{DD} = 5V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
V_{CC}	Supply Voltage Range	11.4	12	12.6	V
V_{DD}	Supply Voltage Range	4.75	5	5.25	V
I_{CC}	Supply Current	18	36	50	mA
I_{DD}	Supply Current	10	18	42	mA
DIGITAL PINS					
OUTPUTS					
	CK11, NDO				
V_{OL}	Low Level Output Voltage (I = -4mA)			0.4	V
V_{OH}	HIgh Level Output Voltage (I = 4mA)	0.7 V_{DD}			V
	MMO (open collector)				
V_{OL}	Low Level Output Voltage (I = -1mA)			0.4	V
I_{LK}	High Level Output Current (leakage)			± 2	µA
INPUTS					
	SERI, DACDL, DACDR, CK728				
V_{IL}	Low Level Input Voltage			0.8	V
V_{IH}	High Level Input Voltage	0.6 V_{DD}			V
I_{LK}	Input Leakage Current			± 2	µA
ANALOG PINS					
I-B/G SELECTOR					
V_{DC}	DC Bias Voltage		2.8		V
R_{IN}	Input Resistance		10		kΩ
C_{IN}	Input Capacitance		10		pF
AGC					
V_{IN}	Input Voltage Range	10	200	1000	mV_{PP}
AGCIv	AGC Low Voltage (V_{IN} = 1V_{PP})		2		V_{PP}
AGChv	AGC High Voltage (V_{IN} = 10mV_{PP})		11		V
AGCta	AGC Attack Time (V_{IN} = 10mV to 1V, C_{AGC} = 100nF)		15		ms
AGCtd	AGC Decay Time (V_{IN} = 1V to 10mV, C_{AGC} = 100nF)		220		ms
QPSK DEMODULATOR (LF1)					
V_{DC}	DC Bias Voltage (SYN = 1)	1	5	10	V
Kd	Phase Detector Constant (no mod.)		33		µA/rad
kv	VCO Constant		3.5		MHz/V
EYE DIAGRAM MONITORS (DF1, DF2)					
V_{DC}	DC Bias Voltage		2.5		V
R_{OUT}	Output Resistance		1.2		kΩ
V_{OUT}	Output Voltage (System I)		0.6		V_{PP}
CLOCK AND DATA RECOVERY (LF2)					
V_{DC}	DC Bias Voltage		2.5		V
Kd	Phase Detector Constant (all 1's)		7		µA/rad
kv	VCXO Constant		4.4		kHz/V

8205-04.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC AND FILTER (LFIL1, RFIL1)					
V_{DC}	DC Bias Voltage		2.5		V
I_{OUT}	Output Current (R_G = 5.6kΩ, DAC full scale)		340		μA_{PP}
V_{RG}	RG Pin DC Voltage		1.25		V
AUDIO MATRIX (AOL, AOR, AMOL, AMOR)					
	DAC SELECTED				
V_{OUT}	Output Voltage (1kHz at -11.75dB, J17 de-emphasis, R_G = 5.6kΩ)	0.39	0.5	0.63	V_{RMS}
S/N	Relative to $0.5V_{RMS}$, noise measured with IEC-179 A-filter	60	70		dB
THD	1kHz at $0.5V_{RMS}$, R_G = 5.6kΩ		0.05	0.2	%
	Crosstalk at 1kHz, $0.5V_{RMS}$		65		dB
Chm	Maximum Channel Matching Error			2	dB
	MONO OR STEREO AUDIO INPUT SELECTED (MAI, SAIL, SAIR)				
S/N	Relative to $0.5V_{RMS}$, noise measured with IEC-179 A-filter		88		dB
THD	1kHz at $0.5V_{RMS}$		0.02		%
	STEREO AUDIO INPUT SELECTED				
	Crosstalk at 1kHz, $0.5V_{RMS}$		75		dB
Chm	Maximum Channel Matching Error			2	dB

8205-05.TBL

APPLICATION DIAGRAMS

Figure 1 : Stand Alone Application (I standard)

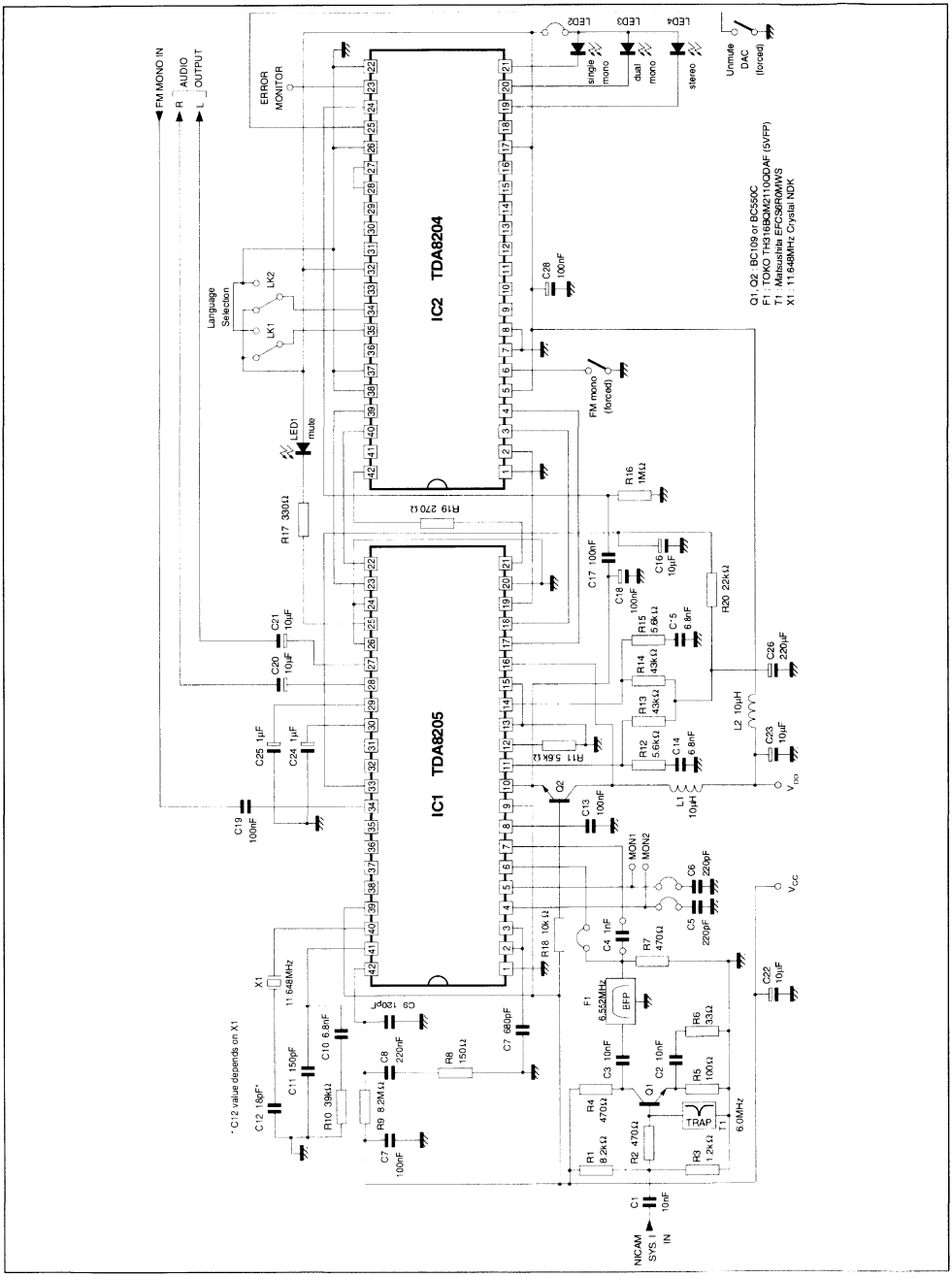
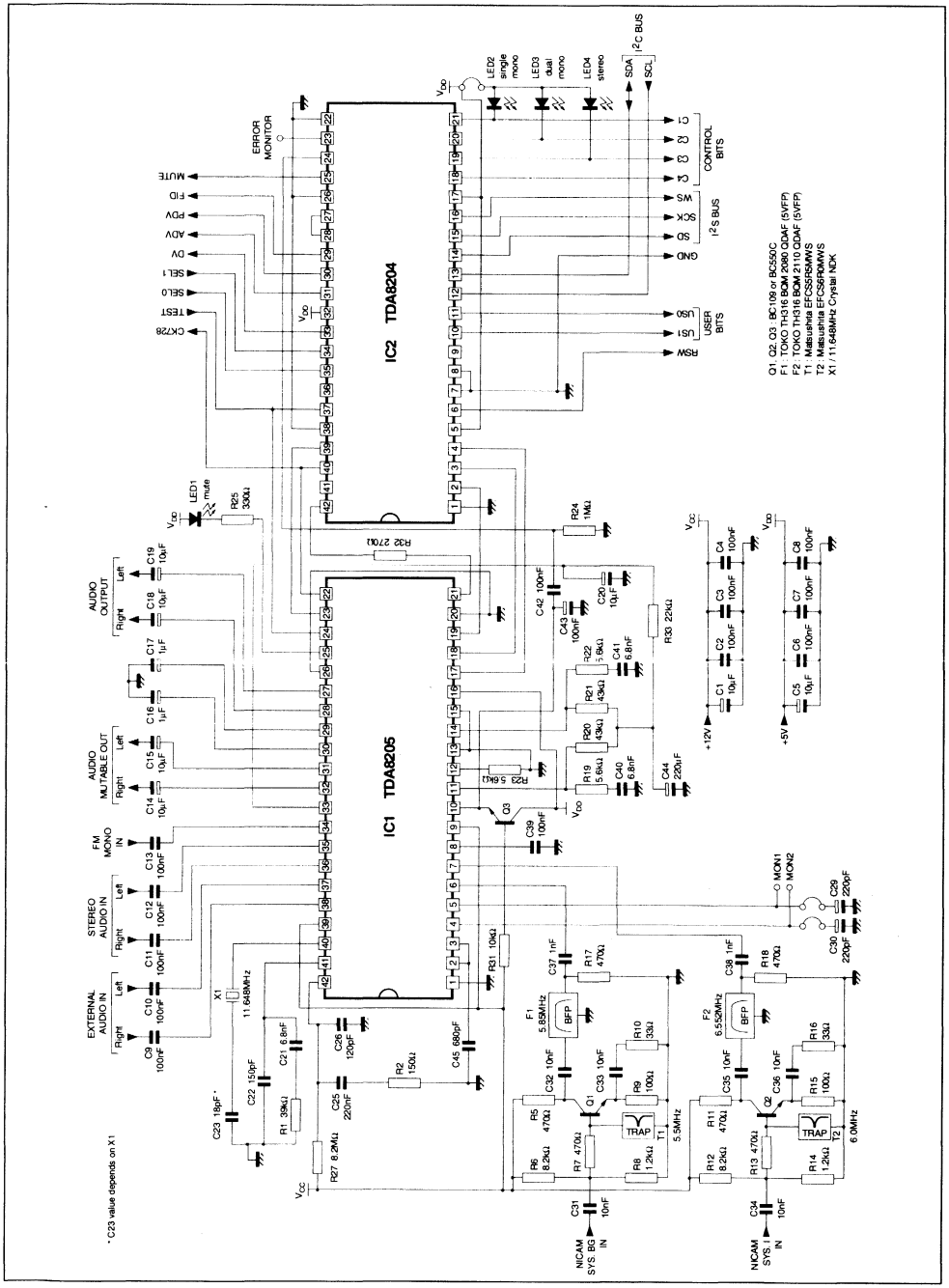


Figure 2 : I^2C Bus Controlled Application (I and B/G standard)



SPECIAL FUNCTION

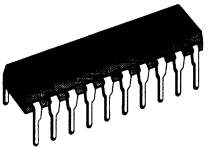
SGS-THOMSON MICROELECTRONICS

L6720
L6721

MINITEL INTERFACE

ADVANCE DATA

- ONE NON INVERTING LINE DRIVER
- ONE NON INVERTING LINE RECEIVER
- LINE TRANSCEIVER: (TOWARDS PERIPHERALS)
  - non inverter from Minitel to peripherals
  - inverter from peripherals to Minitel
- POWER SUPPLY
  - not regolated output voltage
  - internal low drop power switch with antisaturation circuit
  - output protected against short circuit
  - standby mode operation with an external signal
- AUDIO AMPLIFIER
  - one input, one output
  - one pin for supply rejection
  - internal fixed gain
- THERMAL SHUTDOWN



Powerdip 16+2+2

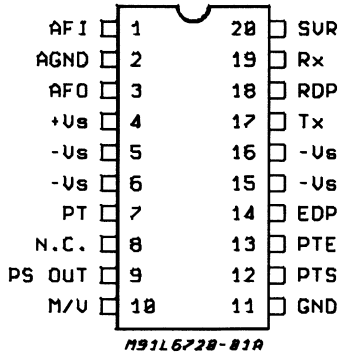
ORDERING NUMERS: L6720
L6721

DESCRIPTION

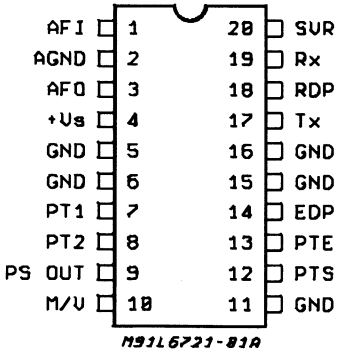
This device performs the functions of a complete interface for Minitel peripheral plug.

It integrates one line driver, one line receiver, one line transceiver, a power supply for peripherals, and an audio amplifier, Two version are provided:
- L6720 which needs a negative supply.
- L6721 which doesn't use a negative supply.

PIN CONNECTIONS



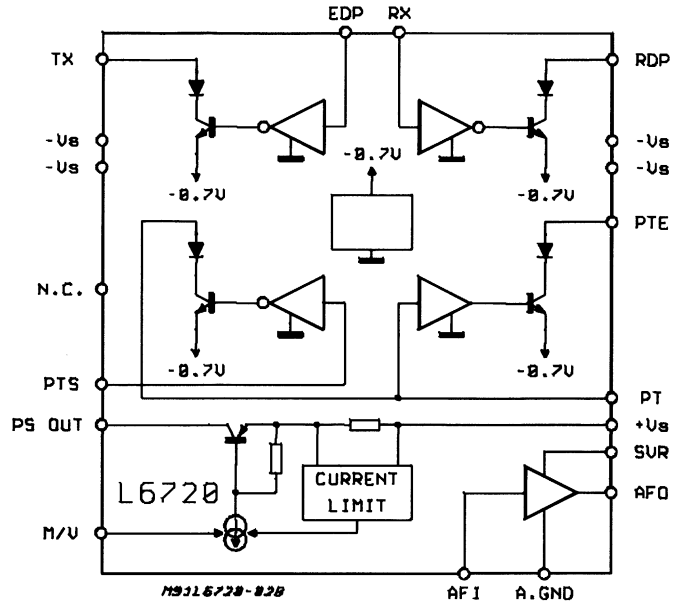
L6720

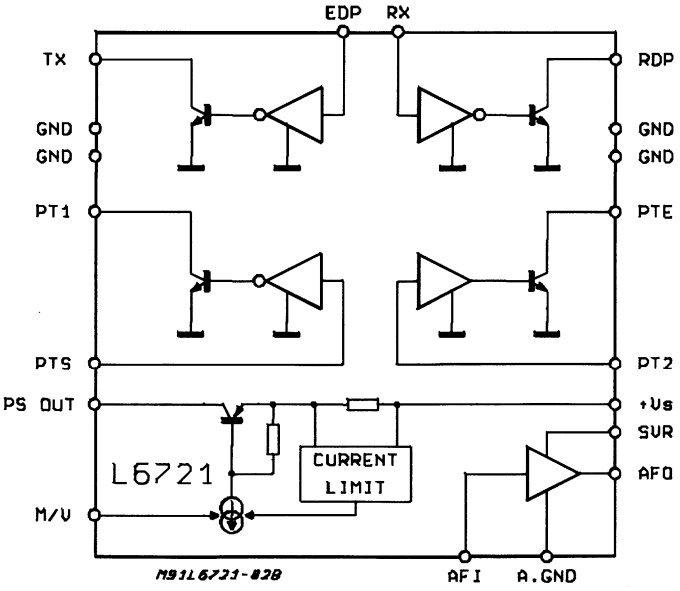


L6721

This advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
$+V_s$,(V_s)	Positive Supply Voltage	+15	V
$-V_s$	Negative Supply Voltage	-13	V
V_{OC}	Open Collectors Voltage	max 20	V
I_{OC}	Open Collectors Current	max 10	mA
P_{tot}	Total Power Dissipation at T_{amb} = 70°C	1.25	W
T_J	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	0 to 70	°C

THERMAL DATA

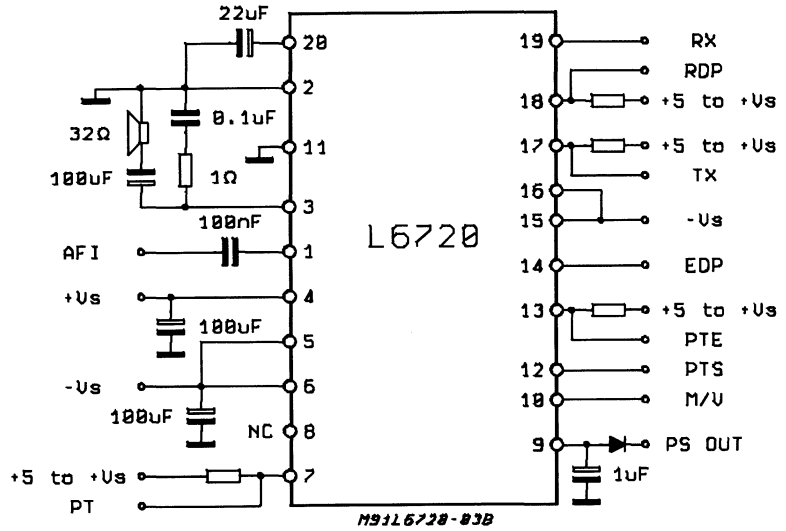
Symbol	Description		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	(*)65	°C/W

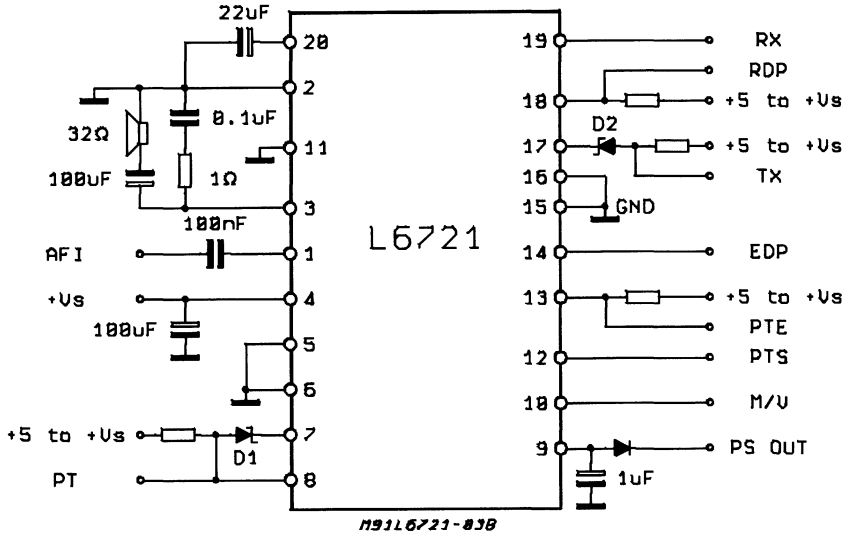
(*) Mounted on board with minimized dissipating copper area

PIN FUNCTIONS

Pin	Name	Function
1	AFI	Audio Frequency input
2	AGND	Audio Amplifier Ground
3	AFO	Audio amplifier output
4	$+V_s$,(V_s)	Power Supply Input (to plug)
5	$-V_S$,(GND)	Negative Supply (GND for L6721)
6	$-V_S$,(GND)	Negative Supply (GND for L6721)
7	PT	Transceiver Input/Output (L6720)
8	N.C.	Not Connected (L6720)
7	PT1	Transceiver Output (to plug) (L6721)
8	PT2	Transceiver Input (from plug) (L6721)
9	PSout	Power Supply Output (to plug)
10	M/V	Inhibition of peripheral output power
11	GND	Ground pin
12	PTS	Line Transceiver Input (from Minitel)
13	PTE	Line Transceiver Output (to Minitel)
14	EDP	Line Driver Input (from Minitel)
15	$-V_S$,(GND)	Negative Supply (GND for L6721)
16	$-V_S$,(GND)	Negative Supply (GND for L6721)
17	T_X	Line Driver Output (to plug)
18	RDP	Line Receiver Output (to Minitel)
19	R_X	Line Receiver Input
20	SVR	Supply Voltage Rejection

APPLICATION DIAGRAMS





D1-D2: SCHOTTKY VF ≤ 0.3V at 10mA
VR = 20Vmin

ELECTRICAL CHARACTERISTICS

I) LINE DRIVER, LINE RECEIVER, LINE TRANCEIVER

L6720: with negative supply

Test Conditions: 10V < +V_S < 12V, -8V <- V_S < -4V, T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT	Pins V_S and $-V_S$ open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time			1		µs

L6721: without negative supply

Test Conditions: 10V < V_S < 12V, T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level (Pins Rx, EDP, PTS, PT2)				0.8	V
V_{IH}	Input High Level (pins Rx, EDP, PTS, PT2)		2			V
I_G	Pull-up Current Generator on Pins Rx, PT2		160	250	340	µA
Z_I	Input Impedance on pins Rx, Tx, PT2	Pins V_S and GND open	68			KΩ
V_{OL}	Output Low Level (pins Tx, PT1)	I_{LOAD} = 6mA			0.15	V
V_{OL}	Output Low Level (pins RDP, PTE)	I_{LOAD} = 6mA			0.4	V
I_R	Output Leakage Current (pins Tx, RDP, PT1, PTE)				10	µA
t_{PLH}, t_{PHL}	Propagation Delay Time	I_{LOAD} = 6mA C_{out} = 50pF		3	5	µs
t_r, t_f	Output Rise and Fall Time	I_{LOAD} = 6mA C_{out} = 50pF		1		µs

II) POWER SUPPLY

L6720: +V_S = 12V, -V_S = -8V
L6721: V_S = 12V
T_j = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_I - V_O	Dropout Voltage	I_{LOAD} = 1A		0.4	0.8	V
I_{SC}	Short Circuit Current		1	1.1	1.2	A
M/V_L	Low Level Disable Pin (1)				0.8	V
M/V_H	High Level Disable Pin (1)		2			V
I_L	Disable Pin Input Current	M/V = 0			100	µA
I_Q	Quiescent Current	I_{LOAD} = 1A I_{LOAD} = 0.25A			60 23	mA mA

Note (1) Power supply is disabled when a zero level voltage is applied on M/V Pin

III) AUDIO AMPLIFIER (2)

L6720: $+V_S = 12V$, $-V_S = -8V$
L6721: $V_S = 12V$
$T_j = 25°C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_i	Input Impedance		20			KΩ
AV	Voltage Gain		28	30	32	dB
BW	Bandwidth		10			KHz
P_O	Output Power	Distortion = 10%, f = 1KHz $R_{LOAD} = 32Ω$, $10V < V_{CC} < 14V$	250			mW

Note (2): The output of the audio amplifier is protected against short circuits toward positive power supply and ground

IV) PROTECTIONS

1) L6720 (With negative supply)

Pins Rx, Tx, PT are protected against any DC voltage ranging from -18V to +18V, with the device supplied or not, without extra components.

2) L6721 (Without negative supply)

Pins Tx, PT1 are not protected: an external schottky diode must be added to protect them from -18V to +18V (see application diagram).
Pins Rx, PT2 are protected against any DC voltage ranging from -18V to +18V.

3) In Both Options

P. Supply pin is not protected: an external diode must be inserted to protect it (see application diagram).
The suggested electrical characteristic of the external diode are:

- $V_{REVERSE}$ > 20V
- Voltage drop at 1A max. 1.2V

4) Thermal Protection

This protection is operating when the chip temperature typically raises above 150°C (hysteresis 20°C Typ; this indicated value is valid with the application circuit on pag. 4), turning off both the power switch and the audio amplifier.

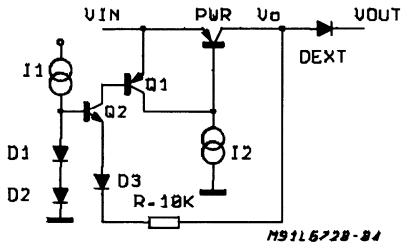
APPLICATION INFORMATION

The external diode on the output of the power switch has the fundamental function of protecting this pin against positive overvoltages.

However the voltage drop on this diode is also important in the correct definition of the thermal hysteresis. This can be understood by considering the circuit applied on the output of the power switch, which has the function of withstanding negative overvoltages.

Let's refer to fig. 1:

Figure 1



D_{EXT}: EXTERNAL DIODE; PWR: POWER TRANSISTOR; I_1, I_2: CURRENT GENERATORS; R: RESISTANCE; D1, D2, D3: DIODES; Q1, Q2: SIGNAL TRANSISTORS

When V_{OUT} = 0.7V Q2 and D3 turn on and also Q1 whose saturation turns off the power PWR. In this condition (BV_{CBO}) it can withstand the maximum negative overvoltage (-18V).

If we now have an overload on V_{OUT} (after the diode) for example with V_{IN} = 12V, V_{OUT} = 8V, P_d = 4W, the temperature of the chip increases to the thermal shutdown intervention, so that V_{OUT} = 0. However Q1 and Q2 cannot turn on because we have 2 diodes (D1 and D2) against 3 diodes (D3, D_{EXT}, Base-Emitter of Q2).
If the over load is on point V_O (before the external diode) as before the chip temperature increases until shutdown. But in that condition (with V_{OUT} = 0) we have now 2 diodes (D1, D2) against other 2 diodes (D3, Q2 Base-Emitter); than the power switch doesn't turn on because of a slight difference between the thermal coefficient of the 4 diodes.

We will have the new switching-on of power switch only when the chip temperature decreases of about 80°C (being kept off by Q1 and Q2).

In conclusion with or without the external diode the absolute value of the thermal shutdown is the same, but the hysteresis is higher without the external diode.

THERMAL CHARACTERISTICS

The transient thermal resistance of the 16+2+2 powerdip package is shown in Fig. 2: a typical $R_{th\ j\text{-}amb}$ of 50° C/W roughly can be seen.To be able to well sink out the heast from the inside of the package, the four control pins can be closely connected to a p.c.b. copper side. By considering the two square sides of Fig. 4, the thermal resistance junction-ambient can be reduced according to Fig. 3.

Figure 2: DIP 16+2+2 Transient Thermal Resistance for single pulses.

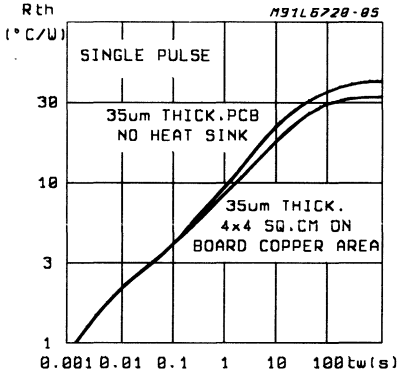


Figure 3: Typical R_{th} j-a of Powerdip 16+2+2 vs side 1 for heat sink on the PCB lower side.

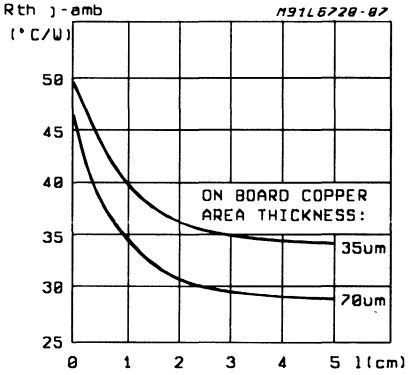
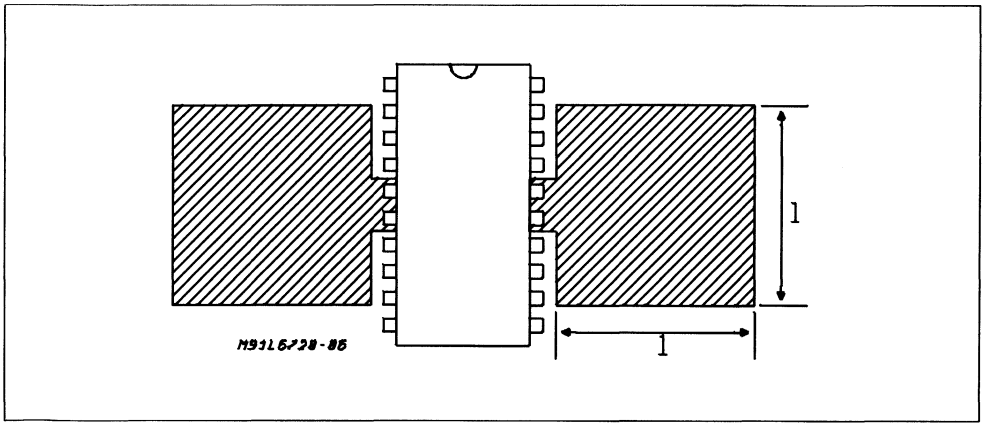


Figure 4: Two "On Board" square heat sink

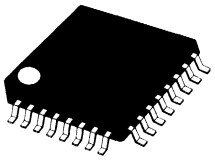


CABLE DRIVER FOR DIGITAL TRANSFER

- 1 DIFFERENTIAL INPUT, 3 DIFFERENTIAL OUTPUTS
- SUFFICIENT DRIVE CAPABILITY FOR A 300m LENGTH COAXIAL CABLE
- STABILITY DUE TO MINIMAL WAVEFORM DISTORTION
- BIPOLAR SILICON MONOLITHIC IC

APPLICATIONS

- DATA TRANSFER BETWEEN DIGITAL SIGNAL PROCESSING EQUIPMENT



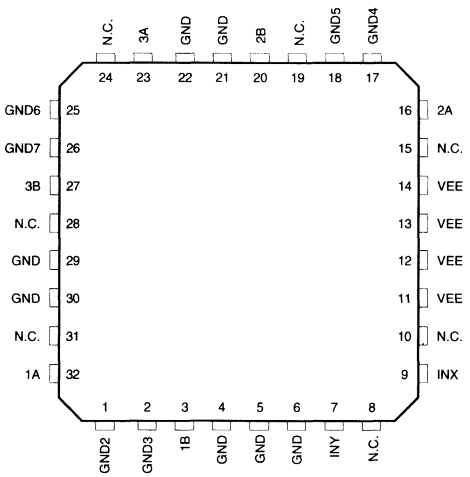
QFP32
(Plastic Package)

ORDER CODE : STV1389AQ

DESCRIPTION

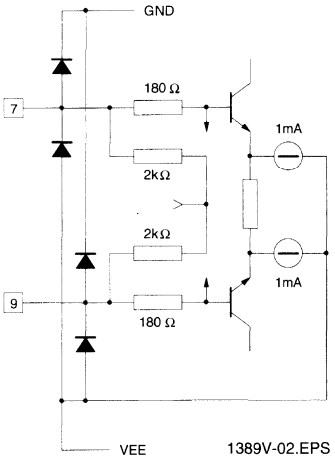
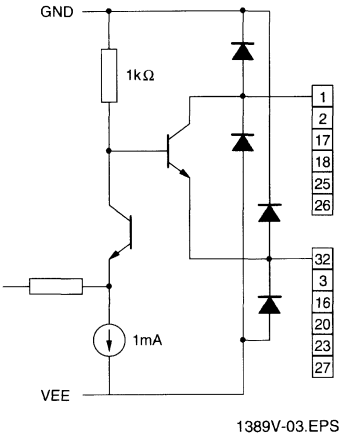
The STV1389AQ offers in a single-chip a complete IC driver for digital data transfer.

PIN CONNECTIONS



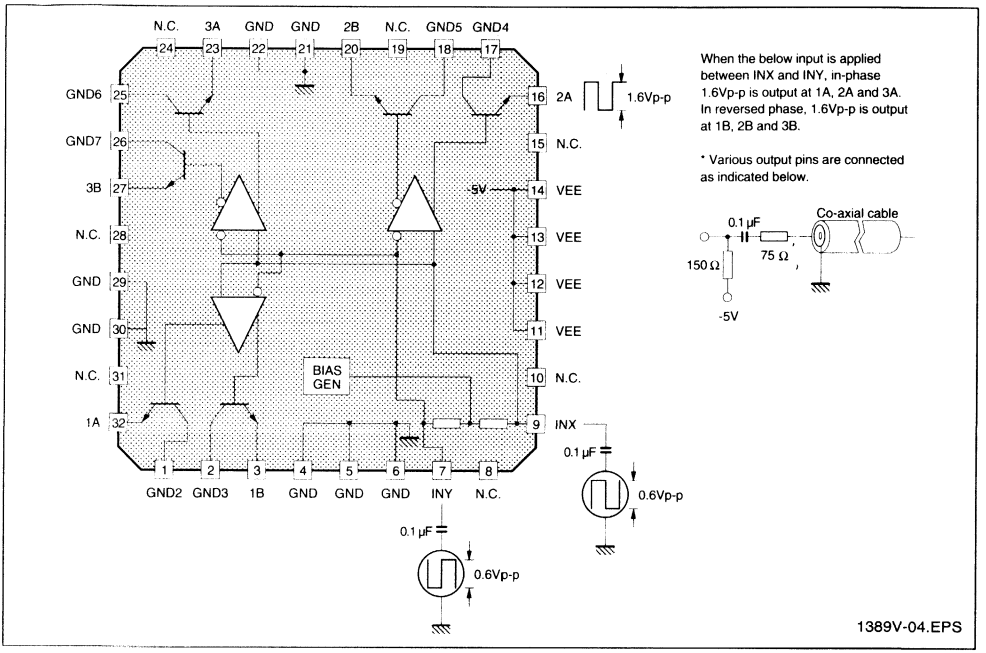
1389V-01.EPS

PIN DESCRIPTION

Pin Number	Symbol	Standard DC Voltage	Equivalent Circuit	Description
7 9	INY INX	- 2.7V		Input pin of the differential amplifier. Input executed after DC portion is cut off.
1 2 17 18 25 26	GND2 GND3 GND4 GND5 GND6 GND7	-		Collector of the emitter follower output Tr. Connect to GND.
32 3 16 20 23 27	1A 1B 2A 2B 3A 3B	- 2.7V		Emitter of emitter follower output Tr. To use, connect pull-down resistor. (Even when only 1 side is used pull-down is executed In pairs.) Pairs 32 16 23 3 20 27

1389V-01.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
T_{stg}	Storage Temperature	- 65, + 150	°C
P_D	Allowable Power Dissipation	500	mW

1389V-02.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.8 to 5.2	V
T_{opr}	Operating Temperature	- 20, + 75	°C

1389V-03.TBL

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Bias Conditions		SW ON	Test Point	Test	Min.	Typ.	Max.	Unit
		V INY	V INX							
V1	Pin Voltage INY	-	-	-	Pin 7	Test of pin voltage	- 2.9	- 2.7	- 2.5	V
V2	Pin Voltage INX	-	-	-	PIn 9		- 2.9	- 2.7	- 2.5	V
A1-1	PIn Voltage 1A	-	-	-	Pin 32		- 3.1	- 2.7	- 2.5	V
B1-1	Pin Voltage 1B	-	-	-	Pin 3		- 3.1	- 2.7	- 2.5	V
A2-1	PIn Voltage 2A	-	-	-	Pin 16		- 3.1	- 2.7	- 2.5	V
B2-1	Pin Voltage 2B	-	-	-	Pin 3		- 3.1	- 2.7	- 2.5	V

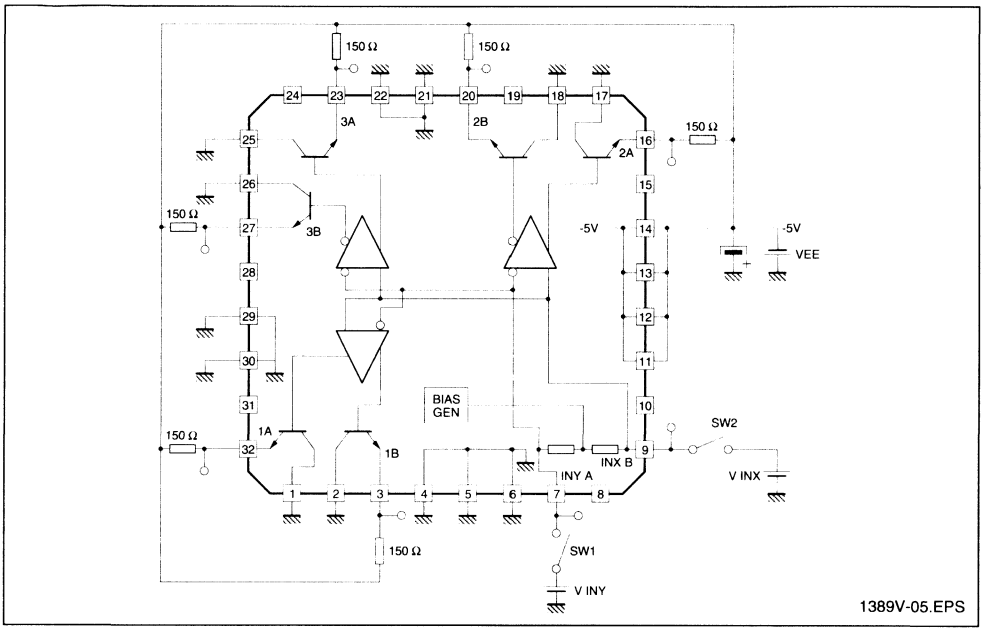
1389V-04.TBL

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Bias Conditions		SW ON	Test Point	Test	Min.	Typ.	Max.	Unit
		V INY	V INX							
A3-1	PIn Voltage 3A	-	-	-	Pin 23	Test of pin voltage	- 3.1	- 2.7	- 2.5	V
B3-1	Pin Voltage 3B	-	-	-	Pin 27		- 3.1	- 2.7	- 2.5	V
IEE	Current Power Supply	-	-	-	VEE	Current power supply at VEE	- 143		- 77	mA
A1-2	DC applied 1A	V1 + 0.2	V2 - 0.2	SW1 SW2	Pin 32	Output DC voltage is tested when +0.2V is applied to INY and - 0.2V to INX. (A1-2) = Test value - (A1-1) (B1-2) = Test value - (B1-1) The difference with the previous pin voltage is recorded. Same for A2-2, B2-2, A3-2, B3-2	0.31	0.39	0.47	V
B1-2	DC applied 1B	↓	↓		Pin 3		- 0.47	- 0.39	- 0.31	V
A2-2	DC applied 2A	↓	↓		Pin 16		0.31	0.39	0.47	V
B2-2	DC applied 2B	↓	↓		Pin 20		- 0.47	- 0.39	- 0.31	V
A3-2	DC applied 3A	↓	↓		Pin 23		0.31	0.39	0.47	V
B3-2	DC applied 3B	↓	↓		Pin 27		- 0.47	- 0.39	- 0.31	V
V1-1	Amplitude 1A + 1B	Calculation				(V1-1) = (A1-2) - (B1-2) Amplitude calculated from T10 with T15 as base, same for V2-1, V3-1.	0.65	0.75	0.85	V
V2-1	Amplitude 2A + 2B	Calculation					0.65	0.75	0.85	V
V3-1	Amplitude 3A + 3B	Calculation					0.65	0.75	0.85	V
-	Amplitude 1A/1B	Calculation				(A1-2) / (B1-2)	0.85	1.0	1.15	-
-	Amplitude 2A/2B	Calculation					0.85	1.0	1.15	-
-	Amplitude 3A/3B	Calculation					0.85	1.0	1.15	-
A1-3	DC applied 1A'	V1 - 0.4	V1 + 0.4	SW1 SW2	Pin 32	Output DC voltage is tested when - 0.4V is applied to INY and + 0.4V to INX. (A1-3) = Test value - (A1-1) (B1-3) = Test value - (B1-1) The difference with the previous pin voltage is recorded. Same for A2-3, B2-3, A3-3, B3-3	- 0.9	- 0.75	- 0.6	V
B1-3	DC applied 1B'	↓	↓		Pin 3		0.6	0.75	0.9	V
A2-3	DC applied 2A'	↓	↓		Pin 16		- 0.9	- 0.75	- 0.6	V
B2-3	DC applied 2B'	↓	↓		Pin 20		0.6	0.75	0.9	V
A3-3	DC applied 3A'	↓	↓		Pin 23		- 0.9	- 0.75	- 0.6	V
B3-3	DC applied 3B'	↓	↓		Pin 27		0.6	0.75	0.9	V
V1-2	Amplitud'e 1A' + 1B	Calculation				(V1-2) = (A1-3) + (B1-3) Amplitude calculated from T22 with T27 as base, same for V2-2, V3-2.	1.3	1.5	1.7	V
V2-2	Amplitude 2A' + 2B'	Calculation					1.3	1.5	1.7	V
V3-2	Amplitude 3A' + 3B'	Calculation					1.3	1.5	1.7	V
-	Amplitude 1A' + 1B'	Calculation				(A1-3) / (B1-3)	0.85	1.0	1.15	V
-	Amplitude 2A' + 2B'	Calculation				(A2-3) / (B2-3)	0.85	1.0	1.15	V
-	Amplitude 3A' + 3B'	Calculation				(A3-3) / (B3-3)	0.85	1.0	1.15	V
V1-3	Linearity 1	Calculation				(V1-2) / (V1-1)	1.7	1.9	2.1	V
V2-3	Linearity 2	Calculation				(V2-2) / (V1-1)	1.7	1.9	2.1	V
V3-3	Linearity 3	Calculation				(V3-2) / (V1-1)	1.7	1.9	2.1	V

1389V-05.TBL

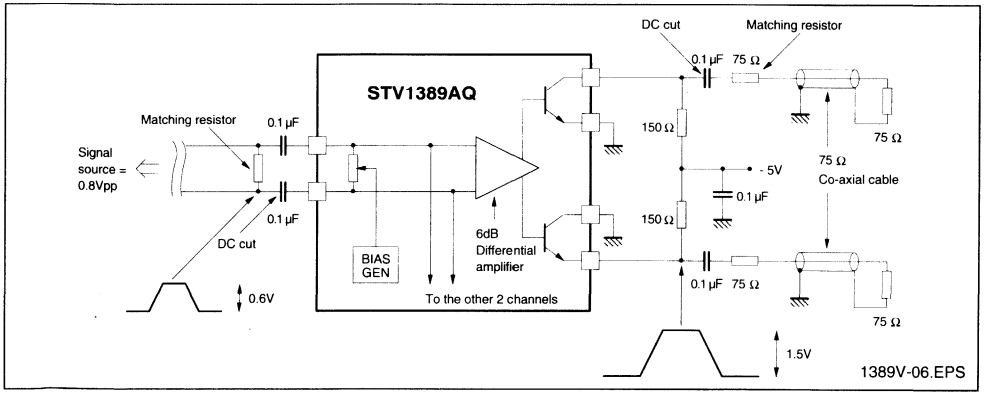
TEST CIRCUIT



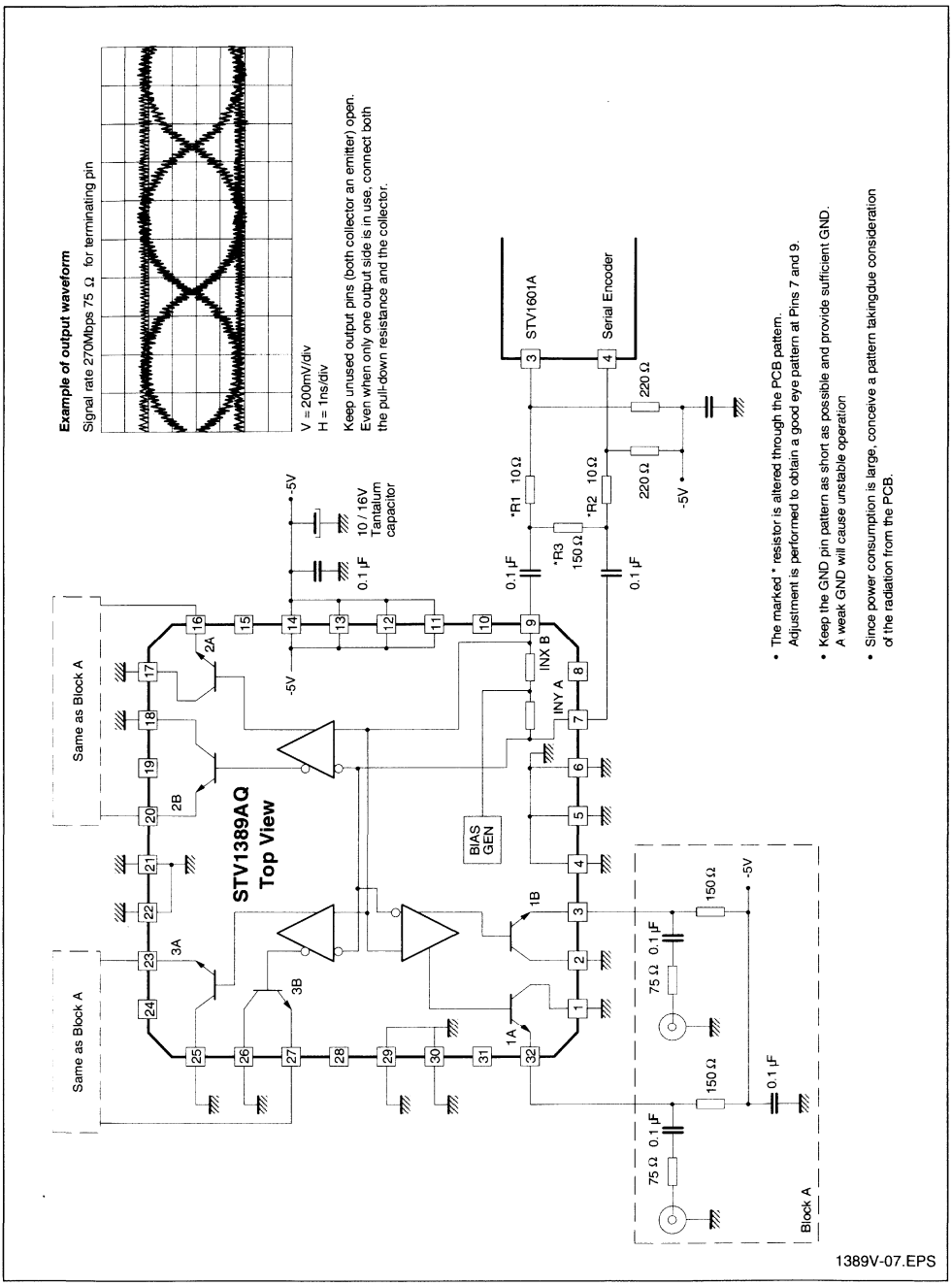
DESCRIPTION OF OPERATION

The STV1389AQ consists of 3 differential amplifier with a common input and a bias generator, and three differential outputs. Each amplifiers provides a 6dB gain and is configured as a differential output feeding the bases of a pair of current boosting on-chip emitter follower transistors. The differential input pins are internally biased and the input signal is ac-coupled to remove the D.C. component.
Between the output pins of each differential amplifier and the coaxial cable, an R-C network is connected to remove D.C. component from the output and for impedance matching. The series resistor has a value of 68 to 75Ω to match a 75Ω coaxial cable. In this manner a signal almost identitical in level to the input signal is transferred to the coaxial cable.

Optimum PCB layout and matching resistor value are chosen to obtain good eye pattern design at the input pins. This is necessary because the waveform distortion at the input pins is directly transferred to the output waveform.



TEST CIRCUIT



SGS-THOMSON MICROELECTRONICS

STV1601A

SERIAL INTERFACE TRANSMISSION ENCODER

THIS IC CONTAINS ALL THE CIRCUITS NEEDED FOR CONVERSION FROM PARALLEL DATA, AND PARALLEL CLOCK, INTO SERIAL DATA. APPLICATIONS ARE STRAIGHTFORWARD AS ONLY A FEW EXTERNAL COMPONENTS ARE NEEDED.

OTHER RELATED IC's INCLUDE :

- STV1602A, A SERIAL TRANSMISSION DECODER (WITH A BUILT-IN CABLE EQUALIZER AND PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION ENCODER

- 100 to 270 Mb/s

APPLICATIONS EXAMPLES

- Serial data transmission of digital television signal 525-625 lines
- 4:2:2 component 270Mb/s (10-BIT)
- 4*FSC PAL composite 177Mb/s (10-BIT)
- 4*FSC NTSC composite 143Mb/s (10-BIT)

FUNCTIONS

- Parallel-to-serial conversion
- Scrambler : Modulo - 2 division by $G(x) = (x^9 + x^4 + 1)(x + 1)$
- PLL for serial clock generation
- PLL lock detection
- Sync word required with the parallel data stream

	8 bit	10 bit
1st word	FFH	3FFH
2nd word	00H	000H
3rd word	00H	000H

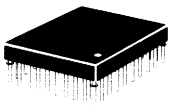
Sync word conversion (8-bit timing reference signal is internally converted to 10-bit).

CODE LIMITATION

The word composing the Sync word listed above shall not appear during data words.
This limitation includes 00 and FF in 8-bit use and 000 through 003 and 3FC through 3FF in 10-bit use.

DESCRIPTION

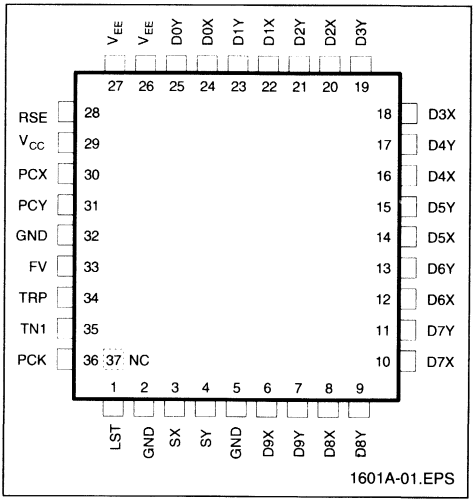
The STV1601A is a Hybrid IC encoder that converts parallel data into serial data for a serial transmission line.



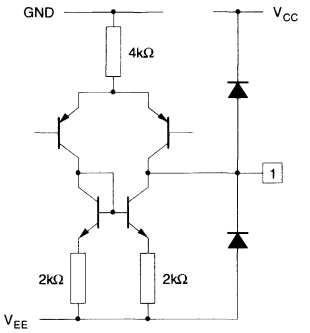
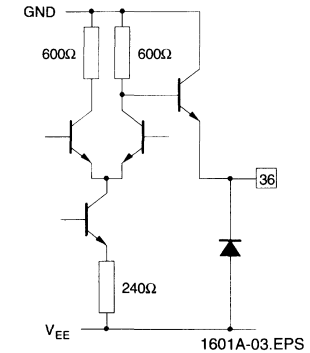
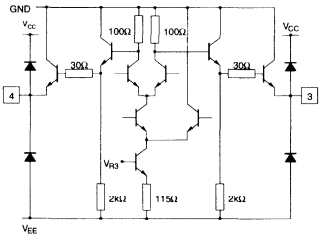
PGA37
(Ceramic Package)

ORDER CODE : STV1601A

PIN CONNECTIONS

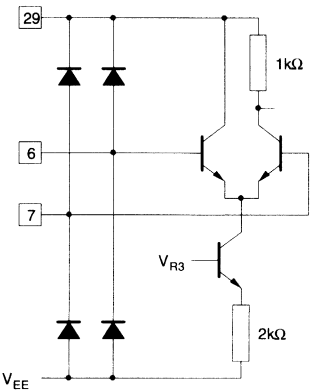
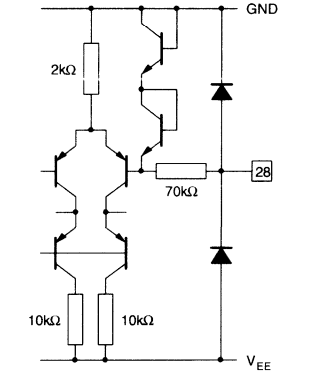


PIN DESCRIPTION

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
1	LST	 1601A-02.EPS	PLL lock detection. Is High while PLL locked. If unlocked, becomes irregular. At free running (TN1 H) turns Low H L	O	 -1.0	 	 -4.0	 V V
36	PCK	 1601A-03.EPS	Clock output frequency divided to 1/10 VCO output. Used to check VCO free running frequency H L	O		 -0.8 -1.6		 V V
3	SX	 1601A-04.EPS	Differential Serial Output Input parallel data is converted to serial, then from scrambled NRZ to NRZI data H L	O		 -1.6 -2.4		 V V
4	SY							

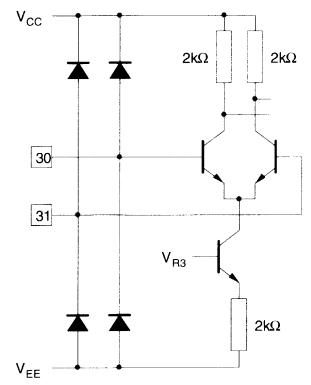
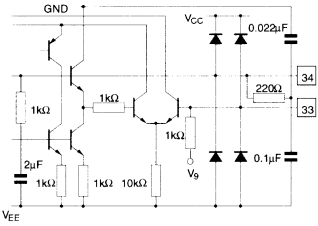
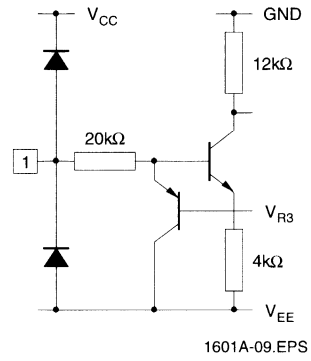
1601A-01.TBL

PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
29	V_{CC}	 1601A-05.EPS	Parallel data and clock input buffers power supply. When this pin is connected to +5V, parallel data clock turns to TTL mode. When this pin is connected to GND, parallel data clock turns to ECL mode.	-				
6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	D9X D9Y D8X D8Y D7X D7Y D6X D6Y D5X D5Y D4X D4Y D3X D3Y D2X D2Y D1X D1Y D0X D0Y		Parallel input ports: LSB : D0X or Y MSB : D9X or Y Signal : DnX Return : DnY For ECL mode, V_{CC} shalll be 0V H L ForTTL mode, VCC shall be +5V H L		 -1.0 2.0	 -1.6 0.8	 V V V V
28	RSE	 1601A-06.EPS	VCO range selection H : high range 140 to 270MHz L : low range 100 to 145MHz H L	I	 -0.4		 -4.0	 V V

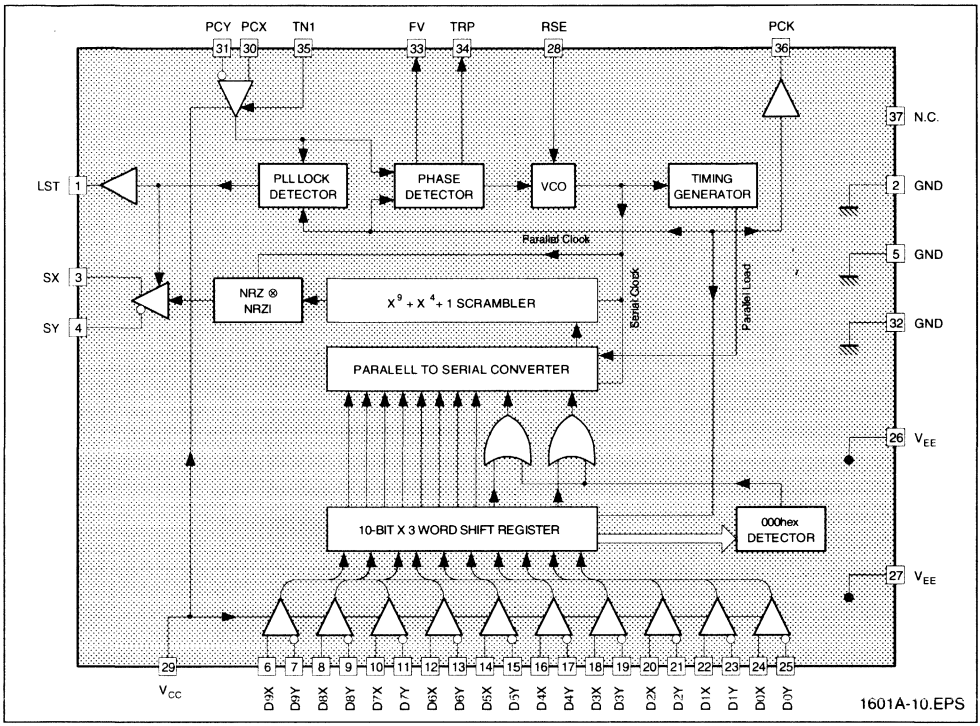
1601A-02.TBL

PIN DESCRIPTION (continued)

Pin N	Symbol	Equivalent circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
30	PCX	 1601A-07.EPS	Parallel clock (PCX) and its return (PCY) For ECL mode, V_{CC} = 0 H L For TTL mode, V_{CC} = +5V H L	I	 -1.0 2.0		 -1.6 0.8	 V V V V
31	PCY							
2, 5, 32	GND		GND					
26	V_{EE}		-5V power supply I/O buffer PLL		-5.2	-5.0	-4.8	V
27	V_{EE}		-5V power supply Logic part		-5.2	-5.0	-4.8	V
33	FV	 1601A-08.EPS	VCO free running frequency adjustment : V_{EE} level gives the lowest frequency. To adjust, set TN1 high.	I		-3.9		V
34	TRP		VCO input and phase comparator output should be connected to a parallel clock frequency trap filter to minimize jitter	O		-3.2		V
35	TN1	 1601A-09.EPS	Test mode : High : VCO free running condition (input disabled) Low : Normal mode (input enabled)	I	-1.0		 -4.5	V V

1601A-03.TBL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{CC}	Supply Voltage	+6	V
V_{IN}	Input Voltage	V_{EE} to V_{CC}	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

1601A-04.TBL

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
V_{CC}	Supply Voltage *	4.8 to 5.2	V
T_{oper}	Operating Temperature	0 to 65	°C

1601A-05.TBL

* For TTL input. Voltages are given with respect to GND

ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{EE}	Supply Current 1		Figure 2		140		mA
I_{CC}	Supply Current 2				7		mA

1601A-06.TBL

ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
V_{IH}	Input Voltage	V_{CC} = GND PCX, PCY, DnX, DnY		-1.0			V
V_{IL}						-1.6	V
V_{IH}		V_{CC} = +5V PCX, PCY, DnX, DnY		2.0			V
V_{IL}						0.8	V
I_{IH}	Input Current	PCX, PCY, DnX, DnY	Figure 3			5	µA
I_{IL}				-1		+1	µA
V_{IH}	Input Voltage	RSE	Figure 7	-0.4			V
V_{IL}						-4.0	V
V_{IH}		TN1	Figure 6	-1			V
V_{IL}						-4.5	V
V_{OH}	Output Voltage	PCK R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_{OH}		LST I_{OH} = -10µA, I_{OL} = +10µA	Figure 5	-1.0			V
V_{OL}						-4.0	V
V_{OH}		SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V
AC CHARACTERISTICS							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 4	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1					14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2					10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 1	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.8			MHz
f_{LP2}						16.5	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.0	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz
tjit	Jitter	f signal = 270MHz RSE = "H"	Figure 8			±0.25	nsec

Tested through PCK : 1/10 of serial clock.

1601A-07.TBL

SWITCHING CHARACTERISTICS (V_{EE} = -5V, V_{CC} = GND/+5V, T_A = 25°C unless otherwise speciied)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	PCK R_P = 1kΩ	Figure 10		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec

1601A-08.TBL

TIMING RELATION OF INPUT CLOCK AND DATA

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_w	Pulse Width	PCX, PCY	Figure11	-5 + t_c/2	t_c/2	+5 + t_c/2	nsec
t_d	Delay Time	PCX - Dn		-5		+5	nsec

1601A-09.TBL

Figure 1 : Test Circuit Diagram Example

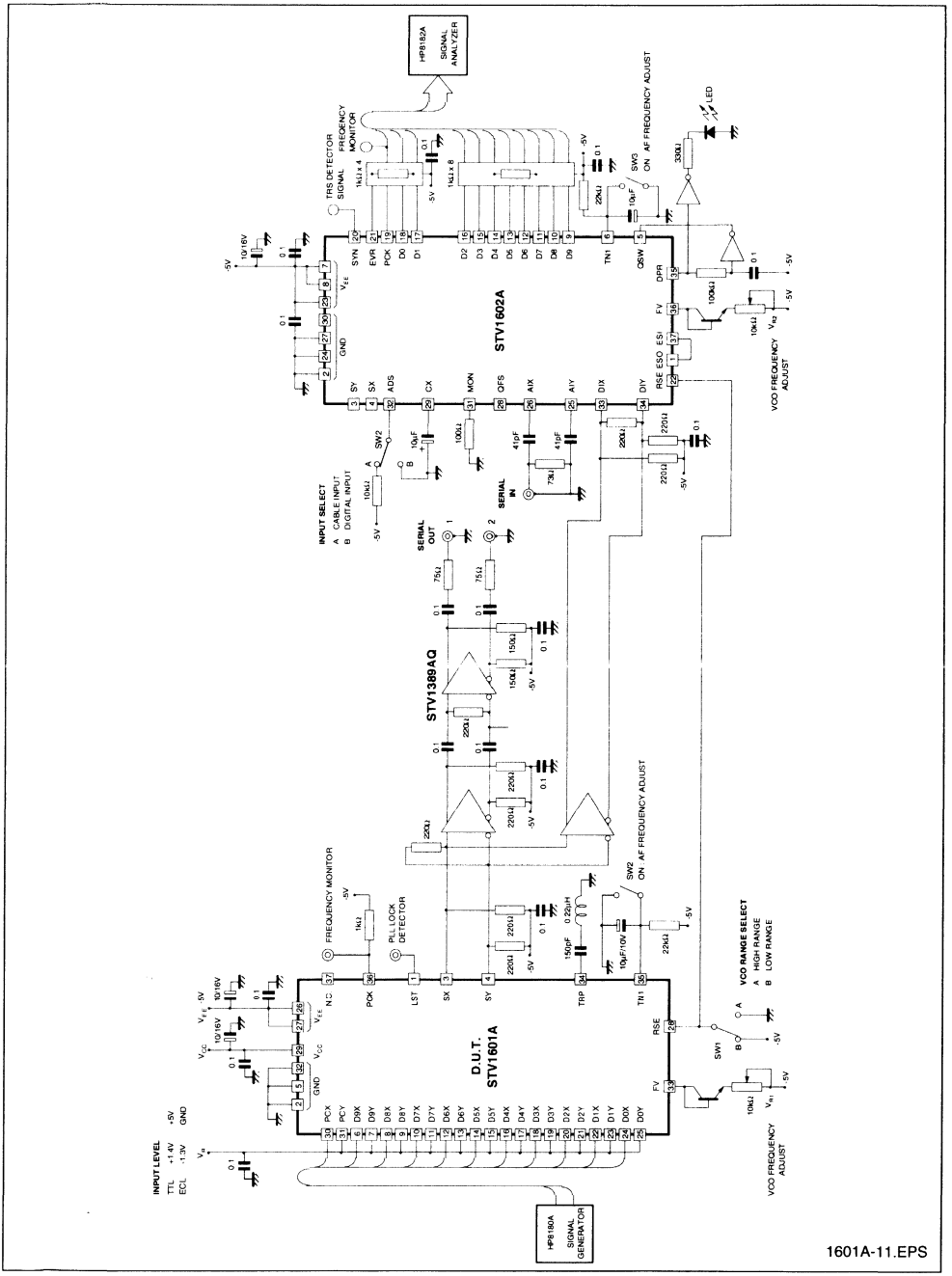


Figure 2

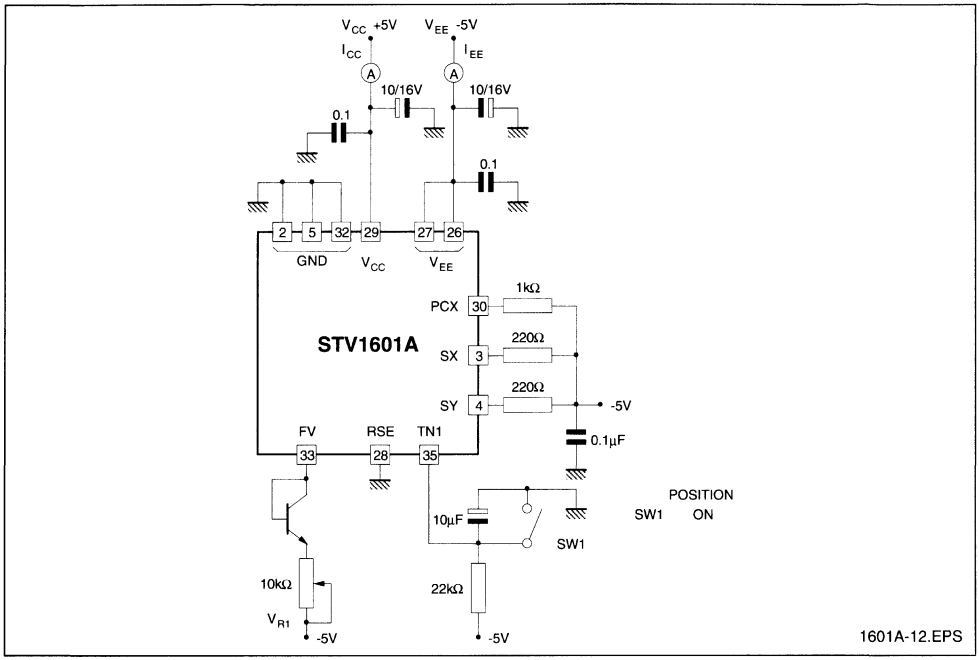


Figure 4

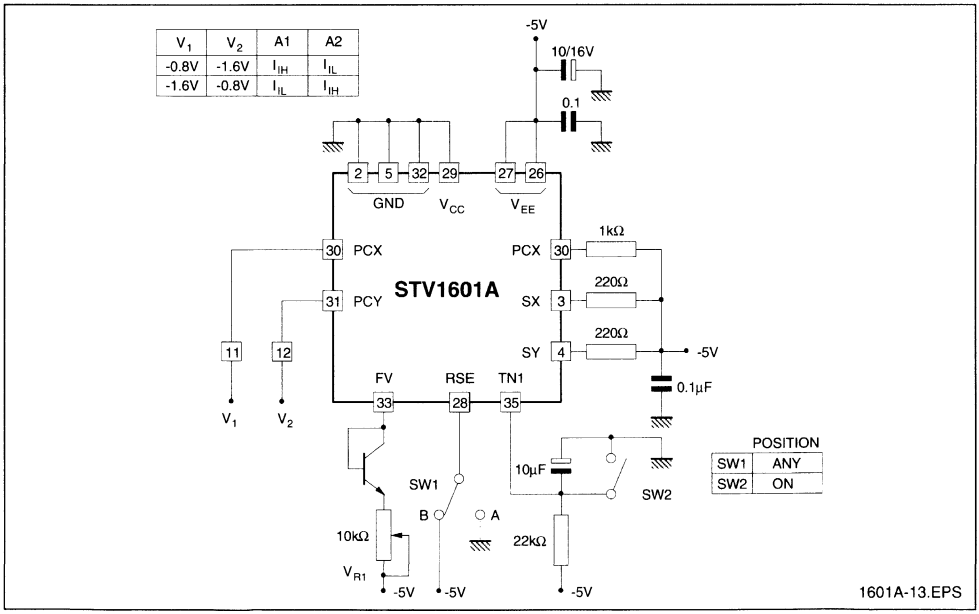


Figure 4

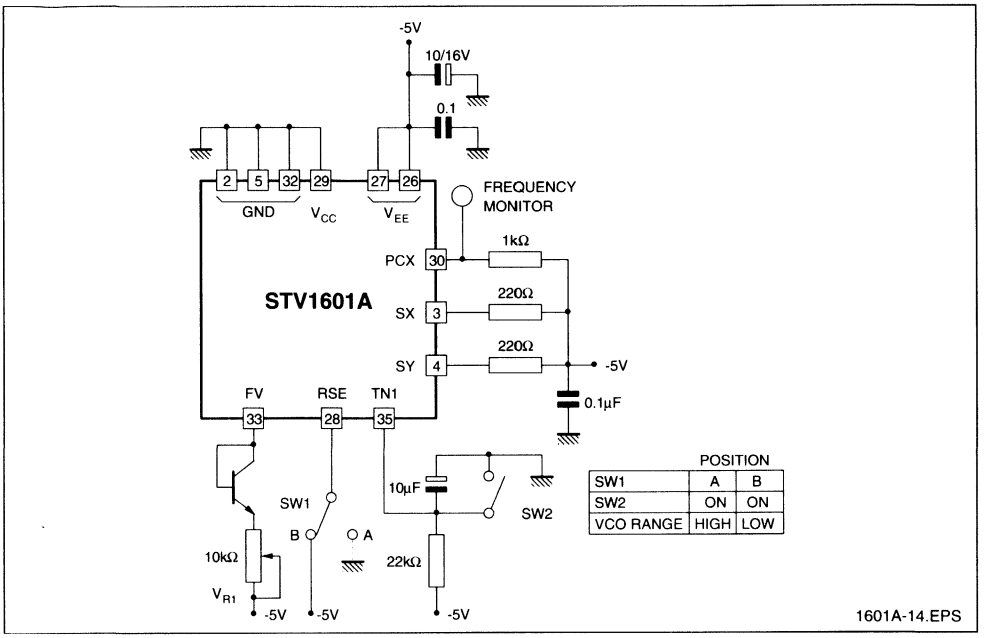


Figure 5

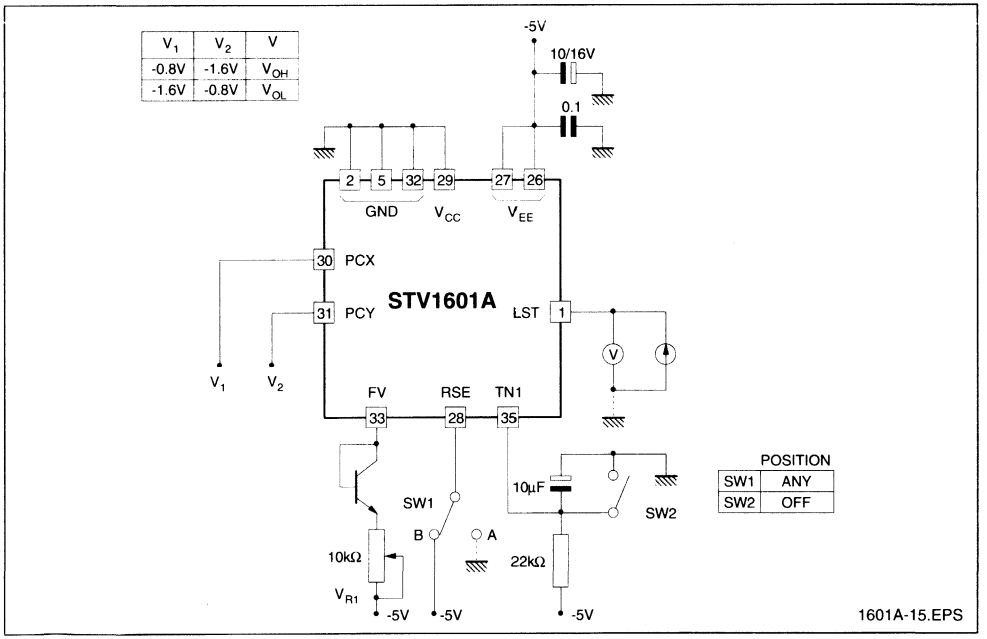


Figure 6

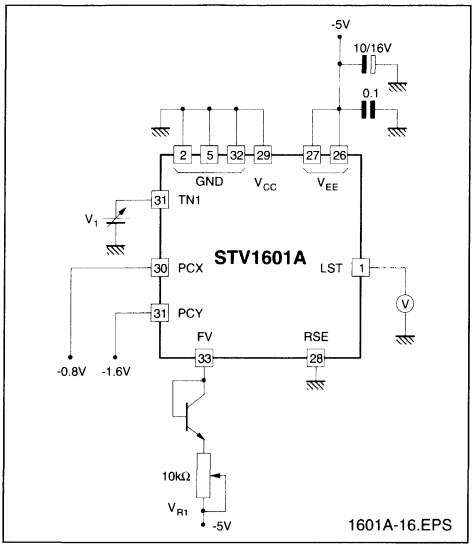


Figure 7

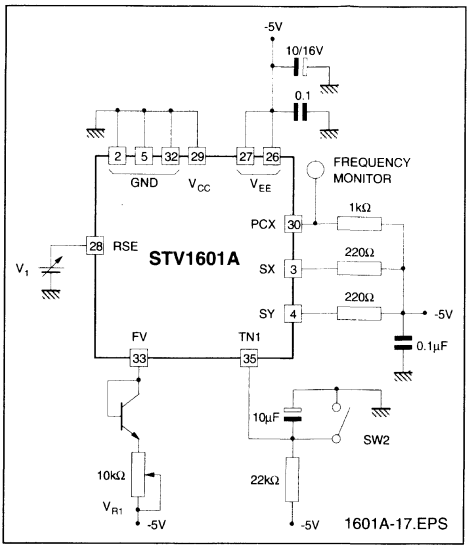


Figure 8

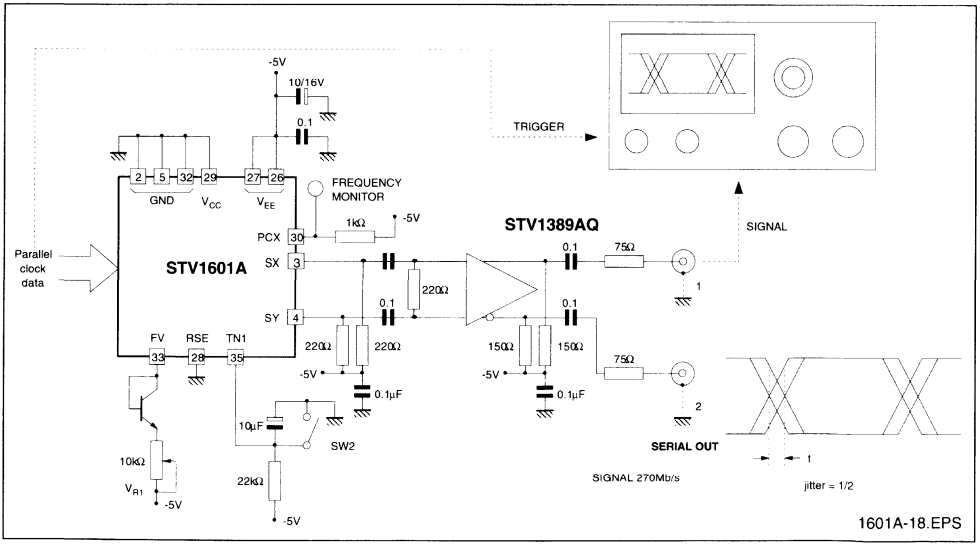


Figure 9 : t_r, t_f Definition

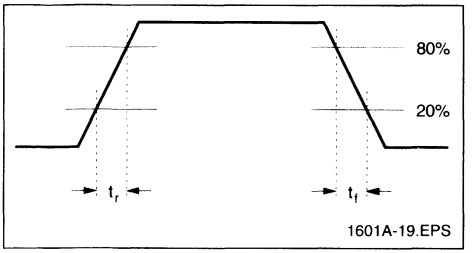
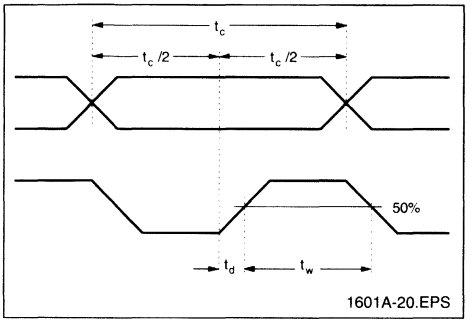


Figure 10 : t_d, t_W Definition



DESCRIPTION

STV1601A internally generates a 10 times clock frequency locked to the parallel input clock thanks to a built-in PLL and converts input parallel data into serial data.

To ease clock extraction at the receiving end, serial data is scrambled. To minimize polarity effect, serial data is then converted to NRZI and output in differential mode.

A PLL lock detection circuit only enables the serial output when locked.

1. Phase relation between input parallel clock and data

The phase relation between the parallel clock and the data is shown in Figure 11. Both clock and data are differential inputs

Parallel clock and data are such that the rising edge of PCX should be at the middle of the data. A clock having the same phase as PCX is internally generated in order to latch the data.

2. TTL input operation

Parallel clock and data can be either TTL or ECL inputs. To use as TTL inputs VCC (Pin 29) shall be connected to +5V. A fixed bias of +1.4V shall be applied to PCY and DnY (n = 0 to 9). TTL signals and their parallel clock will be provided through 1kW resistors to each "X" input. These 1kW resistors are effective to minimize the influence of the TTL input signals to the jitter characteristics of the serial output signal. For 8-bit data, unused LSB(s) must be fixed Low. Fixed bias value can be higher, for example, 2.5V in case of CMOS inputs.

Figure 11 : Phase Relation between Clock and Data

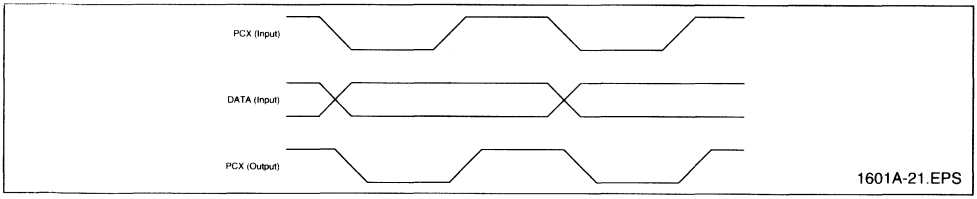
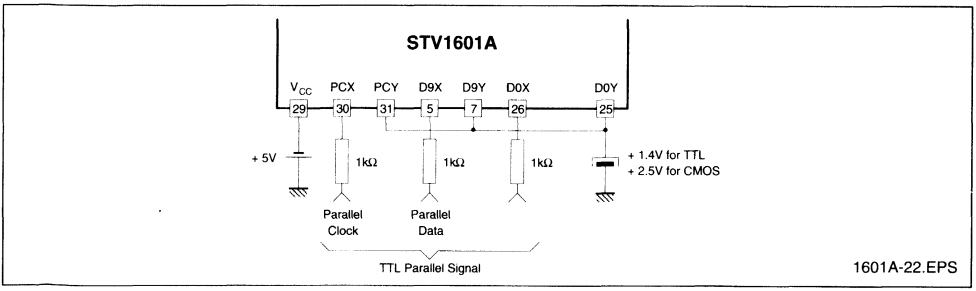


Figure 12 : TTL Input Operation



3. PLL block

PARALLEL CLOCK INPUT CONTROL

PLL, PLL lock detection and the various blocks of the serial output control are shown in Figure 13. When TN1 is connected to GND (set High), the parallel clock input is disabled.

The VCO turns to free running conditions and its frequency can be adjusted through FV.

This frequency decreases when the resistor value between FV and V_{EE} is reduced. Oscillation frequency monotoring is performed through PCK which delivers a frequency divided by ten.

When PLL is locked, PLL and PCX input signal phases are nearly matched. The RC network connected to TN1, temporarily, disables the parallel clock in order to avoid mislocking problems.

VCO oscillation frequency range selection is available through RSE ; High : from 140 to 270MHz ; Low : from 100 to 145MHz.

TRP (Pin 34) is the phase comparator output. To minimize jitter, a trap circuit, consisting in a serial tuned circuit at parallel clock frequency can be used.

PLL LOCK DETECTION

The LST signal is generated by latching the incoming parallel clock by the internal one (which is 1/10 of the VCO frequency). LST is used as a PLL lock detection signal and also controls the serial output.

If the parallel clock input is disabled (by means of TN1), LST turns Low and the serial output is disabled as described in the previous section (SX (Pin 3) = High, SY (Pin 4) = Low).

If the serial output has to be disabled while no parallel clock input is provided, PCX must be set Low and PCY must be set High.

4. Sync word

To convert serial data back to parallel, insertion of some timing reference data indicating the parallel data word boundary in the serial data is needed. This, called TRS (Timing Reference Signal) in the digital interface format, consists of the three consecutive words 3FFH, 000H, 000H.

Conversion to 10-bit TRS from 8-bit (TRS)

8-bit parallel data

8-bit parallel data can be converted into 10-bit data by using the 8th bit as the MSB and by setting the 2 LSBs at logical states as shown in Figure 14.

Figure 13 : PLL and Serial Output Control Block

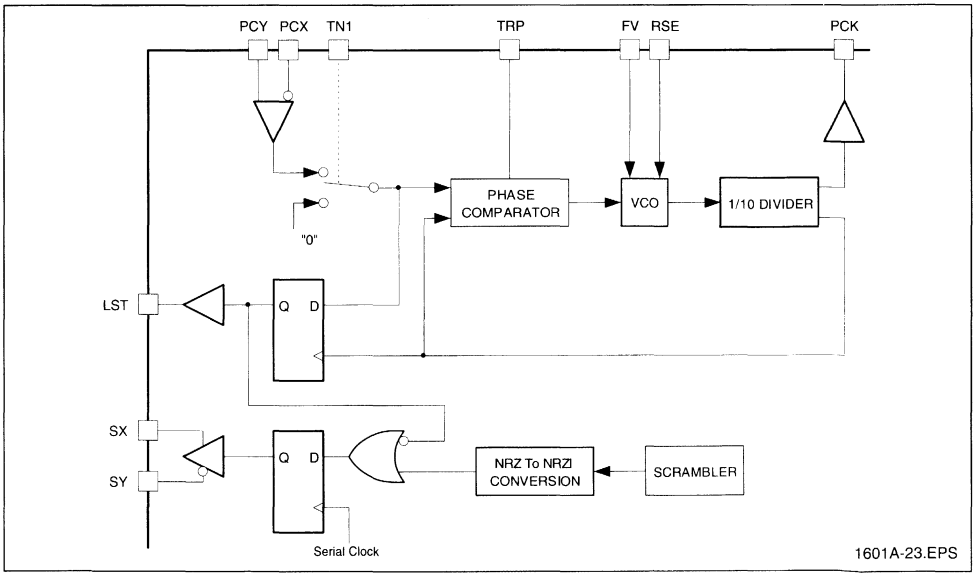
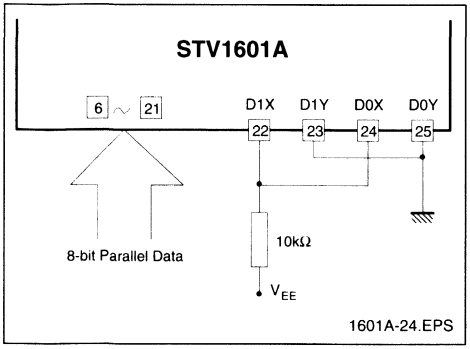
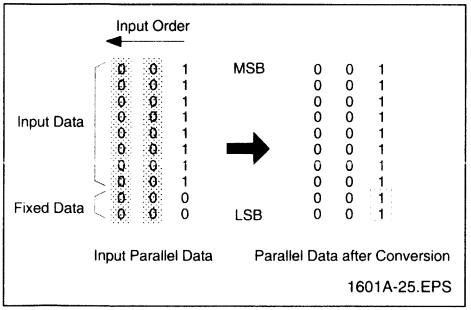


Figure 14 : 8-bit Parallel Input Data (ECL level)



The conversion algorithm detects 2 successive 000H words and sets the two LSBs of the previous word, which is supposed to be FF, according to the standard.

Figure 10 : Conversion from 8-bit TRS to 10-bit TRS



Conversion in the case of more than three successive "000H" words.

If more than 3 consecutive words of 000 in D1 standard, or 4 consecutive words of 000 in D2 standard occur at the parallel input (illegal according to the standard), thus no proper operation is possible.

5. Scrambling and NRZ to NRZI conversion

Figures 16 and 17 show the scrambling circuit, the scrambling polynomial is as follows : $x^9 + x^4 + 1$.

Figure 16 : $(x^9 + x^4 + 1)$ Basic Scrambling Circuit

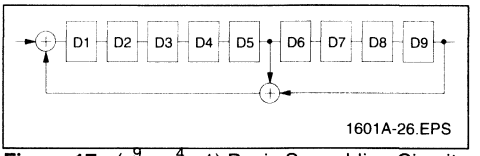
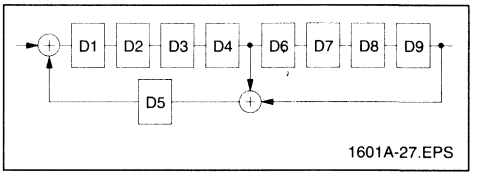


Figure 17 : $(x^9 + x^4 + 1)$ Basic Scrambling Circuit



To eliminate signal polarity of scrambled data, conversion from NRZ to NRZI is performed (Figures 18 and 19).

Therefore, the polarity for output distribution or receiving is not needed. This allows easy system design. The NRZ to NRZI polynominal is x + 1.

VCO temperature compensation and oscillation frequency adjustment

VCO oscillation frequency depends on the temperature as shown in Figures 22 and 23 "Representative characteristics examples". Within the normal range of operation, frequency increases with temperature. FV voltage remains almost constant regardless of temperature. Figure 20 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor connected between FV and V_{EE}. Examples of representative characteristics for various temperatures are shown in Figures 22 and 23 concerning oscillation frequency and PLL pull-in range (signal frequency 270, 177 and 143MHz).

VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO free runs. Wait for 5 to 10 minutes after turning power supply ON (warm up time). While monitoring PCK output (Pin 36) adjust the signal frequency (within ± 1%) with the variable resistor connected between FV and V_{EE}.

Figure 19 : Relation between NRZ and NRZI Signals

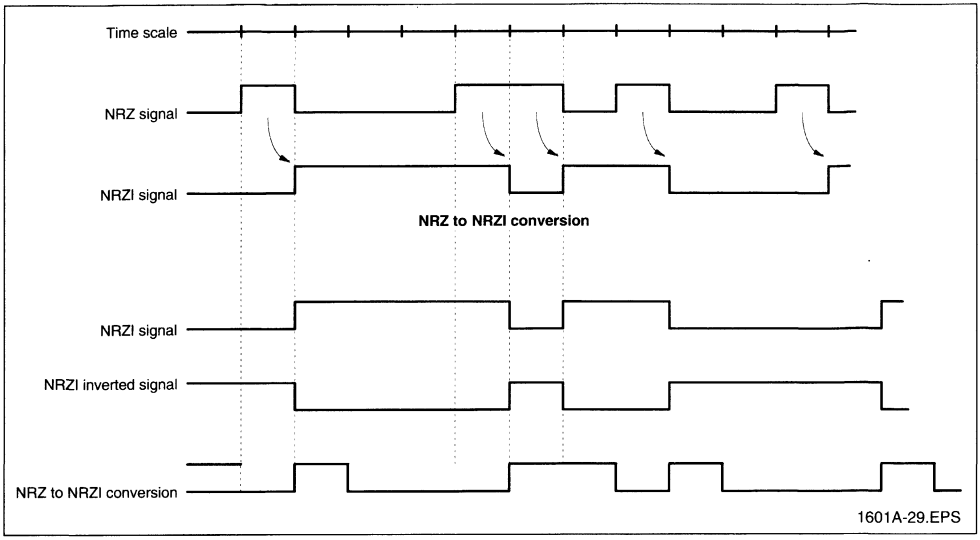
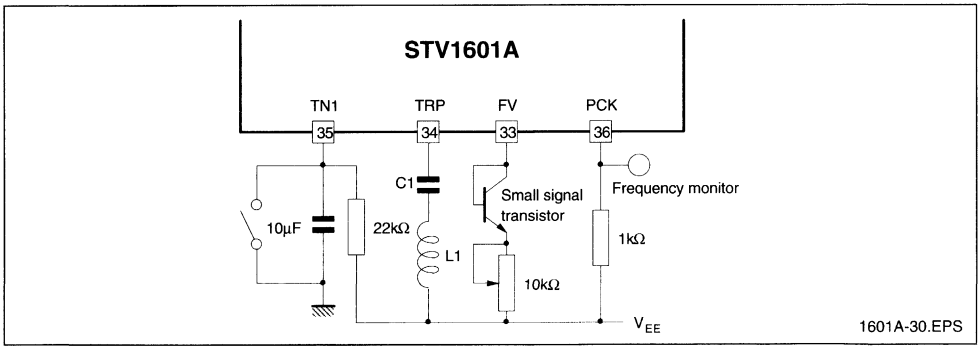


Figure 20 : VCO Temperature Compensation and Free Running Adjustment



Jitter trap

Since the internally generated serial clock is locked to the incoming parallel clock, there exists periodic jitter components which are generated from the phase comparison process of the PLL.

A serial resonant circuit (trap) connected between TRP (Pin 34) and V_{EE} tuned at the parallel clock frequency reduces effectively the fundamental component of the jitter well below the specification (±0.25ns).

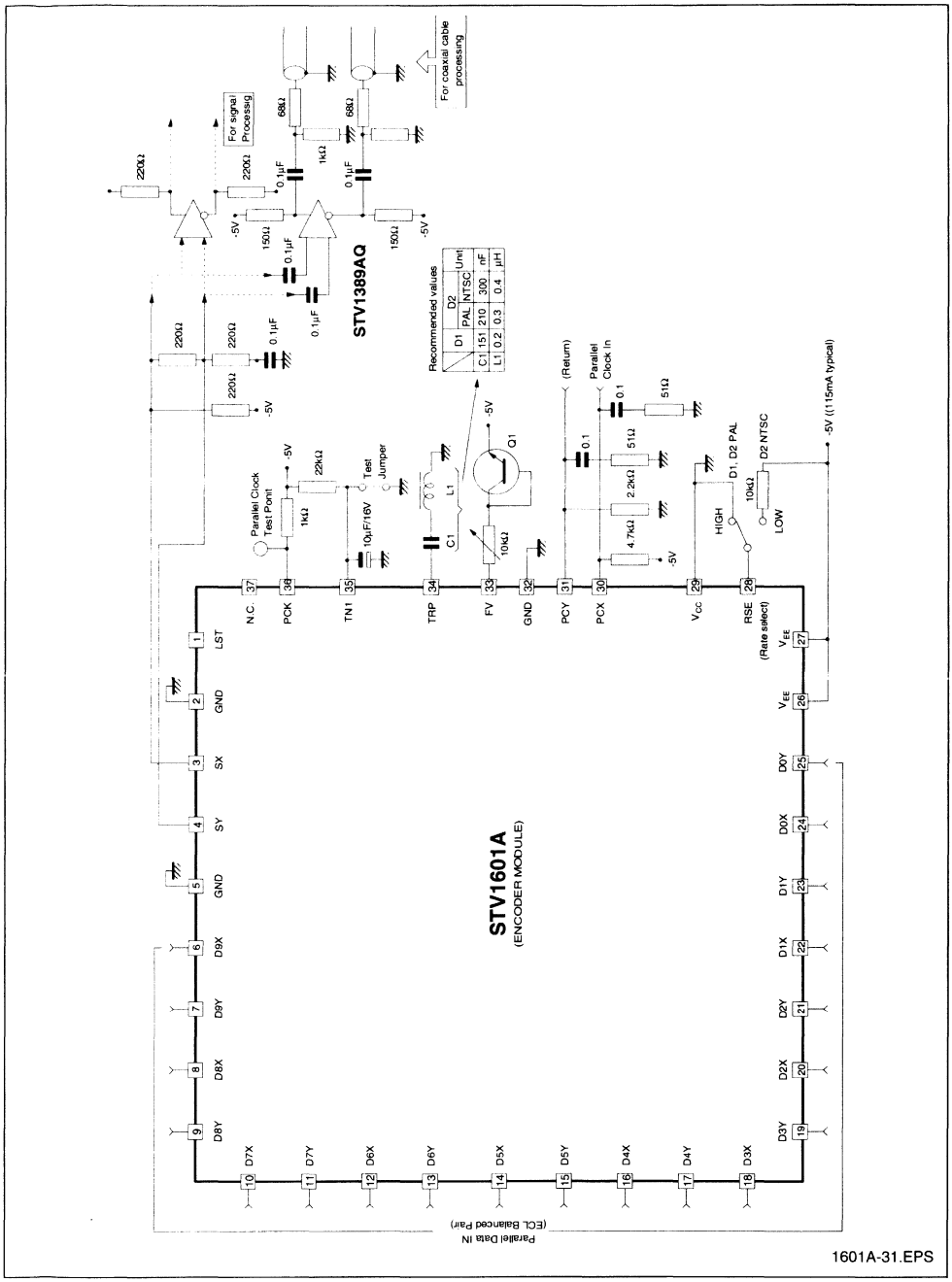
Recommended values of C1 and L1 are given in the following table.

RECOMMENDED VALUES OF THE TRAP CIRCUIT

COMPONENT	STANDARD		
	D1	D2	
		PAL	NTSC
C1 (pF)	150	240	300
L1 (µH)	0.2	0.3	0.4

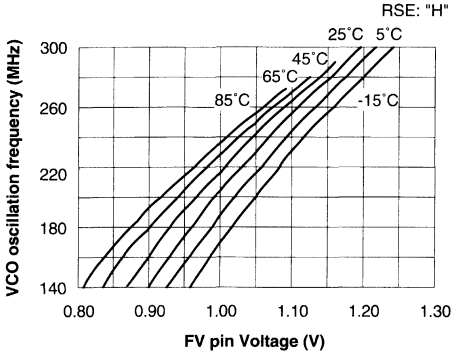
An important remark in a practical implementation is that TRP node is an input of a very sensitive voltage-frequency converter (VCO) which can be easily disturbed by any pick-up noise.
Hence, the trap circuit should be carefully located and be kept as short as possible from the Pin 34 in order to avoid noise problems.

Figure 21 : Application Circuit Example



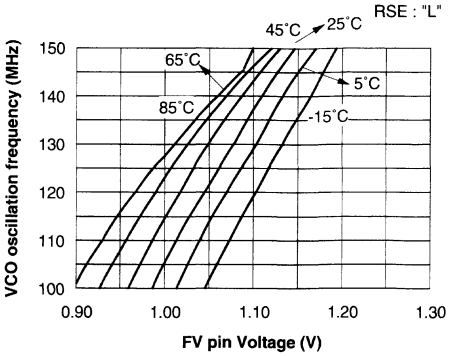
EXAMPLE OF REPRESENTATIVE CHARACTERISTICS

Figure 22 : VCO Oscillation Frequency versus FV Pin Voltage



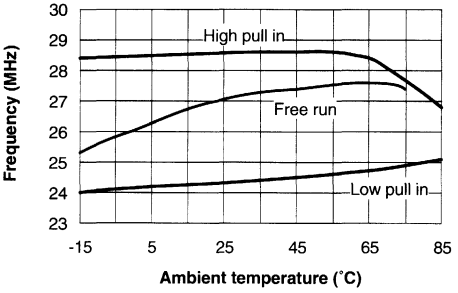
1601A-32.EPS

Figure 23 : VCO Oscillation Frequency versus FV Pin Voltage



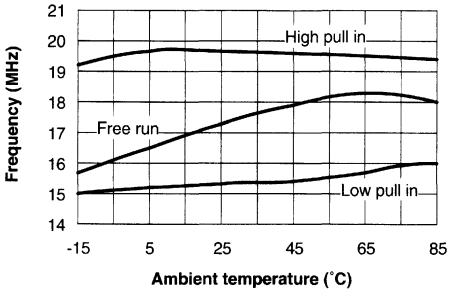
1601A-33.EPS

Figure 24 : Pull in Range and Free Run Frequency (270Mb/s)



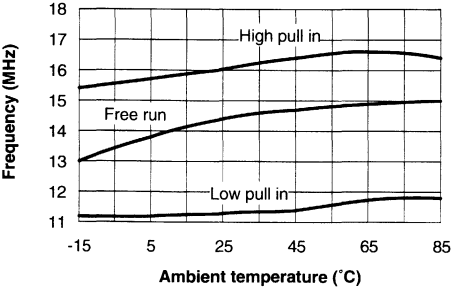
1601A-34.EPS

Figure 25 : Pull in Range and Free Run Frequency (177Mb/s)



1601A-35.EPS

Figure 26 : Pull in Range and Free Run Frequency (143Mb/s)



1601A-36.EPS

SGS-THOMSON MICROELECTRONICS

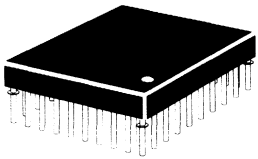
STV1602A

SERIAL INTERFACE TRANSMISSION DECODER

BUILT-IN AUTOMATIC EQUALIZER FOR UP TO 30dB ATTENUATION AT 135MHz (TYPICALLY 300m OF HIGH-GRADE COAXIAL CABLE), PLL CIRCUIT FOR RECLOCKING, AND SERIAL-PARALLEL CONVERSION CIRCUIT.
THIS SERIAL TRANSMISSION DECODER REQUIRES ONLY FEW EXTERNAL COMPONENTS.

OTHER RELATED IC's INCLUDE :

- STV1601A, A SERIAL TRANSMISSION ENCODER (PARALLEL-TO-SERIAL CONVERSION)
- STV1389AQ COAXIAL CABLE DRIVER



PGA37
(Ceramic Package)

ORDER CODE : STV1602A

STRUCTURE

- Hybrid IC

APPLICATIONS

SERIAL DATA TRANSMISSION DECODER

- 100 to 270 Mb/s

APPLICATIONS EXAMPLES

- Serial data transmission of digital television signals 525-625 lines
- 4:2:2 component 270Mb/s (10-bit)
- 4*fsc PAL composite 177Mb/s (10-bit)
- 4*fsc NTSC Composite 143Mb/s (10-bit)

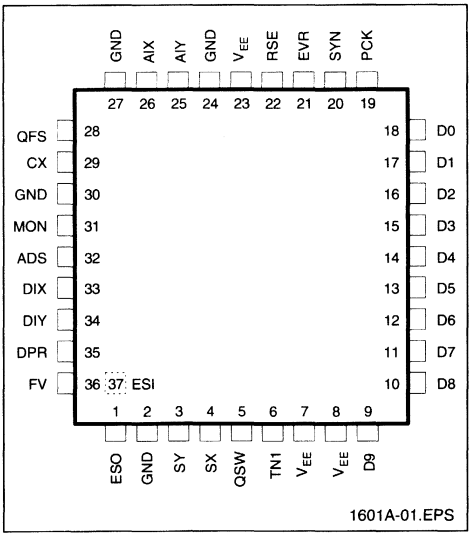
FUNCTIONS

- Cable equalizer (maximum gain : 30dB at 135MHz)
- PLL for serial clock generation
- Reclocked repeater output (active loop through)
- Descrambler : modulo-2 multiplication by $G(x) = (x^9 + x^4 + 1)(x + 1)$
- Parallel-to-serial conversion
- Sync monitor output
- Eye pattern monitoring
- Input signal detector

DESCRIPTION

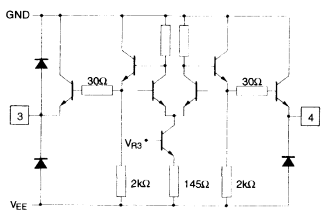
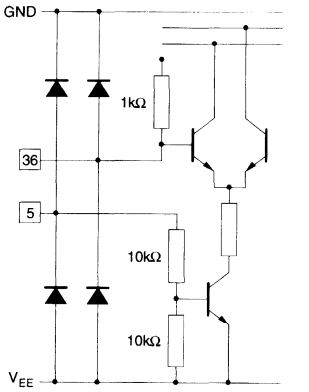
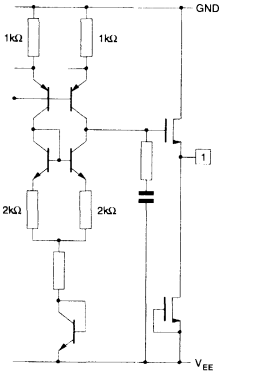
The STV1602A is a Hybrid IC decoder which converts serial data coming from a serial transmission line into parallel data.

PIN CONNECTIONS



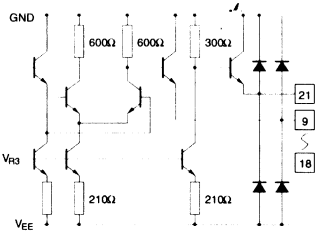
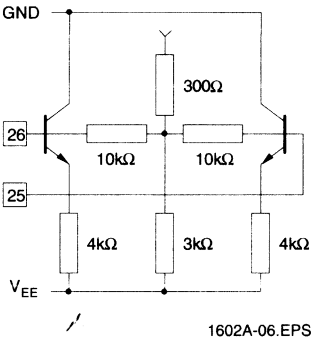
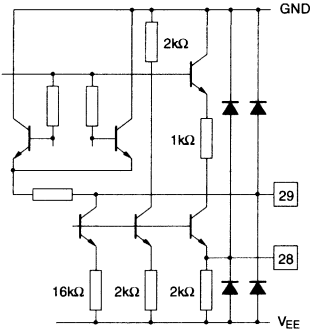
1601A-01.EPS

PIN DESCRIPTION

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
3	SY	 1602A-02.EPS	Reclocked serial data output in differential mode. SX and SY are disabled when TN1 is set High. In this case, SX is set High and SY is set Low	O				
4	SX		H L			-1.6 -2.4		V V
5	QSW (GND)	 1602A-03.EPS	To be connected to GND	I				
36	FV		Adjustment of VCO Free running frequency : V_{EE} level gives the lowest frequency. To adjust it, set TN1 High.	I				
1	ESO	 1602A-04.EPS	Output of phase comparator : must be connected to ESI with the shortest distance	O		-3.2		V

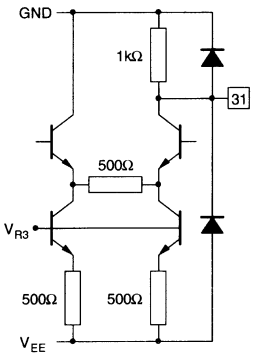
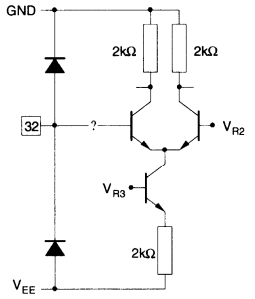
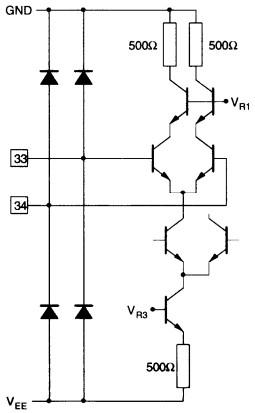
1602A-01.TRI

PIN DESCRIPTION (continued)

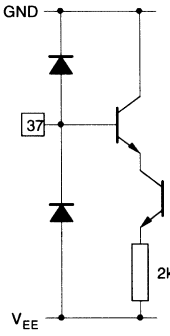
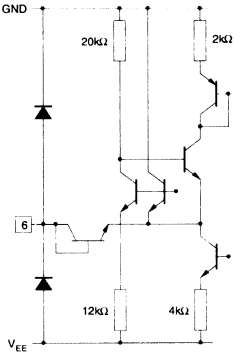
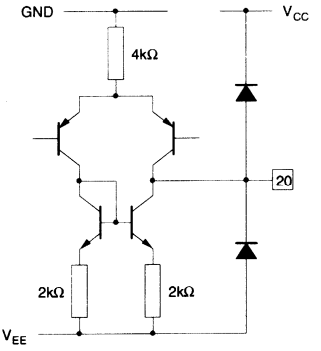
Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
9 to 18	D9 to D0	 1602A-05.EPS	Parallel data output H L	O		 -0.8 -1.6		 V V
19	PCK		Parallel clock output (rising edge at data center) H L	O		 -0.8 -1.6		 V V
21	EVR		Data output reference potential	O		-1.2		V
26	AIX	 1602A-06.EPS	Equalizer differential input	I		-2.0		V
25	AIY							
28	NC	 1602A-07.EPS	To be left open	I		-4.6		V
29	CX		Equalizer detector output; Input signal : absent present	O		 -2.4 -2.0		 V V

1602A-02.TBL

PIN DESCRIPTION (continued)

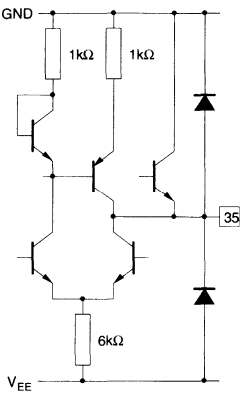
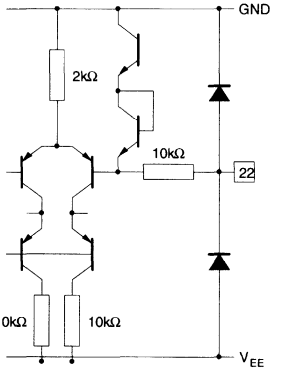
Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
31	MON	 1602A-08.EPS	Equalizer monitor output. Connect 75Ω resistor between MON-GND. Observe using a 50Ω input oscilloscope at the 75Ω coaxial cable.	O		15		mV (pp)
32	ADS	 1602A-09.EPS	Serial data input selection High : Digital input DIX/DIY Low : Equalizer input AIX/AIY H L	I	 -0.5		 -5	 V V
33	DIX	 1602A-10.EPS	Serial data digital differential input	I				
34	DIY		Selected when ADS is High. H L		-1.0		-1.6	V V

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
37	ESI	 1602A-11.EPS	PLL error signal input : must be connected to ESO with the shortest distance	i		-3.2		V
6	TN1	 1602A-12.EPS	Serial data input activation High : Input disabled (VCO free running condition). Low : Input enabled. During switch-on phase, by temporarily hold High for quick start-up	I	-1.0			V V
20	SYN	 1602A-13.EPS	State changes at each TRS Sync word 3FFH 000H 000H H L	O	-1.0		-4.0	V V

1602A-04.TBL

PIN DESCRIPTION (continued)

Pin N°	Symbol	Equivalent Circuit	Description	I/O	Standard			
					Min.	Typ.	Max.	Unit
35	DPR	 1602A-14.EPS	Serial data detection output. When there is an input signal at the input side selected through ADS, this pin goes High. At no signal, it goes Low. H L i.e. - present : High - absent : Low	O	 -1.0		 -4.0	 V V
22	RSE	 1602A-15.EPS	Selects VCO frequency range H : High range 140 to 270MHz L : Low range 100 to 145MHz H L	I	 -0.4		 -4.0	 V V
7 23	V_{EE}		-5V supply I/O buffer, PLL equalizer		-5.2	-5.0	-4.8	V
8	V_{EE}		-5V Supply Logic part		-5.2	-5.0	-4.8	V
2 24 27 30	GND		GND					

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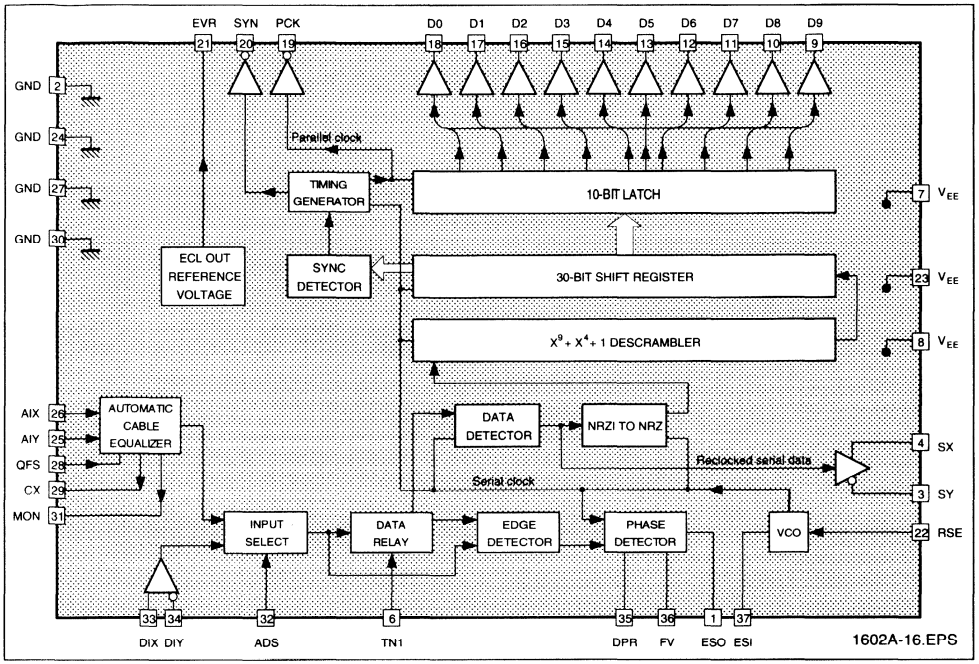
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-6	V
V_{IN}	Input Voltage	V_{EE} to 0	V
I_{OUT}	Output Current	-30	mA
T_{oper}	Operating Temperature	0 to 65	°C
T_{stg}	Storage Temperature	-50 to 125	°C
P_D	Allowable Power Dissipation	2.0	W

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{EE}	Supply Voltage	-4.8 to -5.2	V
T_{oper}	Operating Temperature	0 To 65	°C

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ELECTRICAL CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	TYp.	Max.	Unit
DC CHARACTERISTICS							
I_{EE}	Supply Current	V_{EE} = 5V	Figure 4		185		mA
V_{IH}	Input Voltage	Pin ADS		-0.4			V
V_{IL}						-1.5	V
V_{IH}		Pin RSE	Figure 10	-0.4			V
V_{IL}						-4.0	V
V_{IH}		Pin DIX, DIY		-1.0			V
V_{IL}						-1.6	V
I_{IH}	Input Current	Pin DIX, DIY	Figure 5			5.0	µA
I_{IL}				-1.0		+1.0	µA
V_{IH}	Input Voltage	Pin TN1	Figure 9	-1.0			V
V_{IL}						-4.6	V
V_{OH}	Output Voltage	Pin PCX, Dn R_P = 1kΩ			-0.8		V
V_{OL}					-1.6		V
V_M		Pin EVR, R_P = 1kΩ			-1.2		V
V_{OH}		Pin DPR, SYN I_{OH} = -10µA, I_{OL} = +10µA	Figure 7	-1.0			V
V_{OL}			Figure 8			-4.0	V
V_{OH}		Pin SX, SY R_P = 220Ω			-1.6		V
V_{OL}					-2.4		V
AC CHARACTERISTICS							
f_{MAX1}	VCO Max. Oscillation Frequency 1	RSE = "H"	Figure 6	30.0			MHz
f_{MIN1}	VCO Min. Oscillation Frequency 1	RSE = "H"				14.0	MHz
f_{MAX2}	VCO Max. Oscillation Frequency 2	RSE = "L"		15.0			MHz
f_{MIN2}	VCO Min. Oscillation Frequency 2	RSE = "L"				10.0	MHz
f_{HP1}	PLL Pull in Range	f signal = 270MHz RSE = "H"	Figure 3	27.7			MHz
f_{LP1}						25.5	MHz
f_{HP2}		f signal = 177MHz RSE = "H"		18.5			MHz
f_{LP2}						16.8	MHz
f_{HP3}		f signal = 143MHz RSE = "H"		15.0			MHz
f_{LP3}						13.3	MHz
f_{OP1}	PLL Generator Frequency	RSE = "H"		14.0		27.0	MHz
f_{OP2}		RSE = "L"		10.0		14.5	MHz

Frequency at 1/10 the value of signal frequency (Tested through Pin PCK)

SWITCHING CHARACTERISTICS (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
t_r	Rise Time	Pins PCK, Dn R_P = 1kΩ	Figure 3		0.8		nsec
t_f	Fall Time				1.4		nsec
t_r	Rise Time	Pins SX, SY R_P = 220Ω			0.7		nsec
t_f	Fall Time				0.7		nsec
t_d	Delay Time	Pins PCK, Dn		-3		+3	nsec

EQUALIZER (V_{EE} = -5V, T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Test Circuit	Min.	Typ.	Max.	Unit
V_{MAX}	Equalizer Max. Input Voltage	Pins AIX, AIY	Figure 3	0.88			Vp-p
G_{MAX}	Equalizer Max. Gain				30		dB
C_{IN}	Input Capacity	Pins AIX, freq = 100MHz					pF
R_{IN}	Input Resistance	Pins AIX, freq = 100MHz					Ω

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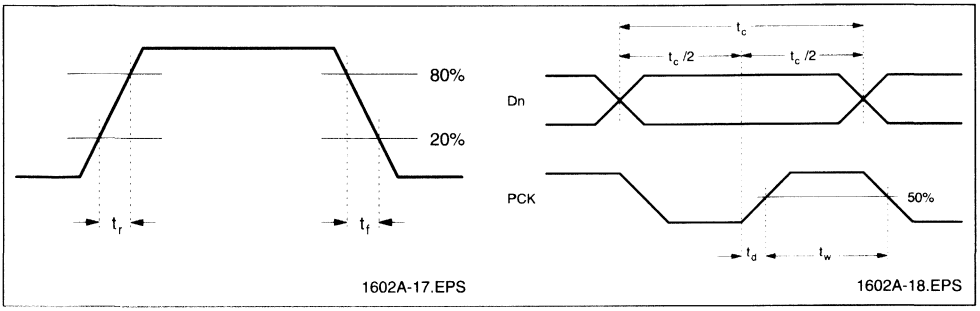
Figure 1 : t_r, t_f, t_c, t_d Definition



SYN pin guaranteed operation range.

SYNC pin and serial to parallel conversion operate normally within the frequency and ambient temperature ranges according to the following considerations.

Reclocked output.

STV1602A may be used as a repeater. The reclocked output, providing characteristics almost identical to the serial output of STV1601A is available from SX (Pin 4) and SY (Pin 3).

When the reclocked output is used, it is recommended not to use simultaneously use the parallel outputs (data and clock) in order to avoid possible logic errors caused by an excessively high temperature which may result from additional power dissipation created by the reclocked output circuit under certain environnmental conditions.

If, for the sake of a design convenience, both reclocked and parallel outputs are to be used, the ambient temperature has to be kept as low as possible or, at least, the airflow around STV1602A must be carefully considered. In addition, it is recommended to put 220Ω resistors on all parallel outputs including the clock as shown in Figure 2. This reduces the magnitude of the spike current resulting from the parallel output circuit inside the chip and helps reduce the probability of logic errors at high temperature.

Power saving in repeater mode

Since the parallell output is not always required for a reclocked repeater, the chip has been designed such that the uncessary parallel logic circuit can be disabled by disconnecting Pin 8, one of V_{EE}s, from the power supply. With this arrangement the power dissipation is reducible to about 45 percent of that of the fully functional mode.

In practice, a test switch should be provided so that some parallel signals may be available during adjustment procedures as shown in Figure 2.

Figure 2 : A Suggested Parallel Clock / Data Output Circuit

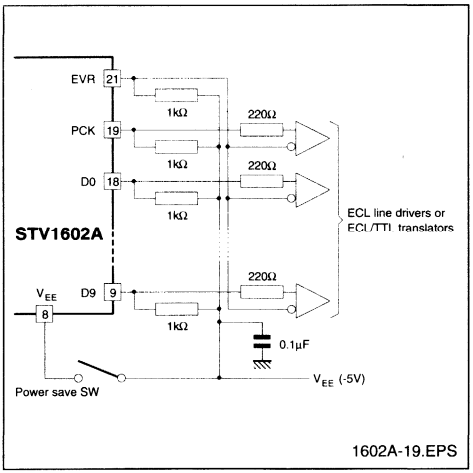


Figure 3 :Test Circuit Diagram Example

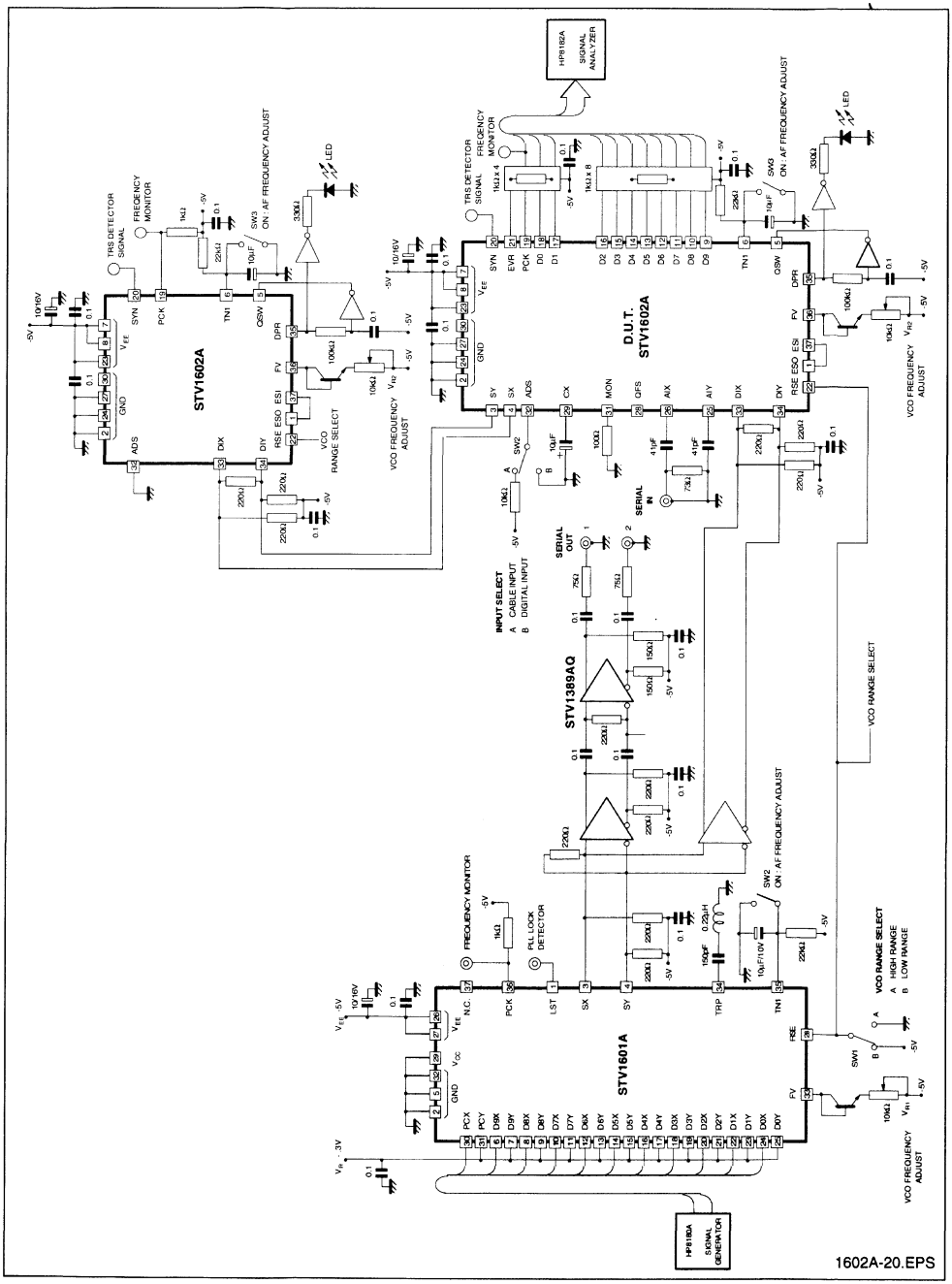


Figure 4

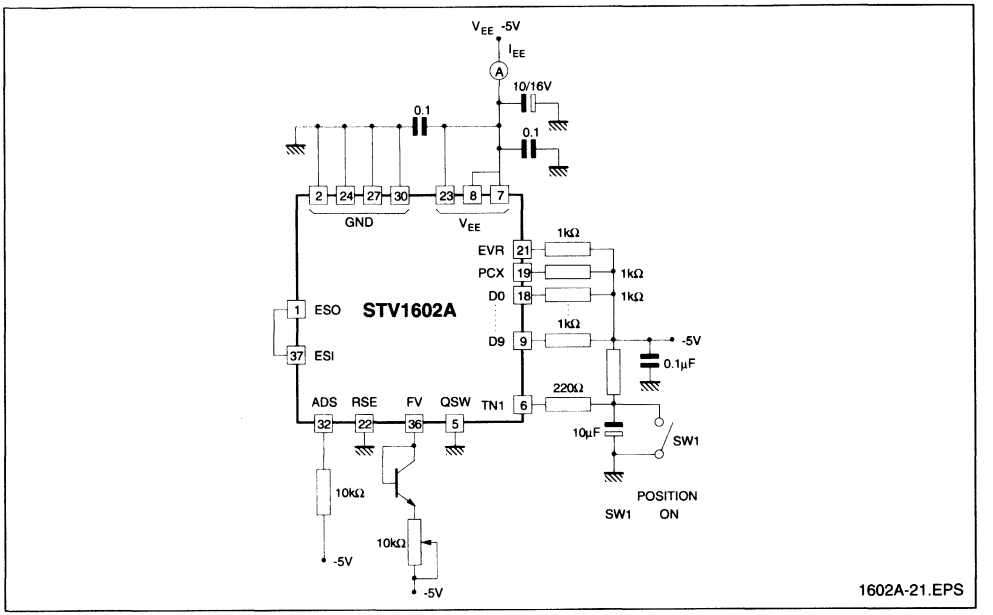


Figure 5

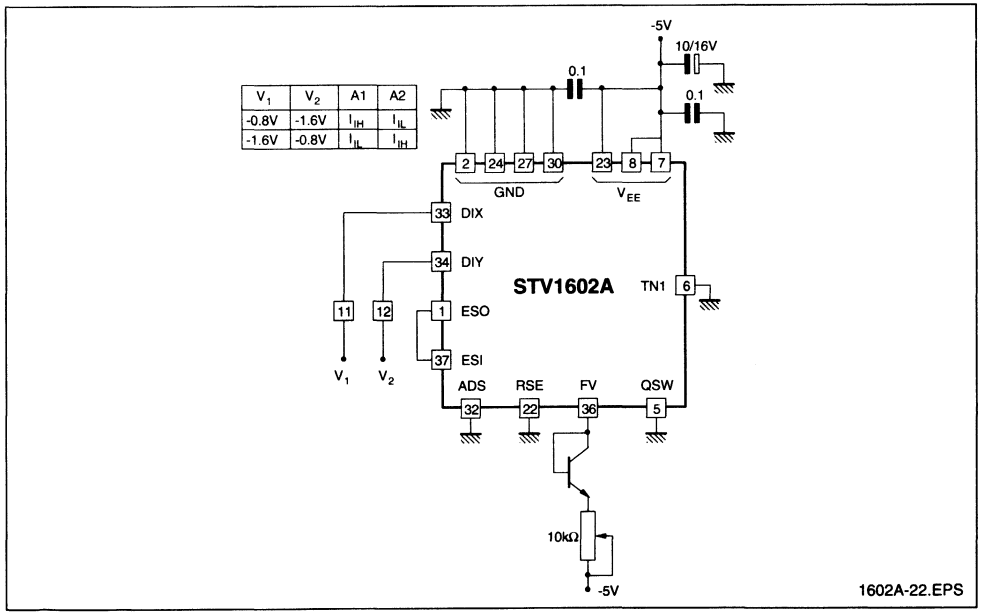


Figure 6

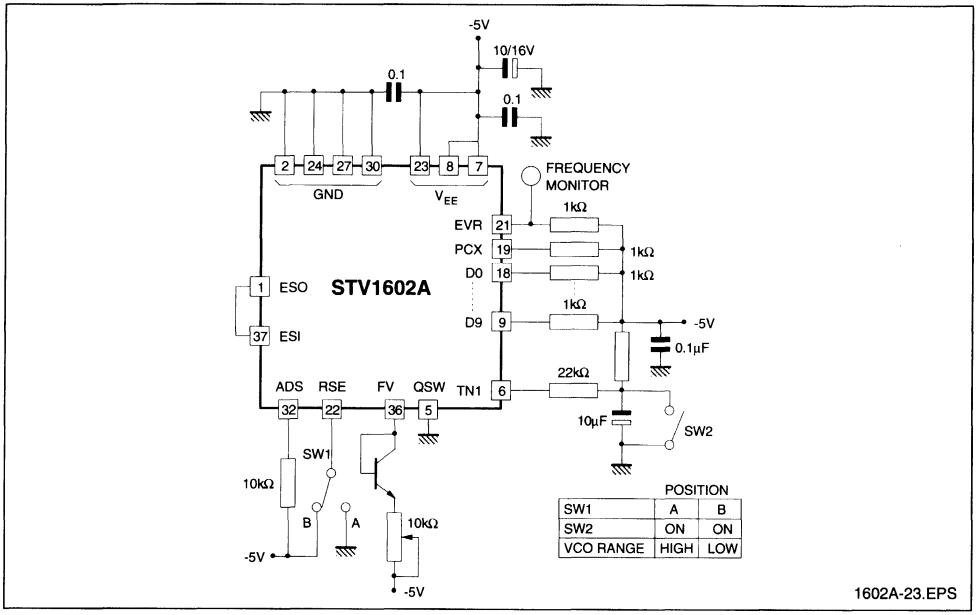


Figure 7

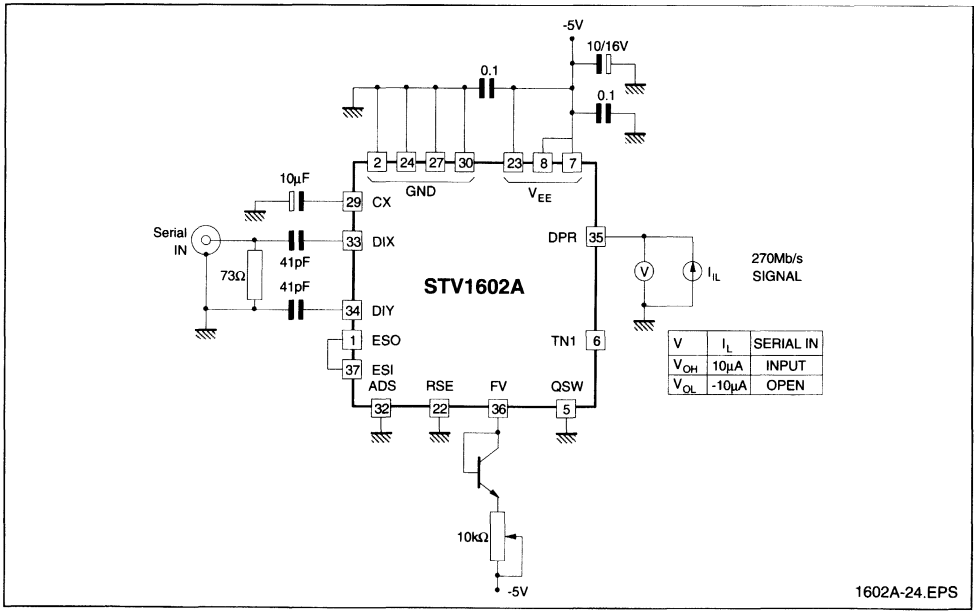


Figure 8

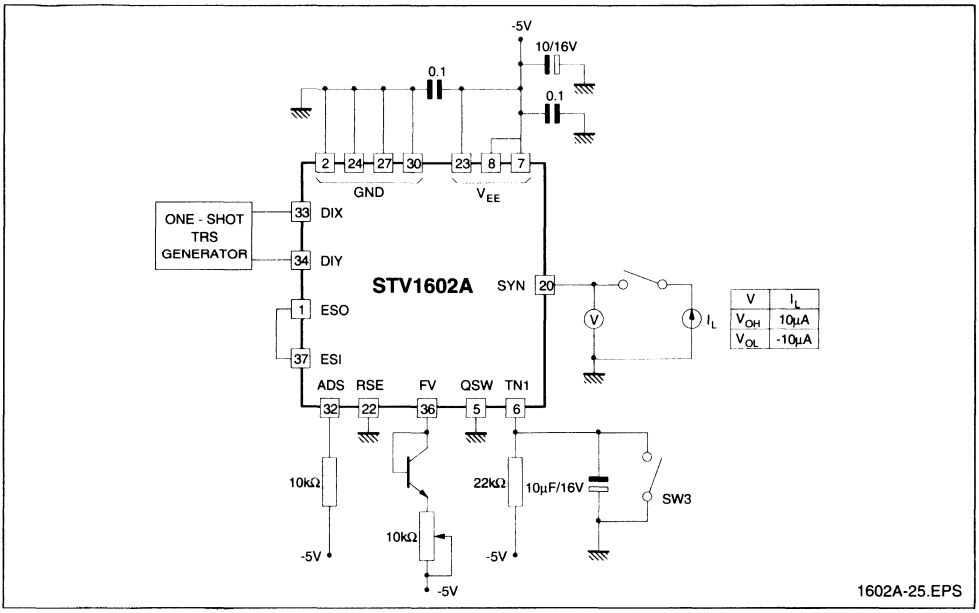


Figure 9

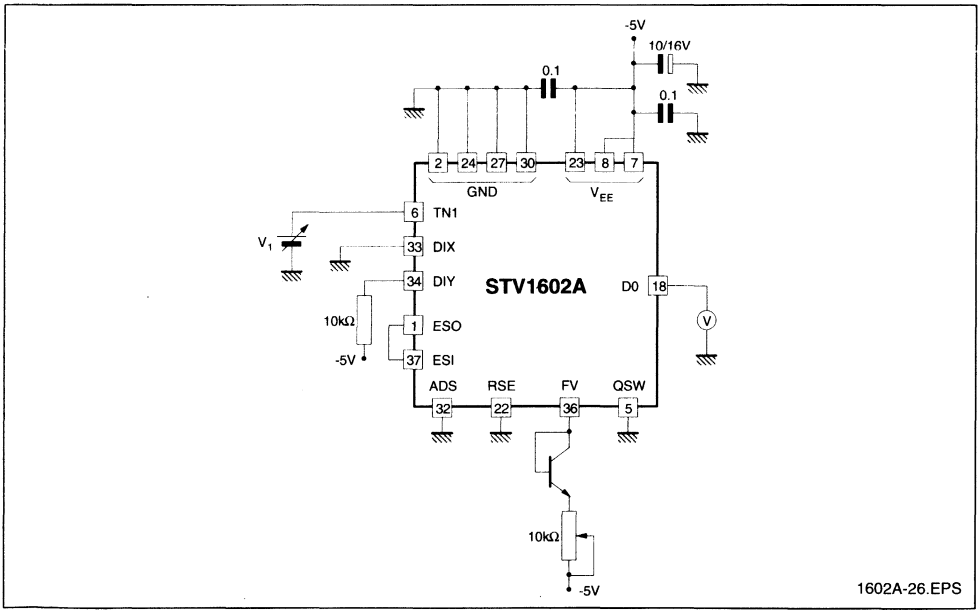
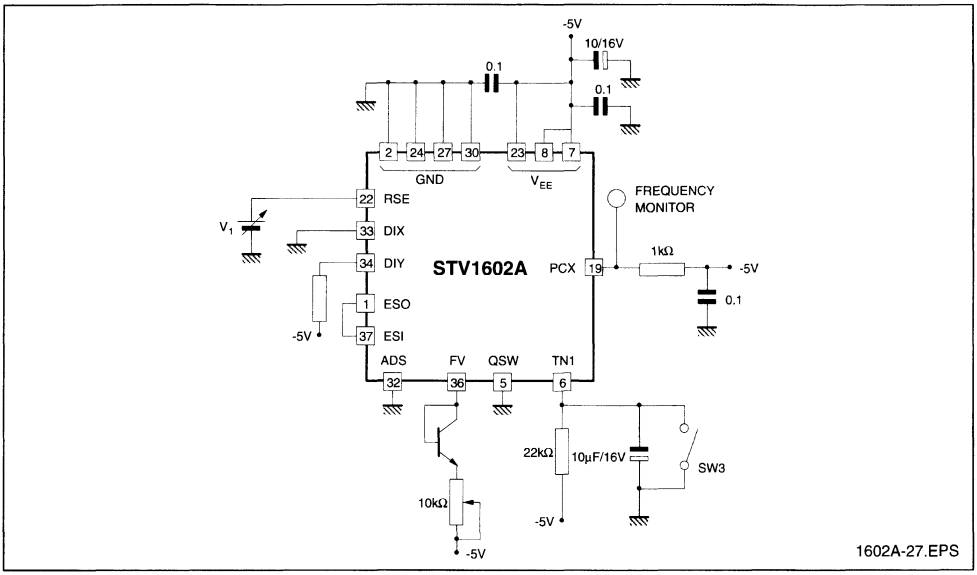


Figure 10



STV1602A GENERAL

As shown in the overall block diagram on page 7, STV1602A is composed of the following functions :

(1) Analog input as a primary input with automatic equalizer to meet the loss characteristics of coaxial cable
(2) Digital input as a secondary input to receive the encoded signal from short distances within the same printed circuit board or the same equipment
(3) Phase locked loop (PLL) variable oscillator
(4) Reclocked serial output
(5) Serial descrambler
(6) SYNC detector
(7) Deserializer
(8) Parallel output buffer amplifiers
(9) Three diagnostic signals : eye monitor, SYNC monitor and input data presence monitor

A brief explanation of each function is given in the following sections.

1. Cable equalizer

Transmission of high speed digital data by means of coaxial cable can greatly attenuate high frequency components. According to the cable length, received signals can widely differ from those sent; in such conditions, clock extraction and data identification could be difficult.

The cable equalizer overcomes this problem.

The IC performs up to 30dB (typical) equalization at 135MHz, typically 300m of high-grade coaxial cable. The equalization is automatically performed according to the coaxial cable length.

The input signal can be delivered either through a transformer or through a capacitor.

When the digital input is selected, the equalizer is disabled. Typical characteristics of the equalization are given in Figure 31.

Figure 11 : Equalizer Capacitor Coupling Input Circuit

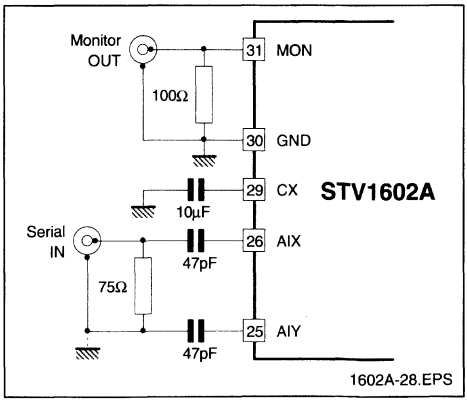
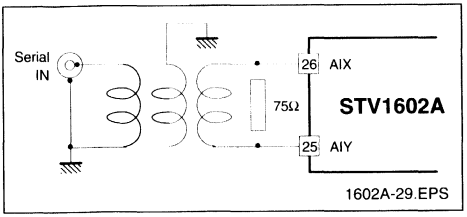
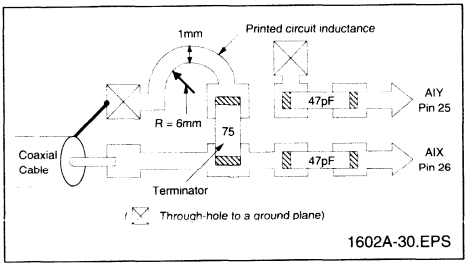


Figure 12 : Equalizer Transformer Input Circuit



In both input circuit configurations, a consideration is required in a practical design to obtain a sufficient return-loss (at least 15dB over a frequency range of 5MHz to the bit rate frequency used). To achieve this, it is effective to add a small inductance in series with the 75Ω termination resistor. Figure 13 shows an implementation example.

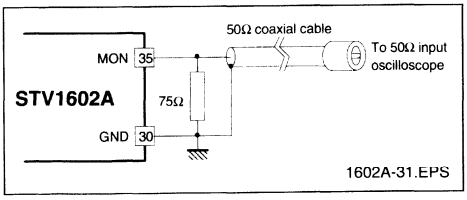
Figure 13 : An example of technique to improve the return-loss figure for the capacitor coupling input case



MON Pin (31)

Equalized signals can be observed at this pin by connecting an oscilloscope input (50Ω).

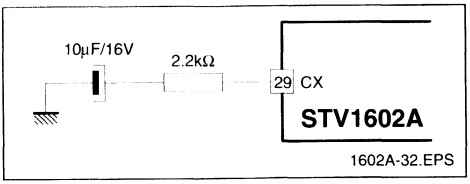
Figure 14 : Equalized Waveforms Monitoring



CX Pin (29) Equalizer AGC time constant

Connect a 10µF capacitor in serial with 2.2kΩ resistor between this pin and GND in order to obtain stable operation at all times. According to input signals, voltage changes from -2V to -2.4V can occur.

Figure 15 : AGC Time Constant



2. Digital input

The serial data input can be used without the equalizer.

DIX (Pin 33) and DIY (Pin 34) are differential inputs for ECL signals.

From these pins, input signals are differentially amplified, therefore with no input signals, the data detection signals could go High and erroneous data would be transferred to the parallel output.

To avoid this, a voltage level conforming to ECL specifications must be applied between DIX and DIY pins.

Also, while the analog input is in use, digital input must be kept "quiet" in order to avoid possible errors caused by cross-talk. This cross-talk problem naturally gets most severe when the analog input cable length is close to the limit of the transmission capability.

3. Serial input selection

Selection of the serial input is performed by ADS (Pin 32); when High the digital input is enabled; this input can be used for very short transmission lines. When Low, the equalizer input is enabled; this input must be used for long transmission lines.

4. PLL

In order to extract clock signals from the equalized serial data, it is processed to generate edge signals which are sent to the phase comparator.

When the PLL is locked, the identifier clock (D - flipflop) will be in phase with the incoming clock. The identifier clock rises at the center of the data period for easy identification.

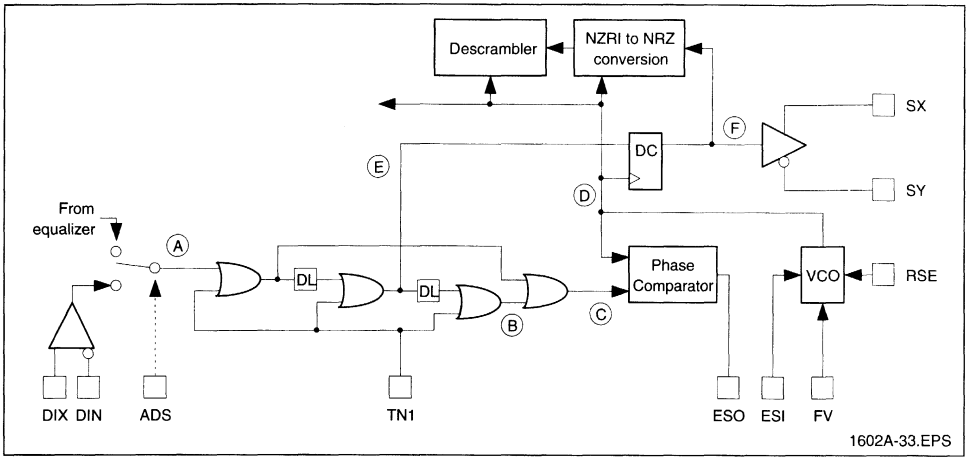
The PLL detailed block diagram is shown in Figure 16.

ESI is the VCO control input (Pin 37). Normally, the phase comparator output ESO (Pin 1) is connected to ESI.

Since the VCO employed has a very high sensitivity, those two nodes must be connected with a shortest distance and a minimum area of conductor

on the printed circuit board. Encircling those two nodes by a ground guarding is an efficient method to prevent errors caused by an "antenna effect".
Through FV (Pin 35) one can adjust the free running frequency; when the FV Voltage is equal to V_{EE}, the free running frequency is the lowest; the voltage adjustment can be performed by using a variable resistor connected between FV and VEE.
RSE (Pin 22) selects the VCO frequency range; High : 140 to 270MHz, Low : 100 to 145MHz.
When TN1 (Pin 6) is set High, input signals are disabled and the VCO free runs. The capacitor connected between TN1 and GND avoids mislocking problem when the power supply is switched on.

Figure 16 : Serial Data Input and PLL



Data detection

Serial data edges are detected and go through low pass filter. The processed signal is available at DPR (Pin 35).DPR goes High when an input signal is detected, otherwise it stays Low.

The driving capability of this pin is weak. It is recommended to load it with a high impedance CMOS or equivalent.

5. NRZI To NRZ conversion, descrambler

Serial data delivered by the identifier is available in differential mode, SX (Pin 4) and SY (Pin 3). At the same time, to recover the original data, NRZI to NRZ conversion and descrambling are performed.

Figure 17 : NRZI to NRZ conversion

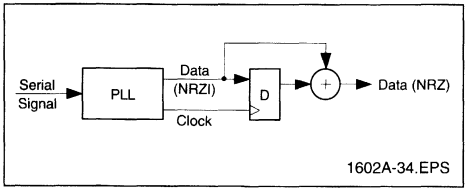


Figure 18 : $x^9 + x^4 + 1$ Descrambler

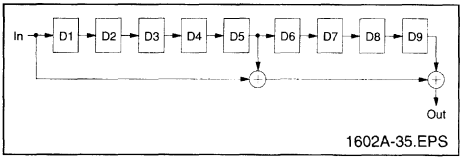
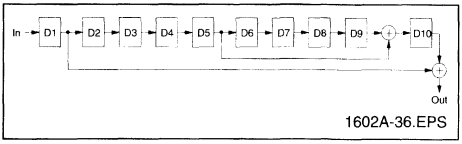


Figure 19 : Actual $x^9 + x^4 + 1$ Descrambler



6. Serial to parallel conversion

After descrambling, serial data is sent to a 30-bit register to detect the sync word (TRS). When the sequence 11111111110000000000000000000 is detected, sync word detection signal is output, the counter which divides the clock frequency by 10 is initialized and data is converted to parallel (10-bit word) to be output.

Each time the sync word is detected, SYN (Pin 20) changes state as shown in Figure 20.

When a receiver using STV1602A is properly implemented and adjusted, the health of the implementation can be checked simply by looking at SYN (Pin 20) output while an encoded signal is present at the input.

SYN is an output of a flip-flop which toggles at each detection of TRS at the SYNC detector. Since the 4:2:2 signal contains two kinds of TRSs, SAV and EAV, when the output of SYN is observed by an oscilloscope it looks like either case A or case B as shown in Figure 20 depending upon the initial condition of the Flip-Flop.

When bit erros are occurring somewhere in the transmission path, SYN output is affected and looks like as shown in case C.

Figure 21 illustrates the case for 4 fsc (D2 NTSC and PAL).

Differing from the 4:2:2 case, SYN output has an equal mark and space ratio due to the periodic occurence (once per one TV line) of the TRS detection. However, transmission path bit errors will cause the SYN output to appear similar to the 4:2:2 case.

If SYN signal is used other than for monitoring purposes, buffering similar to that of DPR is required due to the high impedance nature of SYN output.

7. Phase relation ship between parallel data and parallel clock

Parallel data and clock are output so that the rising edge of the parallel clock is located at the center of the parallel data. Both parallel data and clock (nearly identical to that of single ECL) have DC levels depending on the temperature. In order to simplify the driving amplifier, a reference level (EVR) is available at Pin 21. PCX, Dn and EVR use pull down resistors (identical values). A peripheral circuit example is shown in Figure 23. Figure 24 shows a circuit to disable the parallel clock output.

Figure 20 : SYNC Output in 4:2:2 Case (not to scale)

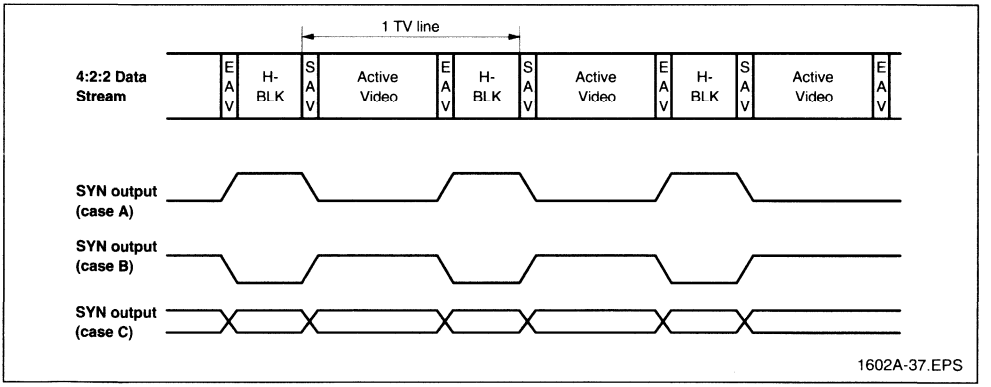


Figure 21 : SYNC Output in 4 fsc Case (not to scale)

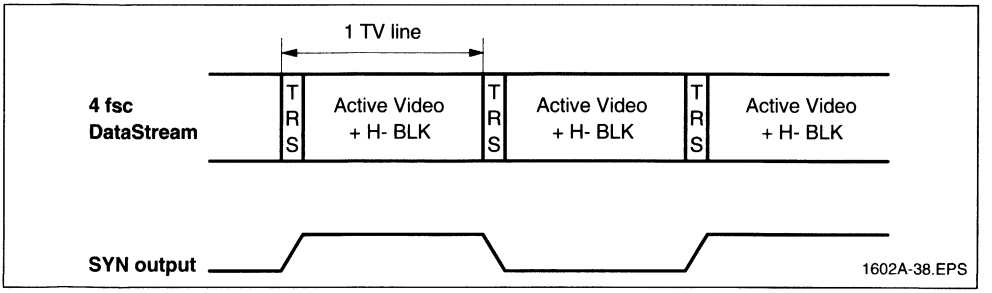


Figure 22 : Phase Relation of Parallel Clock, Data and EVR Voltage Level

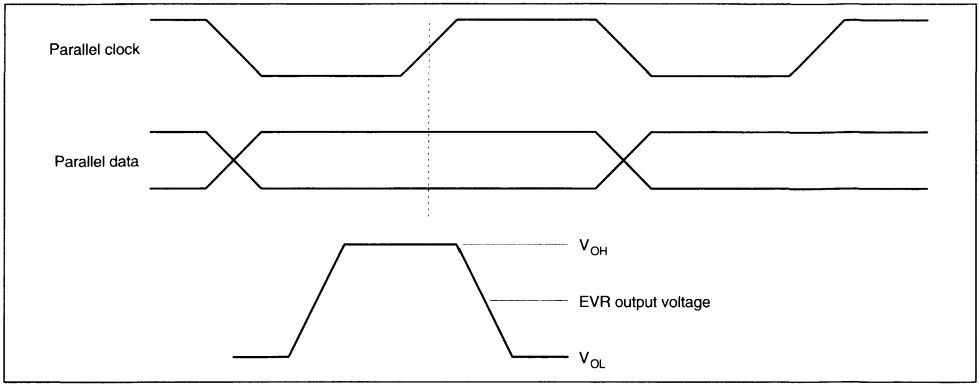


Figure 23 : Parallel Clock Data Output Circuit

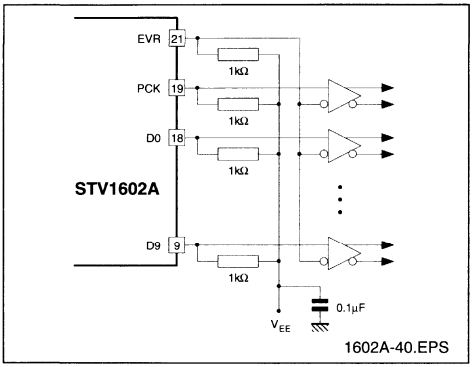
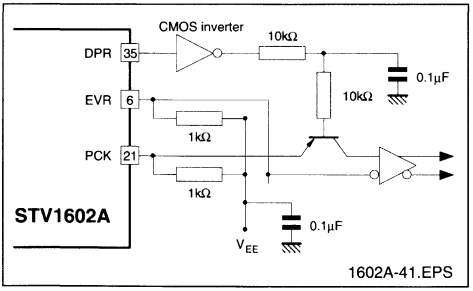


Figure 24 : A Circuit Example to Disable Parallel Clock



8. VCO temperature compensation and oscillation frequency adjustment.

VCO oscillation frequency depends on the temperature as shown in Figures 29 and 30 "Representative characteristics example". Within the normal range of operation, frequency increases with temperature.

FV pin voltage remains almost constant regardless of temperature.

Figure 25 shows an example of a temperature compensation circuit using a diode (transistor with C-B diode short-circuited) and a resistor between FV and V_{EE}.

PLL pull-in range (signal frequency 270, 177 and 143MHz) are given by Figures 32, 33 and 34.

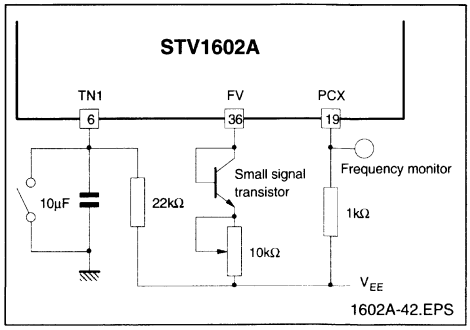
9. VCO free running frequency adjustment

VCO free running frequency adjustment is performed at room temperature.

If TN1 is set High, VCO is free running. Wait for 5 to 10 minutes after turning power supply ON (warm up time).

While monitoring PCK (Pin 19) output, adjust the signal frequency (within ±1%) with the variable resistor connected between FV and V_{EE}.

Figure 25 : VCO Temperature Compensation and Free Running Frequency Adjustment



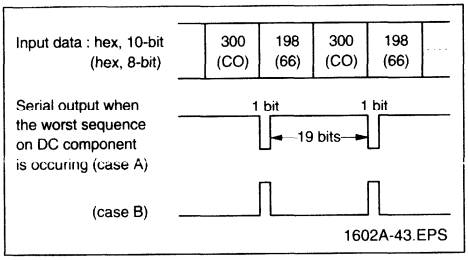
Using particular codes to check overall performance

Althrough the scrambling method employed effectively randomizes the incoming data and puts out a signal with a nearly uniform spectrum, there still exist some combinations of codes that give somewhat unfriendly conditions to the transmission path in terms of low frequency component or of a long run without any transitions.

As shown in Figure 26, it is known that if the code words 300, 198 (hex, 10-bit) are given alternately to the parallel input of the encoder, the largest amount of DC component (nearly one TV line period) can be produced at some place with a certain probability (such a sequence is, however, destroyed when different data is input to the encoder).

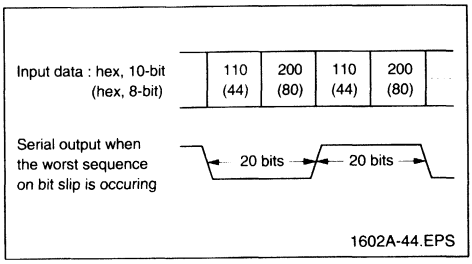
Even with such signals, error-free reception is possible with the STV1602A if a proper implementation is made (refer to section 12 for a recommended circuit).

Figure 26



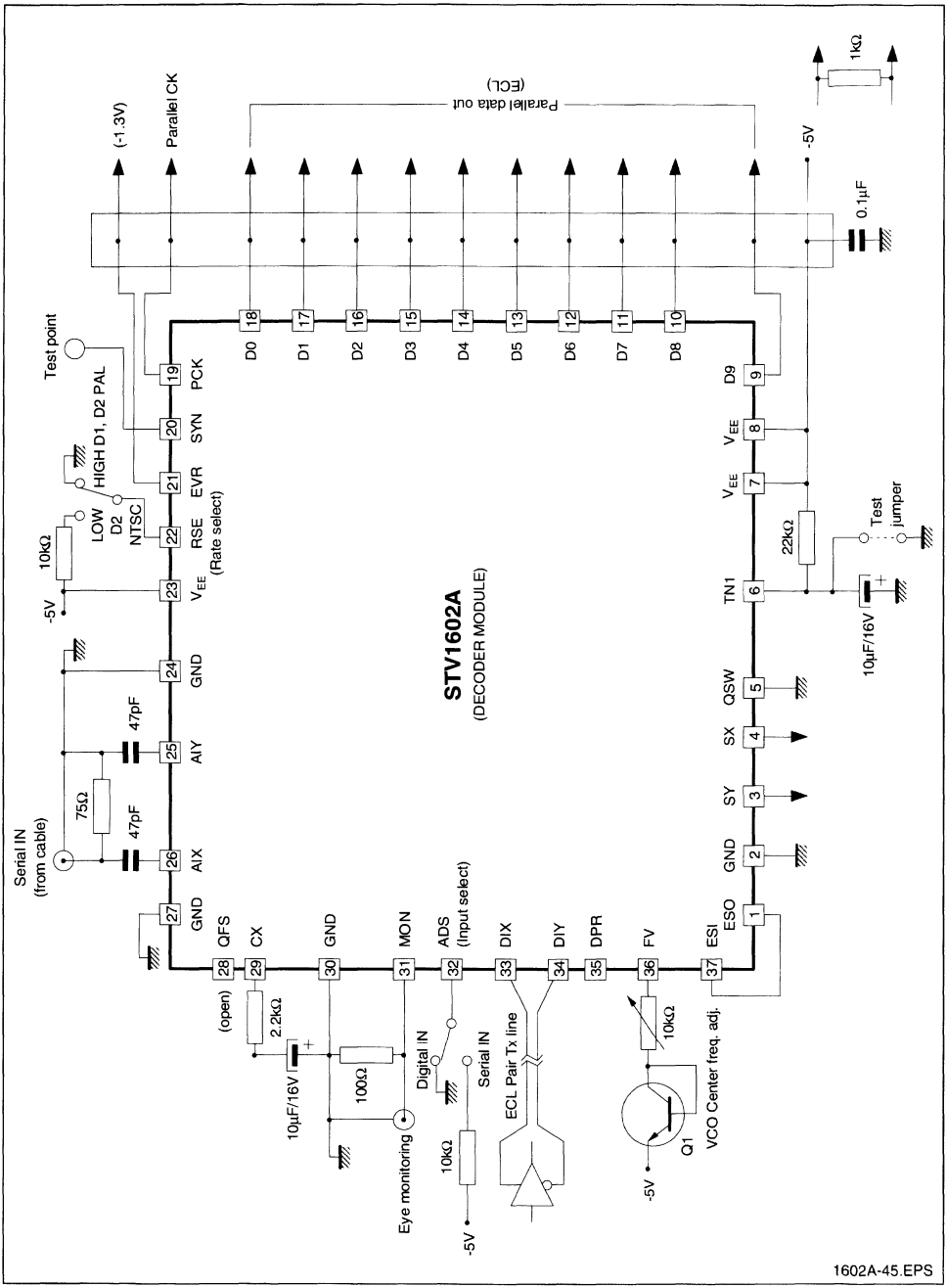
Another particular combination of words, but with a different nature, is 200, 110 (hex, 10-bit) which can generate the sequence which is most vulnerable* to bit slip of nearly one TV line period. Figure 27 illustrates such a situation. Similar to the previous case, the worst sequence stops upon an arrival of a data other than the alternating 200, 110 at the input of the encoder.

Figure 27 : Particular Data words for checking PLL bit slip



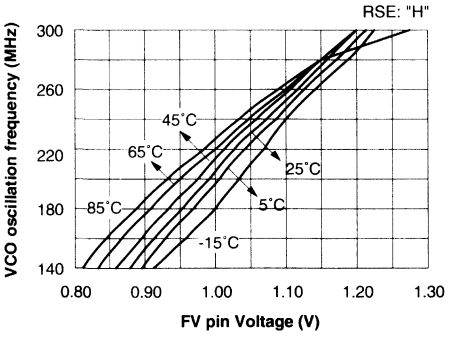
* Stricly speaking the longest isolated run is 38 clocks for 4:2:2 and 43 clocks for 4 fsc NTSC and PAL. However, the above sequence generally shows the most critical situation for the bit slip problem.

Figure 28 : Application Circuit Example



REPRESENTATIVE CHARACTERISTICS EXAMPLE

Figure 29 : VCO Oscillation Frequency versus FV Pin Voltage



1602A-46.EPS

Figure 30 : VCO Oscillation Frequency versus FV Pin Voltage

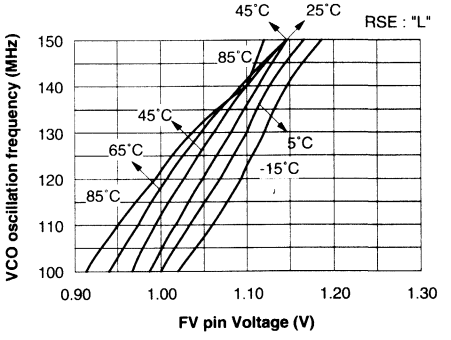


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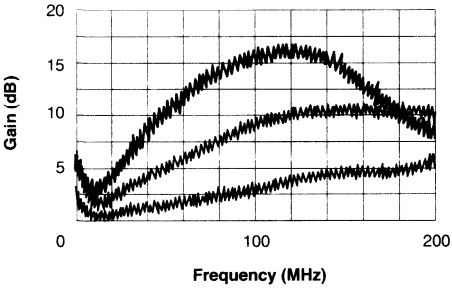
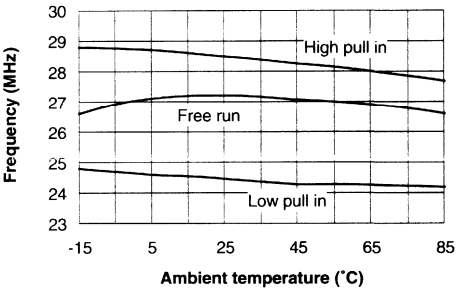
Figure 31 : An example of equalizer characteristics using 5C - 2V coaxial cable with respect to the gain for 0.5meter



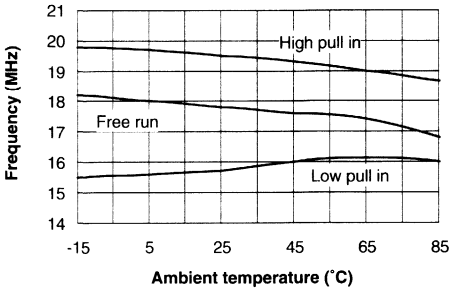
1602A-48.EPS

Figure 32 : Pull-in Range and Free Run Frequency (270Mb/s)



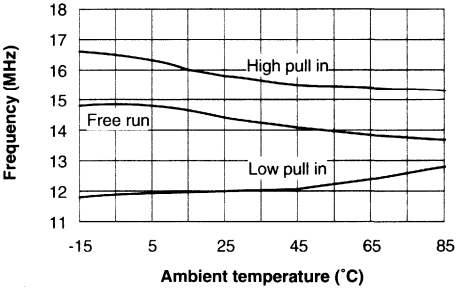
1602A-49.EPS

Figure 33 : Pull-in Range and Free Run Frequency (177Mb/s)



1602A-51.EPS

Figure 34 : Pull-in Range and Free Run Frequency (143Mb/s)



1602A-52.EPS

WIDE BAND VIDEO AMPLIFIER

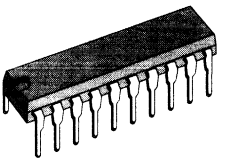
SGS-THOMSON MICROELECTRONICS

TDA9201

WIDE BAND VIDEO PREAMPLIFIER

PRELIMINARY DATA

- CURRENT OUTPUT (up to 300mA)
- 120MHz (-3dB) BANDWIDTH
- 3nsec RISE/FALL TIME
- BRIGHTNESS AND CONTRAST DC CONTROLLED
- INTERNAL CLAMPING PULSE GENERATOR
- CONTRAST PRE-ADJUST FOR COLOR MONITOR APPLICATION
- INTERNAL REFERENCE VOLTAGE GENERATOR
- BLANKING PULSE INPUT
- POS/NEG SYNC POLARITY INPUT



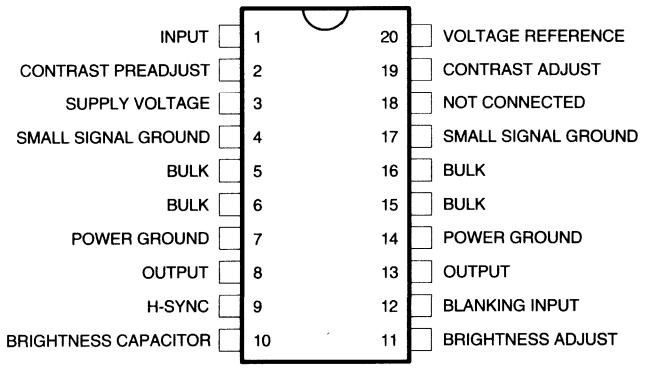
POWERDIP20
(Plastic Package)

ORDER CODE : TDA9201

DESCRIPTION

The TDA9201 is a wide band video amplifier intended for high resolution monochrome or color monitors.
The BRIGHTNESS and CONTRAST are DC controlled.
The brightness loop includes a comparator gated by an internally generated pulse.
Thanks to the contrast pre-adjust pin, this device is well suited for color application too.
The output stage structure (A class current output), allows to use a very cheap high voltage amplifier using only one transistor.

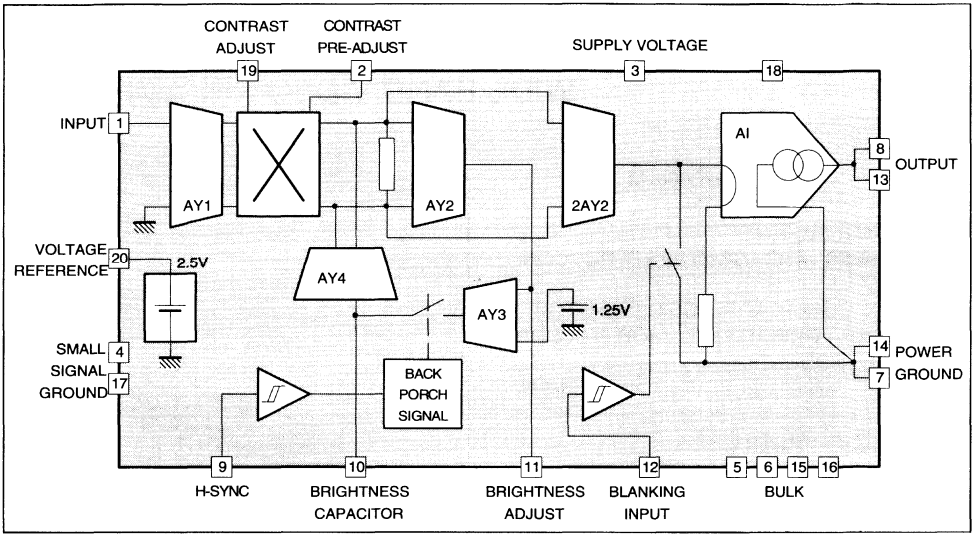
PIN CONNECTIONS



9201-01.EPS

This advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_S	Power Supply (Pin 3)		8	V
I_{OUT}	Output Current		350	mA
V_{IN}	Voltage at any Input Pin		-0.3, V_S	V
T_j	Junction Temperature		0, +150	°C
T_{stg}	Storage Temperature		-40, +150	°C
P_{max}	Power Dissipation	T_{PINS} = 90°C T_{amb} = 70°C	4.3 1	W W

9201-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-P)}$	Junction-Pins Thermal Resistance	Max.	14	°C/W
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	80*	°C/W

9201-02.TBL

* Obtained with GND pins soldered to printed board with minimum area.

DC ELECTRICAL CHARACTERISTICS (V_S = 5V and T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range	Pin 3	4.5	5	5.5	V
I_S	Supply Current	V_S = 5V, Pin 3		82	100	mA
V_{REF}	Voltage Reference	I_{20} = 0, Pin 20	2.30	2.42	2.55	V
I_{REF}	Max. Current from Pin 20 to ground	Pin 20			5	mA
V_1	Input DC Level	Pin 1	0.7	0.8	0.9	V
R_1	Input Impedance	Pin 1		10		kΩ
I_2	Cont Pre-adjust Current from Pin 2 to ground		0.3	0.5	0.7	mA
V_{CONT}	Voltage Range on Contrast Adjust	Pin 19	0		V_2	V
I_{BRTX}	Current for Max. Brigthness (100mA on output pin)	Current from Pin 11 to ground (see Figure 1)		340		µA
I_{BRTI}	Current for Min. Brigthness (100mA on output pin)	Current from Pin 11 to ground (see Figure 1)		64		µA
I_{offs}	DC Offset Current on Pin 11	Pin 11		± 50		µA
V_{OI}	Min. Output Voltage for normal operating	Pin 13 or/and 8	3.5			V

9201-03.TBL

AC ELECTRICAL CHARACTERISTICS (V_S = 5V and T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DI}	Max. Peak-to-peak Input Voltage	Pin 1 (without sync)			1	V
$V_{th\ H}$	Sync. and Blank Inputs Threshold Voltage (Pins 9 and 12)	Low level High Level	 2		0.8	V V
I_{SYNC}	Current On Sync. Input (Pin 9)	Low level High Level			1 5	µA µA
I_{BLANK}	Current On Blank Input (Pin 12)	Low level High Level			-50 1	µA µA
BLK_{D1}	Delay between Blanking Pulse begining and Output Inhibition	Pins 8, 12 and 13			40	nsec
BLK_{D2}	Delay between End of Blanking Pulse and Output Current Switching on	Pins 8, 12 and 13			30	nsec
I_{OBLK}	Output Current during Blanking Pulse	Pins 8 and 13 (see note 1)			100	µA
I_{OR}	Output Current Range Outside of Blanking	Pins 8 and 13 (see note 1)	300			mA
dI_O	Max. Peak-to-peak Output Current	Pins 8 and 13 (see note 1)			225	mA
BW	Min. Small Signal Bandwidth (-3dB) (see note 2)	V_{CONT} = 0.8V, V_{IN} = 100mV_{PP}, I_{OUTDC} = 50mA (BRT), V_{preset} = 2V	120			MHz
t_F, t_R	Output Current Rise and Fall Time (10 to 90%) (see note 2)	Pins 8 and 13 (see note 1)			3	ns

INTERNAL BACK POARCH CLAMPING PULSE GENERATOR

I_{10}	Gated Current on Brightness Capacitor	Measured on Pin 10, 500ns after end of H-sync on Pin 9		500		µA
SPW1	Max. Sync Pulse Width	Pin 9			5	µs
SPW2	Min. Sync Pulse Width	Pin 9	1			µs
BPW	Back Poarch Pulse Width	Internal Pulse		1	1.3	µs

9201-04.TBL

Notes : 1. V_{CONT} = 0, I_{BRT} adjusted for having $I_{OUT\ DC}$ = 50mA outside of BLK.

2. This parameter is not tested in production but is guaranteed by the design and qualify by means of corner lots during the qualification of the product in SGS-THOMSON. This parameter is measured on a AC testing board as described in Figure 2.

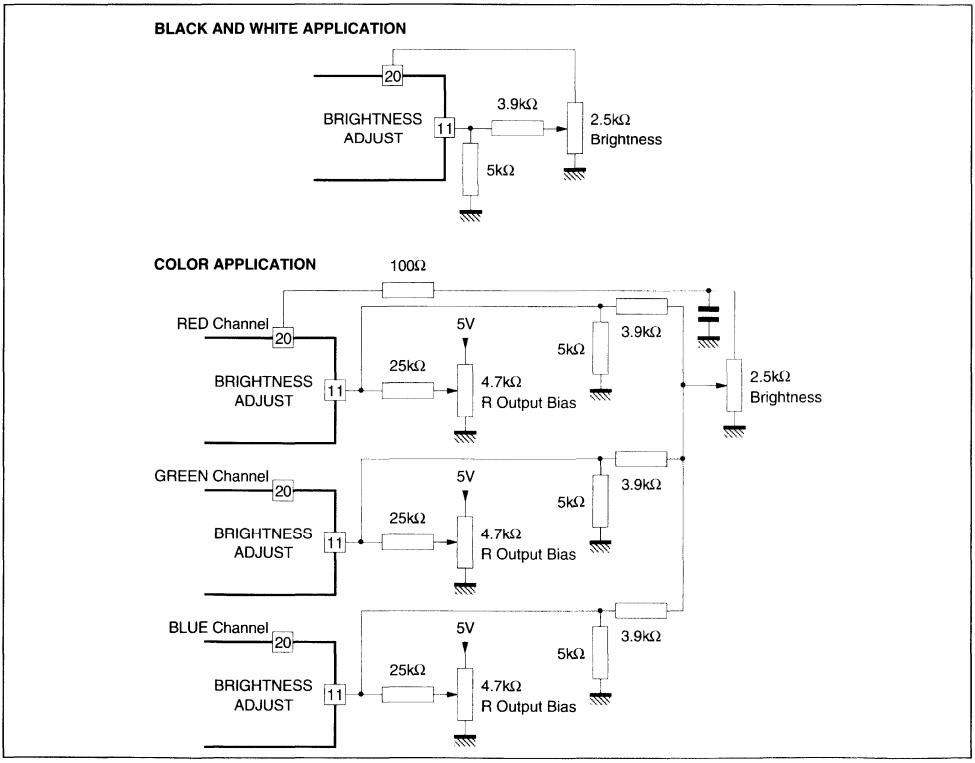
AC ELECTRICAL CHARACTERISTICS (continued)

V_S = 5V and T_{amb} = 25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TYPICAL CONTRAST CHARACTERISTICS						
$G_{Nom.}$	Gain Reference Value	V_{IN} = 1V_{PP}, V_{CONT} = 0.8V, Precontrast is presetted for having I_{OUT} = 125mA_{PP}		0		dB
GL1		V_{CONT} = 0.2 (V_{IN} = 1V_{PP})	-12.46	-11.86	-11.26	dB
GL2		V_{CONT} = 0.4 (V_{IN} = 1V_{PP})	-5.9	-5.6	-5.3	dB
GL3		V_{CONT} = 1.2 (V_{IN} = 1V_{PP})	2.85	3.15	3.45	dB
GL4		V_{CONT} = 1.6 (V_{IN} = 1V_{PP})	4.95	5.55	6.15	dB
GL5		V_{CONT} = 0 (V_{IN} = 1V_{PP})	-35			dB
BRIGHTNESS CHARACTERISTICS						
BRTx	Max. DC Current on Output				100	mA
BRTi	Min. DC Current on Output	for full bandwidth	10			mA
GBRT	Brightness Control Characteristic $I_{out\ DC}$ / $\|I_{11}\|$	DC current output versus $\|I_{11}\|$ (I_{11} in Pin 11 flows from Pin 11 to GND)		326		
V_2	Voltage Range		0		V_{REF}	V
V_{nom}	Voltage for Odb Adjustment (G_{nom})	V_2		2		V

9201-05.TBL

Figure 1 : Details of Brightness Adjustment



9201-03.EPS

Figure 2 : AC Test Circuit for BW and Rt/Ft

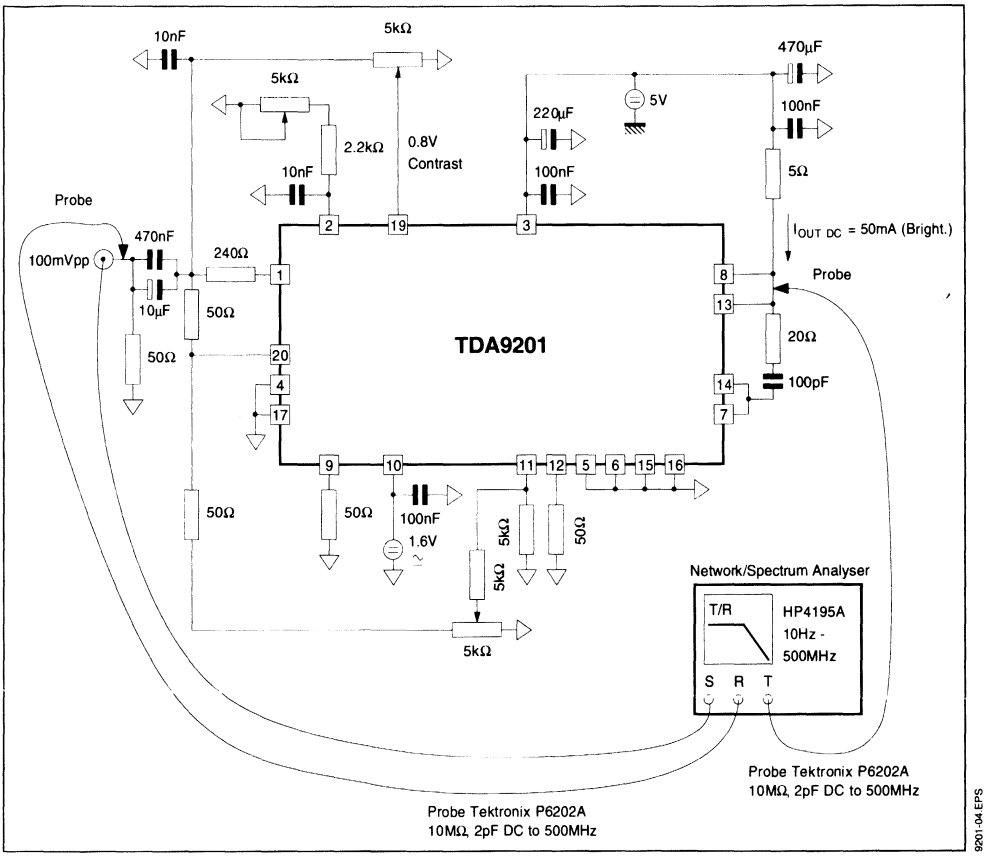


Figure 3 : Typical Gain versus Contrast Voltage Characteristic

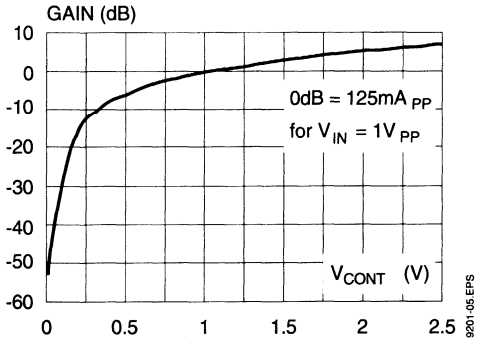


Figure 4 : V_{preset} versus Contrast Voltage for 0dB

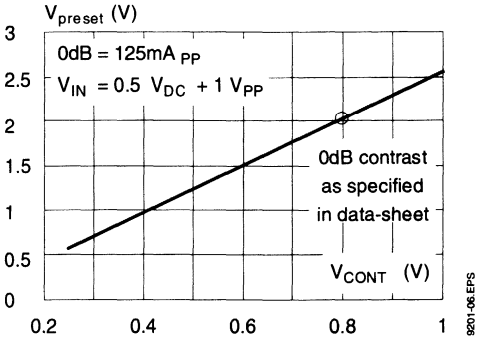


Figure 5 : Typical Application Circuit

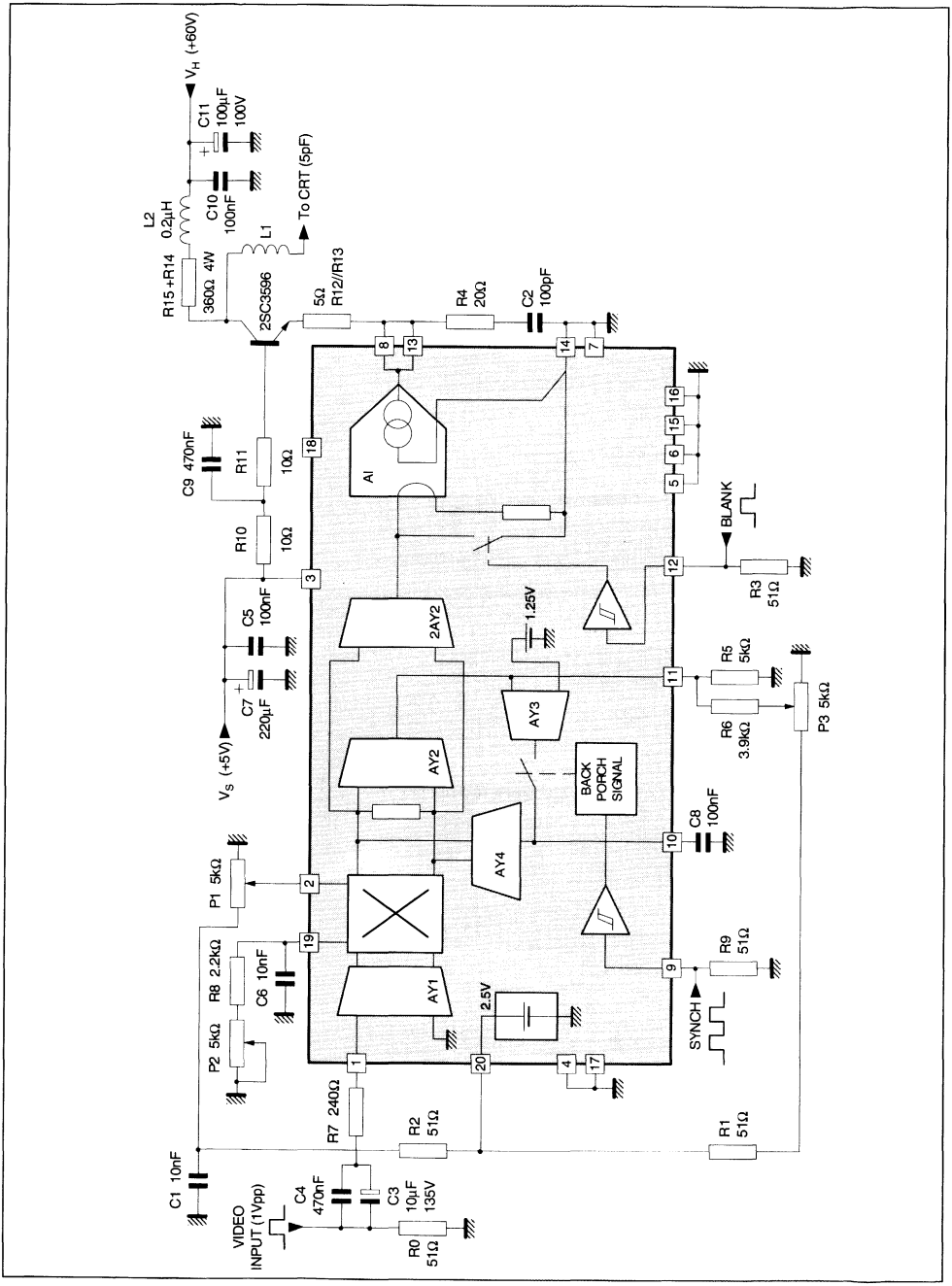


Figure 6 : Components Side

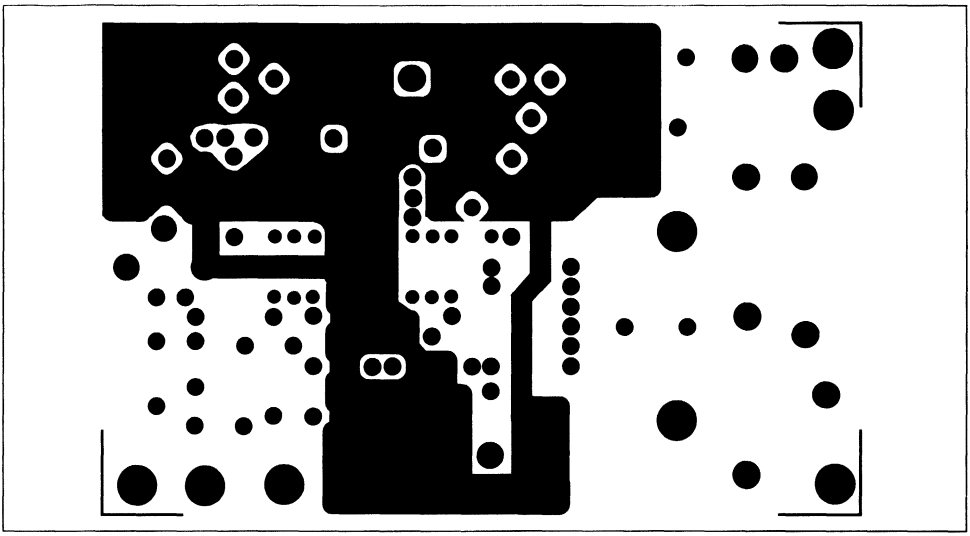


Figure 7 : Solder Side

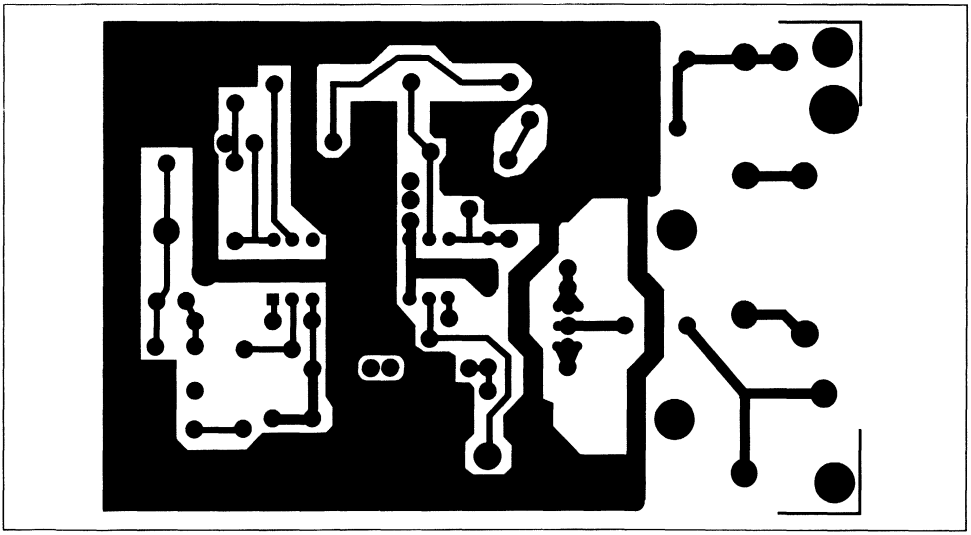
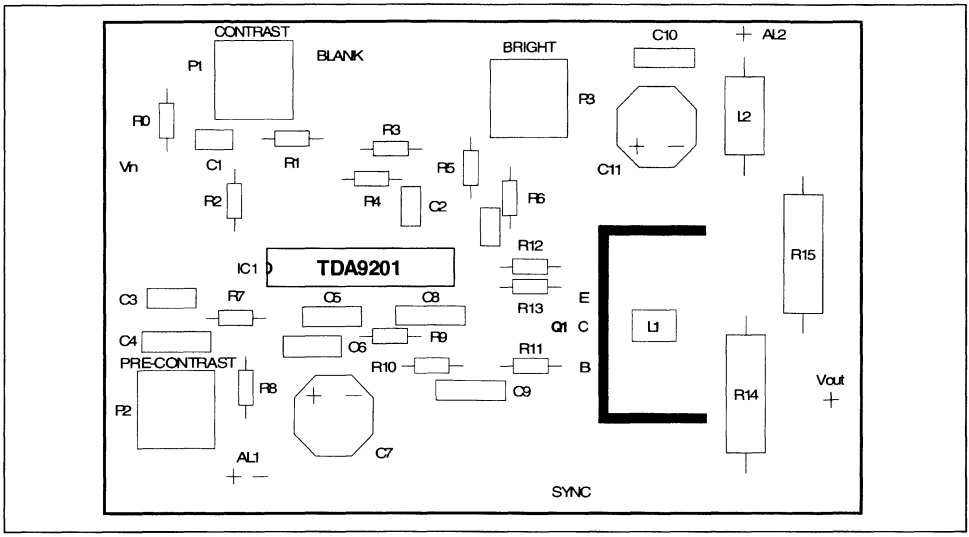


Figure 8 : Assy-plan



COMPONENT LIST

Component	Value
R0, R1, R2, R3, R9	51Ω
R4	20Ω
R5, R6	5.1kΩ
R7	240Ω
R8	2.2kΩ
R10, R11, R12, R13	10Ω
R14, R15	180Ω, 3W
P1, P2, P3	5kΩ
C1, C6	10nF
C2	100pF

Component	Value
C3	10µF/35V Tantale
C4, C9	470nF
C5, C8, C10	100nF
C7	220µF/25V
C11	100µF/100V
L1	Strap
L2	0.2µH
Q1	2SC3596E
IC1	TDA9201

9201-06.TBL

Figure 9 : Output Signal on CRT (bright. and cont.) White Vertical Line on Screen

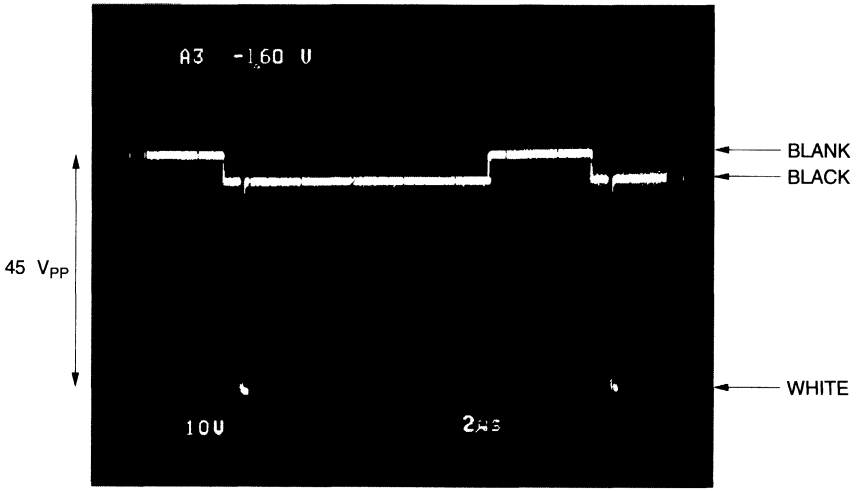


Figure 10 : 1. Input Video (500mV_{PP})
2. Output to CRT 40V_{PP}-12ns (one pixel), 150mA, pixel rate 83MHz, BW ≅ 120MHz

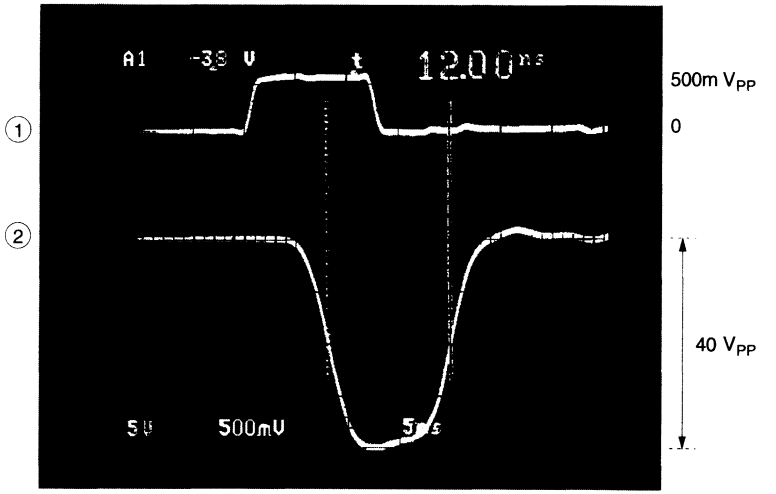
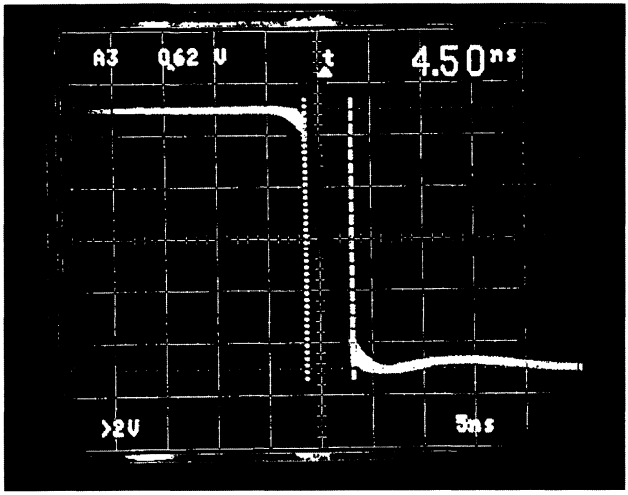
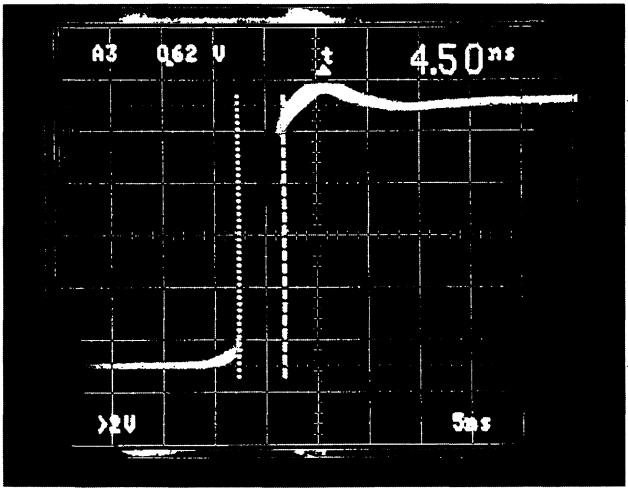


Figure 11 : Fall Time (see test conditions, Figure 13)



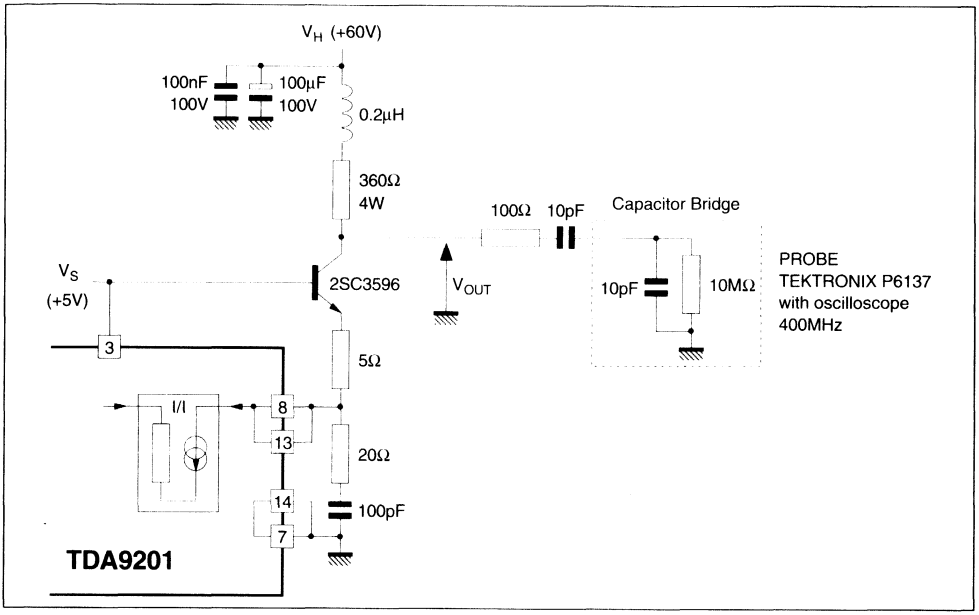
9201-13.EPS

Figure 12 : Rise Time (see test conditions, Figure 13)



9201-14.EPS

Figure 13 : Measurement Conditions



ANALOGUE SATELLITE RECEIVERS

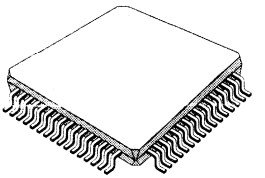
SGS-THOMSON MICROELECTRONICS

STV0030

SATELLITE SOUND AND VIDEO PROCESSOR

ADVANCE DATA

- TWO INDEPENDENTLY PROGAMMABLE SOUND DEMODULATORS
- PLL DEMODULATION WITH 5-9MHz FREQUENCY SYNTHESIS
- 50/75µs, J17 OR NO DE-EMPHASIS PROGRAMMABLE OPTIONS
- DYNAMIC NOISE REDUCTION SYSTEM
- FIXED LEVEL AUXILLIARY AUDIO INPUTS AND OUTPUTS
- GAIN CONTROLLED AND MUTEABLE AUDIO OUTPUTS
- COMPOSITE VIDEO 6-BIT GAIN CONTROL
- COMPOSITE VIDEO SELECTABLE INVERTER
- COMPOSITE VIDEO DEEMPHASIS AMPLIFIER
- 9 x 5 VIDEO MATRIX AND SWITCHES WITH GRAPHICS INPUT
- 8-BIT DAC OUTPUT
- FULLY CONTROLLED VIA I^2C BUS



PQFP64
(Plastic Package)

ORDER CODE : STV0030

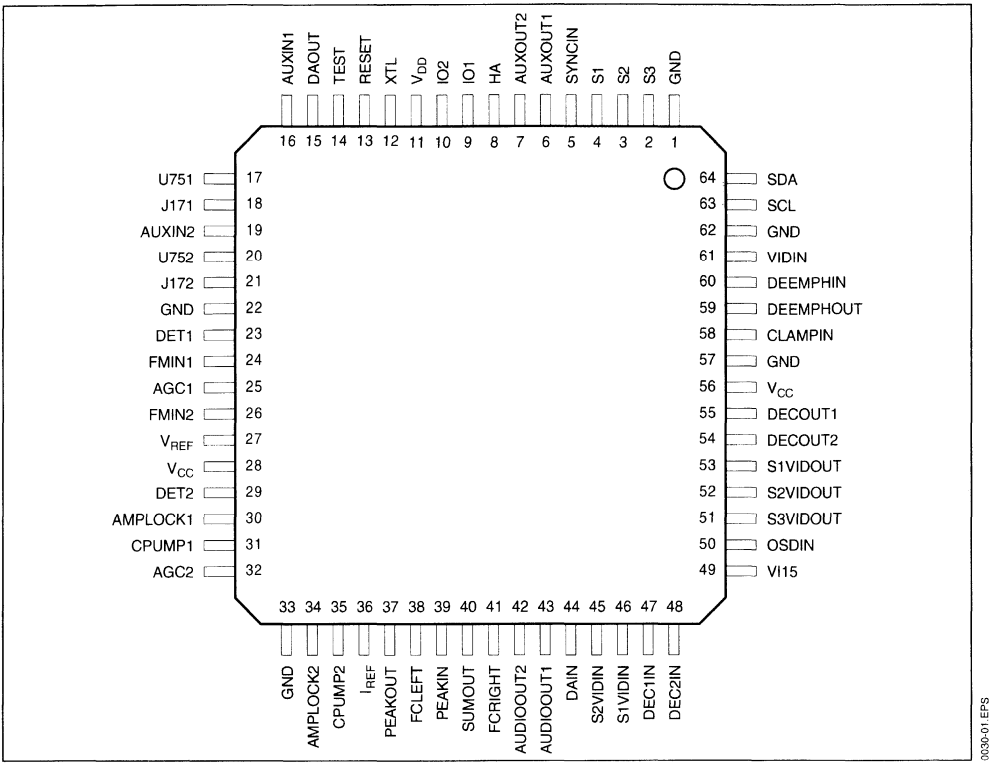
DESCRIPTION

The STV0030 is a BICMOS integrated circuit for use in satellite receivers. The great variety of FM deviations, energy dispersal and subcarrier standards makes the design of satellite receivers able to receive all programs a complex task. The device has been designed to specially adapt to all known conditions in analog video and radio transmissions.

The choice of the surface mounting PQFP64 package ensures optimisation of real-estate requirements.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS



0030-01.EPS

PIN ASSIGNMENT

Pin	Name	Function
1	GND	Digital power ground
2	S3	SCART-3 driver
3	S2	SCART-2 driver
4	S1	SCART-1 driver
5	SYNCIN	Digital or analog sync signal input
6	AUXOUT1	Fixed level audio output left
7	AUXOUT2	Fixed level audio output right
8	HA	Hardware address
9	IO1	Digital input/output 1
10	IO2	Digital input/output 2
11	V_{DD}	Digital 5V power supply
12	XTL	4/8MHz quartz crystal
13	RESET	System reset
14	TEST	Test pin
15	DAOUT	DAC amplifier output
16	AUXIN1	Auxilliary audio input left
17	U751	75µs de-emphasis timeconstant left

0030-01.TBL

PIN ASSIGNMENT (continued)

Pin	Name	Function
18	J171	J17 de-emphasis timeconstant left
19	AUXIN2	Auxilliary audio input right
20	U752	75µs de-emphasis timeconstant right
21	J172	J17 de-emphasis timeconstant right
22	GND	RF and audio ground
23	DET1	FM PLL filter left
24	FMIN1	FM demodulator +ve input
25	AGC1	AGC peak detect capacitor left
26	FMIN2	FM demodulator -ve input
27	VREF	2.44V reference
28	V_{CC}	Audio 12V supply
29	DET2	FM PLL filter right
30	AMPLOCK1	Amplitude detector capacitor left
31	CPUMP1	FM PLL charge pump capacitor left
32	AGC2	AGC peak detector capacitor right
33	GND	Ground for volume control ANRS, VCO
34	AMPLOCK2	Amplitude detector capacitor right
35	CPUMP2	FM PLL charge pump capacitor right
36	IREF	Current reference resistor
37	PEAKOUT	ANRS peak detector capacitor
38	FCLEFT	Audio roll-off left
39	PEAKIN	ANRS peak detector input
40	SUMOUT	ANRS summing output
41	FCRIGHT	Audio roll-off right
42	AUDIOOUT2	Level controlled audio out right
43	AUDIOOUT1	Level controlled audio out left
44	DAIN	Digital/Analog Converter sense input
45	S2VIDIN	External video input 2
46	S1VIDIN	External video input 1
47	DEC1IN	Decoder 1 input (e.g. D2MAC)
48	DEC2IN	Decoder 2 input (e.g. Videocrypt)
49	VI5	Clamped video input
50	OSDIN	On-Screen-Display video input
51	S3VIDOUT	SCART-3 video output (with OSD)
52	S2VIDOUT	SCART-2 video output (with OSD)
53	S1VIDOUT	SCART-1 video output (without OSD)
54	DECOUT2	Satellite decoder drive 2
55	DECOUT1	Satellite decoder drive 1
56	V_{CC}	Video 12V supply
57	GND	Video ground
58	CLAMPIN	Sync-tip clamp input
59	DEEMPHOUT	Video de-emphasis output
60	DEEMPHIN	Video de-emphasis input
61	VIDIN	Video input buffer
62	GND	Video input ground
63	SCL	I^2C bus clock
64	SDA	I^2C bus data

0030-01.TBL

PIN FUNCTION DESCRIPTION

I - SCART DRIVERS WITH OSD

'Text' must be able to be added to the video on command with or without 'blanking'. Blanking adds either a black line around the characters or a black box for the characters to sit in. During 'blanking' the chip will output OSD 'background' level.

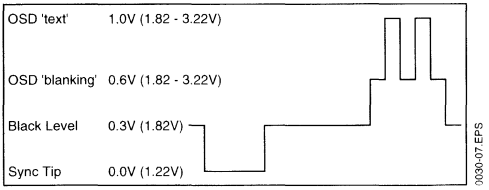
There are 2 basic presentation modes of OSD 'text'.

1) OSD 'text' written on a blank screen of selectable brightness.
2) OSD 'text' written on top of the TV picture.

Additionally the OSD 'text' can be displayed with or without 'blanking'. The blanking from the microcontroller typically comes in two styles. Either as a line around characters or a box for the characters to sit in).

1 of 4 output levels from the SCART are required when using OSD. The diagram below shows part of a TV line displaying a small OSD. It starts with :

a) a line sync pulse of 5µs at 0V then,
b) 13µs at black level, followed by
c) 2µs at OSD 'background' level.
d) This is the OSD 'text' which has been shown as 2µs pulses going to peak white. These would be typically programmed to say 0.8V with the OSD 'background' at 0.3V (1.82V at matrix output).



In order to achieve this two DACs are used to generate the programmable voltage levels for OSD 'background' and 'text'.

The video outputs and terms are :

i) Normal video
   sync tips = +1.22V
   black level = +1.82V
   peak white = +3.22V

ii) Video with OSD
   Video with OSD
   sync tips = +1.22V
   black level = +1.82V
   'background' level = +1.82V to 3.22V, programmable in 8 steps of 0.2V per step
   'text' = +3.22V to 1.82V, programmable in 8 steps of 0.2V per step

iii) 'background' occurs during active video so whenever the micro generates 'blanking' it will force the SCART output to 'background' level (+1.82V to +3.22V).

iv) 'text' occurs during active video so whenever OSD occurs the SCART output is forced to 'peak white' (+3.22V to +1.6V). In fact the OSD 'text' has higher priority than 'background' so gets applied to the signal stream after 'background'.

Described above is an ideal situation with 2.0V_{PP} video with the bottom of the sync pulses at 1.22V. However the actual voltage of the sync tips will vary because the video is AC coupled and the picture content will change. Thus, in order to apply the 'blanking' or 'OSD' we need DC restored video the voltage of the sync tips are known and this is achieved by having 'DC level clamps' on all video input pins.

Pin 2 S3

This is the tri-stateable bi-directional SCART pin 8 driver for SCART-3. Since SCART-1,2 & 3 can be either controller or receiver SCART pin 8 is either an output or input. Since some equipment does not follow the SCART spec fully, the micro has full control of these pins via bits in the 'control' block.

As input; Z_{IN}>10kΩ <5V = logic 0, >9V = logic 1

As output; logic 0 outputs sink 1-3mA to gnd
logic 1 outputs source 1-3mA from V_{CC}-1V

Pin 3 S2

SCART-2 driver, same spec as pin 2.

Pin 4 S1

SCART-1 driver, same spec as pin 2.

2 - CONTROL BLOCK

This has an I^2C bus 2 wire interface. It contains registers

for the control data for the modules on the chip. It also contains 5 bi-directional tri-stateable logic I/O drives.

Pin 1 Ground

The main power ground connection for the control logic, registers, the I^2C bus interface, synthesiser & watchdog.

Pin 8 HA

For the I^2C bus interface it is necessary to have a programmable bit on the address in case the chip address clashes with that of another chip in the application. CMOS input levels must be held high or low externally ; 0 = 06h, 1 = 46h.

Pin 9 IO1

A general purpose I/O pin with dual functionality. It is intended to monitor a MAC decoder module signal line to see if it is receiving a MAC encoded signal.

Pin 10 IO2

A general purpose I/O pin intended to monitor a Videocrypt decoder module signal line to see if it is receiving a Videocrypt encoded signal. It may alternatively be programmed via I^2C bus to output an internally generated 20KHz squarewave for LNB control.

Pin 11 V_{DD}

Digital +5V power supply.

Pin 63 SCL

This is the I^2C bus clock line. Clock = DC to 100kHz. Requires external pull up eg. 10kΩ to 5V.

Pin 64 SDA

This is the I^2C bus data line. Requires external pull up eg. 10kΩ to 5V.

3 - MISCELLANEOUS BITS

Pin 12 XTL

This pin allows for the on-chip oscillator to be either used with a crystal to ground of 4MHz, or to be driven by an external source via a 22kΩ series resistor. The external source can be either 4MHz or 8MHz. A programmable bit in the control block removes a÷ 2 block when the 4MHz option is selected.

Pin 13 RESET

Power on reset output. This is a voltage sensitive circuit and will give a LOW output until both supplies to this chip rise to greater than 80% of their correct value. It has some hysteresis so will remain HIGH until either of the supplies falls below 65%. The output is a current sink, 4mA, with an internal 10kΩ pull-up resistor. It is possible to force the chip into or out of reset and by pass the on-chip delay.

Typical thresholds are:	V_{DD}=5V	V_{CC}=12V
power up	3.8V	9.25V
power down	3.2V	7.5V

Pin 14 TEST

Test pin to enable scan path testing of logic.

Normal operation = L Test mode = H

Pin 15 DAOUT

This is the LNB PSU drive which is the output of an amplifier that compares the input on pin 44 with an 8-bit DAC. The DAC is programmed through the I2C bus interface to set the reference voltage for the LNB drive amplifier. The voltage range is 0 to 2.44 volts (2 bandgaps), hence the feedback signal must be divided down to be in this range.

Pin 44 DAIN

The voltage actually fed to the LNB is divided down & connected here (feedback) for the on-chip regulator.

4 - SOUND DETECTION BLOCK

The different de-emphasis formats are selected through the audio MUX and are the same for both channels. That is, as with the volume control, the I^2C bus registers simultaneously control both channels with each bit of registers.

Pin 6 AUXOUT1

This audio output is sourced directly from the audio MUX, and as a result does not include any volume control function. It will output $1V_{PP}$ biassed at 2.4V with Z_{OUT}=1kΩ. If SCART socket drive is needed then an external buffer will be required.

Pin 7 AUXOUT2

See pin 6.

Pin 16 AUXIN1

This pin allows an auxilliary audio signal to be connected to the input of channel 1 audio processor and hence makes use of the on chip volume control. An on-board MAC decoder is a typical user of this feature.

Pin 17 U751

A capacitor and resistor in parallel of 75µs time constant connected between here and V_{REF} (pin 27) to provide 75µs de-emphasis for channel 1. Internally selectable is an internal resistor that can be programmed to be added in parallel thereby converting the network to approx 50µs

de-emphasis. The value of the internal resistor is 44kΩ ± 30%. The amplifier for this filter is voltage input, current output; with ± 500mV input the output will be ± 55µA.

Pin 18 J171

The external J17 de-emphasis network for channel 1. The amplifier for this filter is voltage input, current output; with ± 500mV input the output will be ± 55µA.

Pin 19 AUXIN2

This pin allows an auxilliary audio signal to be connected to the input of channel 2 audio processor and hence makes use of the on-chip volume control. An on-board MAC decoder is a typical user of this feature.

Pin 20 U752

A capacitor and resistor in parallel of 75µs time constant connect between here and V_{REF} (pin 27) to provide 75µs de-emphasis for channel 2. Internally selectable is an internal resistor that can be programmed to be added in parallel thereby converting the network to approx 50µs de-emphasis (see control block map). The value of the internal resistor is 44kΩ ± 30%. The amplifier for this filter is voltage input, current output; with ± 500mV input the output will be ± 55µA.

Pin 21 J172

The external J17 de-emphasis network for channel 2. The amplifier for this filter is voltage input, output current. Output with ± 500mV input will be ± 55µA.

Pin 22 GND

This ground pin is double bonded ; 1) to channel 1 RF section & VCO and 2) to both AGC amplifiers, channel 1 audio section, audio MUX, internal power & references to audio section.

Pin 23 DET1

The output of FM phase detector 1 (left channel). This is for the connection of an external loop filter for the PLL. The output is a push pull current source with ± 90µA output with æ 500mV input to the internal mixer.

Pin 24 FMIN1

This is the +ve input to the two FM demodulators. It feeds two AGC amplifiers with a bandwidth of at least 5-10MHz. There is one amplifier for each channel both with the same differential input. The AGC amplifiers have a 0dB to + 40dB range and will produce a constant signal of 1.0V about the 2.44V reference into the respective demodulators.

Z_{IN} = 5kΩ Min input = $2mV_{PP}$ per subcarrier

Max input = $500mV_{PP}$ (max when all inputs are added together, when their phases coincide).

Pin 25 AGC1

AGC amplifier 1 peak detector capacitor connection. The output current has an attack/decay ratio of 1:32. That is the ramp up current is approximately 5µA and decay current is approximately 160µA. 11V gives maximum gain. This pin is also driven by a circuit monitoring the voltage on AMPLOCK1.

Pin 26 FMIN2

This is the -ve input to the AGC amplifiers forming a differential input stage. All inputs are biased to V_{REF} (2.44V) via an internal 10kΩ resistor.

Pin 27 VREF (2.44V)

This is the audio processor voltage reference used throughout the FM/audio section of the chip. As such it is essential that it is well decoupled to ground to reduce as far as possible the risk of crosstalk and noise injection. This voltage is derived directly from the bandgap reference of 1.22 volts.

Pin 28 V_{CC} (+12V power supply)

Double bonded main power pin for the audio/FM section of the chip. The two bond connections are; (1 to the ESD and guard rings and 2) to power the circuit and on chip regulators/references.

Pin 29 DET2

The output of FM phase detector 2 (right channel). This for the connection of an external loop filter for the PLL. The output is a push-pull current source with ± 90mA output with ± 500mV input to the internal mixer. See pin 23.

Pin 30 AMPLOCK1

The output of amplitude detector 1. Requires a capacitor and a resistor to GND. The voltage across this is used to decide whether there is a signal being received by FM det 1. The level detector output drives a bit in the 'control block' I^2C bus register 7 bit 0. This also drives AGC amp 1. When the voltage on this pin is $>(V_{REF}+1V_{BE})$ it sinks current to V_{REF} from pin 25 to reduce the AGC gain.

Pin 31 CPUMP1

The output from the frequency synthesiser is a push-pull current source which requires a capacitor

to ground to derive a voltage to pull the VCO to the target frequency. The output is ± 100µA to achieve lock and ± 2µA during lock to provide a tracking time constant of approximately 10Hz.

Pin 32 AGC2

AGC amplifier 2 peak detector capacitor connection. The output current has an attack/decay ratio of 1:32. That is the ramp up current is approximately 5µA and decay current is approximately 160µA. 11V gives maximum gain. This pin is also driven by a circuit monitoring the voltage on AMPLOCK2.

Pin 33 GND

This ground pin is double bonded ; 1) to the volume control, ANRS, ESD and guard rings and 2) to the VCO & RF section of channel 2.

Pin 34 AMPLOCK2

The output of amplitude detector 2. Requires a capacitor and resistor to GND. The voltage across this is used to decide whether there is a signal being received by FM det 2. The level detector output drives a bit in the 'control block' I^2C bus register 7 bit 1. This also drives AGC amp 2. When the voltage on this pin is $>(V_{REF}+1V_{BE})$ it sinks current to V_{REF} from pin 32 to reduce the AGC gain.

Pin 35 CPUMP2

The output from the frequency synthesiser is a push-pull current source which requires a capacitor to ground to derive a voltage to pull the VCO to the target frequency. The output is ± 100µA to achieve lock and ± 2µA during lock to provide a tracking time constant of approximately 10Hz.

Pin 36 IREF

This is a buffered V_{REF} output to an off-chip resistor to produce an accurate current reference, within the chip, for the biasing of amplifiers with current outputs into filters. It is also required for the ANRS circuit to provide accurate rolloff frequencies. This pin should not be decoupled as it will inject current noise. The target current is 10µA ± 2 thus a 240kΩ ± 1% is required.

5 - AUTOMATIC NOISE REDUCTION SYSTEM (ANRS) AND VOLUME CONTROL

There is a ANRS defeat which allows the audio to bypass the ANRS section but still go to the volume control. The volume control will be 32 steps of 1.25dB, with the lowest step being audio 'mute' (no output).

Pin 37 PEAKOUT

The ANRS control loop peak detector output requires a capacitor to ground from this pin. Also a 1.2MΩ resistor to V_{REF} pin 27 to give some accurate decay time constant. The value of the capacitor and resistor control the attack and decay times, typically 0.1ms attack & 25ms decay.

Pin 38 FCLEFT

The variable bandwidth gm amplifier has a current output which is variable depending on the input signal amplitude as defined by the control loop. The output current is then dumped into an off-chip capacitor which together with the accurate current reference define the min/max rolloff frequencies. A 330pF capacitor is connected to ground from this pin for channel 1 (left).

Pin 39 PEAKIN

This is the input to the control loop peak detector and is connected to the output of the off-chip control loop band pass filter. This requires AC coupling between this input pin and the summer output pin 40.

Pin 40 SUMOUT

The two audio inputs are summed together with an amplifier with a gain of 0.5 ie. if both inputs are 1 volt then the output is 1 volt. This amplifier has an input follower buffer which gives a V_{BE} offset in the DC bias voltage. Thus the filter which this amplifier drives must include AC coupling to the next stage (pin 39).

Pin 41 FCRIGHT

The variable bandwidth gm amplifier has a current output which is variable depending on the input signal amplitude as defined by the control loop. The output current is then dumped into an off-chip capacitor which together with the accurate current reference define the min/max rolloff frequencies. A 330pF capacitor is connected to ground from this pin for channel 2 (right).

Pin 42 AUDIOOUT2

The main audio output from the volume control level shifted and amplified to produce $2V_{PP}$ on a DC bias of 4.88 volts. This amplifier has short circuit protection and is intended to drive a SCART connector directly via AC coupling and meets the standard SCART drive requirements. This pin is the channel 1 or left output.

Pin 43 AUDIOOUT1

The main audio output from the volume control

level shifted and amplified to produce $2V_{PP}$ on a DC bias of 4.88 volts. This amplifier has short circuit protection and is intended to drive a SCART connector directly via AC coupling and meets the standard SCART drive requirements. This pin is the channel 2 or right output.

6 - VIDEO BLOCK

Pin 5 SYNCIN

This input can be programmed to accept either a digital or an analog sync stream. The digital input will accept a made up sync signal consisting of the Genlock 'line' and 'frame' sync output. If it is smaller than 0.8V then it produces a sync tip level voltage (1.22V). If it is greater than 2.0V it produces black level (1.52V). This will generate a sync stream signal consisting of syncs only, that will be available on the 'Video Matrix'. The DC level of these syncs at the SCART O/Ps will be sync tip = 1.22V black level = 1.82V. The analog path is connected directly to the video matrix.

When pin-49 is selected for the video MUX, it is still possible to insert an external sync. The input must be a digital sync (Reg 18b6 = 1 > sync enabled) and is typically used to stabilise the OSD on a bad or noisy video on pin-52 only.

Control bits

2 bits	I^2C bus Reg 1	bits 6 ,5	Effect
			Sync source
	default ------	X 0	Digital
		0 1	Analog
		1 1	Pin-49 clamped

Pin 45 S2VIDIN

External video input $1V_{PP}$ AC coupled 75Ω source impedance returned from a VCR for example. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other. The clamp sink current is $1\mu A \pm 30\%$ with the buffer $Z_I > 1M\Omega$. This signal is an input to the Video Matrix and is called SCART-2 Return.

Pin 46 S1VIDIN

External video input $1.0V_{PP}$ AC coupled 75Ω source impedance. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other. The clamp sink current is $1\mu A \pm 30\%$ with the buffer $Z_{IN} > 1M\Omega$. This signal is an input to the Video Matrix and is called SCART-1 Return.

Pin 47 DEC1IN

This input receives a PAL encoded output from, for instance a D2MAC decoder inside the receiver. The signals from pins 47 and 48 go to an internal selector switch that selects which signal goes to the Video Matrix.

Control bit

1 bit	I^2C bus Reg 1	bit	4	Signal selected
	default	---	0	Pin 48 (DEC2IN)
			1	Pin 47 (DEC1IN)

The output signal from the selector switch, which goes to the Video Matrix, is called Internal Decoder Return.

Pin 48 DEC2IN

This input can be driven for instance by the output of a Videocrypt decoder ZOUT = 500Ω video about $1.0V_{PP}$ from the reconstruction filter. This input has a DC restoration clamp on its input. This gets the video to the correct DC level so that OSD can be added later when it is essential that the voltages of the video and OSD are at the correct levels with respect to each other.

The clamp sink current is $1\mu A \pm 30\%$ with the buffer $Z_{IN} > 1M\Omega$. The signals from pins 47 and 48 go to an internal selector switch that selects which signal goes to the Video Matrix.

Control bit

1 bit	Reg 1	bit	4	Signal selected
	default	---	0	Pin 48 (DEC2IN)
			1	Pin 47 (DEC1IN)

Pin 49 VI5

A video input with clamp @ 1.22V internally. It may be employed for use with noisy video signals by overiding the sync clamp externally at about 3V (this overcomes the 1.22V plus 2x V_{BE}).

Pin 50 OSDIN

Typically driven by a combination of an OSD O/P and the 'Blank' output from the OSD bit of the Micro. This input is then threshold detected and two outputs are generated.

Input	Output	
	Background	Text
< 0.8V	0	0
1.5-2.5V	1	0
> 3.5V	1	1

Pin 51 S3VIDOUT

Video driver for SCART-3 with OSD. This requires an external emitter follower buffer to drive a 150Ω load. The average DC voltage to be 1.5V on the O/P. The signal on pin 51 is video 2.0V_{PP} 5.5MHz B/W with sync tip=1.22V. This SCART O/P will be used to drive the TV typically. This pin gets its signal from the Video Matrix. It is then amplified and OSD is added before being output. The signal selected from the Video Matrix for output on this pin is controlled by a control register.

Control bits

3 bits I^2C bus Reg 4 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
		0	1	0	Normal video
default	------	0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

OSD addition is controlled by a control register. It is possible to separately control whether or not to add 'blanking' and/or 'text' to the video stream to this SCART output.

Control bits

2 bits I^2C bus Reg 4 bits		4,	3	Effect enabled
default	------	0	0	Background = Off Text = Off
		0	1	Background = On Text = Off
		1	0	Background = Off Text = On
		1	1	Background = On Text = On

Pin 52 S2VIDOUT

(See 1/ SCART drivers with OSD). Video driver for SCART-2. See pin 51.

Control bits

3 bits I^2C bus Reg 3 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
		0	1	0	Normal video
default	------	0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

OSD addition is controlled by a control register. It is possible to separately control whether or not to add 'blanking' and/or 'text' to the video stream to this SCART output.

Control bits

2 bits I^2C bus Reg 3 bits		4,	3	Effect enabled
default	----	0	0	Background = Off Text = Off
		0	1	Background = On Text = Off
		1	0	Background = Off Text = On
		1	1	Background = On Text = On

See also pin-5 where it is possible to add sync to stabilise OSD or video.

Pin 53 S1VIDOUT

Video driver for SCART 1. See pin 51. No OSD available on this output.

Control bits 3 bits I^2C bus Reg 2 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
		0	1	0	Normal video
default	------	0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 54 DECOUT2

Drives a second decoder such as D2MAC and this is able to pass 10MHz. See pin 53.

Control bits 3 bits I^2C bus Reg 6 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
		0	1	0	Normal video
default	------	0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 55 DECOUT1

This output can drive for instance a decoder. To allow for D2MAC it is able to pass 10MHz ; ZOUT < 75Ω. Video on this pin will be $1.9V_{PP} \pm 0.05V$. When a Videocrypt encoded signal is output to the decoder on this pin its sync tips must be at $1.49V_{DC} \pm 0.05V$. This pin gets its signal from the Video Matrix. It is then level shifted and amplified by 1.9 before being output. The signal selected from the Video Matrix for output on this pin is controlled by a control register.

Control bits 3 bits I^2C bus Reg 5 bits		2,	1,	0	Source selected
		0	0	0	Baseband
		0	0	1	De-emhpasised
		0	1	0	Normal video
default	------	0	1	1	Decoder return
		1	0	0	SCART 1 return
		1	0	1	SCART 2 return
		1	1	0	Syncs
		1	1	1	Nothing selected

Pin 56 V_{CC}

+12V double bonded ; 1) ESD+guard rings & 2) video circuit power.

Pin 57 GND

Strategically placed video power ground connection to reduce video currents getting into rest of circuitry.

Pin 58 CLAMPIN

This pin clamps the most negative extreme of the input (the sync tips) to +1.22V_{DC} (or appropriate voltage). The video at the clamp input is only 1V_{PP}. This clamped video which is de-emphasised, filtered and clamped (energy dispersal removed) is normal, negative syncs, video. This signal drives the Video Matrix input called Normal Video.
It has a weak (1.0µA ± 15%) stable current source pulling the input towards GND. Otherwise the input impedance is very high at DC to 1kHz Z_{IN} > 2MΩ. Video bandwidth through this is -1dB at 5.5MHz. The CLAMP input DC restore voltage is then used as a means for getting the correct DC voltage on the SCART outputs.

Pin 59 DEEMPHOUT

Output of de-emphasis ZOUT < 50Ω 2V_{PP} B/W still 10.25MHz. This is the output that drives the capacitor into the CLAMP. It has to do this via the sound removal filter which may be a 5 or 7 pole low pass filter Z_{IN} = Z_{OUT} = 500Ω -3dB corner about 5.25MHz. Video at pin 59 is positive. Internally the 2V_{PP} video is reduced to 1V_{PP} to drive the internal Video Matrix input called De-emphasised video. This signal also called 'Unclamped Unfiltered' and is the signal required by Filmnet PAL decoders for example. It is called unfiltered because it still has its high frequency sub-carriers (not been through the low pass filter).

Pin 60 DEEMPHIN

Input of de-emphasis stage, with a Z_{IN} of 10kΩ or greater. B/W is 10.25MHz. The network between pins 59 & 60 will give 2x gain at 1.52MHz, about -2dB gain at 5MHz and +17dB gain at 10kHz as in accordance with CCIR 405-1.

Pin 61 VIDIN

AC-coupled Video input from a tuner. This is raw baseband up to 10.25MHz. Input amplitude is 0.25-1.0V_{PP} at 1.52MHz. Z_{IN} > 5kΩ. This drives an on-chip video amplifier. The other input pin of this amp is AC grounded by being connected to an internal V_{REF}. The video amplifier has selectable gain from 0dB to 12.7dB in 63 steps. This is programmable, as is the output selected, whether normal or inverted.

Control bits

6 bits I2C bus Reg 18	bits	5,	4,	3,	2,	1,	0	Gain Selected
default	------	0	0	0	0	0	0	0dB
		n						n x 0.202dB
		1	1	1	1	1	1	+12.7dB

The normal or inverted output selected (which is 1.0V_{PP}) also drives the Video Matrix input called Baseband.

Control bit

1 bit I^2C bus Reg 1	bit	3	Video selected
default	----	0	Normal
		1	Inverted

Pin 62 GND

Ground, especially for the low level input from the tuner.

Figure 1 : Fundamental Block Diagram

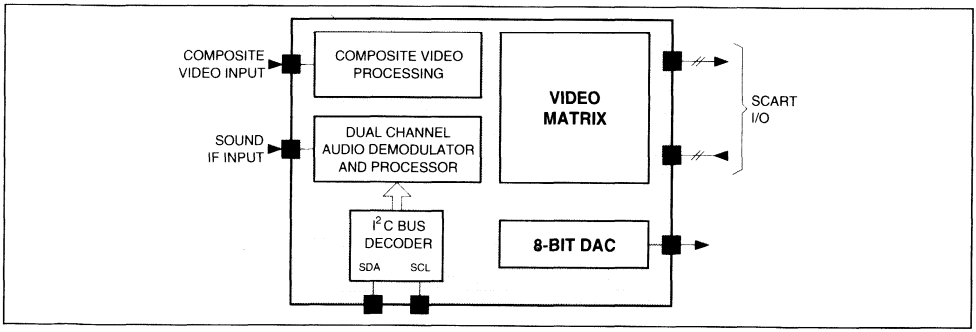


Figure 2 : Video Processing Block Diagram

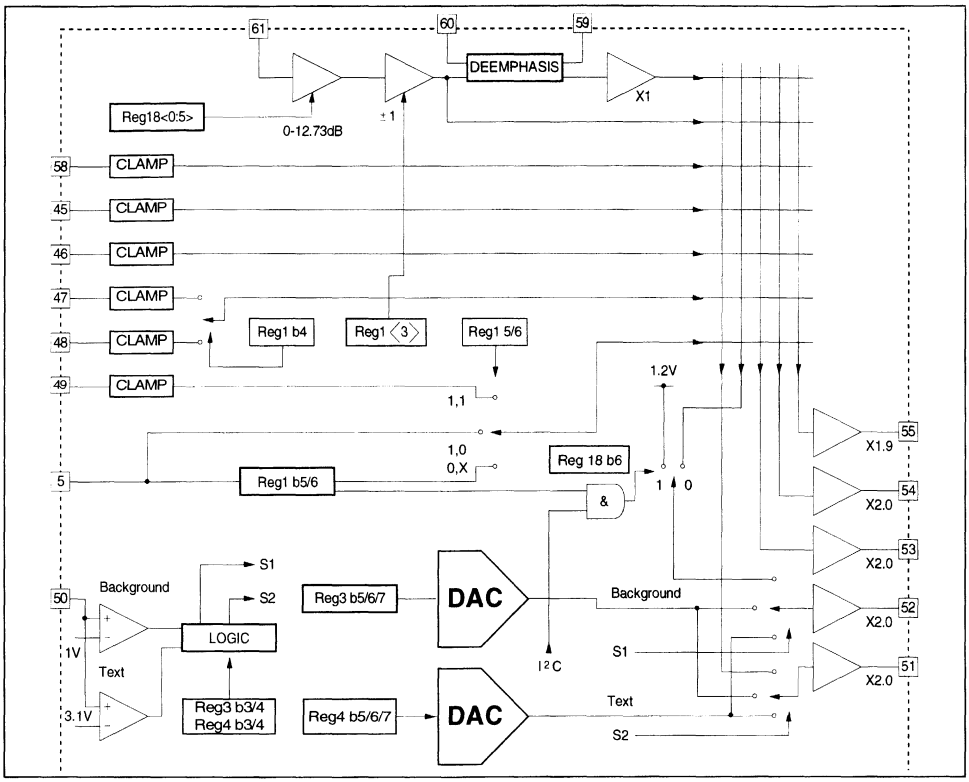


Figure 3 : FM Demodulation Block Diagram

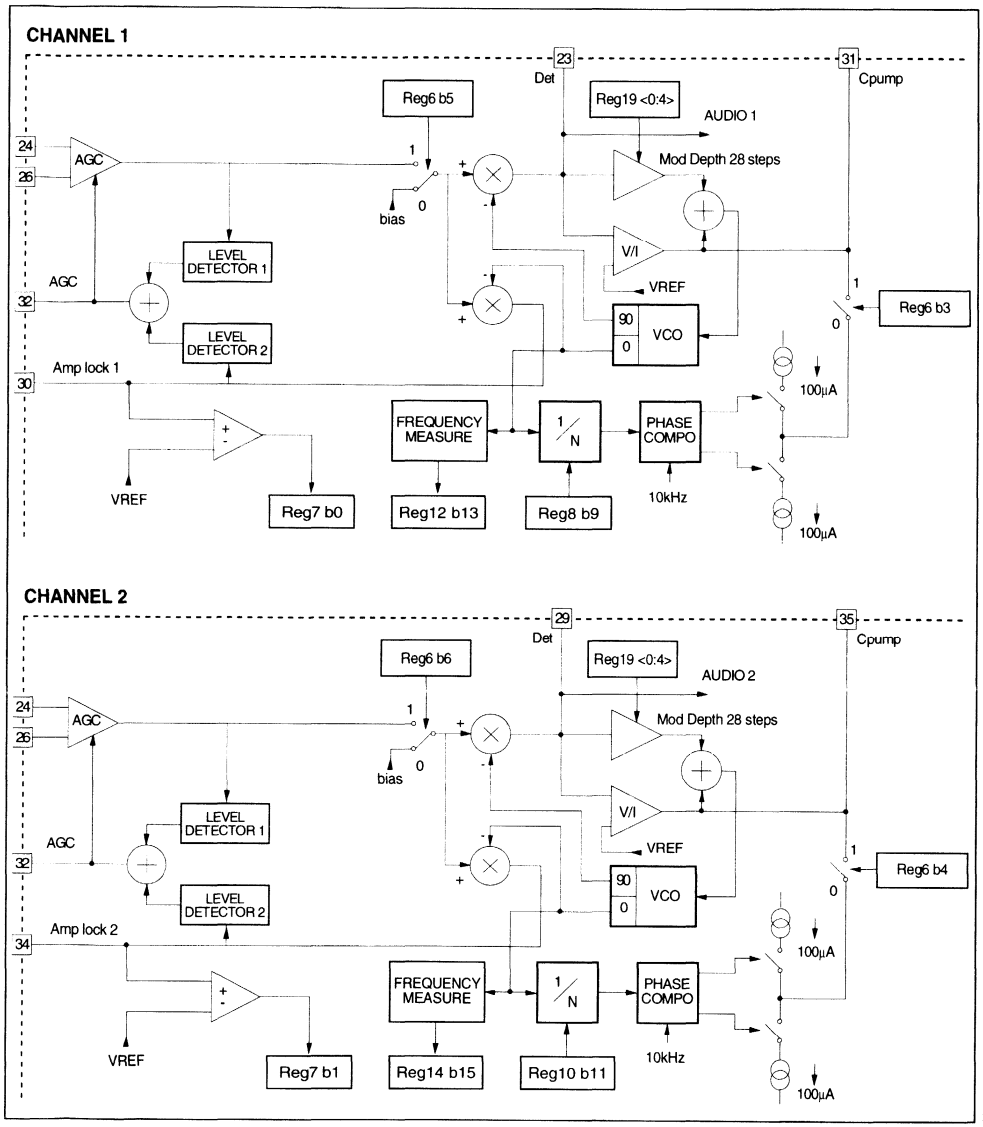
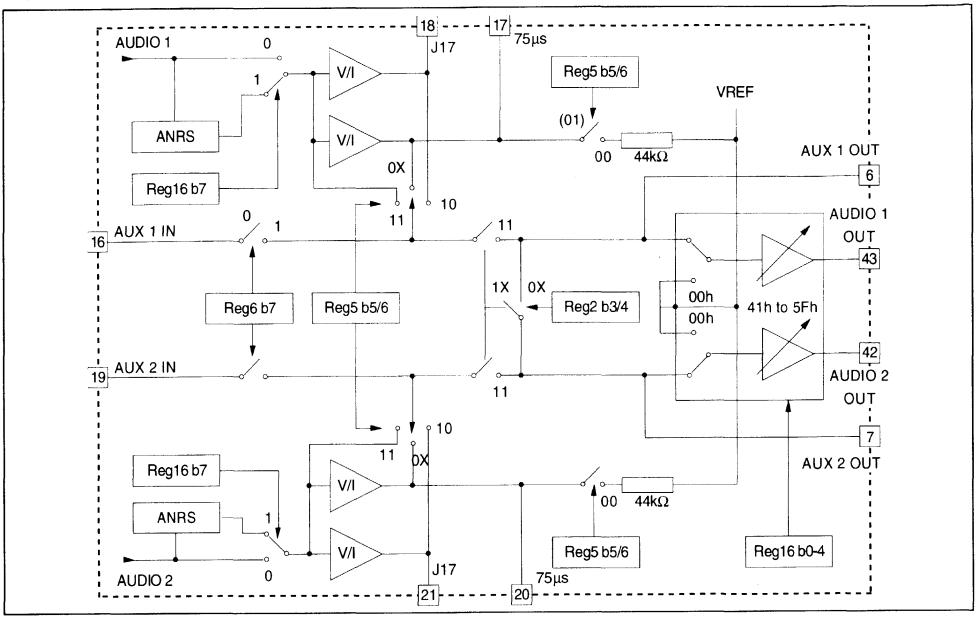


Figure 4 : Audio Processing Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC} V_{DD}	Supply voltage	13.2 7.0	V V
P_{tot}	Total power dissipation	1.0	W
T_{oper}	Operating temperature range	0, +70	°C
T_{stg}	Storage temperature	-55, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Thermal resistance junction-ambient	80	°C/W

0030-04.TBL

DC AND AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} V_{DD}	Supply voltage range		10.8 4.75	12 5.0	13.2 5.25	V V
IQ_{cc} IQ_{dd}	Supply current		70 10			mA mA

0030-05.TBL

DC AND AC ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO DEMODULATOR (see Figure 3)						
FMI	FM subcarrier input level Pin 24 - Pin 26 for AGC action	VCO locked on carrier at 6MHz, 470kΩ load on Pin 30 and Pin 34	5		500	mV_{PP}
DETH	Detector 1 and 2 (Pins 30 and 34) threshold for activating AGC		2.8	3.1	3.4	V
IDETA	Max sink/source Pins 30 and 34 current	With AGC operation		100		µA
IDETS	Max sink/source Pins 30 and 34 current	Without AGC limited gain		200		µA
VCO5	VCO voltage Pins 31 and 35 for 5MHz					V
VCO10	VCO voltage Pins 31 and 35 for 10MHz					V
AP50	1kHz audio level at PLL output Pin 23 and Pin 29	$0.5V_{PP}$ 50kHz deviation FM in Coarse deviation set to 50kHz	0.5	1	1.5	V_{PP}
APA50	1kHz audio level at PLL output Pins 23 and 29	$0.5V_{PP}$ 50kHz dev. FM input Coarse and fine settings used	0.85	1	1.15	V_{PP}
FMDMN	Min. 1kHz deviation allowing nominal audio on Pins 23 and 29	$1V_{PP}$ ±3dB Audio level, Deviation settings = 11111			25	kHz
FMDMX	Max. 1kHz deviation allowing nominal audio on Pins 23 and 29	$1V_{PP}$ ±3dB Audio level, Deviation settings = 00101	190			kHz
APM	Pin 23 Max audio before clipping	1kHz, 10% THD max		2		V_{PP}
DPCO	Digital Phase comparator Pins 31 and 35 output current	Sink and source current to external capacitor		100		µA
AUDIO DE-EMPHASIS						
D50e	1kHz audio level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 2.2nF load Internal 44kΩ off input and settings as APA50	1.13	1.91	2.86	V_{PP}
D50i	1kHz audio level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 3.3nF load Internal 44kΩ on input and settings as APA50	0.73	1.16	1.67	V_{PP}
D75	1kHz audio level on 50µs de-emphasis output Pins 17 and 20	22kΩ and 3.3nF load Internal 44kΩ off input and settings as APA50	1.07	1.80	2.70	V_{PP}
DJ17	1kHz audio level on J17 de-emphasis output Pins 18 and 21	Load as in Figure 3, input and settings as APA50	0.86	1.45	2.17	V_{PP}
R50	Internal resistor for 50/75µs switching		30	44	58	kΩ
AUTOMATIC NOISE REDUCTION SYSTEM						
LRS	Left + Right Summer output Pin 40	Left and right as for APA50 with external 50µs network				V_{PP}
NDRT	PIN 37 level detector rise time constant	External 22nF load		110		µs
NDFT	PIN 37 level detector fall time constant	External 22nF to GND and 1.2MΩ to Pin 27		26.4		ms
NDLL	PIN 37 bias level	No audio in	2.24	2.44	2.64	V
NDML	PIN 37 Max level (internal clamp)	3 V_{PP} 1kHz on Pins 23 and 29		3		V
LLCF	Noise reduction cutoff frequency for low level audio	100mV_{PP} on Pin 23 only				kHz
HLCF	Noise reduction cutoff frequency at high level	1 V_{PP} on Pin 23 and 29				kHz

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AUDIO OUTPUT Pins 42 and 43						
AOLN	Audio output level at nominal input at 0dB attenuation setting, measured on Pins 42 and 43	FM input as for APA50 No de-emphasis No noise reduction	1.57	1.9	2.25	V_{PP}
AOL50	Audio output level at nominal input at 6dB attenuation setting, Measured on Pins 42 and 43	FM input as for APA50 50µs de-emphasis as for D50e No noise reduction	1.03	1.80	2.78	V_{PP}
AOL17	Audio output level at nominal input at 3.75dB attenuation setting, Measured on Pins 42 and 43	FM input as for AP50, J17 de-emphasis No noise reduction	1.03	1.81	2.78	V_{PP}
AMA1	Audio output attenuation with mute on	1kHz audio	70	80		dB
AMA20	Audio output attenuation with mute on	20kHz		70		dB
MXAT	Max attenuation before mute	1kHz, from Aux input Pins 16 and 19 to Pins 42 and 43	32.00	32.75	33.50	dB
MXAG	Max audio gain	1kHz, from Aux input Pins 16 and 19 to Pins 42 and 43	5.50	6.00	6.50	dB
ASTP	Attenuation of each of the 31 steps	1kHz		1.25		dB
MAAO	Max audio out Pins 42 and 43 @10%THD	1kHz AUX. input		5.9		V_{PP}
MFMAO	Max audio out Pins 42 and 43 @10%THD	FM input as AP50		4.5		V_{PP}
I/O's (Pins 2, 3, 4, 9 and 10)						
SCIL	Pin 2, 3 or 4 low level input				2	V
SCIH	Pin 2, 3, or 4 high level input		9.5			V
SCOH	Pin 2, 3 or 4 high level output	10kΩ load to ground	9.5	11		V
SCOL	Pin 2, 3 or 4 low level output	10kΩ load to ground		0.1	2	V
V_{IL}	Pin 9 or 10 low level input				0.8	V
V_{IH}	Pin 9 or 10 high level input		2.4			V
V_{OL}	Pin 9 or 10 low level output	I_{Sink} = 2mA		0.2	0.4	V
V_{OH}	Pin 9 or 10 high level output	I_{Source} = 2mA	3.2	4.6		V
RESET						
RSR	Reset internal pull up resistor	Reset high		10		kΩ
RSI	Reset internal sink current	Reset low		1.5		mA
RTCCU	End of reset for VCC	V_{DD} = 5V, V_{CC} going up		9.2		V
RTCCD	Start of reset threshold for V_{CC}	V_{DD} = 5V, V_{CC} going down		7.5		V
RTDDU	End of reset threshold for V_{DD}	V_{CC} = 12V, V_{DD} going up		3.8		V
RTDDD	Start of reset threshold for V_{DD}	V_{CC} = 12V, V_{DD} going down		3.2		V
D/A CONVERTER ref.: fig. 1						
DA00	Minimum output voltage on Pin 15 for 00 hex	sense input Pin 44 connected to output Pin 15 and 10kΩ load resistor to GND	0		10	mV
DAFF	Max output voltage on Pin 15 for FF hex	as for DA00	2.24	2.44	2.64	V
ILE	Integral Linearity			0.5	2	LSB
DLE	Differential linearity			0.5	1	LSB

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DC AND AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 12V, V_{DD} = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
COMPOSITE SIGNAL PROCESSING (see Figure 2)						
VIDC	Pin 61 DC level	external load current µA	2.24	2.44	2.64	V
ZVI	Pin 61 input impedance			10		kΩ
DEODC	Pin 59 DC output level	1.2kΩ from Pin 59 to Pin 60 and 2kΩ from Pin 60 to GND	3.5	3.9	4.3	V
DEOAC	Pin 59 ac level for GV = 0 dB	Pin 61 level = $1V_{PP}$, 100kHz	1.9	2	2.1	V_{PP}
DEOMX	Pin 59 max ac level before clipping	GV = 0 dB	5	5.6		V_{PP}
DEOISC	Pin 59 max source current			8		mA
DEOISK	Pin 59 max sink current			2		mA
ZDEO	Pin 59 output impedance @ 5MHz			2		Ω
DGV	Gain error vs GV @ 100kHz	for GV = 0 to 12.7 dB	-0.5	0	0.5	dB
DINV	Gain variation when using inverter	@ 100kHz	-0.5	0	0.5	dB
DEBW	Bandwidth at Pin 59 for $1V_{PP}$ input measured on Pin 59	@ - 3dB with GV = 0dB	10			MHz
DFG	Differential gain on sync pulses measured on Pin 59	1 V_{PP} CVBS + 0.5V_{PP} 25Hz sawtooth input Pin 61, GV=0			1	%
CLAMP STAGES						
ISKC	Clamp input sink current pins 45, 46, 47, 48 49 and 58	V_{IN} = 3V	0.6	1	1.4	µA
ISCC	Clamp input source current same pins as ISKC	V_{IN} = 2V	30	50	70	µA
VCL	Sync tip level on selected output pin (pins 51, 52, 53 or 54)	$1V_{PP}$ CVBS through 10nF on input (45,46,47 or 58)	1.1	1.22	1.32	V
VCL5	Sync tip level on pin 55	same as for VCL	1.41	1.49	1.57	V
VIDEO MATRIX						
XTK	Output level on any output when 1Vpp	@ 5MHz	50			dB
	CVBS input is selected for any other					
	output					
BGT	Background graphics threshold PIN 50			1		V
CGT	Character foreground threshold PIN 50			3		V
BMN	Background level for 000 selection	measured on selected output Pin 52 or 53		TBD		V
BMX	Background level for 111 selection	same as BMN		TBD		V
FMN	Foreground level for 000 selection	same as BMN		TBD		V
FMX	Foreground level for 111 selection	Sames as BMN		TBD		V
BFG	Output buffer gain Pins 45,46,47,48,58	@ 100kHz		2		
BFG5	Output buffer gain Pin 55	@ 100kHz		1.9		

0030-06.TBL

CIRCUIT DESCRIPTION : VIDEO SECTION

The composite video is first set to a standard level by means of a 64 step gain controlled amplifier. In the case that the modulation is negative, an inverter can be switched in. The deemphasis network is fed by a wide bandwidth amplifier and energy dispersal is removed by a sophisticated sync tip clamping circuit. This circuit is used on all inputs to a video switching matrix, thus making sure that no DC steps occur when switching video sources.

The matrix can be used to feed video to and from decoders such as D2MAC or scrambled analog video.

Two special inputs allow insertion of graphics on video or clean sync, or a mix of both even when only noise is present at the tuner output.

CIRCUIT DESCRIPTION : AUDIO SECTION

The two audio channels are totally independent except for the possibility given to output on both channels only one of the selected input audio channels.

To allow a very cost effective application, each channel uses PLL demodulation. Except for the overall high pass filter removing the video of the composite signal, no complex filter is needed.

The frequency of the demodulated subcarrier is chosen by a frequency synthesiser which sets the frequency of the internal local oscillator by comparing its phase with the internally generated reference. When the frequency is reached, the microprocessor switches in the STV0030 PLL and the demodulation starts. At any moment the microprocessor can read from the device the actual frequency to which the PLL is locked. It can also verify that a carrier is present at the given frequency, thanks to an amplitude demodulator which is also used for the audio input AGC.

In order to maintain constant amplitude of the recovered audio regardless of variations between satellites or subcarriers, the PLL loop gain may be programmed from 28 values, with coarse (four values) and fine (7 steps) adjustment.

Two different networks can be permanently connected for either 75µs or J17 de-emphasis. If 50µs de-emphasis is required, this can be inserted by an internal switch, thus allowing a worldwide application.

A dynamic noise reduction system (ANRS) is used using a lowpass filter, the cutoff frequency of which is controlled by the amplitude of the audio after insertion of a bandpass filter.

Two audio outputs are provided : one is a fixed $1V_{PP}$ and the other is a gain controlled $2V_{PP}$. These outputs are chosen by an audio matrix between non de-emphasised, 50 or 75µs de-emphasised, J17 deemphasised audio channel. In each case the dynamic noise reduction system can be used. Alternatively the selected outputs can receive the auxilliary audio inputs without processing. The gain controlled amplifier has a gain range from + 6dB to - 32dB with 1.25dB steps. This can also be muted.

The 8-bit Digital to Analog Converter outputs a voltage ranging from 0 and 2.44V via a differential amplifier for digital words from 00 to FF. By adding a suitable output buffer/converter, this DAC can be used to control LNB voltages (or polariser currents) with a range exceeding 0 to 2.44V.

IIC CONTROL REGISTERS

Reg 1 IIC → reg

bit

0 L Not used
1 L Not used
2 L Not used
3 L Delect video invert (H = inverted, L = non-inverted)
4 L Select input (H = Pin 47, L = Pin 48)
5 L Select sync source

bits	6	5	
	X	0	digital sync input
	0	1	analogue sync input
	1	1	Pin 49 clamp input

6 L Select clamp Pin 49
7 Not used

Reg 2 IIC → reg

bit

0 L elect source for SCART 1 O/P
1 H Select source for SCART 1 O/P
2 L Select source for SCART 1 O/P
3 H Select Left/Right/Stereo (see audio mux truth table)
4 H Select Left/Right/Stereo (see audio mux truth table)
5 L Test multiplex control VCOCLK1/Div1000
6 L Test multiplex control VCOCLK2/Div1000
7 L Test multiplex control RESET

Reg 3 IIC → reg

bit

0 L elect source for SCART 2 O/P
1 H Select source for SCART 2 O/P
2 L Select source for SCART 2 O/P
3 L Select OSD effect for SCART 2 (background)
4 L Select OSD effect for SCART 2 (text)
5 L Select OSD "background" level (LSB)
6 L Select OSD "background" level
7 L Select OSD "background" level (MSB)

Reg 4 IIC → reg

bit

0 L elect source for SCART 3 O/P
1 H Select source for SCART 3 O/P
2 L Select source for SCART 3 O/P
3 L Select OSD effect for SCART 3 O/P (background)
4 L Select OSD effect for SCART 3 O/P (text)
5 H Select OSD "text" level (LSB)
6 H Select OSD "text" level
7 H Select OSD "text" level (MSB)

Reg 5 IIC → reg

bit		
0	L	elect source for decoder 1 O/P
1	H	Select source for decoder 1 O/P
2	L	Select source for decoder 1 O/P
3	L	Not used
4	L	Not used
5	H	Select de-emphasis (see audio mux datasheet)
6	L	Select de-emphasis (see audio mux datasheet)
7	?	Not used

Reg 6 IIC → reg

bit		
0	L	elect source for decoder 2 O/P
1	H	Select source for decoder 2 O/P
2	L	Select source for decoder 2 O/P
3	L	Select frequency synth 1 OFF/ON (L=OFF)
4	L	Select frequency synth 2 OFF/ON (L=OFF)
5	H	Select RF source (L=OFF) to FM Det 1
6	L	Select RF source (L=OFF) to FM Det 1
7	L	Select aux audio input for both channels (see audio mux truth table)

Note : These 4 bits must be written to at same time

Reg 7 Reg → IIC

bit	
0	Status of Amp_lock 1
1	Status of Amp_lock 2
2	Not used
3	Not used
4	Not used
5	Not used
6	Not used
7	Not used

Reg 8 IIC → reg

bit		
0	L	Not used
1	L	Not used
2	L	Not used
3	L	Select data direction for I/O 1 (H = output)
4	L	Select data direction for I/O 2 (H = output)
5	L	Not used
6	L	Select frequency for det 1, LSB (bit 0) of 10 bit value
7	H	Select frequency for det 1

Reg 9 IIC → reg

bit		
0	H	Select frequency for det 1, Note : bit 3 of 10 bit value
1	H	Select frequency for det 1
2	H	Select frequency for det 1
3	H	Select frequency for det 1
4	L	Select frequency for det 1
5	H	Select frequency for det 1
6	L	Select frequency for det 1
7	H	Select frequency for det 1 bit 9, MSB (10th bit) of 10 bit value

Reg 10 IIC → reg

bit		
0	L	Select data direction for S1 (L = input state)
1	L	Select data direction for S2 (L = input state)
2	L	Select data direction for S3 (L = input state)
3	L	Text mux contril for LD1 (lock detect channel 1) test only!
4	L	Text mux contril for LD2 (lock detect channel 1) test only!
5	?	Not used
6	L	Select frequency for det 2, LSB (bit 0) of 10 bit value
7	L	Select frequency for det 2

Reg 11 IIC → reg

bit		
0	H	Select frequency for det 2, Note : bit 3 of 10-bit value
1	H	Select frequency for det 2
2	H	Select frequency for det 2
3	H	Select frequency for det 2
4	L	Select frequency for det 2
5	H	Select frequency for det 2
6	L	Select frequency for det 2
7	H	Select frequency for det bit 9, MSB (10th bit) of 10 bit value

Reg 12 IIC → reg (read/write), Note : bits 6, 7 are Read only

bit		
0	L	Select 20kHz or REG12<4> (Pin 10 i/02)
1	L	Not used
2	L	Not used
3	L	Select/Status of I/O 1 (L in = L out)
4	L	Select/Status of I/O 2 (L in = L out)
5	L	Not used
6		Read frequency of watchdog 1, LSB (bit 0) of 10 bit value
7		Read frequency of watchdog 1

Reg 13 Reg → IIC (The watchdog is the vco frequency monitor)

bit	Read frequency of watchdog 1, Note : bit 3 of 10 bit value.
0	Read frequency of watchdog 1
1	Read frequency of watchdog 1
2	Read frequency of watchdog 1
3	Read frequency of watchdog 1
4	Read frequency of watchdog 1
5	Read frequency of watchdog 1
6	Read frequency of watchdog 1
7	Read frequency of watchdog 1 bit 9, MSB (10th bit) of 10 bit

Reg 14 IIC → reg (read/write,) Note : bits 6, 7 are Read only

bit		
0	L	Select/Status of S1
1	L	Select/Status of S2
2	L	Select/Status of S3
3	?	Not used
4	?	Not used
5	?	Not used
6		Read frequ of Watchdog 2, Note : bit 0 of 10 bit value
7		Read frequ of Watchdog 2

Reg 15 Reg → IIC (The watchdog is the vco frequency monitor)

bit	
0	Read frequency of watchdog 2, Note : bit 3 of 10 bit value
1	Read frequency of watchdog 2
2	Read frequency of watchdog 2
3	Read frequency of watchdog 2
4	Read frequency of watchdog 2
5	Read frequency of watchdog 2
6	Read frequency of watchdog 2
7	Read frequency of watchdog 2, MSB (bit 9) of 10 bit value, 0-9

Reg 16 IIC → reg

bit			
0	L	Select 5 bit audio volume control	00H = mute 01H = -32.75dB : : : 1.25dB steps up to 1FH = +6db
1	L	Select 5 bit audio volume control	
2	L	Select 5 bit audio volume control	
3	L	Select 5 bit audio volume control	
4	L	Select 5 bit audio volume control	
5	L	Not used	
6	L	Select 4.000MHz or 8.000MHz clock speed (L = 8MHz)	
7	L	Select ANRS defeat (L = no ANRS, H = ANRS)	

Reg 17 IIC → reg

bit			
0	L	Select LNB voltage. 8 bit value. LSB = bit 0	00H = 0 volts ref FFH = 2.4 volts ref 256 linear steps
1	L	Select LNB voltage. 8 bit value	
2	L	Select LNB voltage. 8 bit value	
3	L	Select LNB voltage. 8 bit value	
4	L	Select LNB voltage. 8 bit value	
5	L	Select LNB voltage. 8 bit value	
6	L	Select LNB voltage. 8 bit value	
7	L	Select LNB voltage. 8 bit value	

Reg 18 IIC → reg (read/write)

bit			
		Not used	
0	L	Select video gain bits	00H = 0dB 01H = +0.202dB 02H = +0.404dB n = +0.202dB x n 3FH = +12.73dB
1	L	Select video gain bits	
2	L	Select video gain bits	
3	L	Select video gain bits	
4	L	Select video gain bits	
5	L	Select video gain bits	
6	L	Sync enable (for noisy video Pin 52 only H = enabled)	
7	?	Not used	

Reg 19 IIC → reg (read/write)

bit		
0	L	Select PLL loop gain bits, default value for 50kHz modulation
1	H	Select PLL loop gain bits
2	H	Select PLL loop gain bits
3	L	Select PLL loop gain bits
4	H	Select PLL loop gain bits
5	L	Not used
6	L	Not used
7	L	Not used

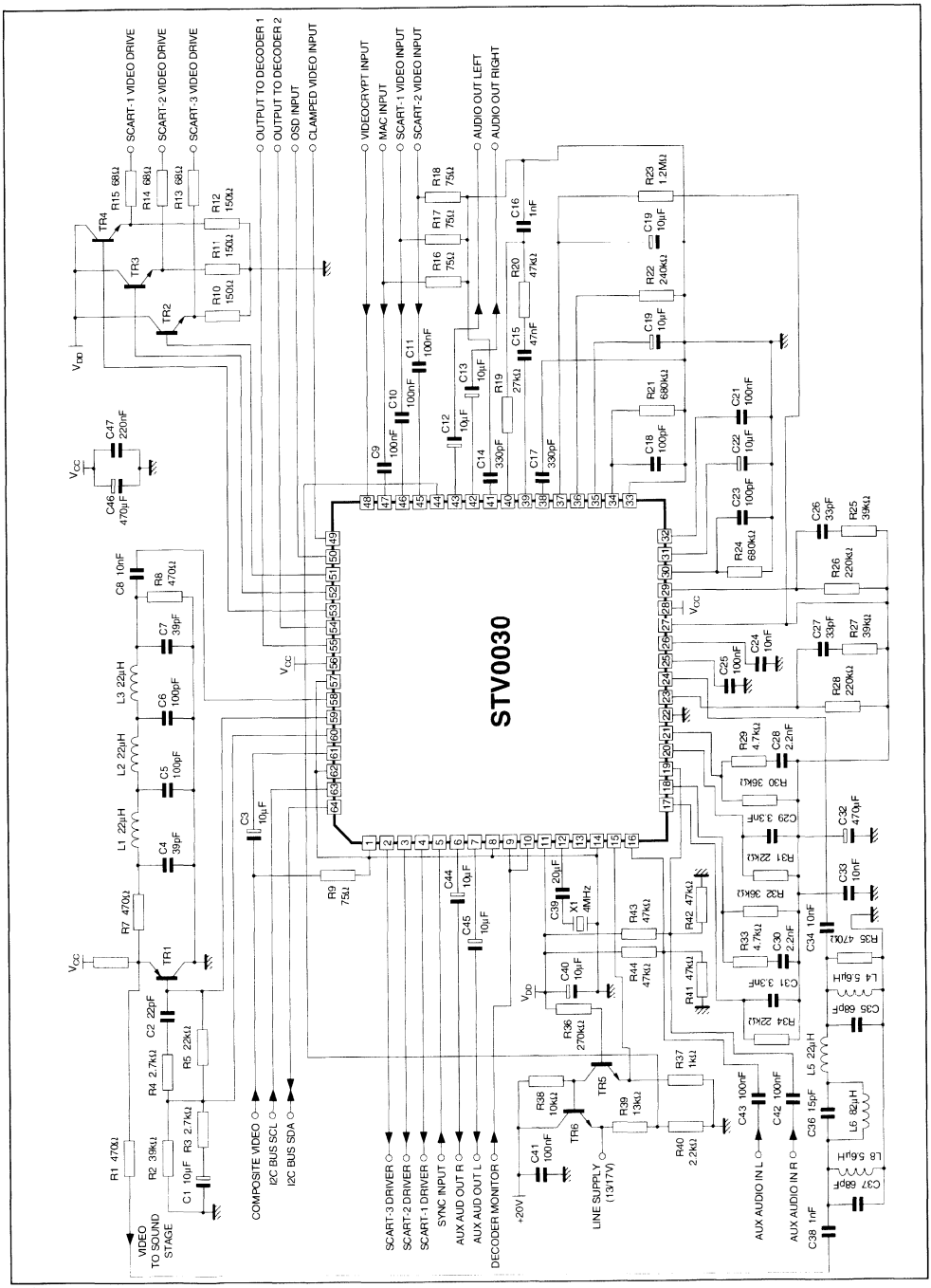
Audio Mux Table

Register	2		5		6	
Bits	4	3	6	5	7	Function Selected
	0	0	X	X	X	mono left / channel 1
	1	0	X	X	X	mono right / channel 2
	1	1	X	X	X	stereo left & right
	X	X	0	0	0	PLL audio 50µs de-emphasis
	X	X	X	0	1	Aux audio - no de-amphasis
	X	X	0	1	X	PLL audio J17 de-emphasis
	X	X	1	0	0	PLL audio 75µs de-emphasis
	X	X	1	1	X	PLL audio no de-emphasis

Register 19 Truth Table for Programmable PLL Gain

4	3	2	1	0	Selected Nominal Carrier Modulation
0	0	0	0	0	cal : do not use = 0.3373V offset on VCO
0	0	0	0	1	cal : do not use = 0.3053V offset on VCO
0	0	0	1	0	cal : do not use = 0.2763V offset on VCO
0	**0**	**0**	**1**	**1**	**calibration setting = 0.25V offset on VCO**
0	0	1	0	0	296kHz modulation
0	0	1	0	1	267kHz modulation
0	0	1	1	0	242kHz
0	0	1	1	1	218kHz
0	1	0	0	0	198kHz
0	1	0	0	1	179kHz
0	1	0	1	0	161kHz
0	1	0	1	1	146kHz
0	1	1	0	0	133kHz
0	1	1	0	1	120kHz
0	1	1	1	0	109kHz
0	1	1	1	1	98.3kHz
1	0	0	0	0	89.7kHz
1	0	0	0	1	80.9kHz
1	0	0	1	0	73.1kHz
1	0	0	1	1	66.0kHz
1	0	1	0	0	60.0kHz
1	0	1	0	1	54.4kHz
1	**0**	**1**	**1**	**0**	**49.1kHz = default power-up state**
1	0	1	1	1	44.3kHz
1	1	0	0	0	39.8kHz
1	1	0	0	1	35.9kHz
1	1	0	1	0	32.4kHz
1	1	0	1	1	29.1kHz
1	1	1	0	0	26.7kHz
1	1	1	0	1	24.3kHz
1	1	1	1	0	21.9kHz
1	1	1	1	1	19.7kHz

APPLICATION CIRCUIT



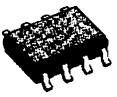
PROTECTION DEVICES

MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY I_{PP} = 40 A 8/20µs
- UP TO 6 UNIDIRECTIONAL TRANSIL FUNCTIONS
- BREAK DOWN VOLTAGE : V_{BR}= 6V1
- LOW CLAMPING FACTOR (V_{CL} / V_{BR}) AT HIGH CURRENT LEVEL
- LOW LEAKAGE CURRENT

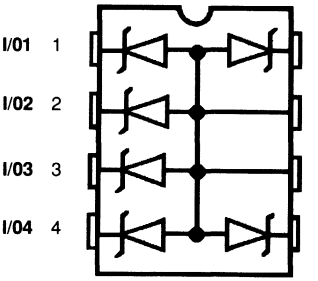


SO8
(Plastic)

DESCRIPTION

This is a specific transil array for RS422, RS485 interface protection developed in monolithic chip form in order to provide a high surge capability and a low clamping voltage.

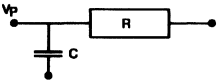
FUNCTIONAL DIAGRAM



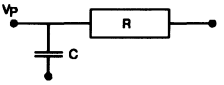
EQUIVALENT TO 6 UNIDIRECTIONAL TRANSILS

IN ACCORDANCE WITH :

- ESD standard :
  - . IEC 801-2 15kV 5ns / 50ns
  - . IEC 801-4 40A 5ns / 50ns
  - . IEC 801-5 1kV 1.2 / 50µs
    25A 8/20µs
  - . MIL STD 883C - Methode 3015-2
    V_P = 25kV
    C = 150pF
    R = 150Ω
    5 s duration



- Human body test :
  V_P = 4kV
  C = 150pF
  R = 150Ω

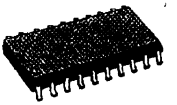


MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY
  I_{PP} = 40 A 8/20µs
- UP TO 8 UNIDIRECTIONAL TRANSIL FUNCTIONS
- BREAKDOWN VOLTAGE= 6V1
- LOW LEAKAGE CURRENT
- LOW CLAMPING FACTOR (V_{CL}/ V_{BR}) AT HIGH CURRENT LEVEL.



SO 20
(Plastic)

DESCRIPTION

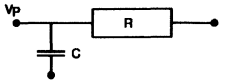
Specially developed for RS 422 , RS 485 interface protection, this monolithic chip component offers a high surge capability and a low clamping voltage.

The internal wire bonding, "4 points connection", ensures a reliable protection against very fast transient overvoltages like ESD.

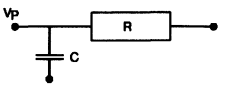
A low clamping voltage is guaranteed, eliminating all spikes due to the perturbation itself and also spikes induced by parasitic inductances created by external wiring.

IN ACCORDANCE WITH :

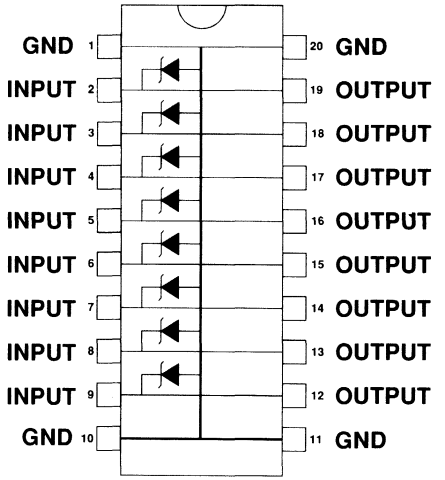
- ESD standard :
  . IEC 801-2 15kV 5ns / 50ns
  . IEC 801-4 40A 5ns / 50ns
  . IEC 801-5 1kV 1.2 / 50µs
  25A 8/20µs
  . MIL STD 883C - Methode 3015-2
  V_P = 25kV
  C = 150pF
  R = 150Ω
  5 s duration



- Human body test :
  V_P = 4kV
  C = 150pF
  R = 150Ω



FUNCTIONAL DIAGRAM



EQUIVALENT TO 8 UNIDIRECTIONAL TRANSILS

SGS-THOMSON MICROELECTRONICS

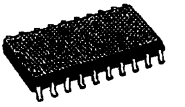
ITA6V1M3

MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY I_{PP} = 40A 8/20µs
- UP TO 18 UNIDIRECTIONAL TRANSIL FUNCTIONS
- BREAKDOWN VOLTAGE = 6V1
- LOW CLAMPING FACTOR (V_{CL}/V_{BR}) AT HIGH CURRENT LEVEL.

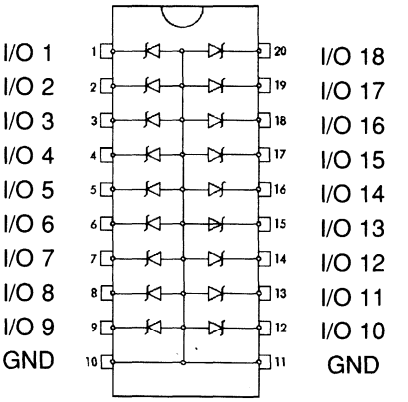


SO 20
(Plastic)

DESCRIPTION

This is a specific Transil Array for Centronics interface protection developed in monolithic chip form in order to provide a high surge capability and a low clamping voltage.

FUNCTIONAL DIAGRAM



EQUIVALENT TO 18 UNIDIRECTIONAL TRANSILS

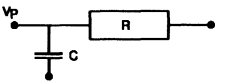
IN ACCORDANCE WITH :

- ESD standard :

. IEC 801-2	15kV	ns / 50ns
. IEC 801-4	40A	5ns / 50ns
. IEC 801-5	1KV	1.2 / 50µs
	25A	8/20µs

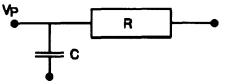
. MIL STD 883C - Methode 3015-2

V_P = 25kV
C = 150pF
R = 150Ω
5 s duration



- Human body test :

V_P = 4kV
C = 150pF
R = 150Ω



ITA6V5B1 / ITA10B1 ITA18B1 / ITA25B1

MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

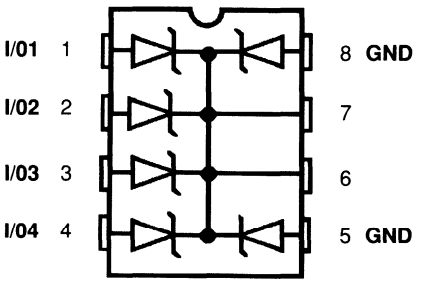
- HIGH SURGE CAPABILITY TRANSIL ARRAY IPP = 40 A 8/20µs
- UP TO 5 BIDIRECTIONAL TRANSIL FUNCTIONS
- BREAK DOWN VOLTAGE AND MAXIMUM DIFFERENTIAL VOLTAGE BETWEEN TWO INPUT PINS :
  ITA6V5 = 6.5 V
  ITA10 = 10 V
  ITA18 = 18 V
  ITA25 = 25 V
- LOW CLAMPING FACTOR (VCL / VBR) AT HIGH CURRENT LEVEL
- LOW LEAKAGE CURRENT
- LOW INPUT CAPACITANCE

SO8
(Plastic)

DESCRIPTION

This is a specific transil array for RS232, RS423 interface protection developed in monolithic chip form in order to provide a high surge capability and a low clamping voltage

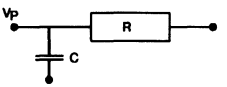
FUNCTIONAL DIAGRAM



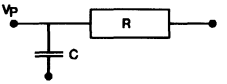
EQUIVALENT TO 4 BIDIRECTIONAL TRANSILS

IN ACCORDANCE WITH :

- ESD standard :
  . IEC 801-2 15kV 5ns / 50ns
  . IEC 801-4 40A 5ns / 50ns
  . IEC 801-5 1kV 1.2 / 50µs
  25A 8 / 20µs
  . MIL STD 883C - Method 3015-2
  V_P = 25kV
  C = 150pF
  R = 150Ω
  5 s duration



- Human body test :
  V_P = 4kV
  C = 150pF
  R = 150Ω



SGS-THOMSON MICROELECTRONICS

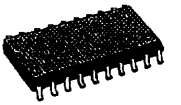
ITA6V5B3 / ITA10B3 ITA18B3 / ITA25B3

MONOLITHIC TRANSIL® ARRAY FOR DATA LINE PROTECTION

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY IPP = 40 A 8/20µs
- UP TO 9 BIDIRECTIONAL TRANSIL FUNCTIONS
- BREAKDOWN VOLTAGE AND MAXIMUM DIFFERENTIAL VOLTAGE BETWEEN TWO INPUT PINS :
  ITA 6V5 = 6,5 V
  ITA10 = 10 V
  ITA18 = 18 V
  ITA25 = 25 V
- AVAILABLE IN SO 20 PACKAGES



SO 20
(Plastic)

DESCRIPTION

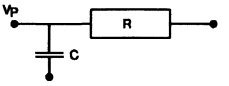
Specially developed for RS 232, RS 423 interface protection, this monolithic chip component offers a high surge capability and a low clamping voltage.

The internal wire bonding, "4 points connection", ensures a reliable protection against very fast transient overvoltages like ESD.

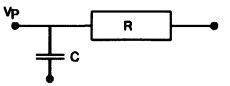
A low clamping voltage is guaranteed,eliminating all spikes due to the perturbation itself and also spikes induced by parasitic inductances created by external wiring.

IN ACCORDANCE WITH :

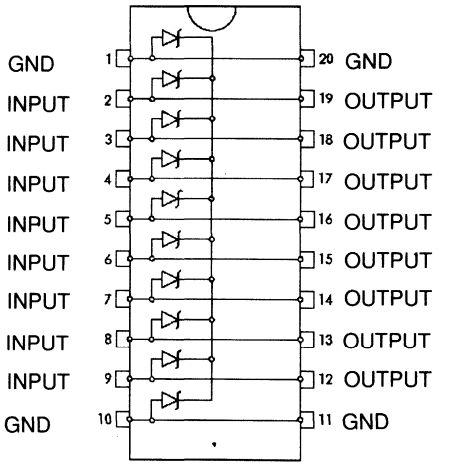
- ESD standard :
  . IEC 801-2 15kV 5ns / 50ns
  . IEC 801-4 40A 5ns / 50ns
  . IEC 801-5 1kV 1.2 / 50µs
  25A 8/20µs
  . MIL STD 883C - Methode 3015-2
  V_P = 25kV
  C = 150pF
  R = 150Ω
  5 s duration



- Human body test :
  V_P = 4kV
  C = 150pF
  R = 150Ω



FUNCTIONAL DIAGRAM



EQUIVALENT TO 8 BIDIRECTIONAL TRANSILS

SGS-THOMSON MICROELECTRONICS

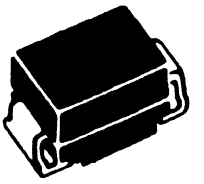
SM4T6V8,A/220,A
SM4T6V8C,CA/220C,CA

TRANSIL

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- PEAK PULSE POWER= 400 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- JEDEC REGISTRED.



SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them praticularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	400	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	50	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

SGS-THOMSON MICROELECTRONICS

SM6T6V8,A/220,A
SM6T6V8C,CA/220C,CA

TRANSIL

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- PEAK PULSE POWER= 600 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).
- JEDEC REGISTRED.

SOD 6
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter		Value	Unit
P_p	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	600	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	5	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	100	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

SGS-THOMSON MICROELECTRONICS

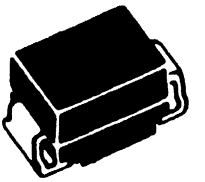
SM15T6V8,A/220,A
SM15T6V8C,CA/220C,CA

TRANSIL

For complete specifications refer to "PROTECTION DEVICES". (Order Code: DBPROTEEST/2)

FEATURES

- PEAK PULSE POWER= 1500 W @ 1ms.
- BREAKDOWN VOLTAGE RANGE : From 6V8 to 220 V.
- UNI AND BIDIRECTIONAL TYPES.
- LOW CLAMPING FACTOR.
- FAST RESPONSE TIME: Tclamping : 1ps (0 V to VBR).



SOD 15
(Plastic)

DESCRIPTION

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous reponse to transients makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

MECHANICAL CHARACTERISTICS

- Body marked with : Logo, Date Code, Type Code, and Cathode Band (for unidirectional types only).
- Full compatibility with both gluing and paste soldering technologies.
- Excellent on board stability.
- Tinned copper leads.
- High temperature resistant resin.

ABSOLUTE RATINGS (limiting values)

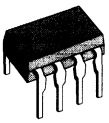
Symbol	Parameter		Value	Unit
P_{pp}	Peak pulse power dissipation See note 1 and derating curve Fig 1.	Tamb = 25°C	1500	W
P	Power dissipation on infinite heatsink See note 1 and derating curve Fig 1.	Tlead = 50°C	10	W
I_{FSM}	Non repetitive surge peak forward current. For unidirectional types.	Tamb = 25°C t =10 ms	250	A
T_{stg} T_j	Storage and junction temperature range		- 65 to + 175 150	°C °C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

STANDARD LINEAR ICs

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW VOLTAGE NOISE : **4.5nV/√Hz**
- HIGH GAIN BANDWIDTH PRODUCT : **15MHz**
- HIGH SLEW RATE : **7V/µs**
- LOW DISTORTION : 0.002%
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2kV



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

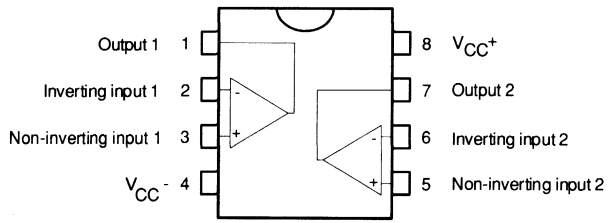
The LM833 is a monolithic dual operational amplifier dedicated to audio applications. The LM833 offers low voltage noise (4.5nV/√Hz) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the LM833 has also a very low distortion (0.002%) and excellent phase/gain margins.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LM833	-40, +105°C	•	•

833-01.TBL

PIN CONNECTIONS (top view)



833-01.EPS

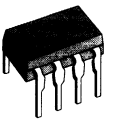
SGS-THOMSON MICROELECTRONICS

MC4558

WIDE BANDWIDTH DUAL BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- INTERNALLY COMPENSATED
- SHORT–CIRCUIT PROTECTION
- GAIN AND PHASE MATCH BETWEEN AMPLIFIERS
- LOW POWER CONSUMPTION
- PIN TO PIN COMPATIBLE WITH MC1458/LM358
- GAIN BANDWIDTH PRODUCT (at 100kHz) 5.5MHz



N
DIP8
(Plastic Package)
J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The MC4558 is a high performance monolithic dual operational amplifier.

The circuit combines all the outstanding features of the MC1458 and, in addition, possesses three times the unity gain bandwidth of the industry standard.

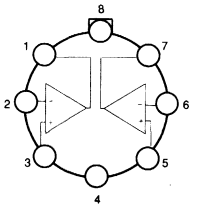
ORDER CODES

Part Number	Temperature Range	Package			
		H	N	J	D
MC4558C	0°C, +70°C	•	•	•	•
MC4558I	-40°C, +105°C	•	•	•	•
Example : MC4558CN					

4558-01.TBL

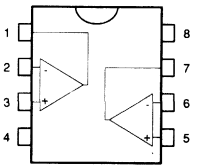
PIN CONNECTIONS (top views)

TO99



4558-01.EPS

DIP8/CERDIP8
SO8



4558-02.EPS

1 – Output 1
2 – Inverting input 1
3 – Non-inverting input 1
4 – V_{CC}^-
5 – Non-inverting input 2
6 – Inverting input 2
7 – Output 2
8 – V_{CC}^+

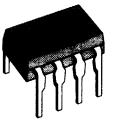
SGS-THOMSON MICROELECTRONICS

MC33078

LOW NOISE DUAL OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW VOLTAGE NOISE : **4.5nV/√Hz**
- HIGH GAIN BANDWIDTH PRODUCT : **15MHz**
- HIGH SLEW RATE : **7V/µs**
- LOW DISTORTION : 0.002%
- LARGE OUTPUT VOLTAGE SWING : +14.3V/-14.6V
- LOW INPUT OFFSET VOLTAGE
- EXCELLENT FREQUENCY STABILITY
- ESD PROTECTION 2kV



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

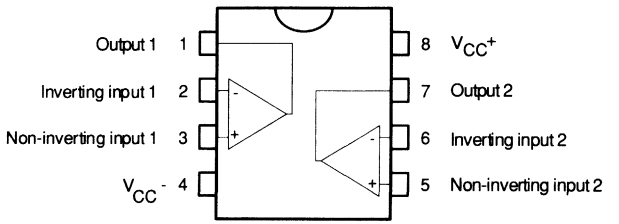
The MC33078 is a monolithic dual operational amplifier dedicated to audio applications. The MC33078 offers low voltage noise (4.5nV/√Hz) and high frequency performances (15MHz gain bandwidth product, 7V/µs slew rate).
In addition the MC33078 has a very low distortion (0.002%) and excellent phase/gain margins.
The output stage allows a large output voltage swing and symmetrical source and sink currents.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33078	-40, +105°C	•	•

33078-01.TBL

PIN CONNECTIONS (top view)



33078-01.EPS

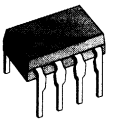
SGS-THOMSON MICROELECTRONICS

MC33171 - MC35171

LOW POWER SINGLE BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD SINGLE OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33171 series are single bipolar operational amplifiers offering both low consumption (200µA) and good speed (2.1MHz, 2V/µs).

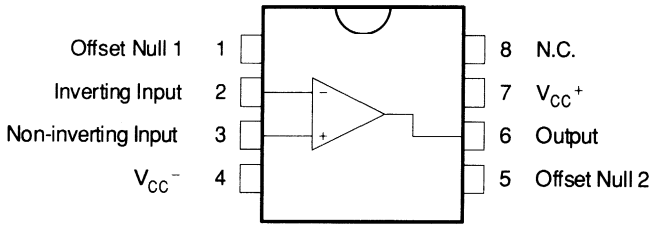
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33171	-40°C, +105°C	•	•
MC35171	-55°C, +125°C	•	•
Example: MC33171N			

33171-01.TBL

PIN CONNECTIONS (top view)



33171-01.EPS

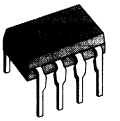
SGS-THOMSON MICROELECTRONICS

MC33172 - MC35172

LOW POWER DUAL BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^- : 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD DUAL OP AMPs



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The MC33172 series are dual bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs).

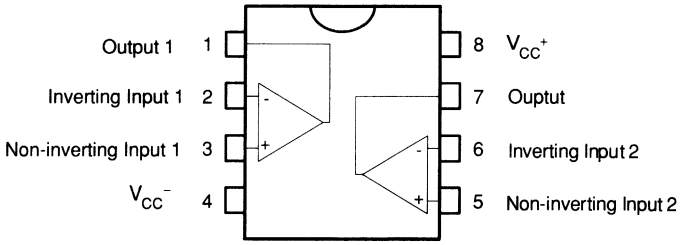
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33172	-40°C, +105°C	•	•
MC35172	-55°C, +125°C	•	•
Example: MC33172N			

33172-01.TBL

PIN CONNECTIONS (top view)



33172-01.EPS

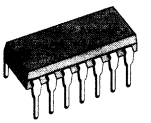
SGS-THOMSON MICROELECTRONICS

MC33174 - MC35174

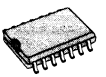
LOW POWER QUAD BIPOLAR OPERATIONAL AMPLIFIERS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- GOOD CONSUMPTION/SPEED RATIO : ONLY 200µA/Amp FOR 2.1MHz, 2V/µs
- SINGLE (OR DUAL) SUPPLY OPERATION FROM +4V TO +44V (±2V TO ±22V)
- WIDE INPUT COMMON MODE VOLTAGE RANGE INCLUDING V_{CC}^-
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO V_{CC}^-: 100mV TYPICAL
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP AMPs
- ESD PROTECTION



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

DESCRIPTION

The MC33174 series are quad bipolar operational amplifiers offering both low consumption (200µA/Amp) and good speed (2.1MHz, 2V/µs).

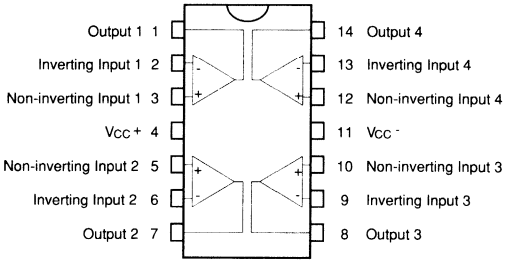
Moreover the Input Common Mode Range extends down to the lower supply rail, allowing single supply operation from +4V to +44V.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
MC33174	-40°C, +105°C	•	•
MC35174	-55°C, +125°C	•	•
Example: MC33174N			

33174-01.TBL

PIN CONNECTIONS (top view)



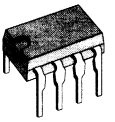
33174-01.EPS

SGS-THOMSON MICROELECTRONICS

TDA2320

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)



N
DIP8
(Plastic Package)

ORDER CODE : TDA2320N

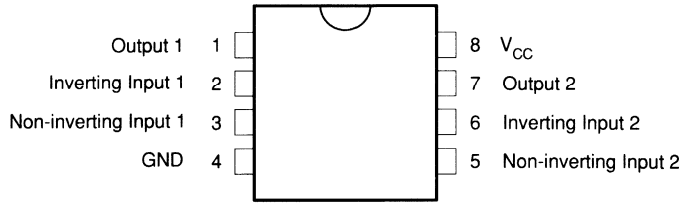
DESCRIPTION

The TDA2320 is a monolithic integrated circuit in Dip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.

The TDA2320 incorporates a two-stage amplkifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709A/M710A/MOS transmitters.

The TDA2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.

PIN CONNECTIONS (top view)



2320-01.EPS

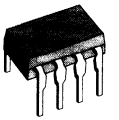
SGS-THOMSON MICROELECTRONICS

TL082
TL082A - TL082B

GENERAL PURPOSE DUAL J-FET OPERATIONAL AMPLIFIERS

For complete specifications refer to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW POWER CONSUMPTION
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

H
TO99
(Metal Can)

DESCRIPTION

The TL082, TL082A and TL082B are high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset current, and low offset voltage temperature coefficient.

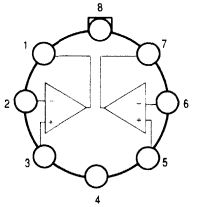
ORDER CODES

Part Number	Temperature	Package		
		H	N	D
TL082M/AM/BM	−55°C, +125°C	•	•	•
TL082I/AI/BI	−40°C, +105°C	•	•	•
TL082C/AC/BC	0°C, +70°C	•	•	•
Examples : TL082CD, TL082IN				

082-01.TBL

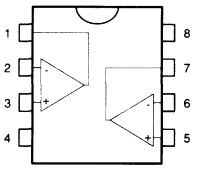
PIN CONNECTIONS (top views)

TO99



082-01.EPS

DIP8/CERDIP8
SO8



082-02.EPS

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

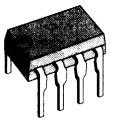
SGS-THOMSON MICROELECTRONICS

TSH150

WIDE BANDWIDTH AND BIPOLAR INPUTS SINGLE OPERATIONAL AMPLIFIER

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 190V/µs
- VERY FAST SETTLING TIME : 20ns (0.1%)



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH150 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

Low noise and low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

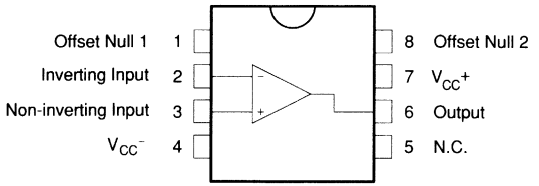
The THS150 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH150C	0°C, 70°C	•	•
TSH150I	-40°C, 105°C	•	•
TSH150M	-55°C, 125°C	•	•

150-01.TBL

PIN CONNECTIONS (top view)



150-01.EPS

This is information on a new product. Details are subject to change without notice.

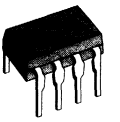
SGS-THOMSON MICROELECTRONICS

TSH151

WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIER

For complete specifications refert to "Industrial Standard Analog ICs Databook". (Order Code: DBSTANDANAST/2)

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 200V/µs
- VERY FAST SETTLING TIME : 70ns (0.1%)
- VERY HIGH INPUT IMPEDANCE



N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH151 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

The TSH151 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

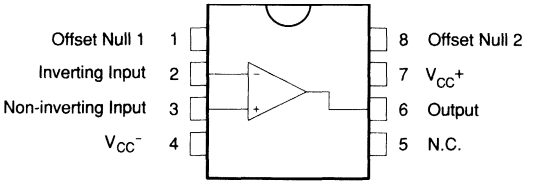
The THS151 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH151C	0°C, 70°C	•	•
TSH151I	-40°C, 105°C	•	•
TSH151M	-55°C, 125°C	•	•

151-01.TBL

PIN CONNECTIONS (top view)



151-01.EPS

This is information on a new product. Details are subject to change without notice.

MEMORIES

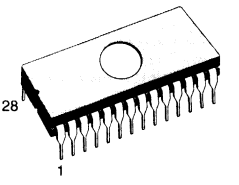
SGS-THOMSON MICROELECTRONICS

M27C64A

CMOS 64K (8K x 8) UV EPROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 150ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.5V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- HIGH SPEED PROGRAMMING (less than 1 minute)



FDIP28W (F)

DESCRIPTION

The M27C64A is a high speed 65,536 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 8,192 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram

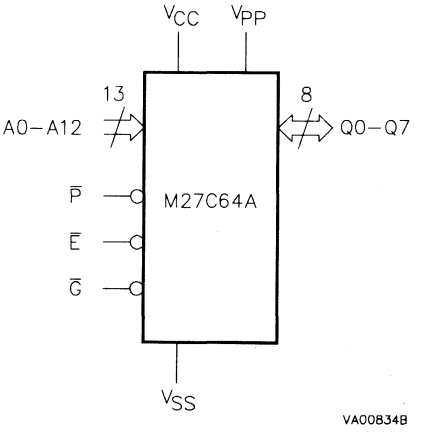


Table 1. Signal Names

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

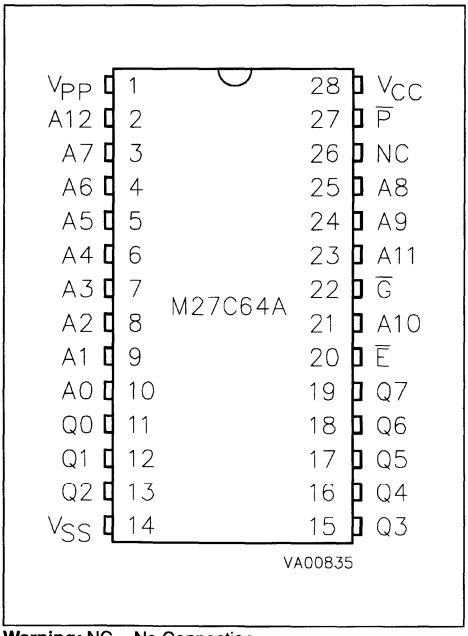
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2. DIP Pin Connections



Warning: NC = No Connection

DEVICE OPERATION

The modes of operation of the M27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C64A has a standby mode which reduces the active current from 30mA to 100µA. The M27C64A is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

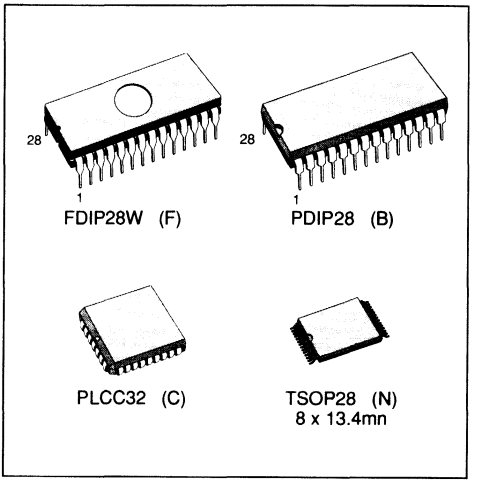
SGS-THOMSON MICROELECTRONICS

M27C256B

CMOS 256K (32K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 70ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C256B is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems. It is organized as 32,768 by 8 bits.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C256B is offered in Plastic Dual-in-Line, Plastic Leaded Chip Carrier, and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

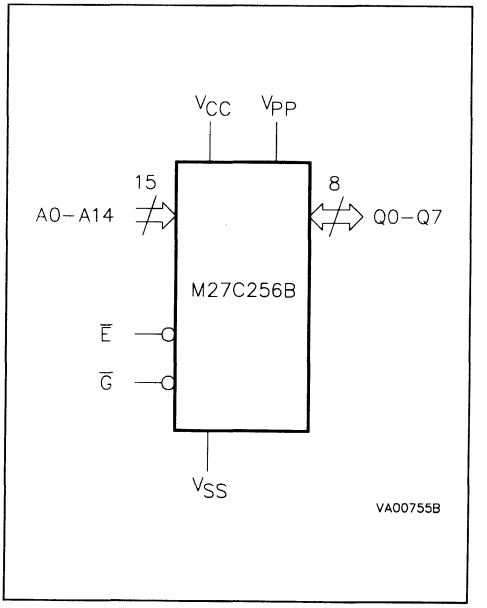


Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

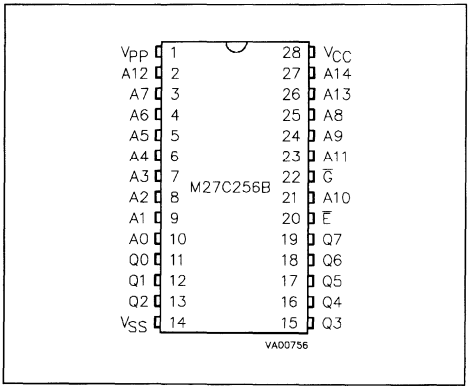
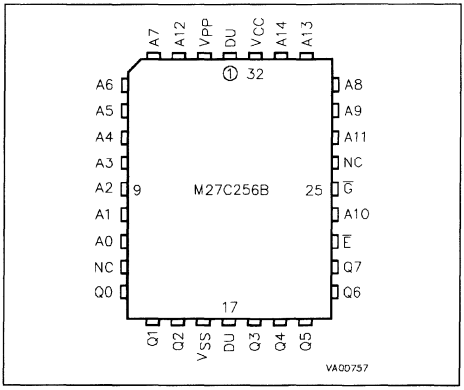
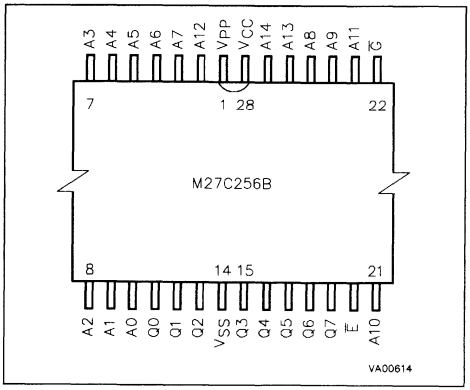


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

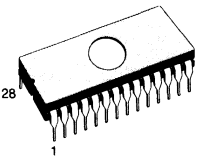
SGS-THOMSON MICROELECTRONICS

M87C257

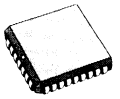
ADDRESS LATCHED CMOS 256K (32K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- INTEGRATED ADDRESS LATCH
- VERY FAST ACCESS TIME: 100ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 3sec. (PRESTO II ALGORITHM)



FDIP28W (F)



PLCC32 (C)

DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically programmable memory EPROM. The M87C257 incorporates latches for all address inputs to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M87C257 is offered in Plastic Leaded Chip Carrier, package.

Figure 1. Logic Diagram

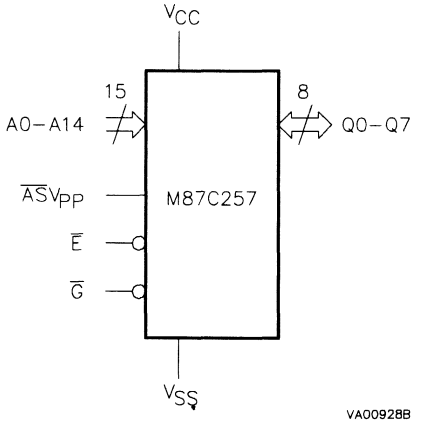


Table 1. Signal Names

A0 - A14	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{AS}V_{PP}$	Address Strobe / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

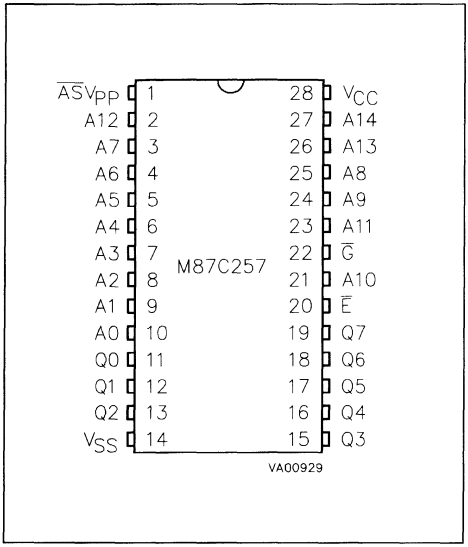
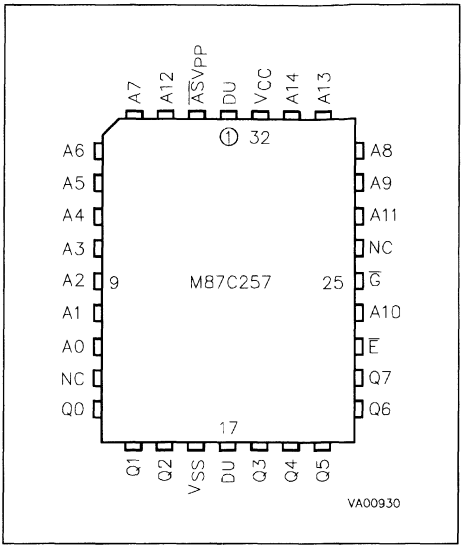


Figure 2C. LCC Pin Connections



Warning: NC = No Connection, DU = Dont't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M87C257 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable ($\overline{AS}$ = V_{IH}) or latched ($\overline{AS}$ = V_{IL}), the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

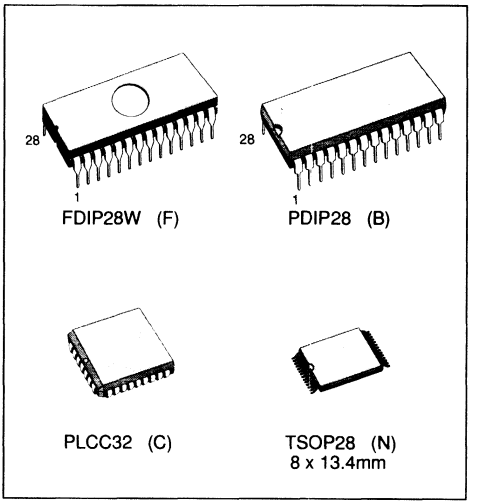
SGS-THOMSON MICROELECTRONICS

M27C512

CMOS 512K (64K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 60ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)



DESCRIPTION

The M27C512 is a high speed 524,288 bit UV erasable and electrically programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 65,536 by 8 bits.

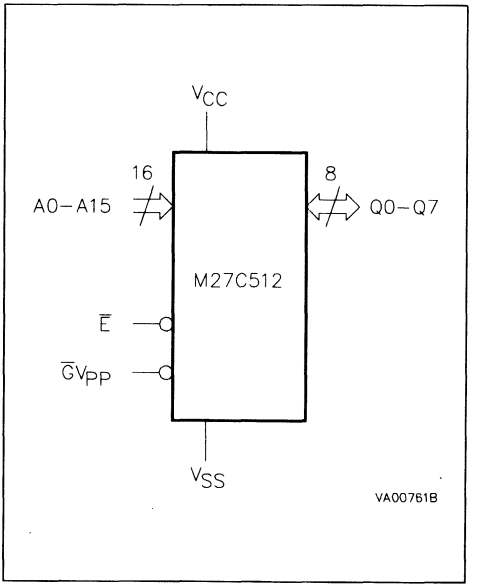
The 28 pin Window Ceramic Frit-Seal Dual-in-Line package has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C512 is offered in Plastic Dual-in-Line, Plastic Thin Small Outline and Plastic Leaded Chip Carrier packages.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2A. DIP Pin Connections

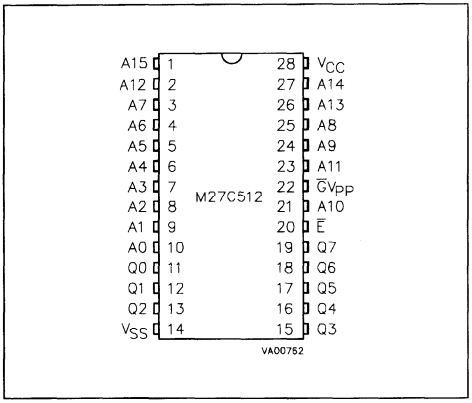
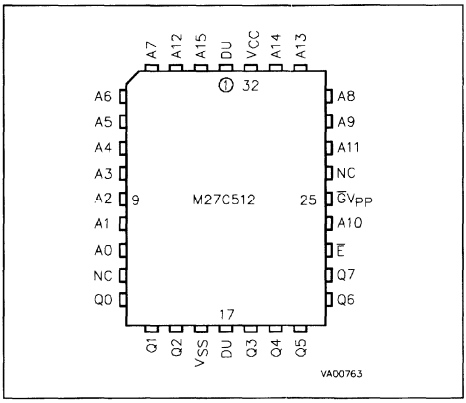
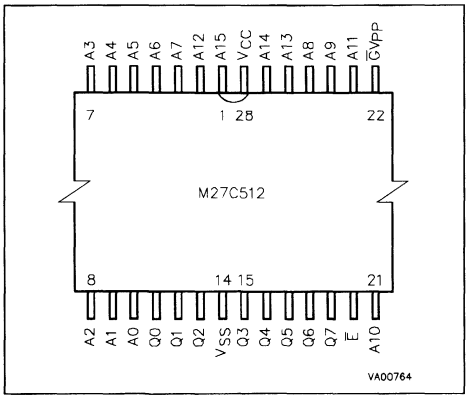


Figure 2B. LCC Pin Connections



Warning: NC = No Connection, DU = Don't Use

Figure 2C. TSOP Pin Connections



DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

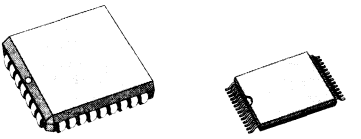
Read Mode

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection.

LOW VOLTAGE CMOS 512K (64K x 8) OTP ROM

ABBREVIATED DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 10mA
  - Standby Current 10µA
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 6sec. (PRESTO IIB ALGORITHM)
- M27V512 is PROGRAMMABLE as M27C512 with IDENTICAL SIGNATURE



PLCC32 (K)

TSOP28 (N)
8 x 13.4mm

DESCRIPTION

The M27V512 is a low voltage, low power 512K One Time Programmable ROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements. Its is organized as 524,288 by 8 bits.

The M27V512 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges. The M27V512 can also be operated as a standard 512 EPROM (similar to M27C512) with a 5V power supply .

For equipment requiring a surface monted, low profile package, theM27V512 is offered in Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

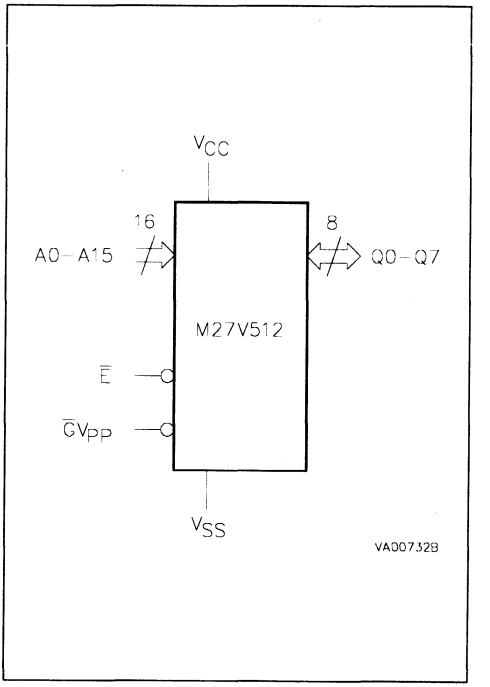


Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. LCC Pin Connections

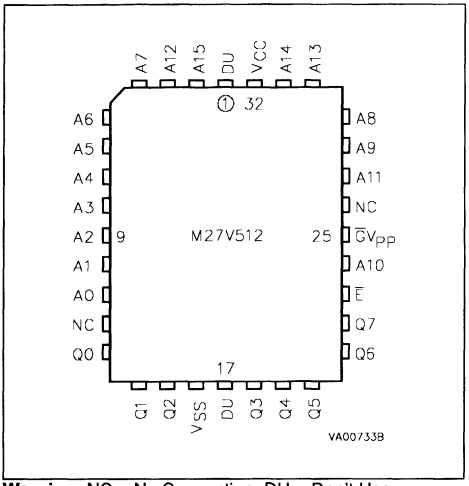
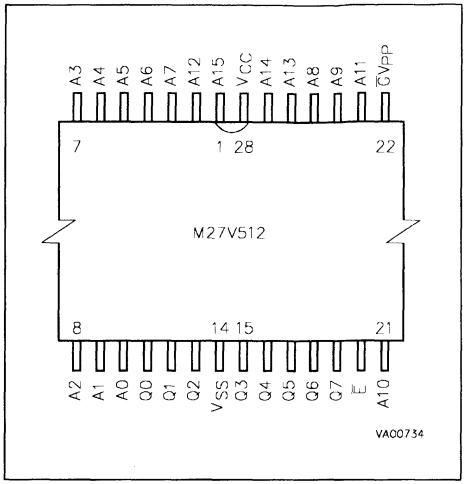


Figure 2B. TSOP Pin Connections



Warning: NC = No Connection, DU = Don't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27V512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

Read Mode

The M27V512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

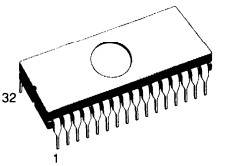
SGS-THOMSON MICROELECTRONICS

M27C1001

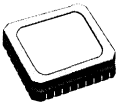
CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

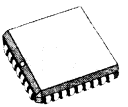
- VERY FAST ACCESS TIME: 60ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)



FDIP32W (F)



LCCC32W (L)



PLCC32 (C)

TSOP32 (N)
8 x 20mm

DESCRIPTION

The M27C1001 is a high speed 1 Megabit UV erasable and electrically programmable memory EPROM ideally suited for microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

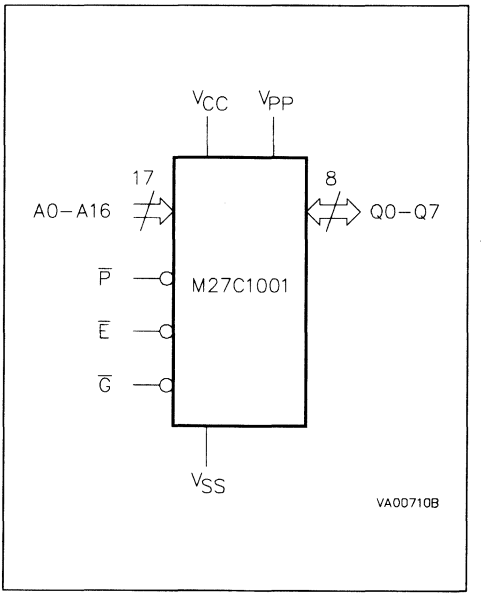
The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C1001 is offered in both Plastic Dual-in-Line, Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Table 1. Signal Names

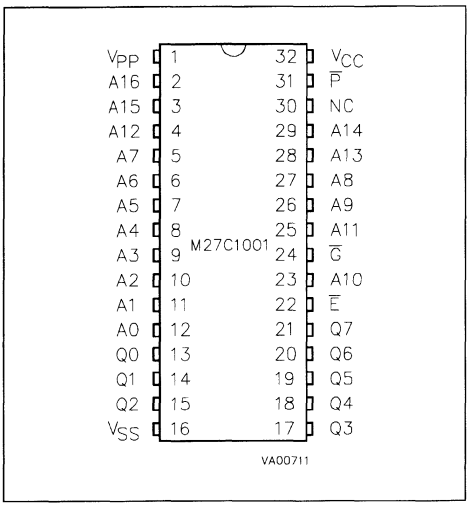
A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



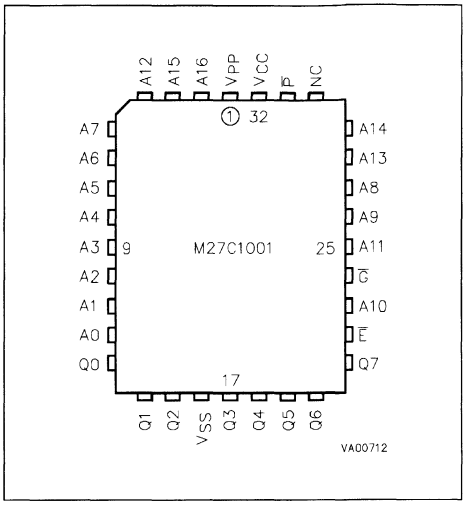
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



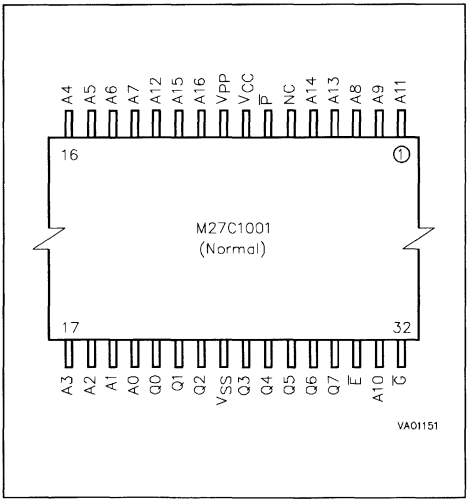
Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Read Mode

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C1001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

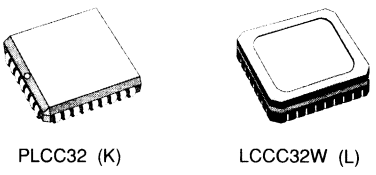
SGS-THOMSON MICROELECTRONICS

M27V101

LOW VOLTAGE CMOS 1 Megabit (128K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 120, 150 and 200ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 12sec. (PRESTO II ALGORITHM)
- M27V101 is PROGRAMMABLE as M27C1001 with IDENTICAL SIGNATURE



PLCC32 (K)

LCCC32W (L)

TSOP32 (N)
8 x 20mm

DESCRIPTION

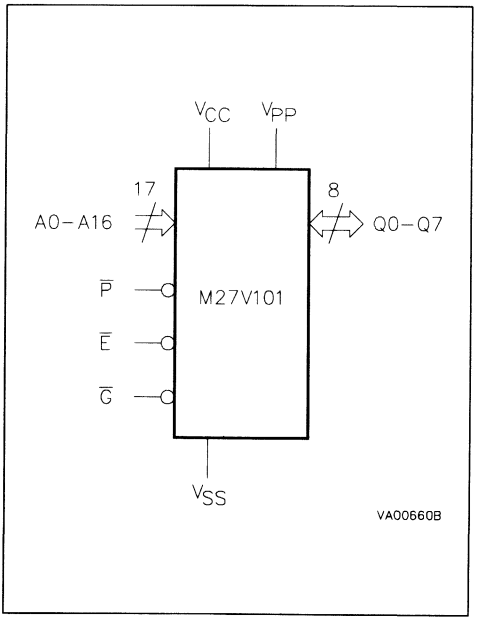
The M27V101 is a low voltage, low power 1 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 131,072 by 8 bits.

The M27V101 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

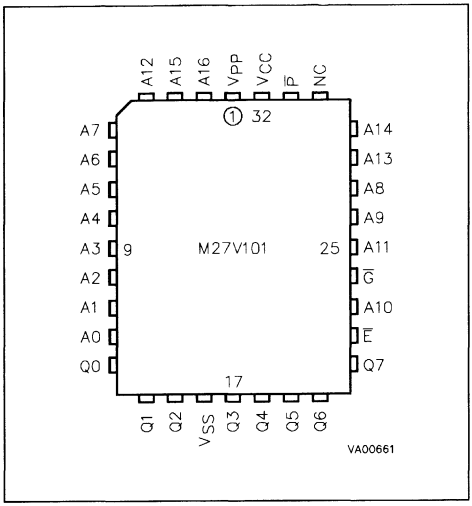
A0 - A16	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



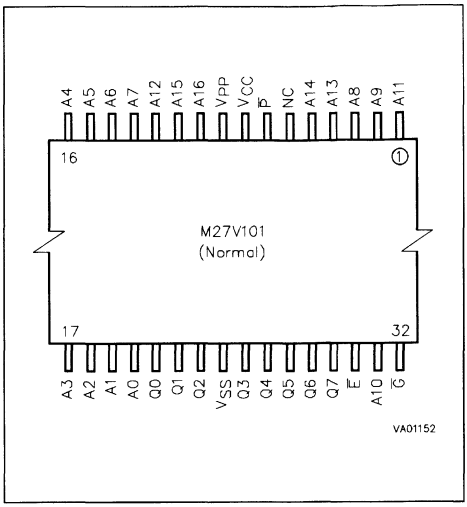
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. LCC Pin Connections



Warning: NC = No Connection.

Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

The M27V101 can also . , operated as a standard 1 Megabit EPROM (similar to M27C1001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V101 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

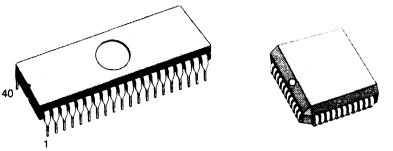
SGS-THOMSON MICROELECTRONICS

M27C1024

CMOS 1Megabit (64K x16) UV EPROM and OTP ROM

ABBREVIATED DATA

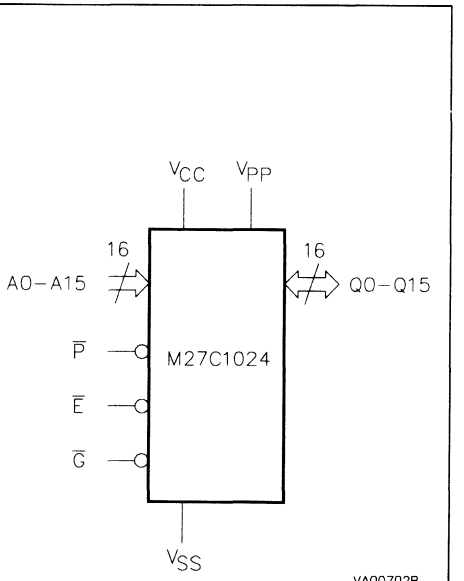
- FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 35mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIME of AROUND 6 sec. (PRESTO II ALGORITHM)



FDIP40W (F)

PLCC44 (C)

Figure 1. Logic Diagram



DESCRIPTION

The M27C1024 is a 1 Megabit UV erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits.

The 40 pin Ceramic Frit Seal Window package has a transparent lid whide allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

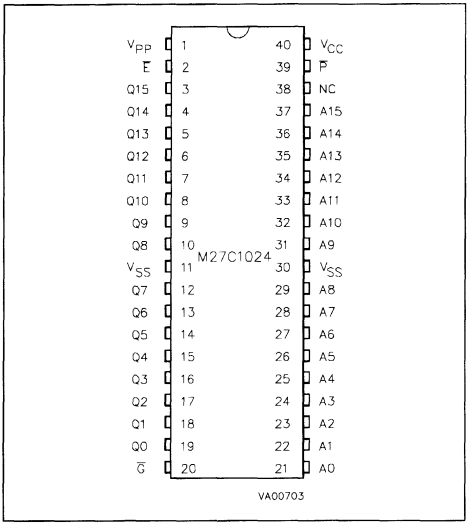
For application where the content is programmed only one time and erasure is not required, the M27C1024 is offered in a Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A15	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

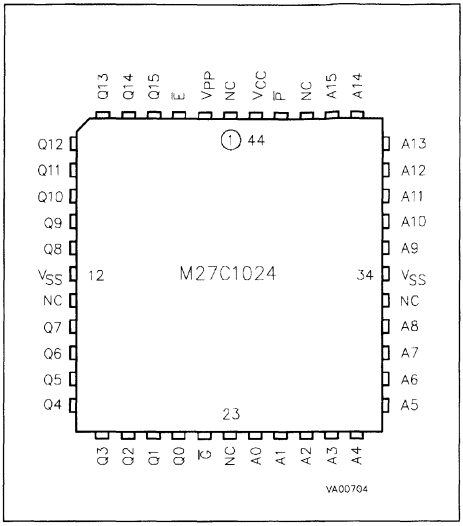
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection.

Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

Read Mode

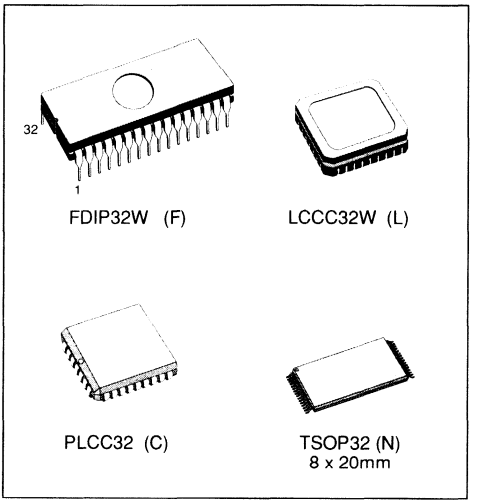
The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}).

Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

CMOS 2 Megabit (256K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C2001 is a high speed 2 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

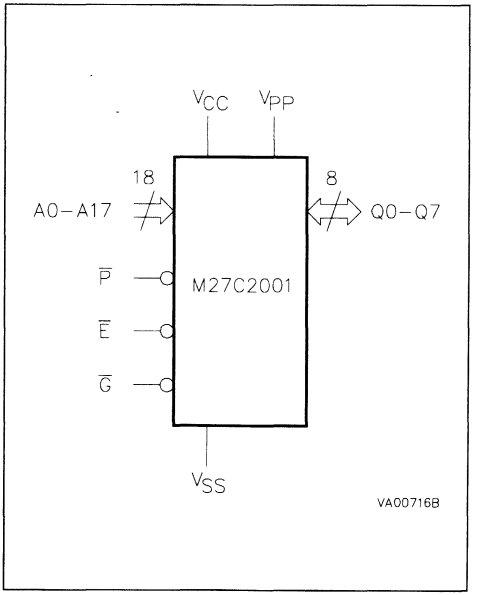


Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

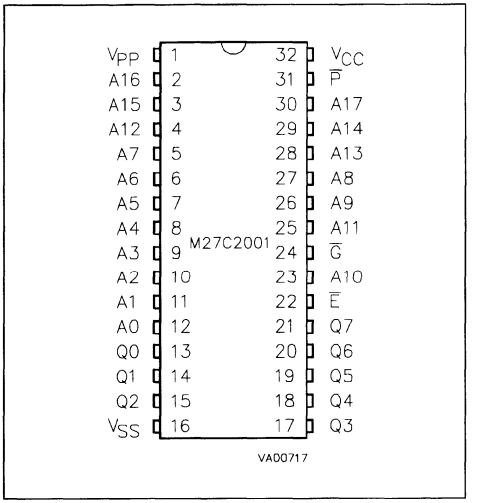


Figure 2B. LCC Pin Connections

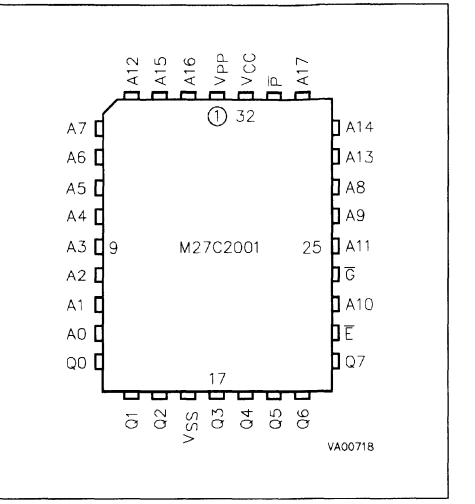
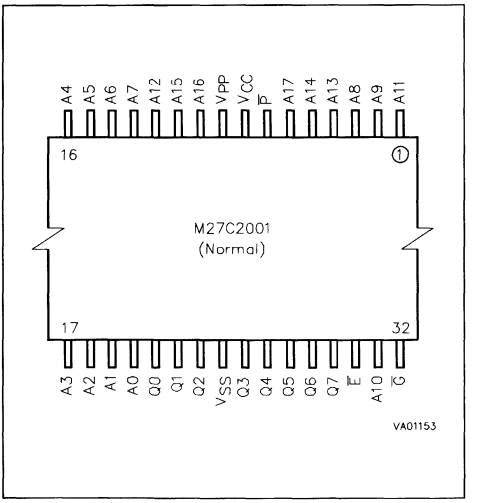


Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

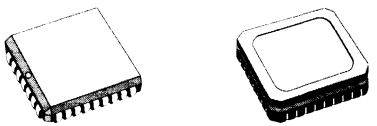
SGS-THOMSON MICROELECTRONICS

M27V201

LOW VOLTAGE CMOS 2 Megabit (256K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)
- M27V201 is PROGRAMMABLE as M27C2001 with IDENTICAL SIGNATURE



PLCC32 (K) LCCC32W (L)

TSOP32 (N)
8 x 20mm

DESCRIPTION

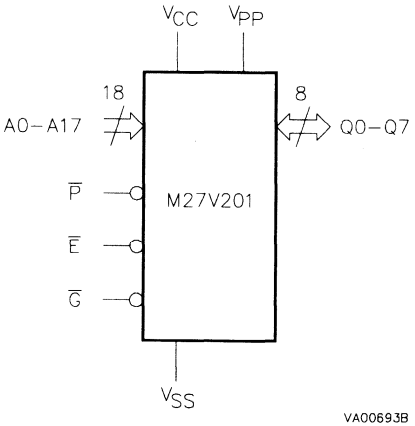
The M27V201 is a low voltage, low power 2 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 262,144 by 8 bits.

The M27V201 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{P}$	Program
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. LCC Pin Connections

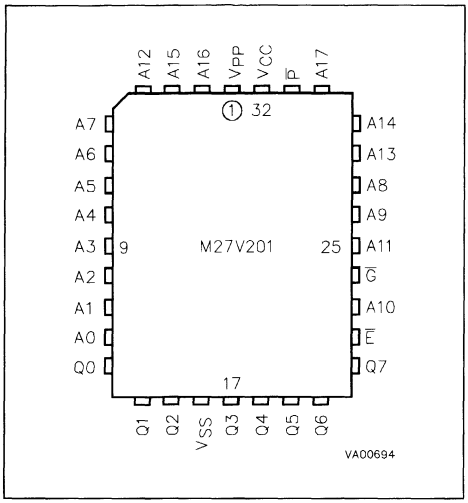
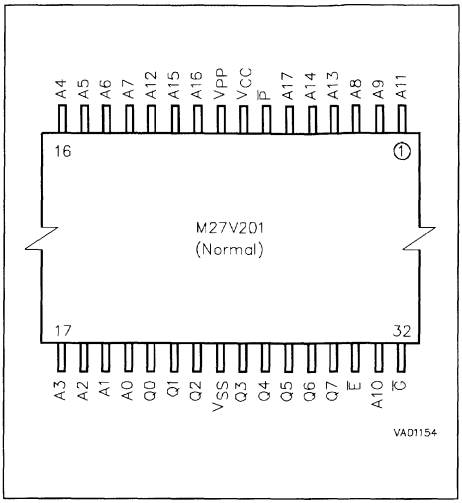


Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

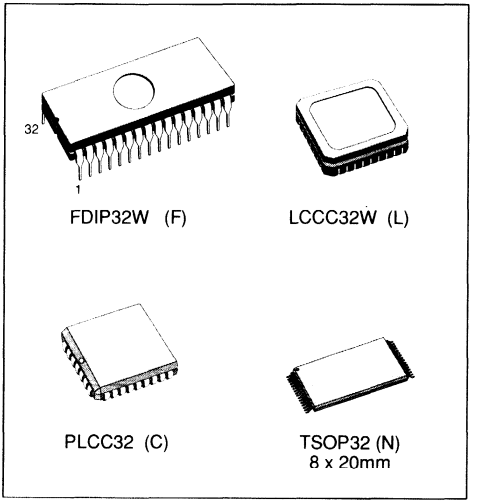
The M27V201 can also be operated as a standard 2 Megabit EPROM (similar to M27C2001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V201 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

CMOS 4 Megabit (512K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 30mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4001 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 524,288 by 8 bits.

The 32 pin Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

Figure 1. Logic Diagram

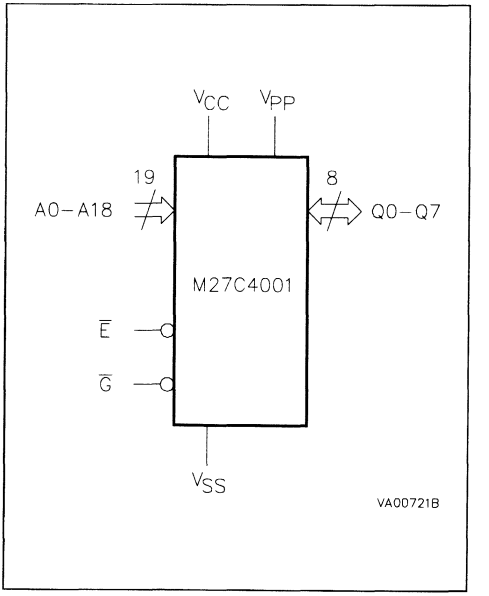


Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

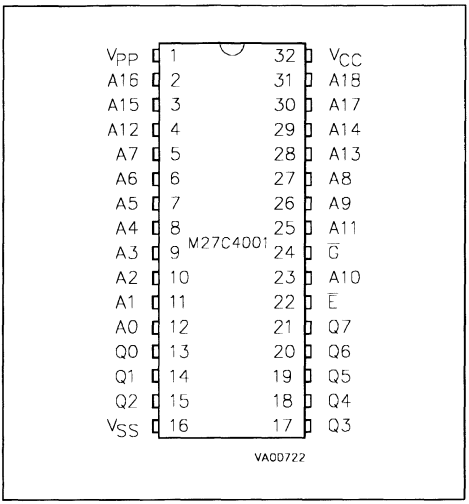


Figure 2B. LCC Pin Connections

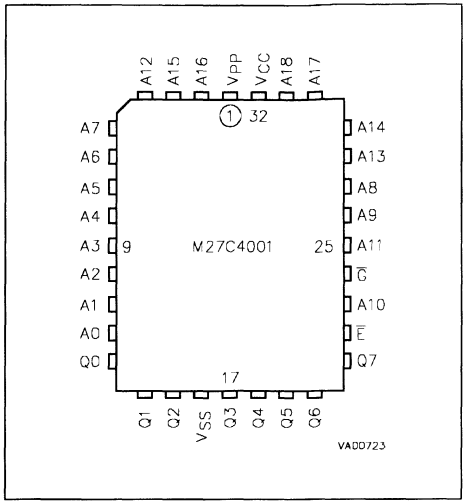
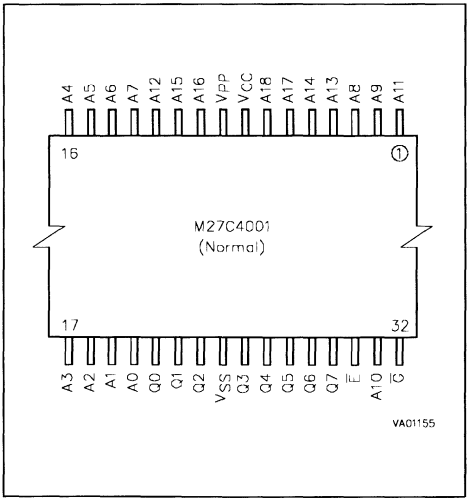


Figure 2C. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C4001 has a standby mode which reduces the active current from 50mA to 100µA. The M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

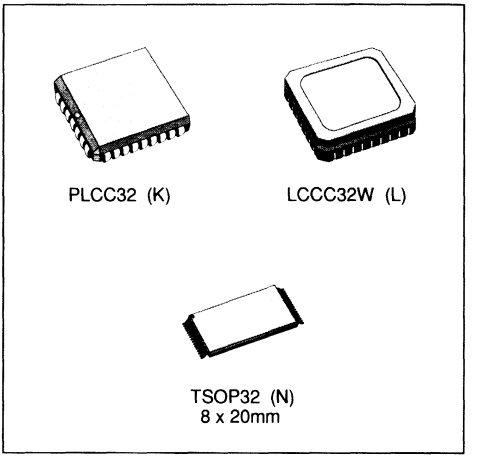
SGS-THOMSON MICROELECTRONICS

M27V401

LOW VOLTAGE CMOS 4 Megabit (512K x 8) UV EPROM and OTP ROM

ABBREVIATED DATA

- LOW VOLTAGE READ OPERATION
  - V_{CC} Range: 3V to 5.5V (T_A = 0 to 70°C)
  - V_{CC} Range: 3.2V to 5.5V (T_A = –40 to 85°C)
- ACCESS TIME: 200 and 250ns
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 15mA
  - Standby Current 20µA
- SMALL PACKAGES for SURFACE MOUNTING:
  - Ceramic: LCCC32W, ultra-thin 2.8mm (max) height
  - Plastic: PLCC32 and TSOP32
- PROGRAMMING VOLTAGE: 12.75V
- PROGRAMMING TIMES of AROUND 48sec. (PRESTO II ALGORITHM)
- M27V401 is PROGRAMMABLE as M27C4001 with IDENTICAL SIGNATURE



DESCRIPTION

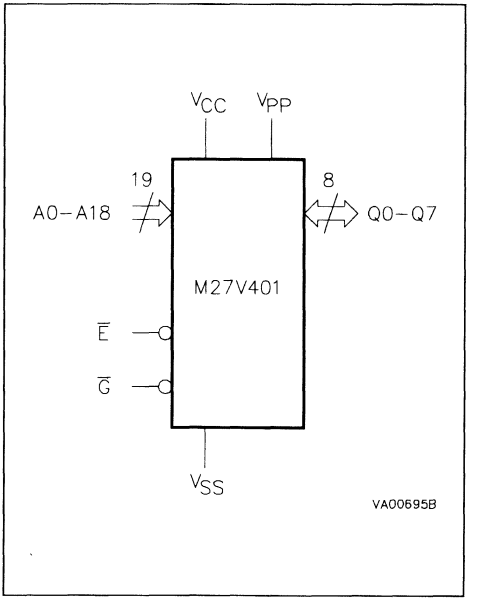
The M27V401 is a low voltage, low power 4 Megabit electrically programmable memory (EPROM), ideally suited for handheld and portable microprocessor systems requiring large programs. It is organized as 524,288 by 8 bits.

The M27V401 operates in the read mode with a supply voltage as low as 3V (3.2V between –40 to 85°C). The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

Table 1. Signal Names

A0 - A18	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. LCC Pin Connections

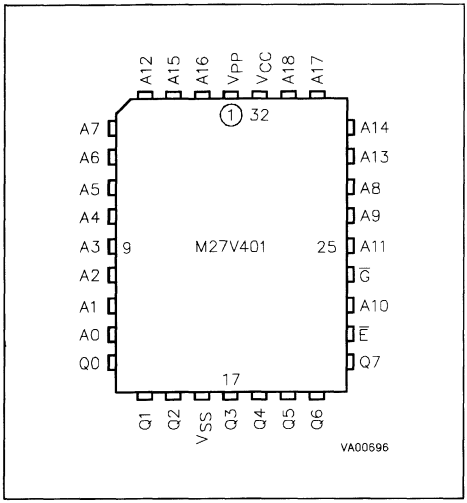
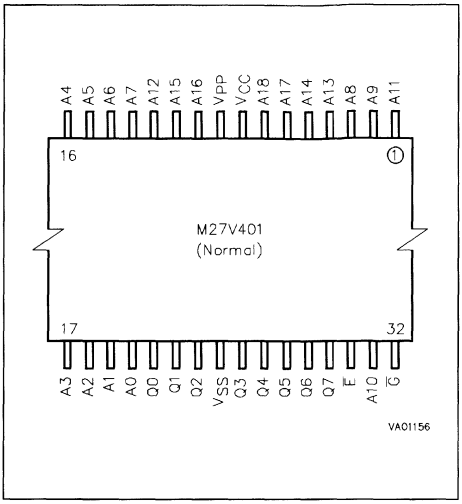


Figure 2B. TSOP Pin Connections



Note: This is advance information on a new product now in development. Details are subject to change without notice.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DESCRIPTION (cont'd)

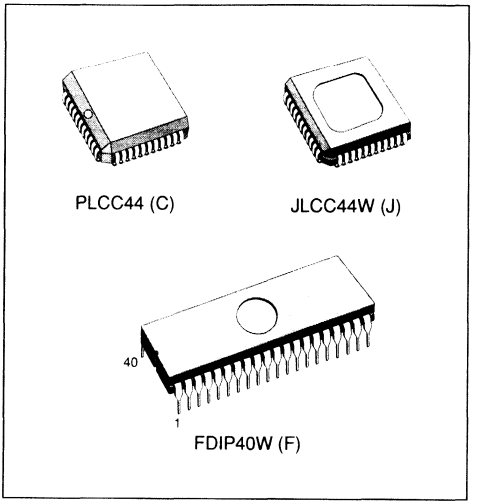
The M27V401 can also be operated as a standard 4 Megabit EPROM (similar to M27C4001) with a 5V power supply .

The 32 pin Window, Leadless Chip Carrier package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure. For applications where the content is programmed only one time and erasure is not required, the M27V401 is offered in both Plastic Leaded Chip Carrier and Plastic thin Small Outline packages.

CMOS 4 Megabit (256K x 16) UV EPROM and OTP ROM

ABBREVIATED DATA

- VERY FAST ACCESS TIME: 80ns
- COMPATIBLE with HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE
- LOW POWER "CMOS" CONSUMPTION:
  - Active Current 50mA at 5MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE: 12.75V
- ELECTRONIC SIGNATURE for AUTOMATED PROGRAMMING
- PROGRAMMING TIMES of AROUND 24sec. (PRESTO II ALGORITHM)



DESCRIPTION

The M27C4002 is a high speed 4 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large programs. It is organised as 262,144 by 16 bits.

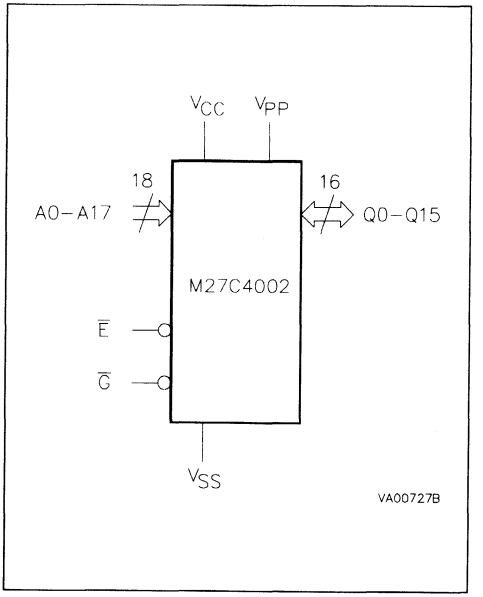
The Window Ceramic Frit-Seal Dual-in-Line and J-Lead Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C4002 is offered in Plastic Leaded Chip Carrier package.

Table 1. Signal Names

A0 - A17	Address Inputs
Q0 - Q15	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

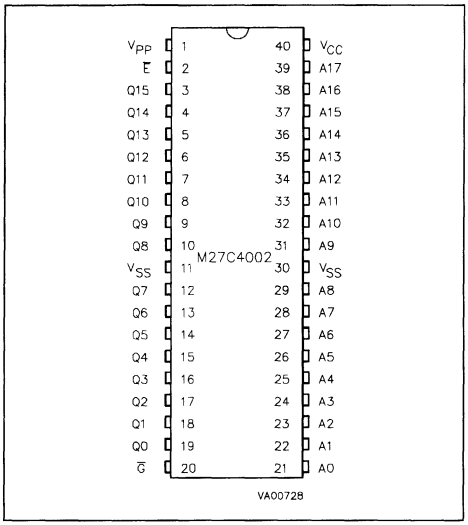
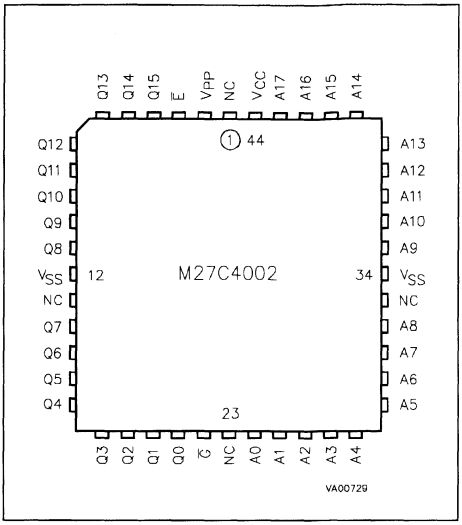


Figure 2B. LCC Pin Connections



Warning: NC = No Connection.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

DEVICE OPERATION

The modes of operations of the M27C4002 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C4002 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

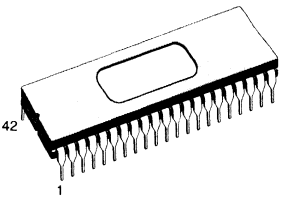
SGS-THOMSON MICROELECTRONICS

M27C160

CMOS 16 Megabit (2M x 8 or 1M x 16) UV EPROM

ABBREVIATED DATA

- FAST ACCESS TIME: 150ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit, 42 Pin, MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
  - Active Current 70mA at 8MHz
  - Standby Current 100µA
- PROGRAMMING VOLTAGE 12.5V ± 0.3V
- PROGRAMMING TIME of AROUND 10sec. (PRESTO III ALGORITHM)



FDIP42W (F)

DESCRIPTION

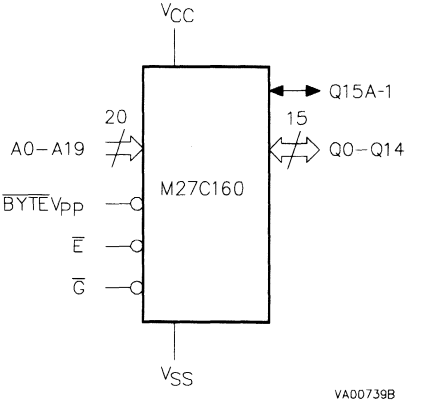
The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2M words of 8 bit or 1M words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

Table 1. Signal Names

A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{BYTE}V_{PP}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

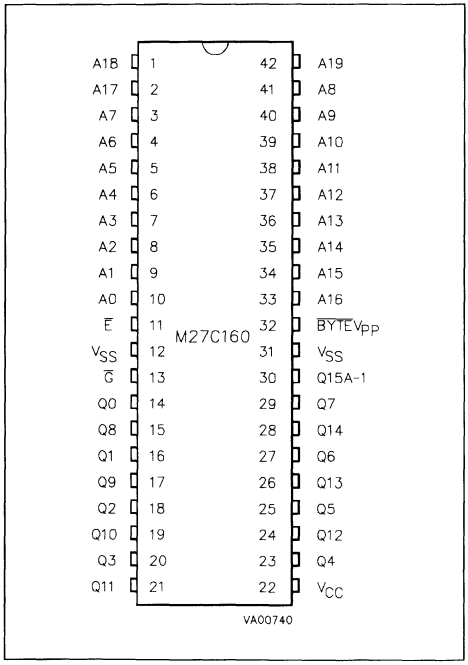
Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (2)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the $\overline{BYTE}V_{PP}$ pin. When $\overline{BYTE}V_{PP}$ is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the $\overline{BYTE}V_{PP}$ pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected. The $\overline{E}$ signal is the power control and should be used for device selection. The $\overline{G}$ signal is the output control and should be used to gate data to the output pins. With $\overline{E}=V_{IL}$ and $\overline{G}=V_{IL}$ the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable. The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and $\overline{E}=V_{IL}$, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} –0.2V to $\overline{E}$. When in the standby mode the outputs are in an high impedance state, independant of the $\overline{G}$ input level.

SGS-THOMSON MICROELECTRONICS

M28F256

CMOS 256K (32K x 8, Chip Erase) FLASH MEMORY

ABBREVIATED DATA

- FAST ACCESS TIME: 120ns
- 1,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 100µs (PRESTO F PROGRAMMING)
- ELECTRICAL CHIP ERASE IN 1s RANGE

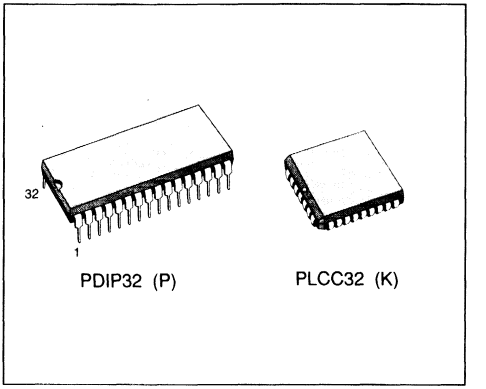
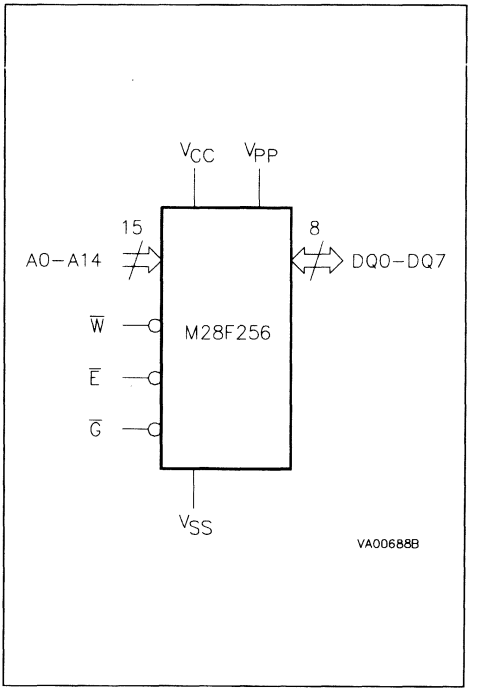


Figure 1. Logic Diagram



DESCRIPTION

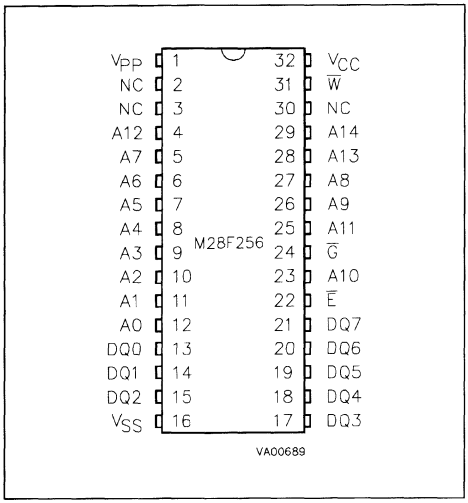
The M28F256 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

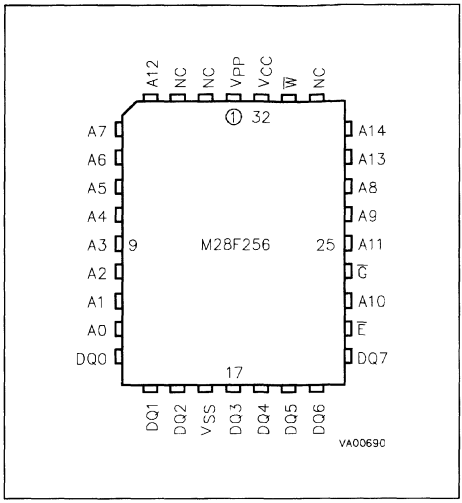
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F256 FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

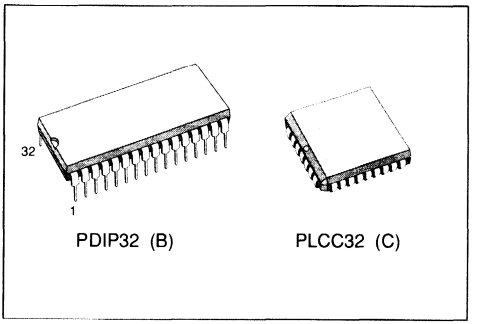
SGS-THOMSON MICROELECTRONICS

M28F256A

CMOS 256K (32K x 8, Chip Erase) FLASH MEMORY

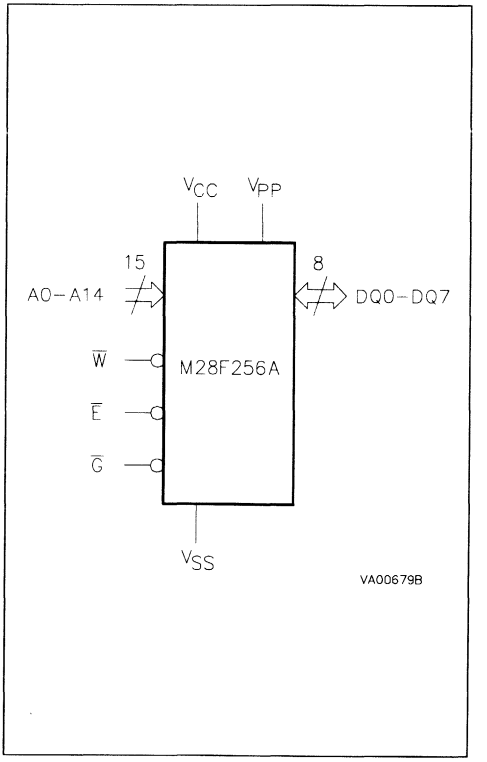
ABBREVIATED DATA

- FAST ACCESS TIME: 120ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (B) PLCC32 (C)

Figure 1. Logic Diagram



DESCRIPTION

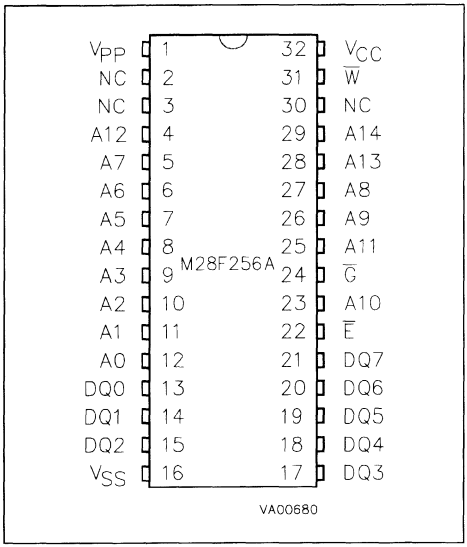
The M28F256A FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 32K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F256A FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

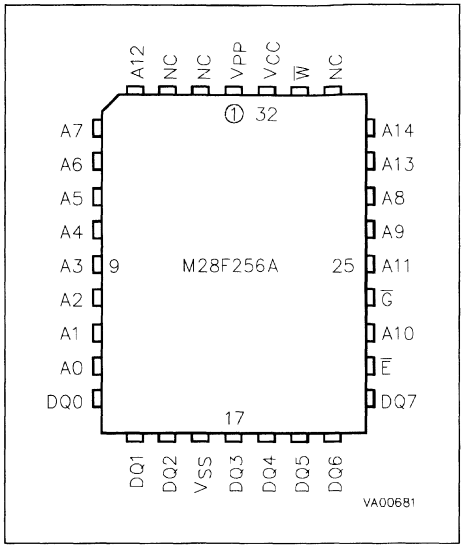
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

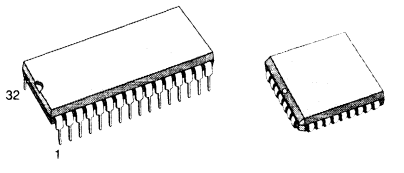
DEVICE OPERATION

The M28F256A FLASH MEMORY employs a technology similar to a 256K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F256A functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

CMOS 512K (64K x 8, Chip Erase) FLASH MEMORY

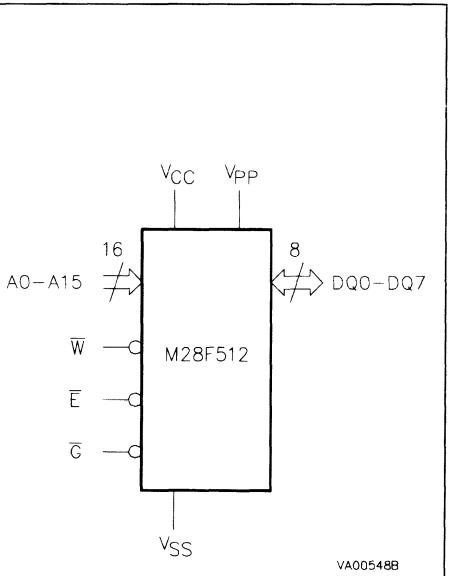
ABBREVIATED DATA

- FAST ACCESS TIME: 120ns
- LOW POWER CONSUMPTION
  - Standby Current: 200µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE IN 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (B) PLCC32 (C)

Figure 1. Logic Diagram



DESCRIPTION

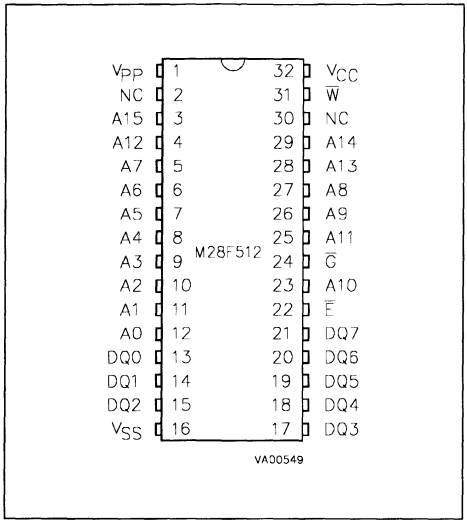
The M28F512 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 64K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F512 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

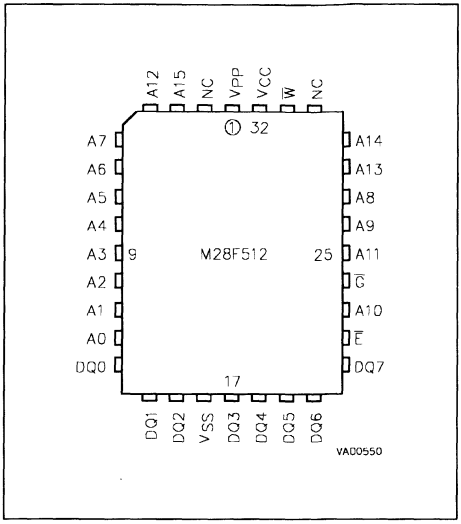
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F512 FLASH MEMORY employs a technology similar to a 512K EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F512 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command register is enabled and this provides, in addition, Erase and Program operations.

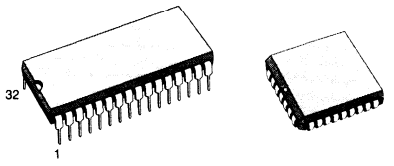
SGS-THOMSON MICROELECTRONICS

M28F101

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

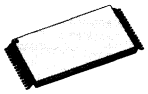
ABBREVIATED DATA

- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (P)

PLCC32 (K)



TSOP32 (N)
8 x 20 mm

DESCRIPTION

The M28F101 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed byte-by-byte. It is organised as 128K bytes of 8 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F101 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Figure 1. Logic Diagram

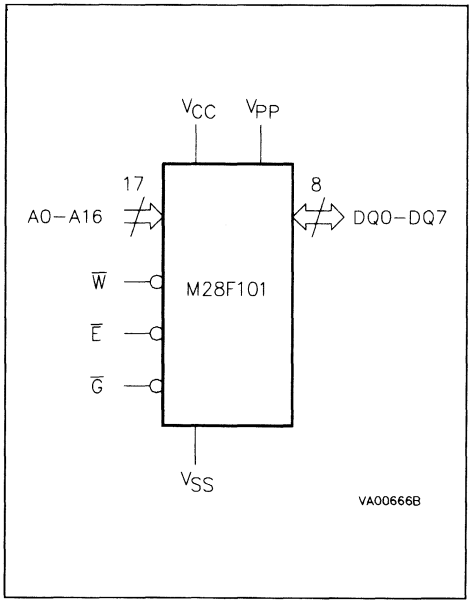
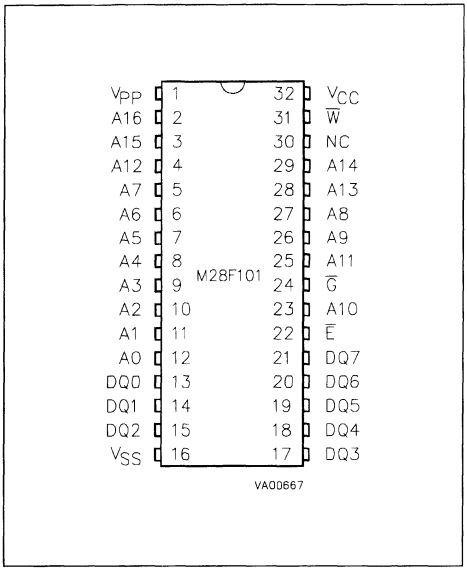


Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

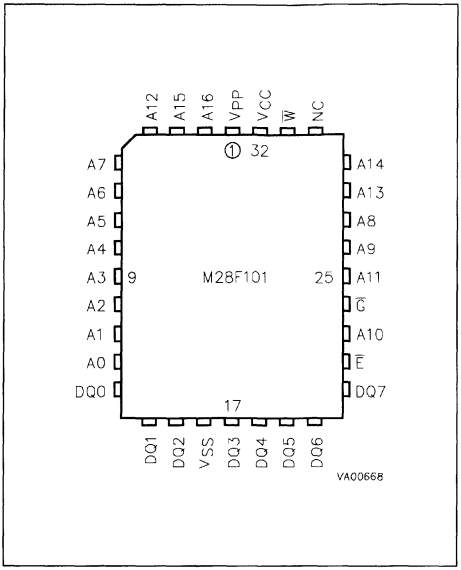
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



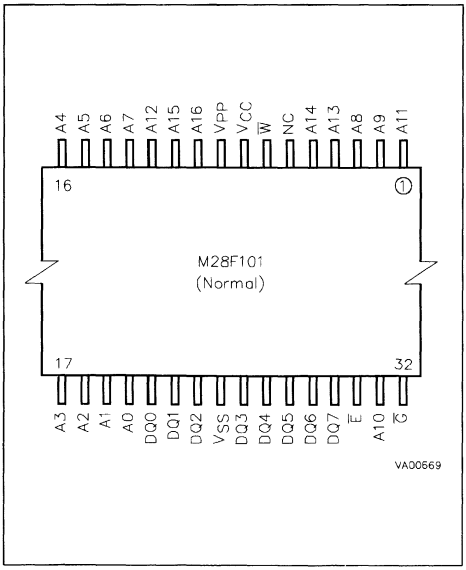
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



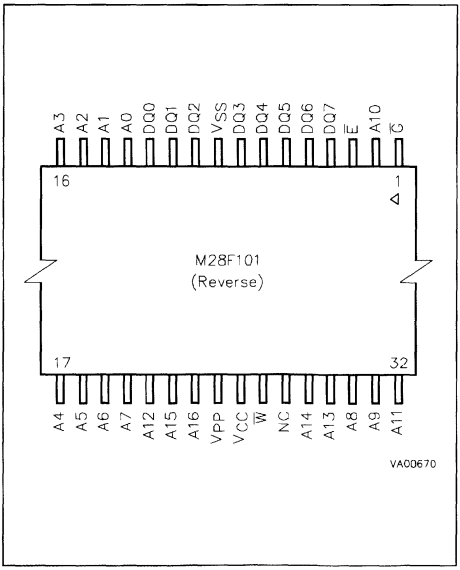
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

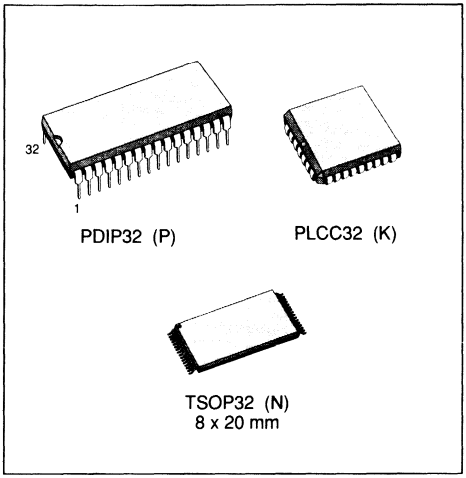
SGS-THOMSON MICROELECTRONICS

M28F101A
M28V101A

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

ABBREVIATED DATA

- MEMORY CHIP ERASE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F101A version
  - 3.3V ± 0.3V for M28V101A version
- 12V PROGRAMMING VOLTAGE
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F101A
  - 10,000 for M28V101A
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E. C. Status
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
- FAST ACCESS TIMES
  - 60ns for M28F101A version
  - 150ns for M28V101A version



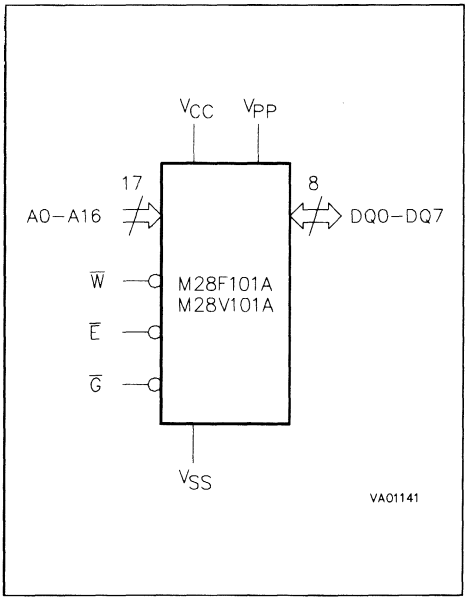
DESCRIPTION

The M28F101A, M28V101A FLASH MEMORY products are non-volatile memories that may be erased electrically in bulk and programmed byte-by-byte. The interface is directly compatible with most microprocessors. The device is available in PDIP32, PLCC32 and TSOP32 (8 x 20mm). Both normal and reverse pin outs are available for the TSOP32 package.

Table 1. Signal Names

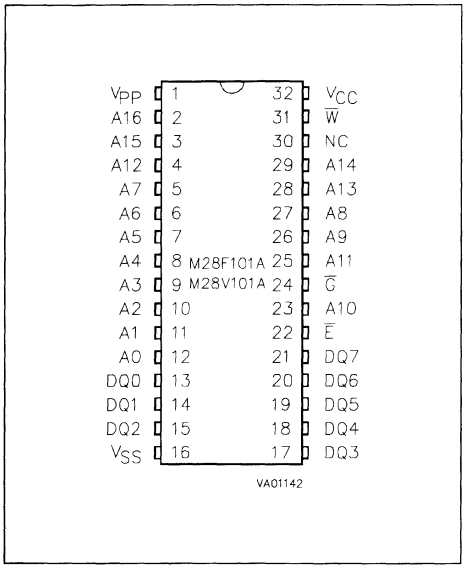
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



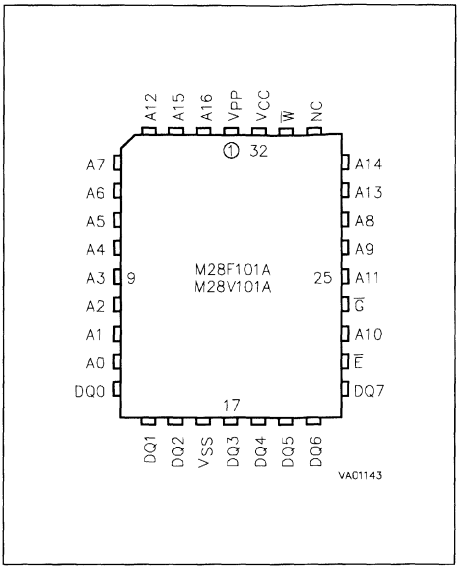
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



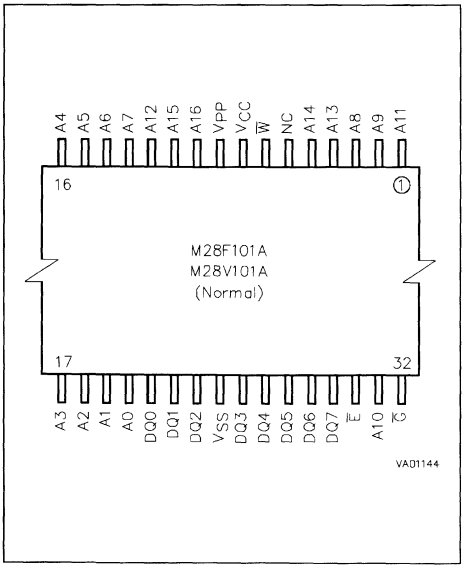
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



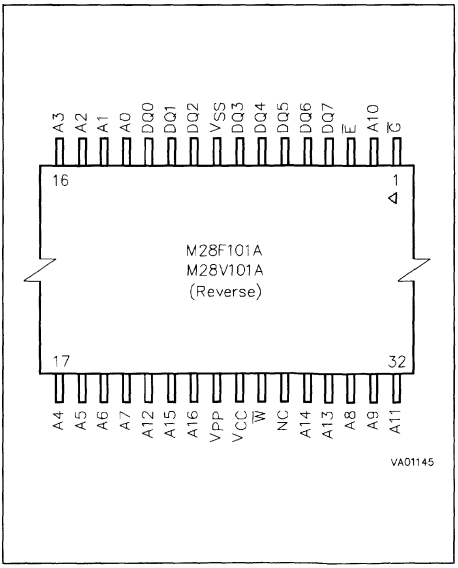
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

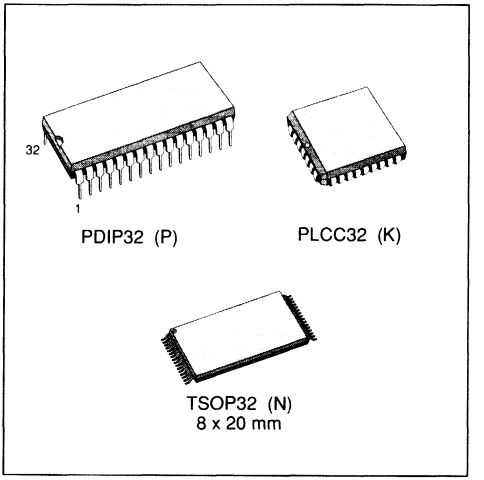
SGS-THOMSON MICROELECTRONICS

M28F101B
M28V101B

CMOS 1 Megabit (128K x 8, Chip Erase) FLASH MEMORY

ABBREVIATED DATA

- FAST ACCESS TIMES
  - 60ns for M28F101B version
  - 150ns for M28V101B version
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 PROGRAM/ERASE CYCLES
- 12V PROGRAMMING VOLTAGE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F101B version
  - 3.3V ± 0.3V for M28V101B version
- TYPICAL BYTE PROGRAMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



DESCRIPTION

The M28F101B, M28V101B FLASH MEMORY products are non-volatile memories which may be erased electrically at the chip level and programmed byte-by-byte. They are organised as 128K bytes of 8 bits. They use a command register architecture to select the operating modes and thus provide a simple microprocessor interface. The M28F101B, M28V101B FLASH MEMORY products are suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 60ns makes the device suitable for use in high speed microprocessor systems, while the low supply voltage capability makes it ideal for portable applications.

Figure 1. Logic Diagram

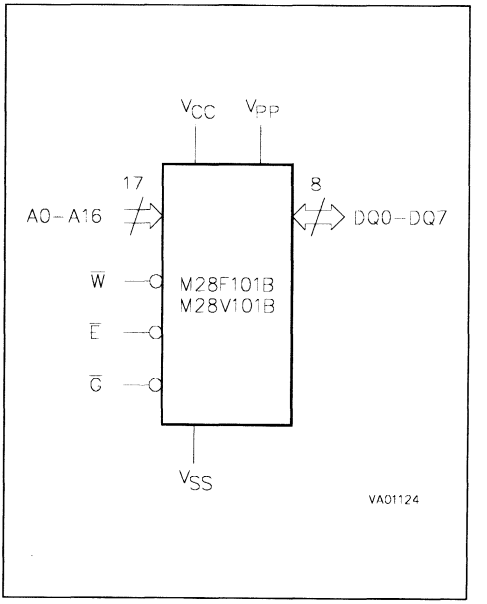
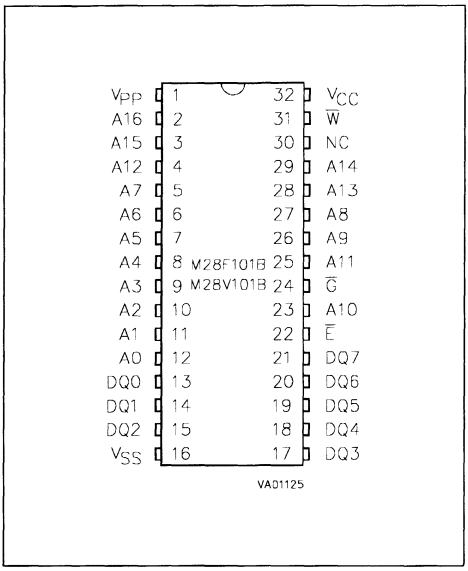


Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

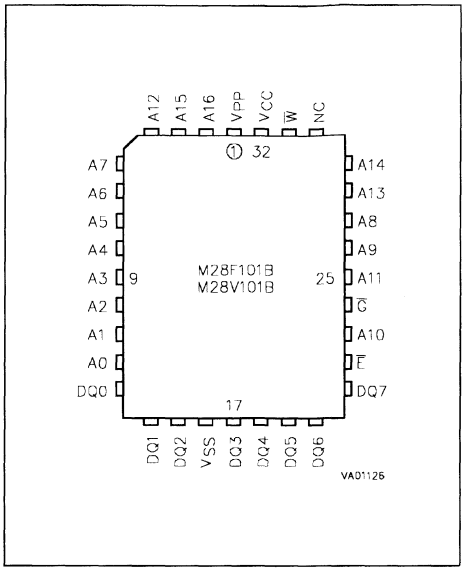
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



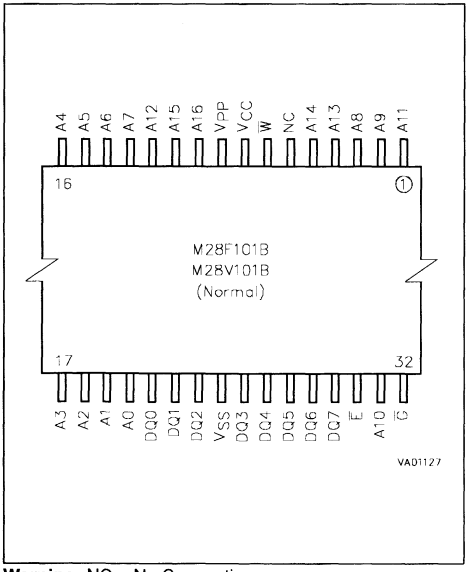
Warning: NC = No Connection

Figure 2B. LCC Pin Connections



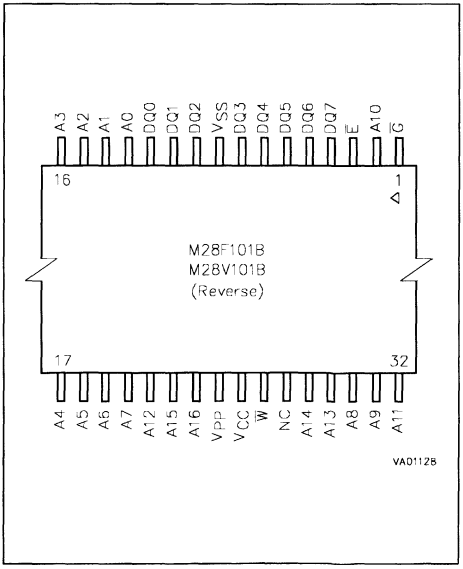
Warning: NC = No Connection

Figure 2C. TSOP Pin Connections



Warning: NC = No Connection

Figure 2D. TSOP Reverse Pin Connections



Warning: NC = No Connection

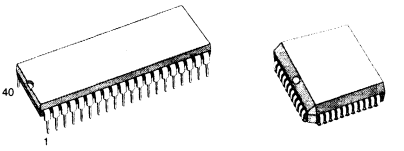
SGS-THOMSON MICROELECTRONICS

M28F102

CMOS 1 Megabit (64K x 16, Chip Erase) FLASH MEMORY

ABBREVIATED DATA

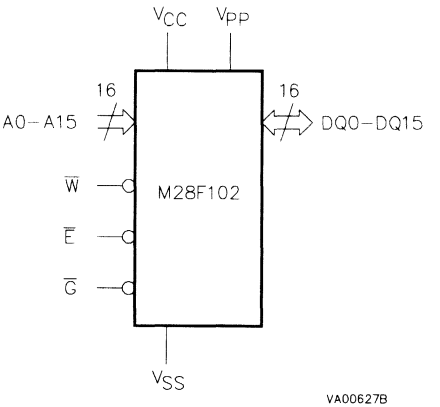
- FAST ACCESS TIME: 100ns
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 ERASE/PROGRAM CYCLES
- 12V PROGRAMMING VOLTAGE
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP40 (P)

PLCC44 (K)

Figure 1. Logic Diagram



DESCRIPTION

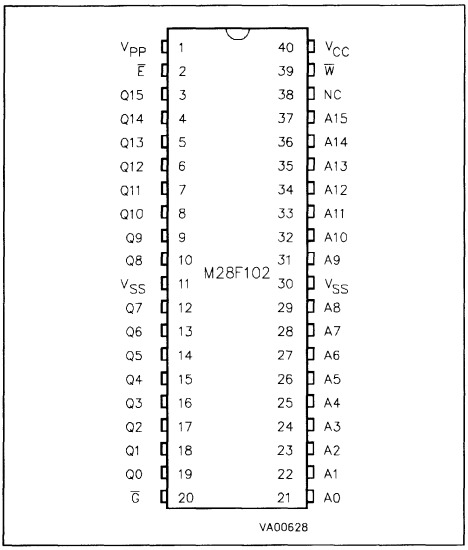
The M28F102 FLASH MEMORY is a non-volatile memory which may be erased electrically at the chip level and programmed word-by-word. It is organised as 64K words of 16 bits. It uses a command register architecture to select the operating modes and thus provides a simple microprocessor interface. The M28F102 FLASH MEMORY is suitable for applications where the memory has to be reprogrammed in the equipment. The access time of 100ns makes the device suitable for use in high speed microprocessor systems.

Table 1. Signal Names

A0 - A15	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

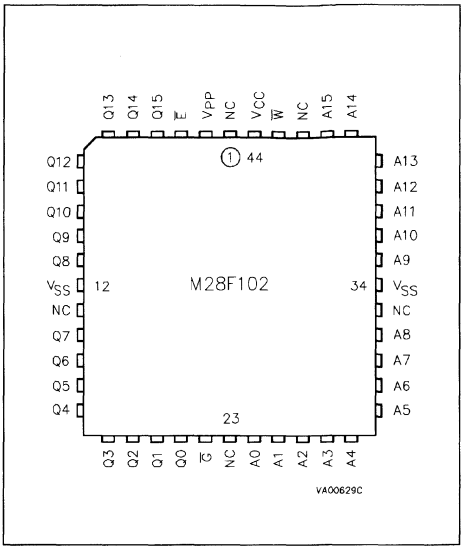
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. LCC Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO}	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{A9}	A9 Voltage		–0.6 to 13.5	V
V_{PP}	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

DEVICE OPERATION

The M28F102 FLASH MEMORY employs a technology similar to a 1 Megabit EPROM but adds to the device functionality by providing electrical erasure and programming. These functions are managed by a command register. The functions that are addressed via the command register depend on the voltage applied to the V_{PP}, program voltage, input. When V_{PP} is less than or equal to 6.5V, the command register is disabled and M28F102 functions as a read only memory providing operating modes similar to an EPROM (Read, Output Disable, Electronic Signature Read and Standby). When V_{PP} is raised to 12V the command regsiter is enabled and this provides, in addition, Erase and Program operations.

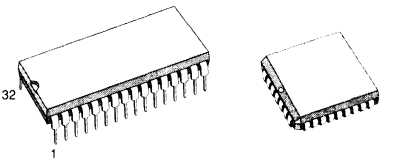
SGS-THOMSON MICROELECTRONICS

M28F201
M28V201

CMOS 2 Megabit (256K x 8, Chip Erase) FLASH MEMORY

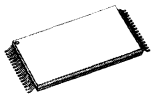
ABBREVIATED DATA

- FAST ACCESS TIMES
  - 60ns for M28F201 version
  - 150ns for M28V201 version
- LOW POWER CONSUMPTION
  - Standby Current: 100µA Max
- 10,000 PROGRAM/ERASE CYCLES
- 12V PROGRAMMING VOLTAGE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M20F201 version
  - 3.3V ± 0.3V for M20V201 version
- TYPICAL BYTE PROGRAMMING TIME 10µs (PRESTO F ALGORITHM)
- ELECTRICAL CHIP ERASE in 1s RANGE
- INTEGRATED ERASE/PROGRAM-STOP TIMER



PDIP32 (P)

PLCC32 (K)



TSOP32 (N)
8 x 20 mm

DESCRIPTION

The M28F201, M28V201 FLASH MEMORY products are non-volatile memories which may be erased electrically at the chip level and programmed byte-by-byte. They are organised as 256K bytes of 8 bits. They use a command register architecture to select the operating modes and thus provide a simple microprocessor interface. The M28F201, M28V201 FLASH MEMORY products are suitable for applications where the memory has to be reprogrammed in the equipment.

Figure 1. Logic Diagram

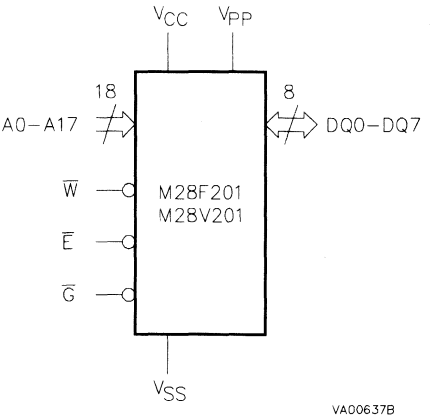


Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

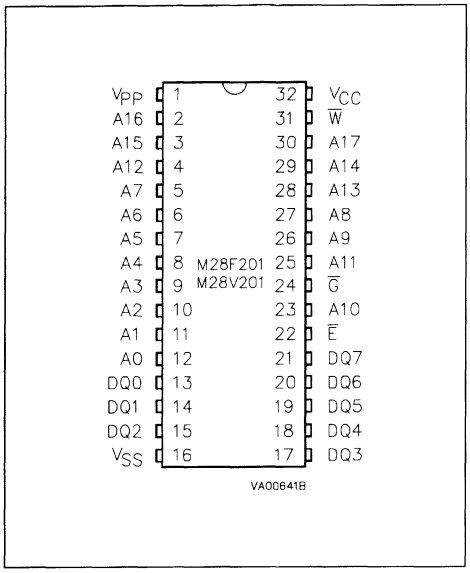


Figure 2B. LCC Pin Connections

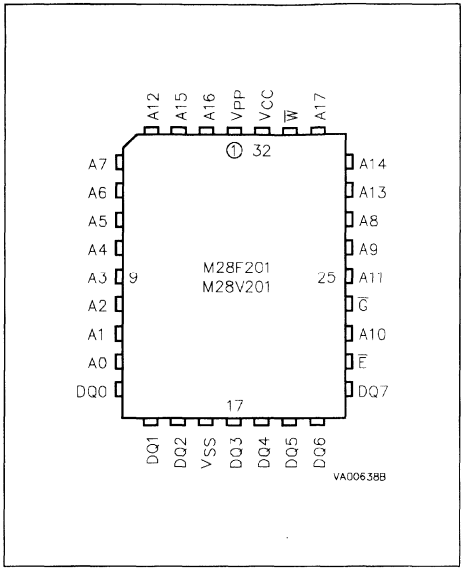


Figure 2C. TSOP Pin Connections

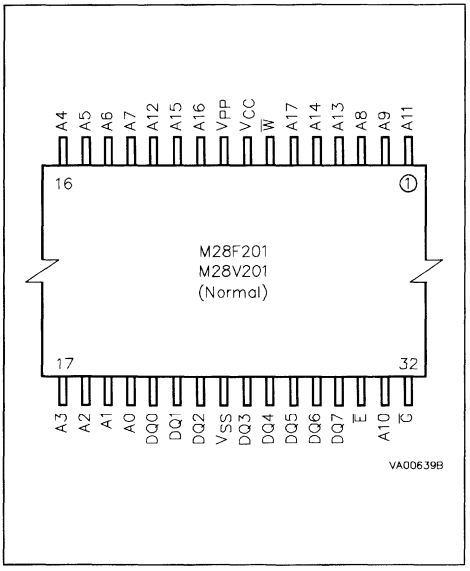
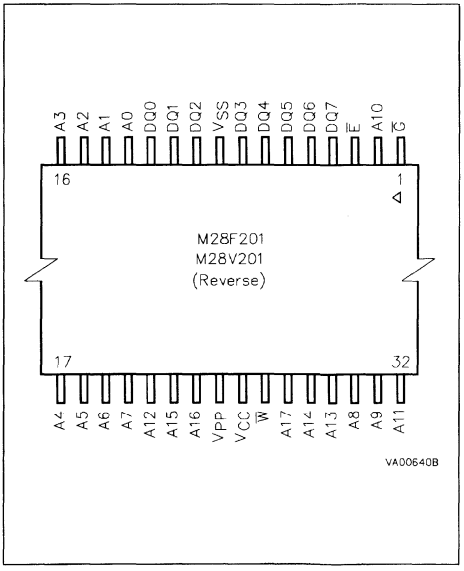


Figure 2D. TSOP Reverse Pin Connections



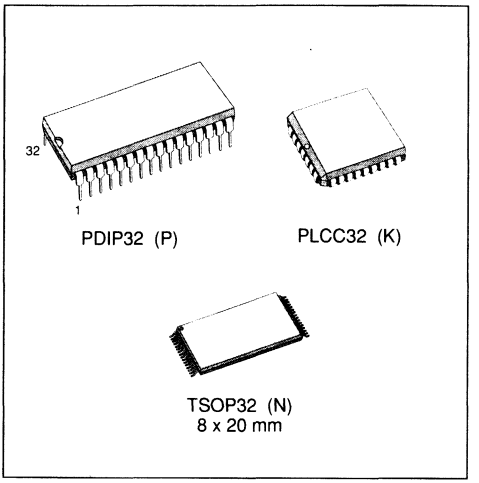
SGS-THOMSON MICROELECTRONICS

M28F201A
M28V201A

CMOS 2 Megabit (256K x 8, Chip Erase) FLASH MEMORY

ABBREVIATED DATA

- MEMORY CHIP ERASE
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F201A version
  - 3.3V ± 0.3V for M28V201A version
- 12V PROGRAMMING VOLTAGE
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F201A
  - 10,000 for M28V201A
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Data Polling and Toggle Protocol for P/E. C. Status
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
- FAST ACCESS TIMES
  - 60ns for M28F201A version
  - 150ns for M28V201A version



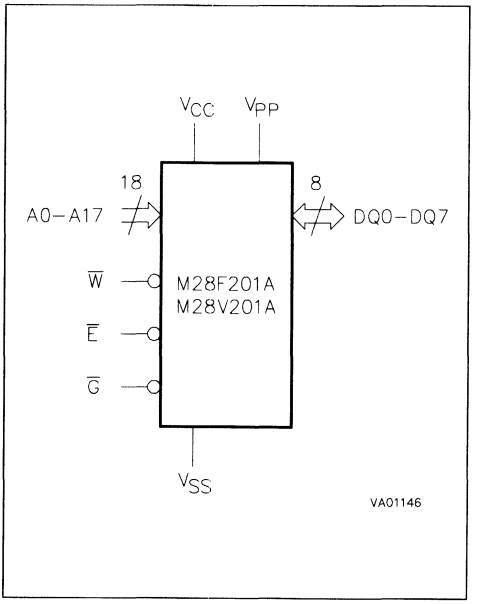
DESCRIPTION

The M28F201A, M28V201A FLASH MEMORY products are non-volatile memories that may be erased electrically in bulk and programmed byte-by-byte. The interface is directly compatible with most microprocessors. The device is available in PDIP32, PLCC32 and TSOP32 (8 x 20mm). Both normal and reverse pin outs are available for the TSOP32 package.

Table 1. Signal Names

A0 - A17	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

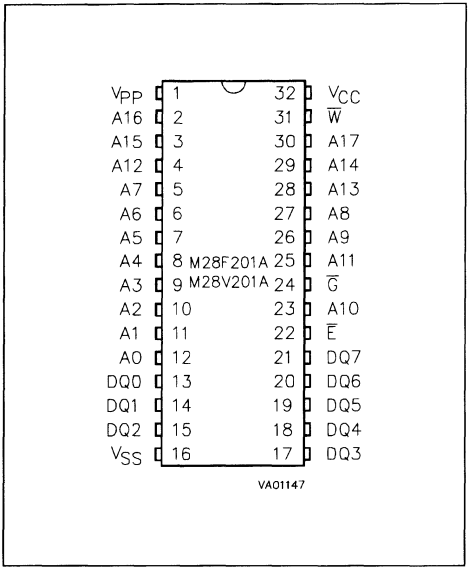


Figure 2B. LCC Pin Connections

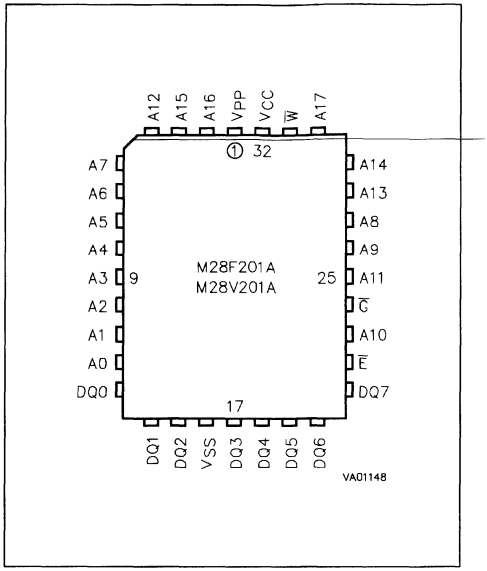


Figure 2C. TSOP Pin Connections

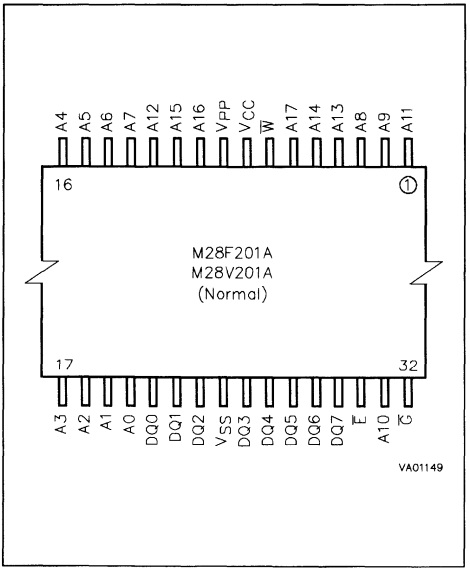
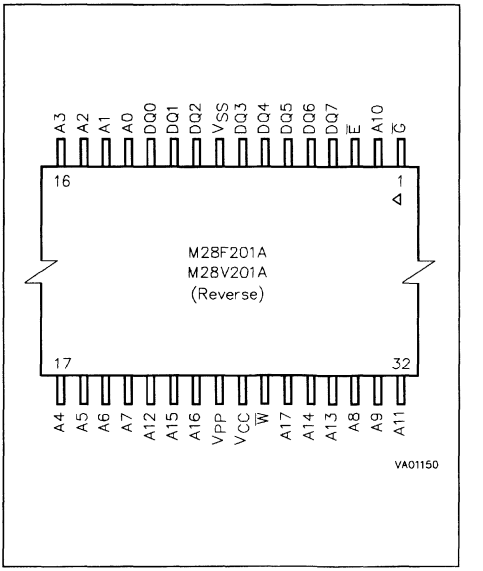


Figure 2D. TSOP Reverse Pin Connections



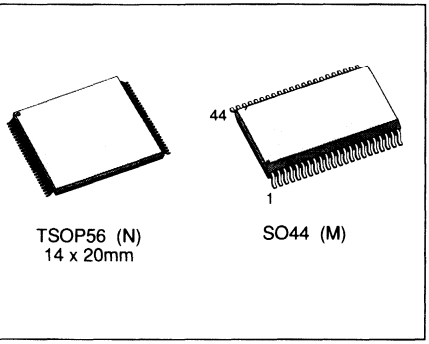
SGS-THOMSON MICROELECTRONICS

M28F410, F420
M28V410, V420

CMOS 4 Megabit (x8 or x16, 7 Block Erase) FLASH MEMORY

ABBREVIATED DATA

- SMALL SIZE TSOP56 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP version
- DUAL x8 and x16 ORGANISATION
- MEMORY ERASE in BLOCKS
  - One 16K Boot Block (top or bottom location) with hardware write protection
  - Two 8K bytes Key Parameter Blocks
  - One 96K bytes Main Block
  - Three 128K bytes Main Blocks
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F410, F420 versions
  - 3V to 5.5V for M28V410, V420 versions
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F410, F420 versions
  - 10,000 for M28V410, V420 versions
- PROGRAM/ERASE CONTROLLER
- LOW POWER CONSUMPTION
  - 80µA Typical in Standby for M28F410, F420
  - 50µA Typical in Standby for M28V410, V420
  - 0.2µA Typical in Deep Power Down for all versions
- FAST ACCESS TIMES
  - 60-80ns for M28F410, F420
  - 150-200ns for M28V410, V420



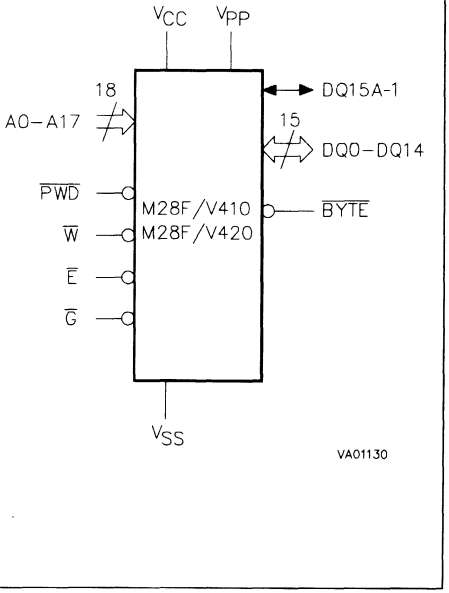
TSOP56 (N)
14 x 20mm

SO44 (M)

Table 1. Signal Names

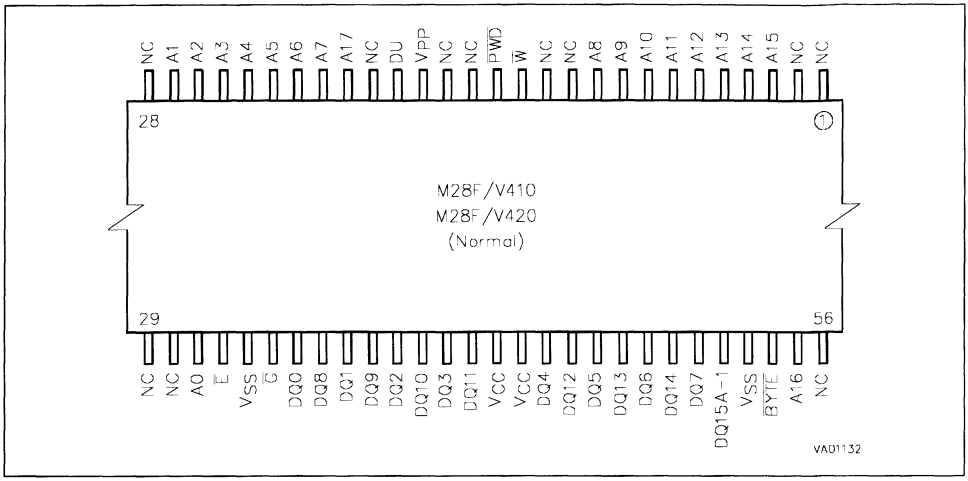
A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
DQ8-DQ14	Data Input / Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{BYTE}$	Byte/Word Organisation
$\overline{PWD}$	Power Down/Boot Block Lock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



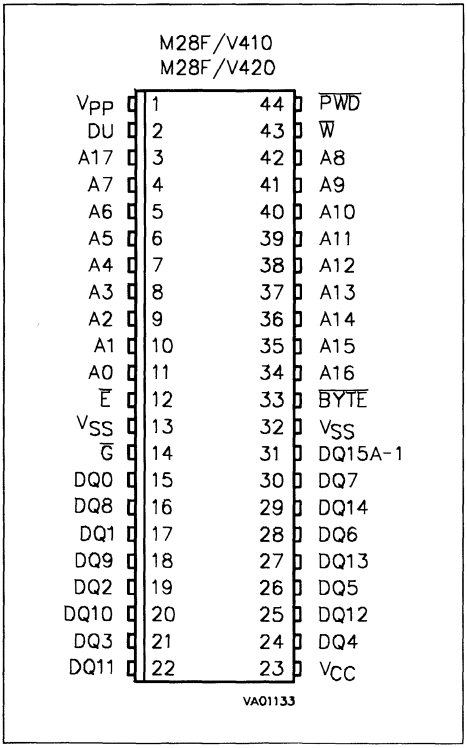
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. TSOP Pin Connections



Warning: NC = No Connections, DU = Don't Use

Figure 2B. SO Pin Connections



Warning: DU = Don't Use

DESCRIPTION

The M28F410, F420 and M28V410, V420 FLASH MEMORY products are non- volatile memories that may be erased electrically at the block level and programed by byte or word. The interface is directly compatible with most microprocessors. Plastic PTSO56 (Normal and Reverse pinout) and PSO44 packages are used.

Organisation

The organisation, as 512K x 8 or 256K x 16, is selectable by an external $\overline{BYTE}$ signal. When $\overline{BYTE}$ is Low and the x8 organisation is selected, the Data Input/Output signal DQ15 acts as Address line A-1 and selects the lower or upper byte of the memory word for output on DQ0-DQ7, DQ8-DQ15 remain high impedance. When $\overline{BYTE}$ is High the memory uses the Address inputs A0-A18 and the Data Input/Outputs DQ0-DQ15. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down/Boot block unlock, tri-state, input places the memory in deep power down, normal operation or enables programing and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one 'Boot' block of 16K, two 'Key Parameter' blocks of 8K, one 'Main' block of 96K and three 'Main' blocks of 128K. The M28F410, V410 memories have the Boot block at the top of the memory address space and the M28F420, V420 locate the Boot block starting at the bottom.

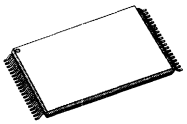
SGS-THOMSON MICROELECTRONICS

M28F411, F421
M28V411, V421

CMOS 4 Megabit (512K x 8, 7 Block Erase) FLASH MEMORY

ABBREVIATED DATA

- SMALL SIZE TSOP40 PLASTIC PACKAGE
  - Normal and Reverse Pinout
- MEMORY ERASE in BLOCKS
  - One 16K Boot Block (top or bottom location) with hardware write protection
  - Two 8K Key Parameter Blocks
  - One 96K Main Block
  - Three 128K Main Blocks
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F411, F421 versions
  - 3V to 5.5V for M28V411, V421 versions
- PROGRAM/ERASE CYCLES
  - 100,000 for M28F411, F421 versions
  - 10,000 for M28V411, V421 versions
- PROGRAM/ERASE CONTROLLER
- LOW POWER CONSUMPTION
  - 80µA Typical in Standby for M28F411, F421
  - 50µA Typical in Standby for M28V411, V421
  - 0.2µA Typical in Deep Power Down for all versions
- FAST ACCESS TIMES
  - 60-80ns for M28F411, F421
  - 150-200ns for M28V411, V421



TSOP40 (N)
10 x 20mm

Figure 1. Logic Diagram

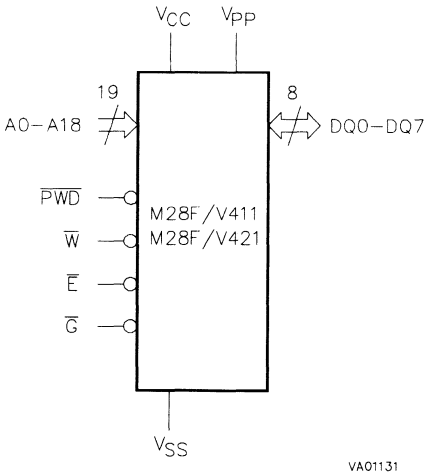
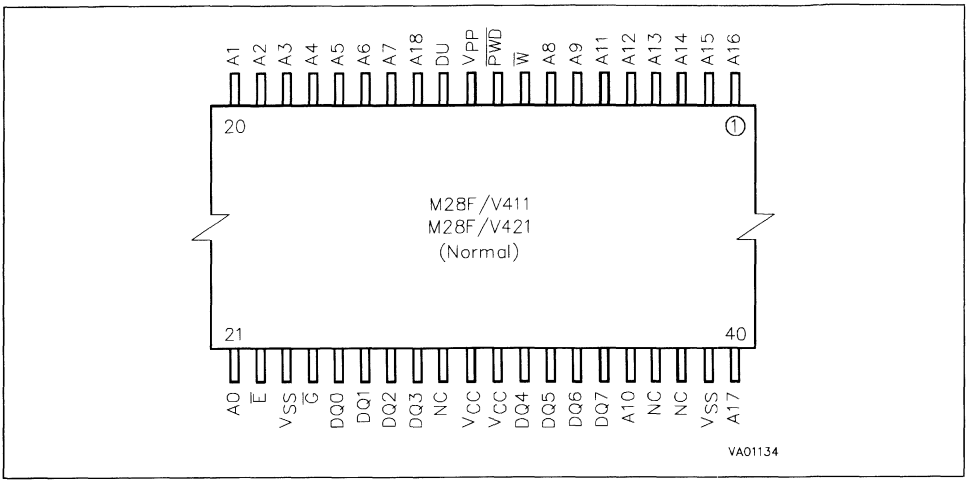


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down/Boot Block Lock
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2. TSOP Pin Connections



Warning: NC = No Connection, DU = Don't Use

DESCRIPTION

The M28F411, F421 and M28V411, V421 FLASH MEMORY products are non- volatile memories that may be erased electrically at the block level and programed byte-by-byte. The interface is directly compatible with most microprocessors. Plastic TSOP40 (Normal and Reverse pinout) package is used.

Organisation

The organisation is 512K x 8 with Address lines A0-A18 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down/Boot block unlock, tri-state, input places the memory in deep power down, normal operation or enables programing and erasure of the Boot block.

Blocks

Erasure of the memories is in blocks. There are 7 blocks in the memory address space, one 'Boot' block of 16K, two 'Key Parameter' blocks of 8K, one 'Main' block of 96K and three 'Main' blocks of 128K. The M28F411, V411 memories have the Boot block at the top of the memory address space and the M28F421, V421 locate the Boot block starting at the bottom. Erasure of each block takes typically 1-2 seconds and each block may be programed and erased over 100,000 cycles (10,000 for M28V411, V421). The Boot block is protected from accidental programing or erasure by a hardware protection depending on the $\overline{PWD}$ signal. Program/Erase commands in the Boot block are executed only when $\overline{PWD}$ is at 12V. Block erasure may be suspended while data is read from other blocks of the memory, then resumed.

Command Interface

Commands can be written to a Command Interface latch to perform read, programming, erasure and to monitor the memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array. Five operations can be performed by the appropriate bus cycles, Read Byte from the Array, Read Electronic Signature, Output Disable, Standby and Write a Command of an Instruction.

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status.

Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the array, the Electronic Signature or the Status Register.

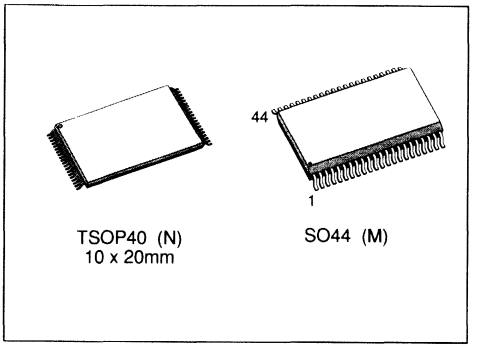
SGS-THOMSON MICROELECTRONICS

M28F841
M28V841

CMOS 8 Megabit (1Meg x 8, 16 x 64K Sector Erase) FLASH MEMORY

ABBREVIATED DATA

- SMALL SIZE TSOP40 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP versions
- MEMORY ERASE in SECTORS, 16 x 64K
- SUPPLY VOLTAGE in READ OPERATION
  - 5V ± 10% for M28F841 version
  - 3V to 5.5V for M28V841 version
- PROGRAM/ERASE CYCLES per SECTOR
  - 100,000 for M28F841 version
  - 10,000 for M28V841 version
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume
  - Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- FAST ACCESS TIMES
  - 85-120ns for M28F841
  - 200ns for M28V841



TSOP40 (N)
10 x 20mm

SO44 (M)

Figure 1. Logic Diagram

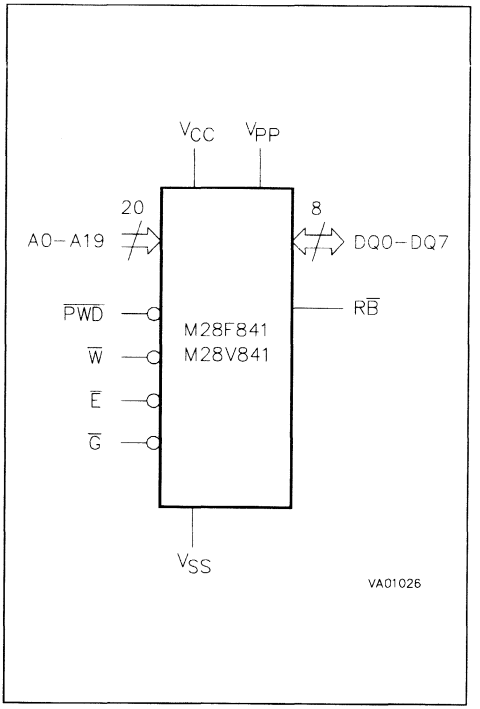
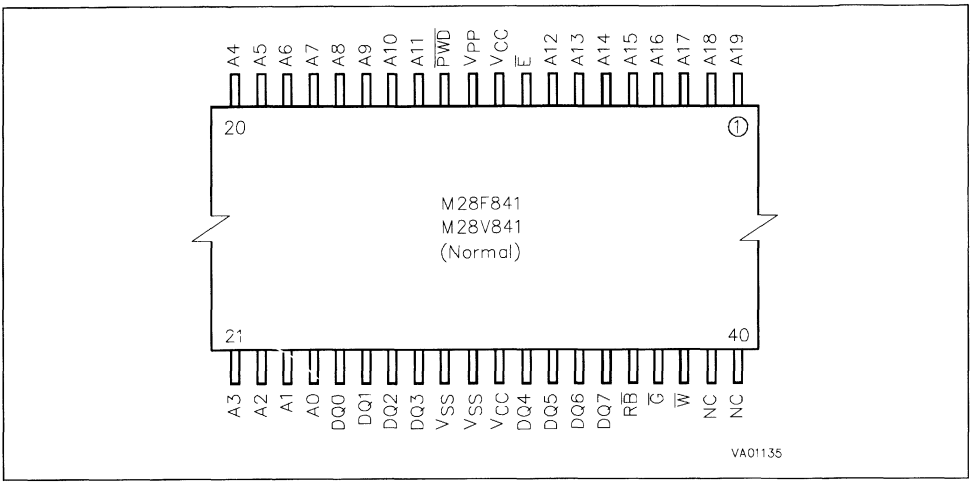


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down
$\overline{RB}$	Ready Busy Output
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

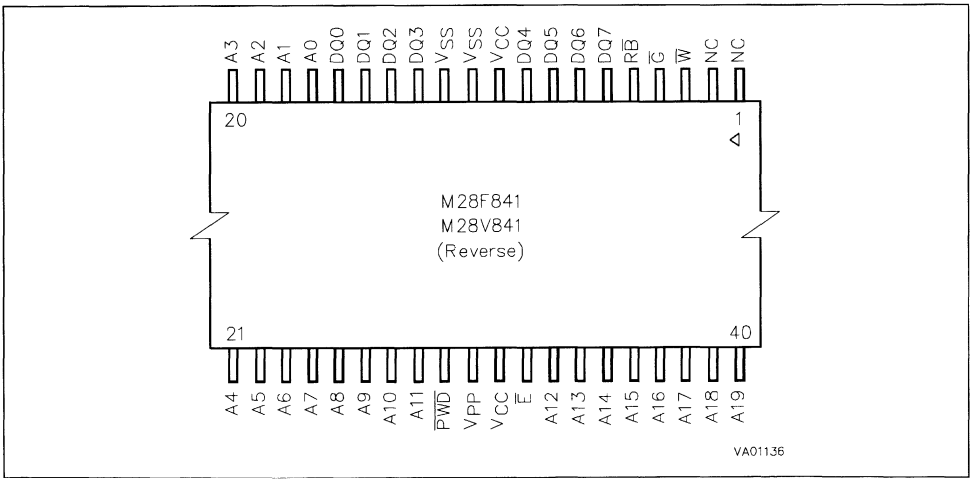
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. TSOP Pin Connections



Warning: NC = No Connection

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = No Connection

DESCRIPTION

The M28F841, M28V841 FLASH MEMORY products are non-volatile memories that may be erased electrically at the sector level and programed byte-by-byte. The interface is directly compatible with most microprocessors. They are intended for computer file systems applications. Plastic TSOP40 (Normal and Reverse pinout) and SO44 packages are used.

Organisation

The organisation is 1 Meg x 8 with Address lines A0-A19 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

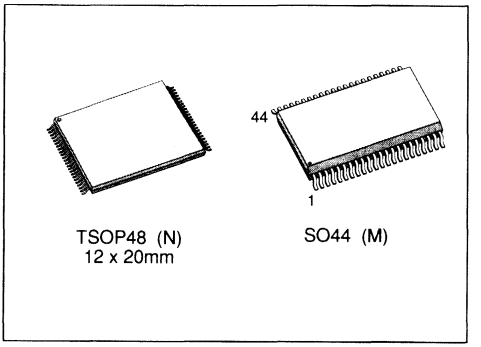
SGS-THOMSON MICROELECTRONICS

M28F161

CMOS 16 Megabit (2Meg x 8, 32 x 64K Sector Erase) FLASH MEMORY

ABBREVIATED DATA

- SMALL SIZE TSOP48 and SO44 PLASTIC PACKAGES
  - Normal and Reverse Pinout for TSOP versions
- MEMORY ERASE in SECTORS, 32 x 64K
- SUPPLY VOLTAGE in READ OPERATION
  - 3.3V ± 0.3V
- 12V PROGRAMMING VOLTAGE
- 10,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume
  - Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- FAST ACCESS TIMES: 100ns Max



TSOP48 (N)
12 x 20mm

SO44 (M)

Figure 1. Logic Diagram

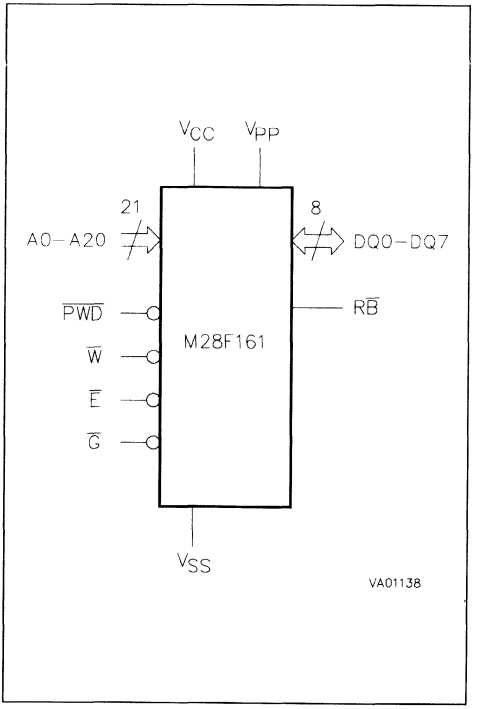
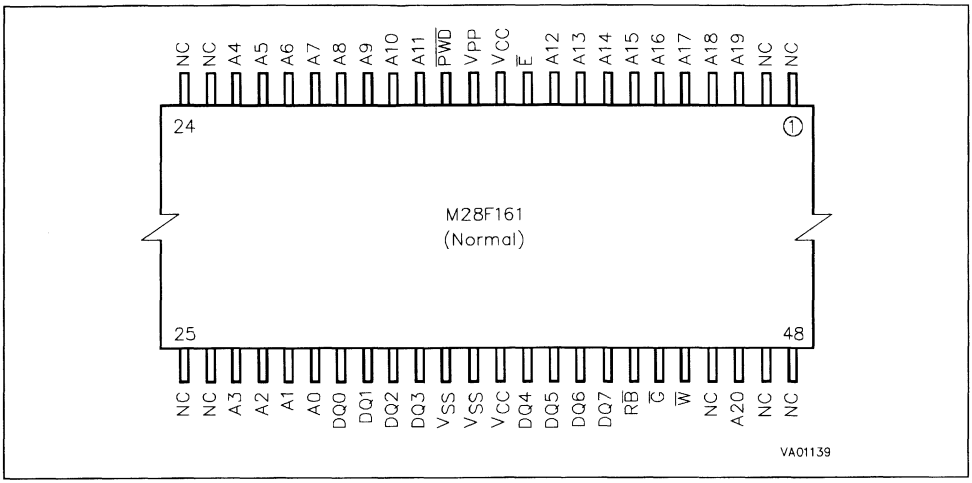


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{PWD}$	Power Down
$\overline{RB}$	Ready Busy Output
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

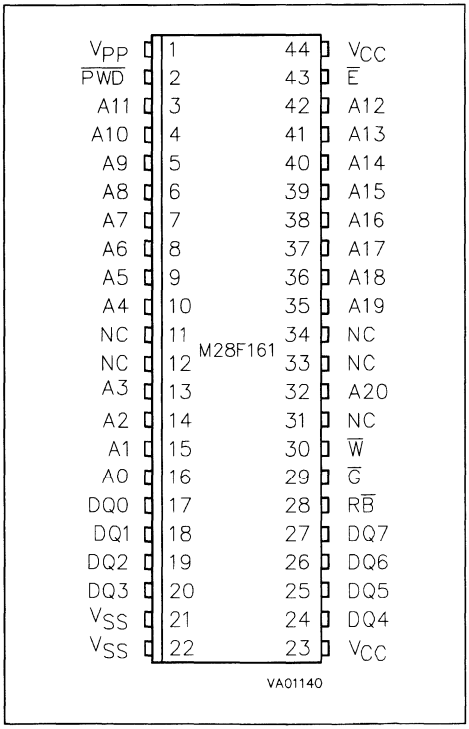
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. TSOP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

DESCRIPTION

The M28F161 FLASH MEMORY is a non-volatile memory that may be erased electrically at the sector level and programed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems applications. Plastic TSOP48 (Normal and Reverse pinout) and SO44 packages are used.

Organisation

The organisation is 2 Meg x 8 with Address lines A0-A20 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 32 sectors in the memory address space, each of 64K bytes. Programing of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programed and erased over 10,000 cycles. All sectors are protected from programming or erasure when the Power Down PWD signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

SERIAL ACCESS CMOS 1K (128 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C01 version
  - 3V to 5.5V for ST24x01C versions
  - 2.5V to 5.5V for ST25C01, ST25x01C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W01C and ST25W01C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES FOR "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C01C and ST24/25W01C

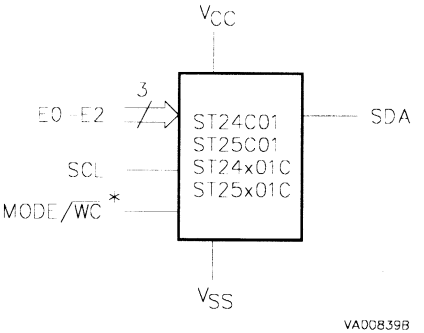
PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

This specification covers a range of 1K bits I^2C bus EEPROM products, the ST24/25C01, the ST24/25C01C and the ST24/25W01C. In the text, products are referred to as ST24/25x01C, where

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W01C products.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

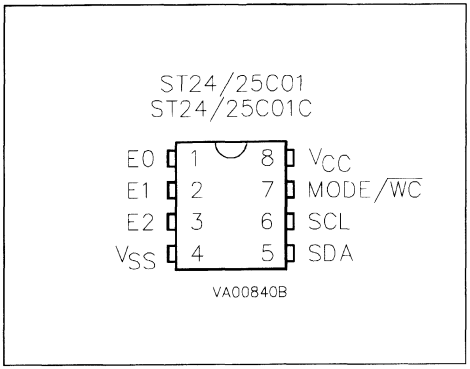


Figure 2B. SO Pin Connections

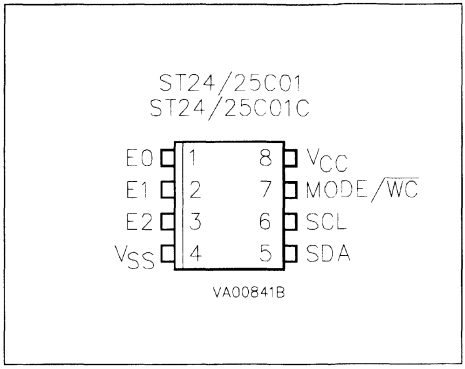


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C01 ST24/25x01C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C01 ST24/25x01C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C01 ST24/25x01C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x01C are 1K bit electrically erasable programmable memories (EEPROM), organized as 128 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

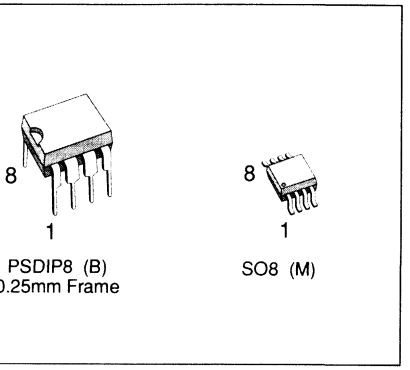
SGS-THOMSON MICROELECTRONICS

ST24C02A, ST25C02A
ST24x02C, ST25x02C

SERIAL ACCESS CMOS 2K (256 x 8) EEPROMs

ABBREVIATED DATA

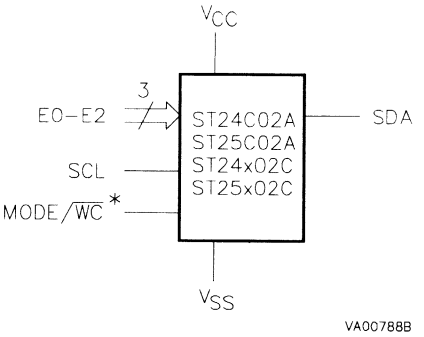
- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24C02A version
  - 3V to 5.5V for ST24x02C versions
  - 2.5V to 5.5V for ST25C02A, ST25x02C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W02C and ST25W02C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C02C and ST24/25W02C



PSDIP8 (B)
0.25mm Frame

SO8 (M)

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02C products.

DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02A, the ST24/25C02C and the ST24/25W02C. In the text, products are referred to as ST24/25x02C, where

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

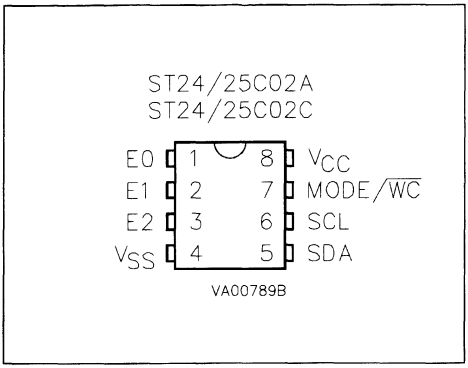


Figure 2B. SO Pin Connections

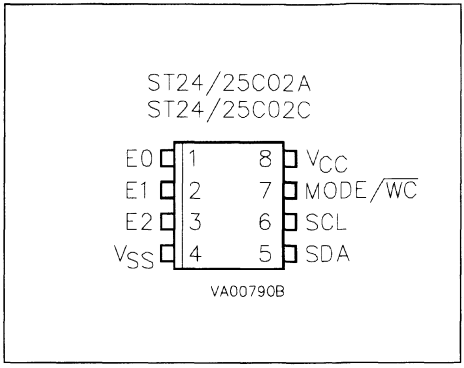


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C02A ST24/25x02C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C02A ST24/25x02C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C02A ST24/25x02C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x02C are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V.

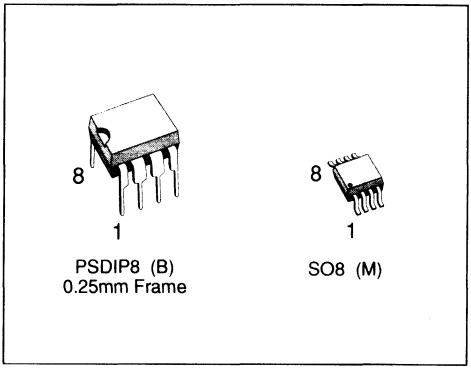
Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

ST24C04, ST25C04
ST24x04C, ST25x04C

SERIAL ACCESS CMOS 4K (512 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C04 version
  - 3V to 5.5V for ST24x04C versions
  - 2.5V to 5.5V for ST25C04, ST25x04C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W04C and ST25W04C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGNS: ST24/25C04C and ST24/25W04C



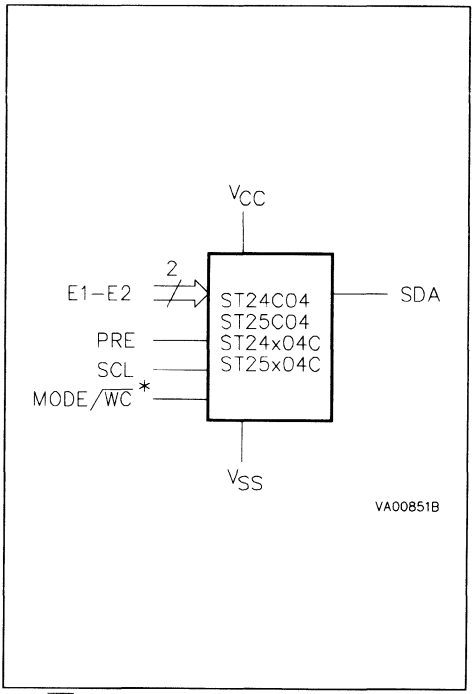
DESCRIPTION

This specification covers a range of 4K bits I^2C bus EEPROM products, the ST24/25C04, the ST24/25C04C and the ST24/25W04C. In the text, products are referred to as ST24/25x04C, where

Table 1. Signal Names

PRE	Write Protect Enable
E1 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W04C products.

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

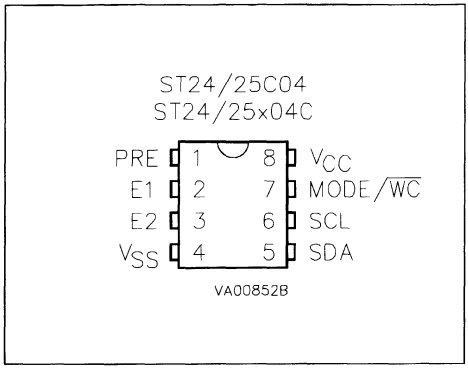


Figure 2B. SO Pin Connections

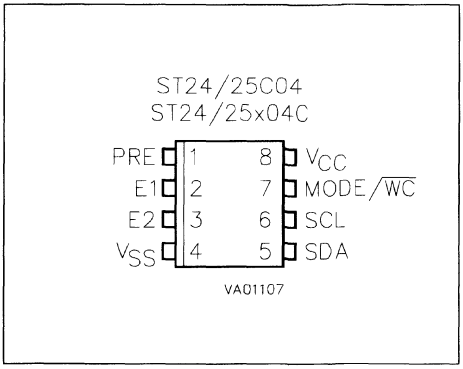


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C04 ST24/25x04C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C04 ST24/25x04C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C04 ST24/25x04C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

"x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x04C are 4K bit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

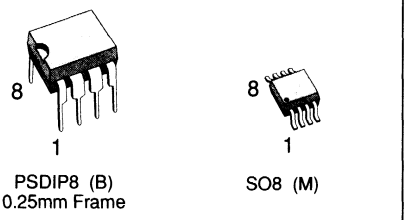
SGS-THOMSON MICROELECTRONICS

ST24C08, ST25C08
ST24x08C, ST25x08C

SERIAL ACCESS CMOS 8K (1024 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24C08 version
  - 3V to 5.5V for ST24x08C versions
  - 2.5V to 5.5V for ST25C08, ST25x08C versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W08C and ST25W08C
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES for "C" VERSIONS
- PREFERRED DEVICES for NEW DESIGN: ST24/25C08C and ST24/25W08C



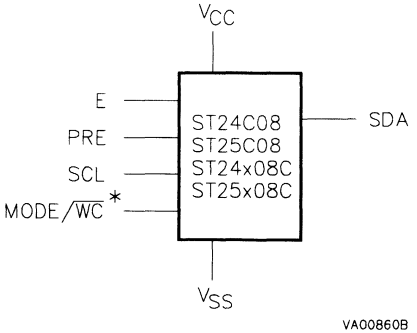
PSDIP8 (B)
0.25mm Frame

SO8 (M)

DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08, the ST24/25C08C and the ST24/25W08C. In the text,

Figure 1. Logic Diagram



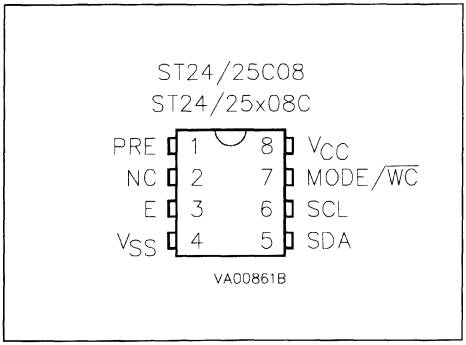
Note: $\overline{WC}$ signal is only available for ST24/25W08C products.

Table 1. Signal Names

PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

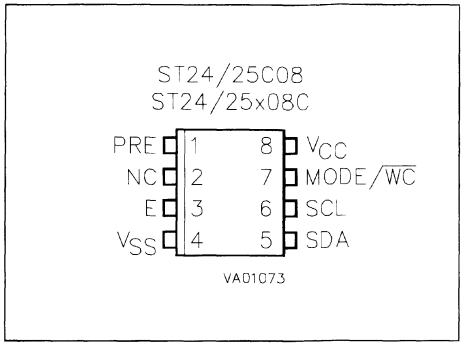
This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage	ST24/25C08 ST24/25x08C		–0.3 to V_{CC} +0.6 –0.3 to 6.5	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		ST24/25C08 ST24/25x08C	2000 4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		ST24/25C08 ST24/25x08C	500 500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

products are referred to as ST24/25x08C, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

The ST24/25x08C are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits.

They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years.

The memories operate with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

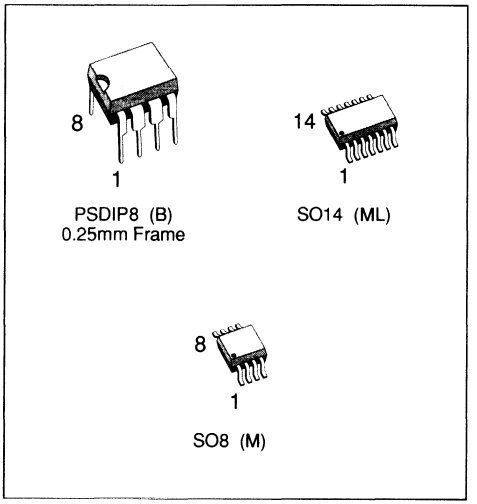
SGS-THOMSON MICROELECTRONICS

ST24C16, ST25C16 ST24W16, ST25W16

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

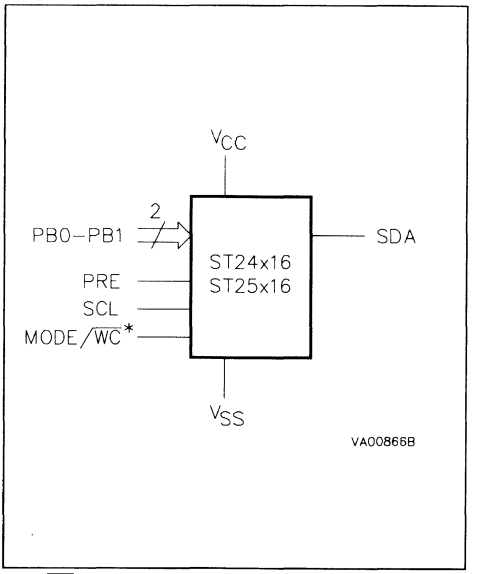
This specification covers a range of 16K bits I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{W}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

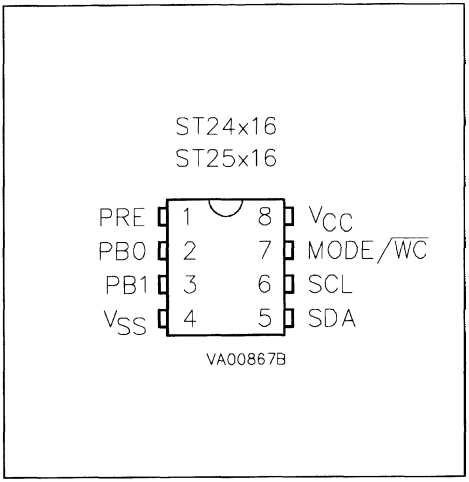
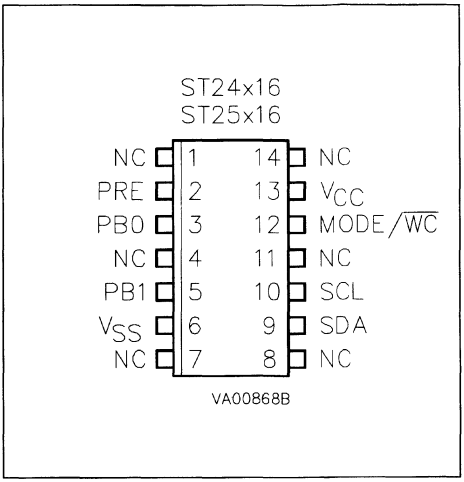
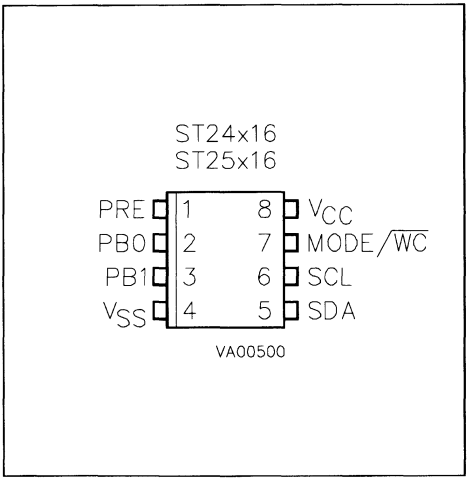


Figure 2B. SO14 Pin Connections



Warning: NC = No Connection

Figure 2C. SO8 Pin Connections



DESCRIPTION (cont'd)

in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years.

The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

SGS-THOMSON MICROELECTRONICS

ST24E16D
ST25E16D

SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS

ABBREVIATED DATA

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24E16D version
  - 2V to 5.5V for ST25E16D version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

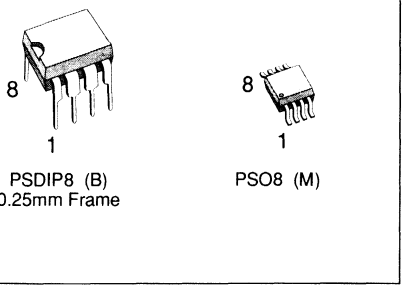
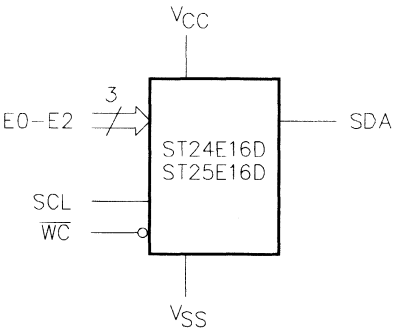


Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E16D are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. It is manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years. The ST25E16D operates with a power supply value as

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

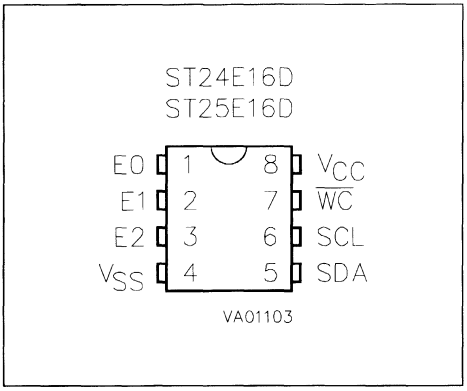


Figure 2B. SO Pin Connections

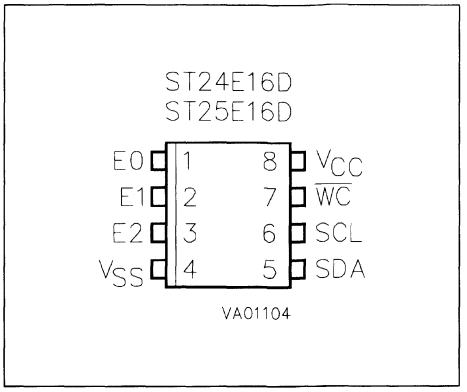


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

low as 2.0V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E16D carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E16D behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master.

The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

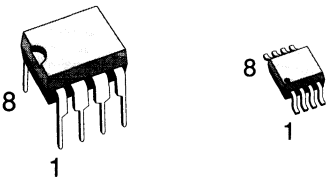
SGS-THOMSON MICROELECTRONICS

MK41T56

CMOS 64 x 8 SERIAL ACCESS TIMEKEEPER SRAM

ABBREVIATED DATA

- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH and YEARS
- SOFTWARE CALIBRATION
- AUTOMATIC POWER FAIL DETECT and SWITCH CIRCUITRY
- I^2C BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA



PSDIP8 (N)
0.4mm Frame

SO8 (S)
0.15mm Frame

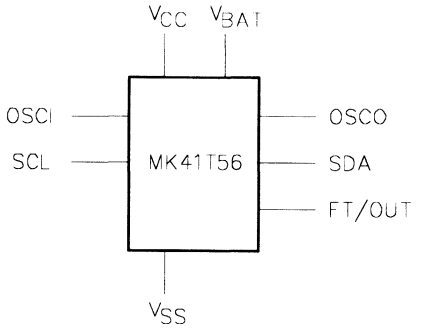
DESCRIPTION

The MK41T56 TIMEKEEPER™ RAM is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (externally crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in BCD format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell.

Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test/Output Driver
SDA	Serial Data Address Input/Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



This is an abbreviated version of the complete document. The full document is available separately.

Figure 2A. DIP Pin Connections

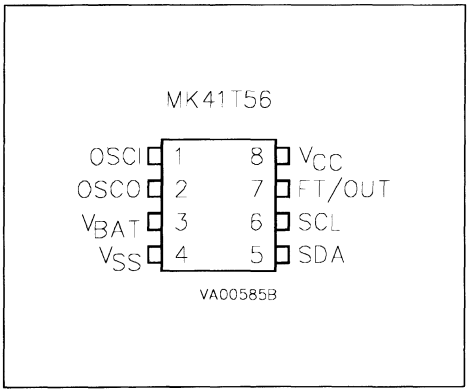


Figure 2B. SO Pin Connections

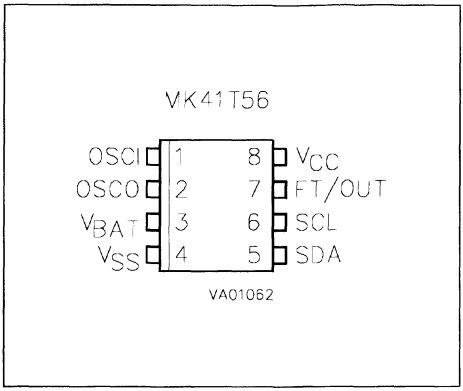


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–55 to 125	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	0.25	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST								Seconds	00-59
1	X								Minutes	00-59
2	X	X							Hour	00-23
3	X	X	X	X	X				Day	01-07
4	X	X							Date	01-31
5	X	X							Month	01-12
6									Year	00-99
7	OUT	FT	S						Control	

Keys: **S** = SIGN Bit; **FT** = FREQUENCY TEST Bit; **ST** = STOP Bit; **OUT** = Output level; **X** = Don't care.

DEDICATED MCUs

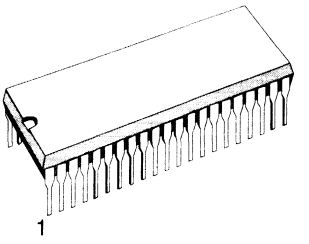
SGS-THOMSON MICROELECTRONICS

ST6365, ST6375, ST6385
ST6367, ST6377, ST6387

8-BIT HCMOS MCUs WITH ON-SCREEN DISPLAY FOR TV TUNING

PRELIMINARY DATA

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program ROM: up to 20140 bytes
- Reserved Test ROM:up to 340 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 42-Pin Shrink Dual in Line Plastic Package
- Up to 22 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- SPI for external frequency synthesis tuning
- 14 bit counter for voltage synthesis tuning
- Up to Six 6-Bit PWM D/A Converters
- AFC A/D converter with 0.5V resolution
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- All ROM types are supported by pin-to-pin EPROM and OTP versions.
- The development tool of the ST636x,7x,8x microcontrollers consists of the ST638x-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PSDIP42

DEVICE SUMMARY

DEVICE	ROM (Bytes)	D/A Converter
ST6365	8K	4
ST6367	8K	6
ST6375	14K	4
ST6377	14K	6
ST6385	20K	4
ST6387	20K	6

February 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 3. ST6365,67,75,77,85,87 Block Diagram

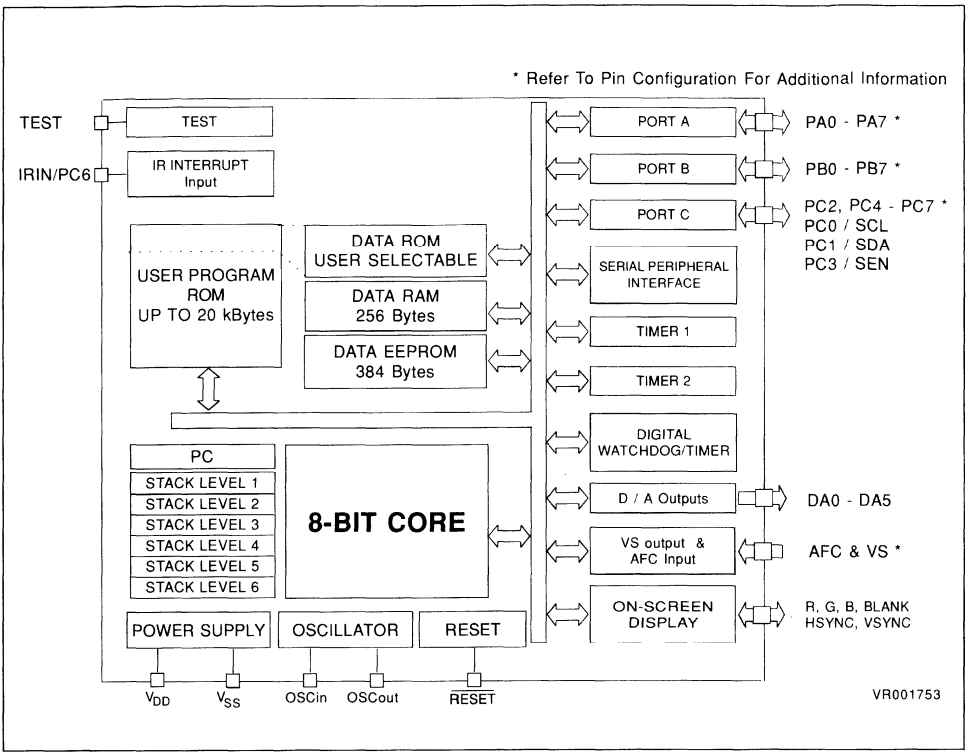


Table 1. Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	COLOUR PINS	EMULATING DEVICES
ST6365	8K	256	384	YES	YES	4	3	ST63E85, ST63T85
ST6367	8K	256	384	YES	YES	6	3	ST63E87, ST63T87
ST6375	14K	256	384	YES	YES	4	3	ST63E85, ST63T85
ST6377	14K	256	384	YES	YES	6	3	ST63E87, ST63T87
ST6385	20K	256	384	YES	YES	4	3	ST63E85, ST63T85
ST6387	20K	256	384	YES	YES	6	3	ST63E87, ST63T87

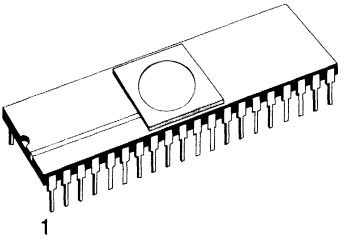
SGS-THOMSON MICROELECTRONICS

ST63E85, T85
ST63E87, T87

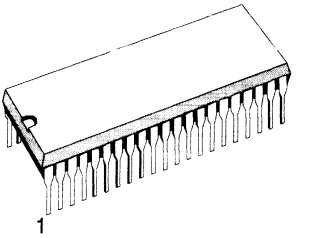
8-BIT EPROM HCMOS MCUs WITH ON-SCREEN DISPLAY FOR TV TUNING

PRELIMINARY DATA

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program EPROM: up to 20140 bytes
- Reserved Test EPROM: up to 340 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 42-Pin Shrink Ceramic Dual in Line Package for EPROM version
- 42-Pin Shrink Plastic Dual in Line Package for OTP version
- Up to 22 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- SPI for external frequency synthesis tuning
- 14 bit counter for voltage synthesis tuning
- Up to Six 6-Bit PWM D/A Converters
- AFC A/D converter with 0.5V resolution
- Five interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters
- These EPROM and OTP versions are fully pin to pin compatible with their respective ROM version.
- The development tool of the ST636x,7x,8x microcontrollers consists of the ST638x-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.
- EPROM programming board ST63E8X-EPB



CSDIP42W



PSDIP42

DEVICE SUMMARY

EPROM DEVICE	OTP DEVICE	D/A Converter	EPROM (Bytes)	EEPROM (Bytes)
ST63E85	ST63T85	4	20K	384
ST63E87	ST63T87	6	20K	384

February 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 3. ST63E85, T85, E87, T87 Block Diagram

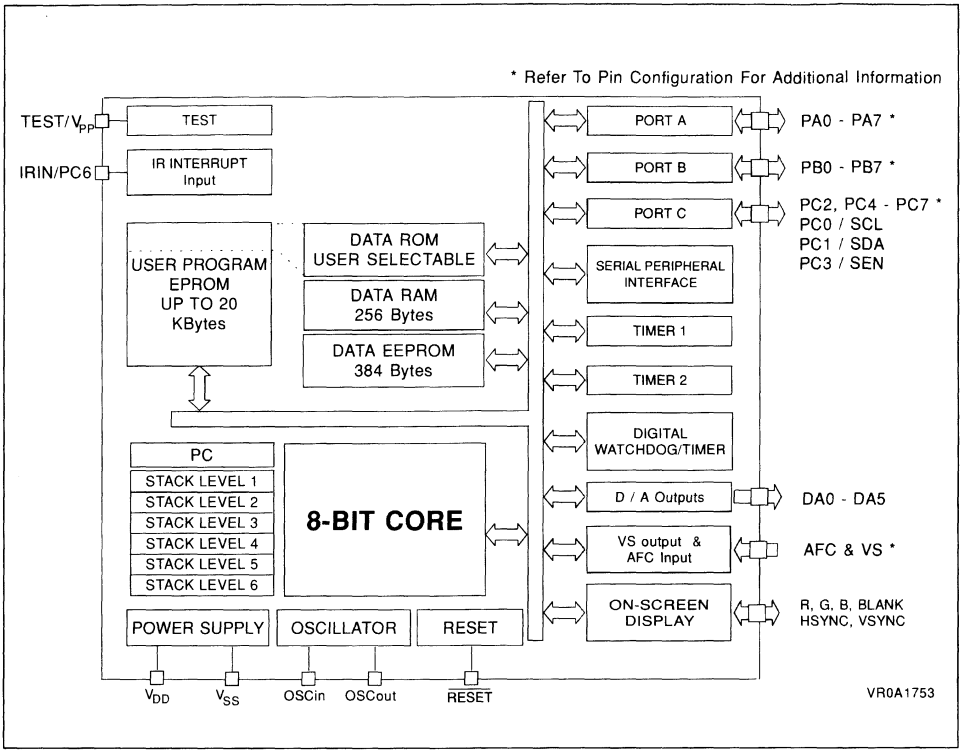


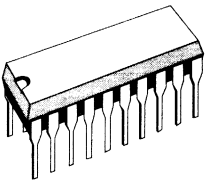
Table 1. Device Summary

DEVICE	EPROM (Bytes)	OTPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	AFC	VS	D/A	COLOUR PINS	TARGET ROM DEVICES
ST63E85	20K		256	384	YES	YES	4	3	ST6365, 75, 85
ST63T85		20K	256	384	YES	YES	4	3	ST6365, 75, 85
ST63E87	20K		256	384	YES	YES	6	3	ST6367, 77 87
ST63T87		20K	256	384	YES	YES	6	3	ST6367, 77, 87

ON-SCREEN DISPLAY

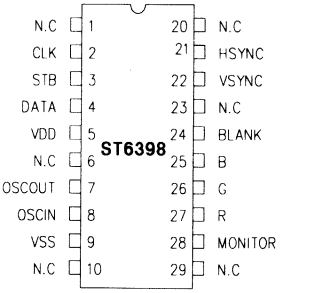
ADVANCE DATA

- Display format of 26 characters x 11 rows
- Character Matrix of 12 x 18 pixels
- Character color selectable on a character by character basis. (up to four different colors per screen).
- Character fonts: 128 ROM and 4 RAM based characters.
- Character background selectable on a character by character basis (no background, background 1 or background 2 ; one backround color set per screen).
- Character border (fringe) enable/disable for each row (one border color per screen).
- Programmable vertical and horizontal start position for the display.
- Programmable horizontal offset position for each row.
- Row enable/disable feature.
- Raster Control: The whole screen can be displayed in a color (display off, screen background enabled) or together with the characters (display on, screen background enabled); or transparent (display on/off,screen backround disabled).
- Vertical row spacing: Rows can be spaced or squeezed by up to 17 lines; a squeezed row will have its height reduced by skipping the required number of lines.
- An extra pin MONITOR (enable / disable) is available to indicate the presence of a character pixel or border (fringe).
- Microcontroller interface with a 3 line serial bus
- Oscillator enable/disable.
- Package: 20 pins DIP (300 mils).
- Power Supply: 4.5 to 5.5 volts.



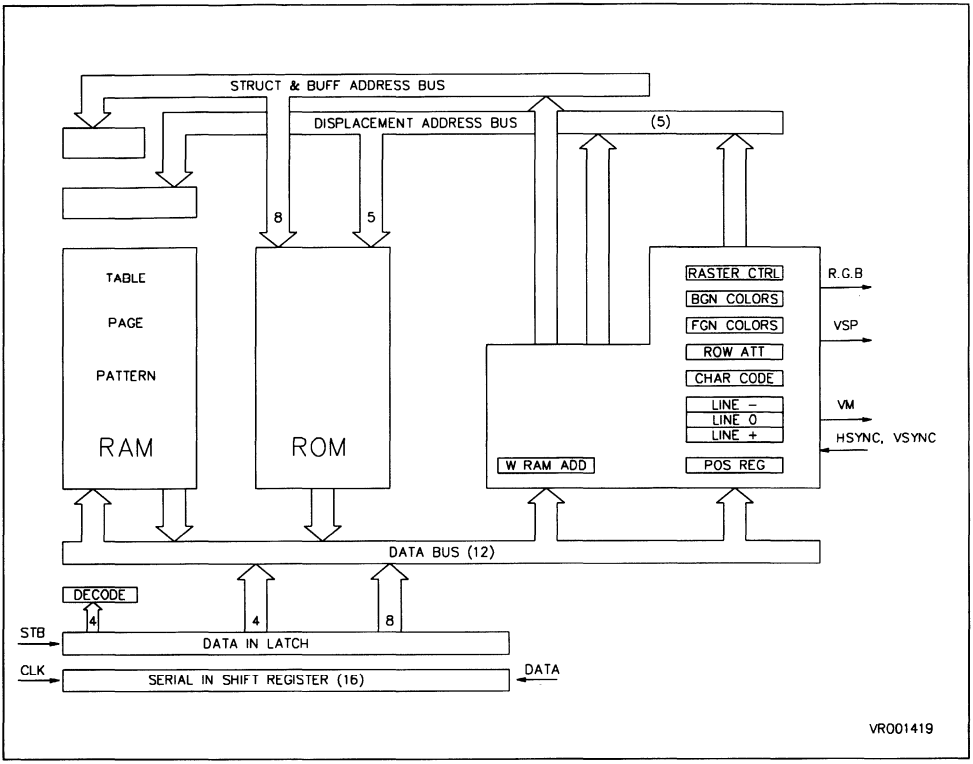
PDIP20

Figure 1. ST6398 Pin Configuration



June 1991

Figure 2. ST6398 Block Diagram



GENERAL DESCRIPTION

The ST6398 is a stand alone on-screen-display peripheral with advanced features.

The device is controlled by an external microcontroller via the serial bus interface. Four characters which can be defined in RAM give great flexibility since characters can be defined and redefined via the serial bus without limit and without changing the character ROM mask. Updating of control registers and characters via the serial bus is not limited to the flyback intervals but can also be performed during the display of characters. Most information is stored in on-chip RAM organized in three main structures: page, attribute and pattern store. The data for the 12-bit words is entered via the serial bus however it is not necessary to redefine all twelve bits via the serial bus when writing similar data to successive addresses.

The device (sales type ST6398B1/B) is delivered with a standard set of ROM based characters; extra characters particular to the application are defined via the RAM characters. If a customized set of ROM based characters is required then contact your SGS-THOMSON sales office.

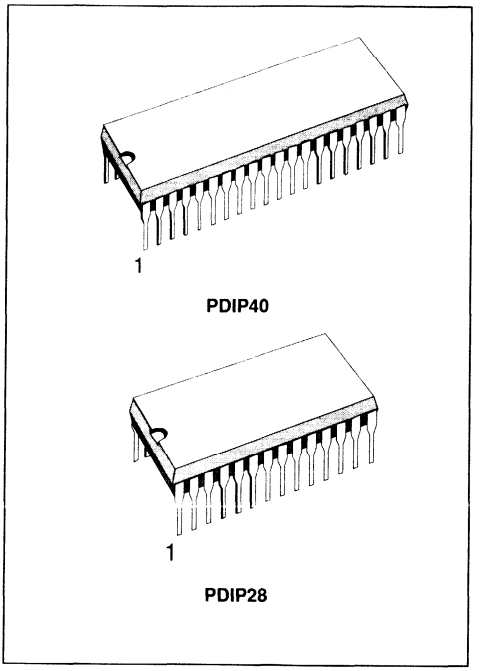
SGS-THOMSON MICROELECTRONICS

ST63140, ST63142
ST63126, ST63156

8-BIT HCMOS MCUs FOR TV FREQUENCY & VOLTAGE SYNTHESIS WITH OSD

PRELIMINARY DATA

- 4.5 to 6V operating Range
- 8MHz Maximum Clock Frequency
- User Program ROM: 7948 bytes
- Reserved Test ROM: 244 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 128 bytes
- 40-Pin Dual in Line Plastic Package for the ST63126, 156
- 28-Pin Dual in Line Plastic Package for the ST63140, 142
- Up to 18 software programmable general purpose Inputs/Outputs, including 8 direct LED driving Outputs
- 3 Inputs for keyboard scan (KBY0-2)
- Up to 4 high voltage outputs (BSW0-3)
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- Up to Four 6-bit PWM D/A Converters
- 62.5kHz Output pin
- 14 bit counter for voltage synthesis tuning (ST63156, ST63140)
- AFC A/D converter with 0.5V resolution
- Four interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters (2 banks)
- All ROM types are supported by pin-to-pin EPROM and OTP versions.
- The development tool of the ST631xx microcontrollers consists of the ST63TVS-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PDIP40

PDIP28

DEVICE SUMMARY

DEVICE	ROM (Bytes)	TUN.	I/O Pins	Package
ST63126	8K	FS	12	PDIP40
ST63156	8K	VS	11	PDIP40
ST63140	8K	VS	6	PDIP28
ST63142	8K	FS	6	PDIP28

August 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 3. ST631xx Block Diagram

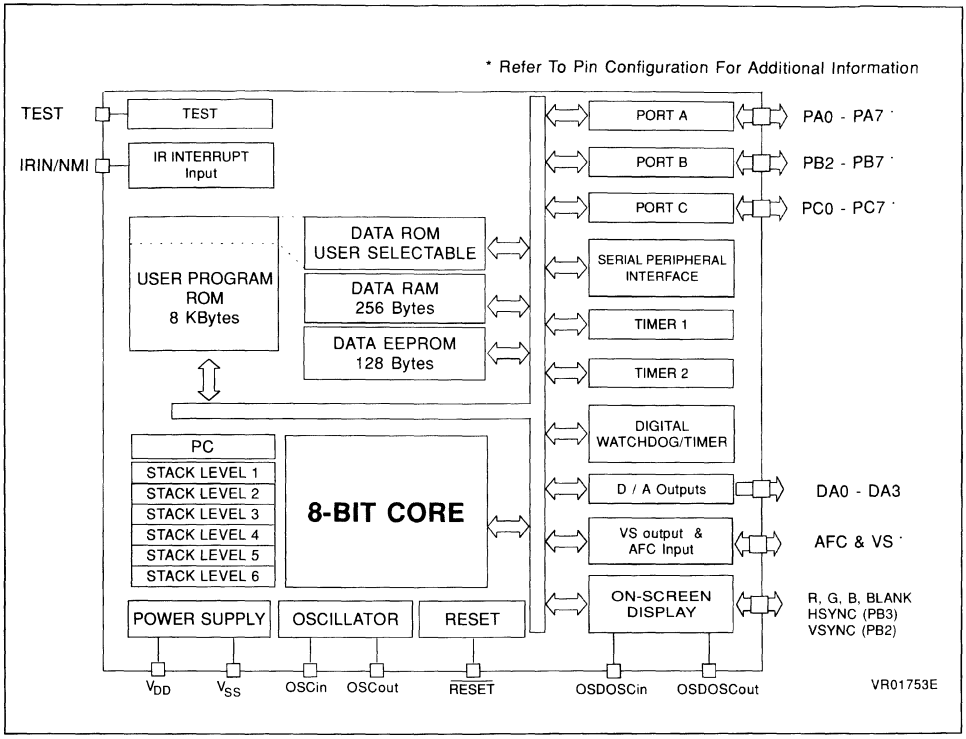


Table 1. Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	VS	D/A	PACK.	EMUL. DEVICES
ST63126	8K	256	128	12	3	4	YES	NO	4	PDIP40	ST63E126
ST63156	8K	256	128	11	3	4	YES	YES	4	PDIP40	ST63E156
ST63140	8K	256	128	6	3	3	YES	YES	1	PDIP28	ST6E140
ST63142	8K	256	128	6	3	3	YES	NO	1	PDIP28	ST63E142

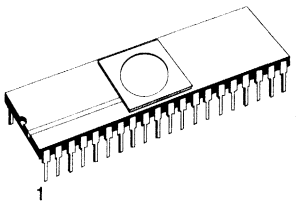
SGS-THOMSON MICROELECTRONICS

ST63E140/T140, E142/T142
ST63E126/T126, E156/T156

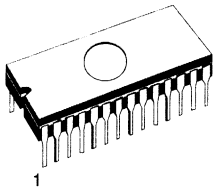
8-BIT EPROM HCMOS MCUs FOR TV FREQUENCY & VOLTAGE SYNTHESIS WITH OSD

PRELIMINARY DATA

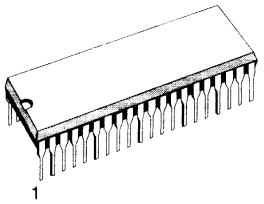
- 4.5 to 6V operating Range
- 8MHz Maximum Clock Frequency
- User Program EPROM: 7948 bytes
- Reserved Test EPROM: 244 bytes
- Data EPROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 128 bytes
- 40-Pin Dual in Line Package for the ST63x126, x156
- 28-Pin Dual in Line Package for the ST63x140, x142
- Up to 18 software programmable general purpose Inputs/Outputs, including 8 direct LED driving Outputs
- 3 Inputs for keyboard scan (KBY0-2)
- Up to 4 high voltage outputs (BSW0-3)
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- Up to Four 6-bit PWM D/A Converters
- 62.5kHz Output pin
- 14 bit counter for voltage synthesis tuning (ST63156, ST63140)
- AFC A/D converter with 0.5V resolution
- Four interrupt vectors (IRIN/NMI, Timer 1 & 2, VSYNC.)
- On-chip clock oscillator
- 5 Lines by 15 Characters On-Screen Display Generator with 128 Characters (2 banks)
- These EPROM and OTP versions are fully pin to pin compatible with their respective ROM versions
- The development tool of the ST631xx microcontrollers consists of the ST63TVS-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.
- EPROM programming board ST63E1XX-EPB



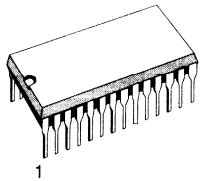
CDIP40W



CDIP28W



PDIP40



PDIP28

September 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 3. ST631xx family Block Diagram

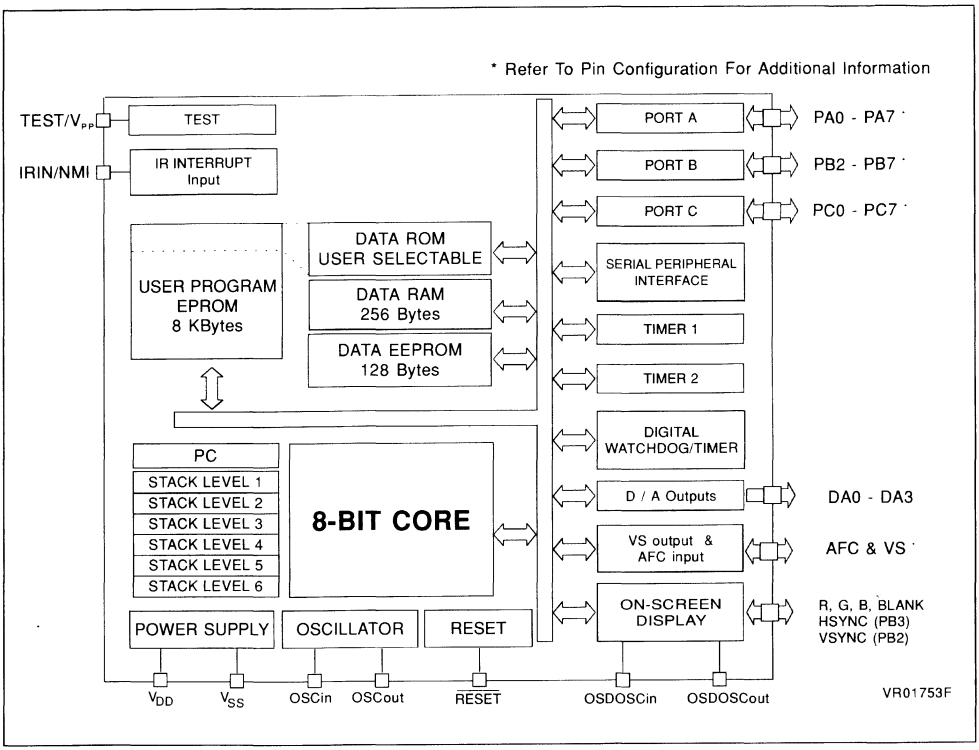


Table 1. Device Summary

DEVICE	EPROM (Bytes)	OTP ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	I/O	KBY I/O	BSW OUT	AFC	VS	D/A	PACK.	TARGET ROM DEVICES
ST63E140	8K		256	128	6	3	3	YES	YES	1	PDIP28	ST63140
ST63T140		8K	256	128	6	3	3	YES	YES	1	PDIP28	ST63140
ST63E142	8K		256	128	6	3	3	YES	NO	1	PDIP28	ST63142
ST631T42		8K	256	128	6	3	3	YES	NO	1	PDIP28	ST63142
ST63E126	8K		256	128	12	3	4	YES	NO	4	PDIP40	ST63126
ST63T126		8K	256	128	12	3	4	YES	NO	4	PDIP40	ST63126
ST63E156	8K		256	128	11	3	4	YES	YES	4	PDIP40	ST63156
ST63T156		8K	256	128	11	3	4	YES	YES	4	PDIP40	ST63156

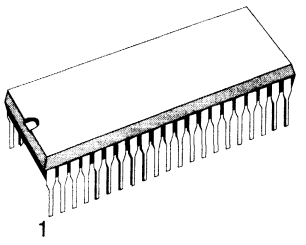
SGS-THOMSON MICROELECTRONICS

ST6369

8-BIT HCMOS MCU FOR DIGITAL CONTROLLED MULTI FREQUENCY MONITOR

PRELIMINARY DATA

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program ROM: 7948 bytes
- Reserved Test ROM: 244 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 40-Pin Dual in Line Plastic Package
- Up to 23 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- One 14-Bit PWM D/A Converter
- Six 6-Bit PWM D/A Converters
- One A/D converter with 0.5V resolution
- Five interrupt vectors (HSYNC/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- ST6369 is supported by pin-to-pin EPROM and OTP versions.
- The development tool of the ST6369 microcontroller consists of the ST6369-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.



PDIP40

DEVICE SUMMARY

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	D/A Conv.
ST6369	8K	256	384	7

February 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 2. ST6369 Block Diagram

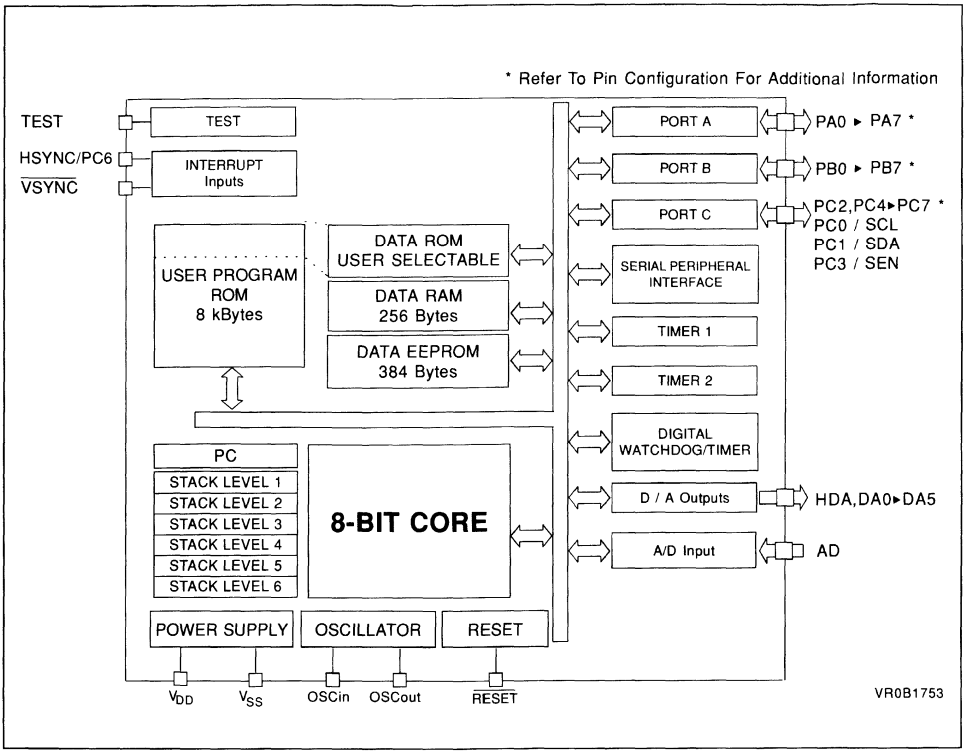


Table 1. Device Summary

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	A/D	14-bit D/A	6-bit D/A	EMULATING DEVICES
ST6369	8K	256	384	1	1	6	ST63E69, ST63T69

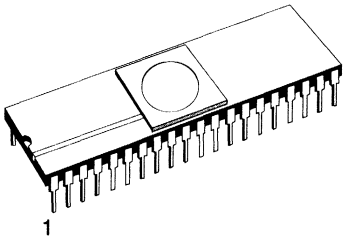
SGS-THOMSON MICROELECTRONICS

ST63E69
ST63T69

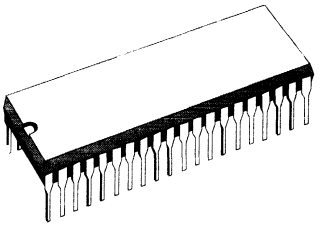
8-BIT EPROM HCMOS MCUs FOR DIGITAL CONTROLLED MULTI FREQUENCY MONITOR

PRELIMINARY DATA

- 4.5 to 6V supply operating range
- 8MHz Maximum Clock Frequency
- User Program EPROM: 7948 bytes
- Reserved Test EPROM: 244 bytes
- Data ROM: user selectable size
- Data RAM: 256 bytes
- Data EEPROM: 384 bytes
- 40-Pin Ceramic Dual in Line Package for EPROM version
- 40-Pin Plastic Dual in Line Package for OTP version
- Up to 23 software programmable general purpose Inputs/Outputs, including 2 direct LED driving Outputs
- Two Timers each including an 8-bit counter with a 7-bit programmable prescaler
- Digital Watchdog Function
- Serial Peripheral Interface (SPI) supporting S-BUS/ I^2C BUS and standard serial protocols
- One 14-Bit PWM D/A Converter
- Six 6-Bit PWM D/A Converters
- One A/D converter with 0.5V resolution
- Five interrupt vectors (HSYNC/NMI, Timer 1 & 2, VSYNC, PWR INT.)
- On-chip clock oscillator
- These EPROM and OTP versions are fully pin to pin compatible with ST6369 ROM version.
- The development tool of the ST6369 microcontrollers consists of the ST6369-EMU emulation and development system to be connected via a standard RS232 serial line to an MS-DOS Personal Computer.
- EPROM programming board ST6369-EPB



CDIP40W



PDIP40

DEVICE SUMMARY

EPROM DEVICE	OTP DEVICE	EPROM (Bytes)	EEPROM (Bytes)	D/A Converter
ST63E69	ST63T69	8K	384	7

February 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

Figure 2. ST63E69, T69 Block Diagram

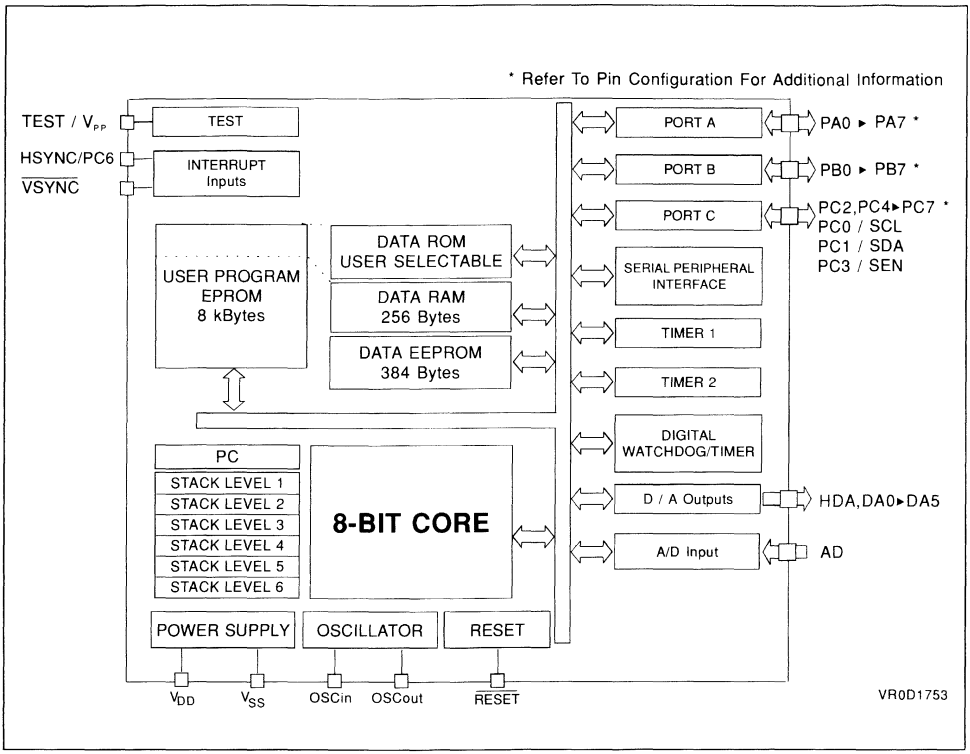


Table 1. Device Summary

DEVICE	EPROM (Bytes)	OTPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	A/D	14-bit D/A	6-bit D/A	TARGET ROM DEVICE
ST63E69	8K		256	384	1	1	6	ST6369
ST63T69		8K	256	384	1	1	6	ST6369

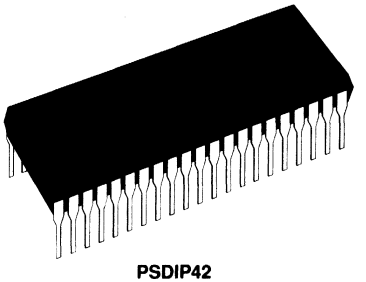
SGS-THOMSON MICROELECTRONICS

ST7271

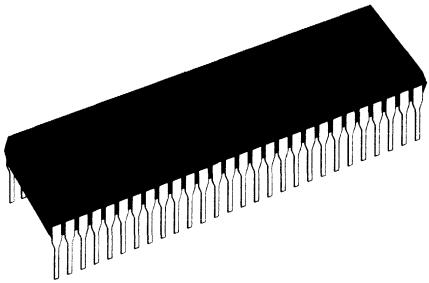
8-BIT HCMOS MCUs WITH EEPROM AND TV/MONITOR DEDICATED FUNCTIONS

PRELIMINARY DATA

- 5V ± 10% supply operating range
- 4MHz Maximum Internal Clock Frequency
- Fully static operation
- 0 to +70°C Operating Temperature Range
- Run, Wait, and Stop Modes
- User ROM: up to 15144 bytes
  Data RAM: up to 256 bytes
  EEPROM: up to 512 bytes
  Sync Processor EEPROM: 256 bytes
- 56 pin Shrink Dual In Line Package (ST7271N)
  42 pin Shrink Dual In Line Package (ST7271J)
- up to 25 I/O lines
  8 I/O Open Drain with 12V capability
- up to 8 lines programmable as interrupt wake-up inputs
- 16-bit timer with 2 input captures and 2 output compares
- Sync Processor for video timing analysis
- East/West Pin Cushion Automatic Correction with DAC output.
- Watchdog for system reliability and integrity
- 8-bit Analog to Digital Converter with up to 8 channels
- 16 10-bit PWM/BRM Digital to Analog outputs
- 2 12-bit PWM/BRM Digital to Analog outputs
- Industry Standard Serial Peripheral Interface
- User mask options:
  - SPI Data Rate
  - Watchdog enable/disable after Reset
  - Watchdog enable during WAIT mode
- Master Reset and Power-on reset
- Full Hardware Emulator
- 8-bit data manipulation
- 74 basic instructions
- 10 main addressing modes
- 8x8 unsigned multiply instruction
- true bit manipulation
- Complete development support on Real-time emulator with PC/DOS
- Full software package (Cross Assembler, debugger)



PSDIP42



PSDIP56

DEVICE SUMMARY

DEVICE	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	PACKAGE
ST7271N5	16K	256	512	PSDIP56
ST7271N3	12K	256	512	PSDIP56
ST7271N1	8K	192	384	PSDIP56
ST7271J1	8K	192	384	PSDIP42

October 1993

This is Preliminary information from SGS-THOMSON. Details are subject to change without notice.

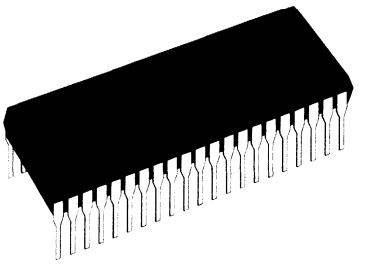
SGS-THOMSON MICROELECTRONICS

ST9291

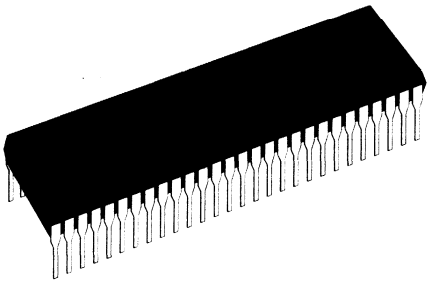
8-32K ROM HCMOS MCU WITH ON SCREEN DISPLAY AND VOLTAGE TUNING OUTPUT

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 8 to 32K bytes of ROM, 128/640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package or 56-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 32 (42 pin package) / 42 (56 pin package) fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- 14-bit Voltage Synthesis for tuning reference voltage
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42



PSDIP56

August 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1.1 GENERAL DESCRIPTION

The ST9291 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development.

The nucleus of the ST9291 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9291 with up to 32/42 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

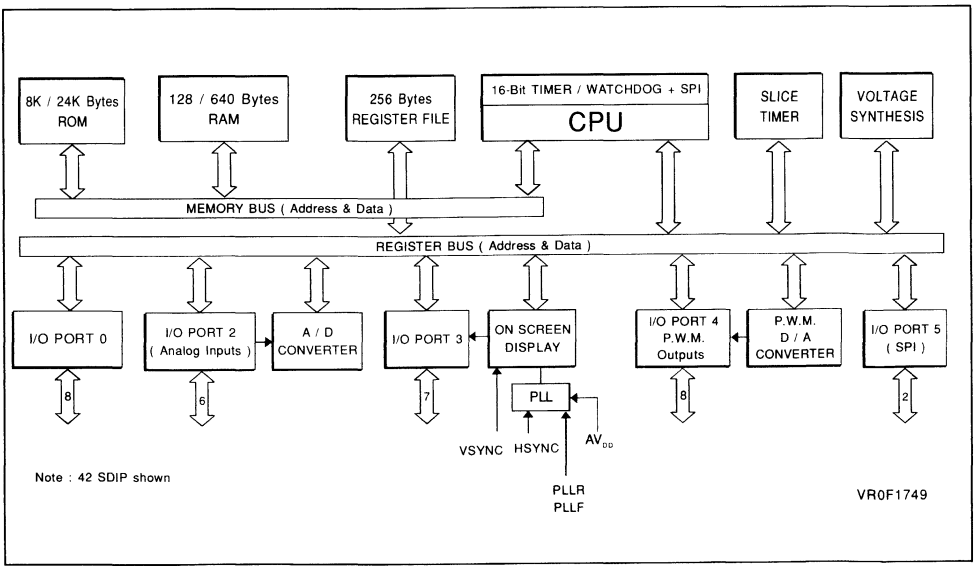
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler.

The human interface is provided by the On Screen Display module, this can produce up to 15 lines of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

14-bit Voltage Synthesis using the PWM (Pulse Width Modulation)/BRM (Bit Rate Modulation) technique to generate tuning voltages for low-mid range TV set applications. The tuning voltage is output on one of two separate output pins.

Figure 1-2. ST9291 Block Diagram



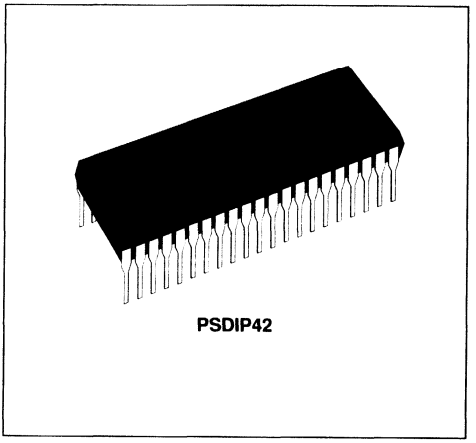
SGS-THOMSON MICROELECTRONICS

ST9293

48K ROM HCMOS MCUs WITH ON SCREEN DISPLAY AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16 to 48K bytes of ROM, 256 to 768 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 4 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42

DEVICE SUMMARY

Device	ROM	RAM	PACKAGE
ST9293J7	48K	768	PSDIP42
ST9293J5	32K	640	PSDIP42
ST9293J3	24K	512	PSDIP42
ST9293J1	16K	256	PSDIP42

May 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1.1GENERAL DESCRIPTION

The ST9293 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as standalone microcontrollers with 48K/32K/24K/16 bytes of on-chip ROM.

The nucleus of the ST9293 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9293 with up to 31/41 I/O lines dedicated to digital Input/Output.

These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

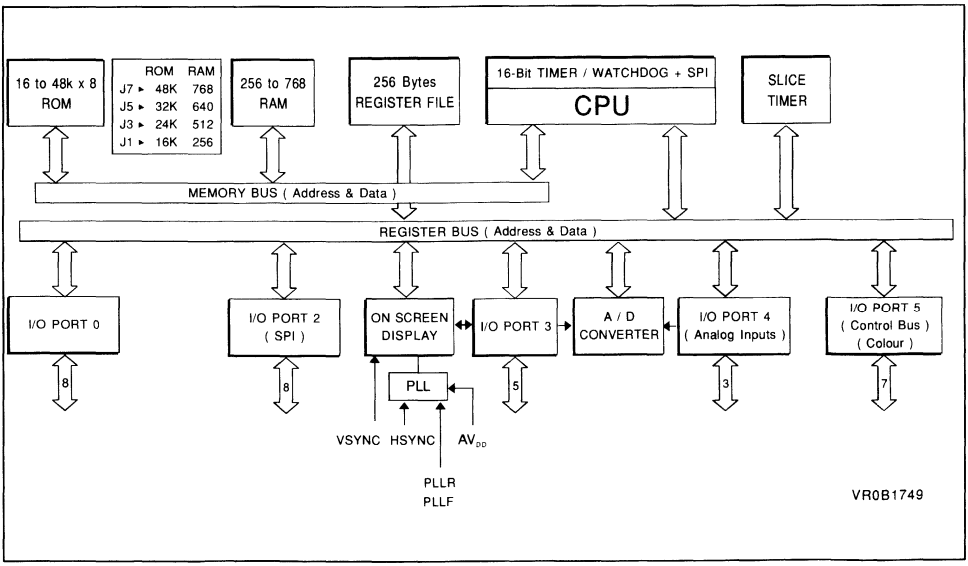
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler and 6 operating modes allows simple use for waveform-generation and measurement, PWM functions and many other system timing functions.

The human interface is provided by the On Screen Display module, this can produce up to 8 lines of of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.5µs conversion time and 6-bit guaranteed resolution.

Figure 1-2. ST9293 Block Diagram



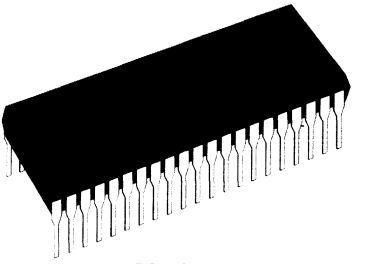
SGS-THOMSON MICROELECTRONICS

ST9294

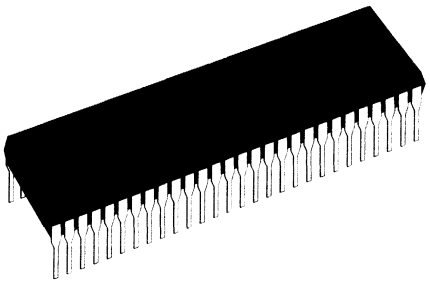
24K ROM HCMOS MCU WITH ON SCREEN DISPLAY AND CLOSED-CAPTION DATA SLICER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 12 to 32K bytes of ROM, 384/640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Shrink DIP package or 56-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 (42 pin package) / 42 (56 pin package) fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- Digital Data Slicer extracting closed caption data from video
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



PSDIP42



PSDIP56

May 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1.1 GENERAL DESCRIPTION

The ST9294 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development.

The nucleus of the ST9294 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9294 with up to 31/42 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

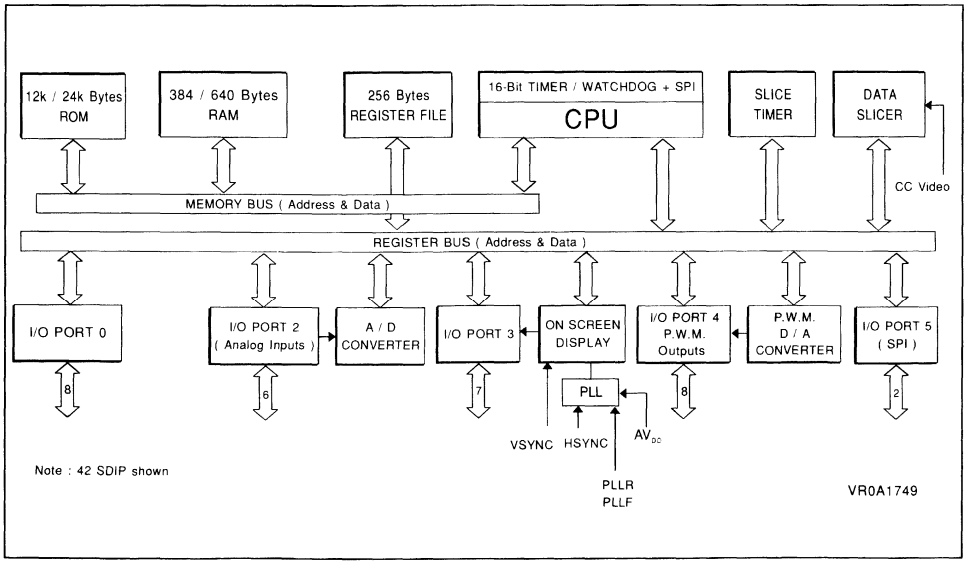
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler.

The human interface is provided by the On Screen Display module, this can produce up to 15 lines of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

Closed Caption control for the display of information transmitted through the video input is facilitated with the Data Slicer. This module has manual and automatic Slicing levels for both Sync and Data and allows the user to select the video line containing the data relative to the Vertical synchronisation pulse.

Figure 1-2. ST9294 Block Diagram



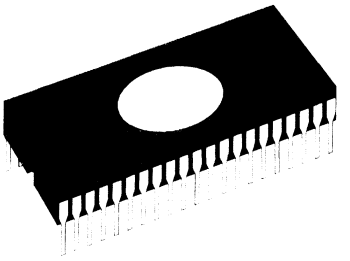
SGS-THOMSON MICROELECTRONICS

ST92E93
ST92T93

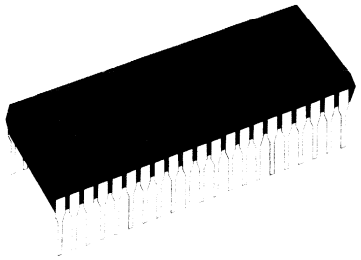
48K/32K EPROM AND OTP HCMOS MCUs WITH ON SCREEN DISPLAY AND CLOSED-CAPTION DATA SLICER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 48K/32K bytes of EPROM, 768/640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead Window Ceramic Shrink DIP package for ST92E93
- 42-lead Plastic Shrink DIP package for ST92T93
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 4 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9293 ROM device



CSDIP42-W



PSDIP42

May 1993

This is Preliminary Information from SGS-THOMSON. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST92E93 is an EPROM member in windowed ceramic (E) and plastic OTP (T) packages of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9293 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST92E93 may be used for the prototyping and pre-production phases of development.

The nucleus of the ST92E93 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92E93 with up to 31 I/O lines dedicated to digital Input/Output.

These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software-control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

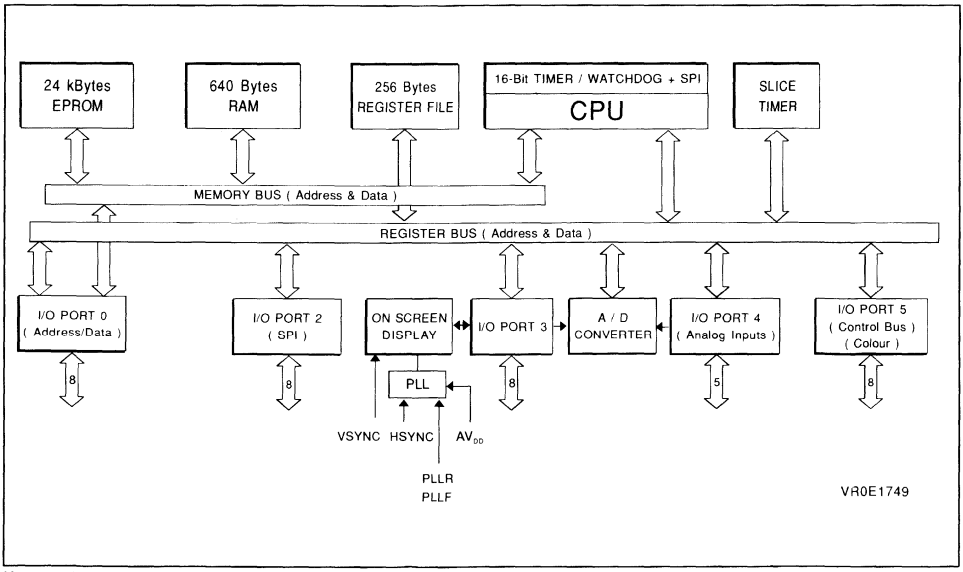
Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler and 6 operating modes allows simple use for waveform-generation and measurement, PWM functions and many other system timing functions.

The human interface is provided by the On Screen Display module, this can produce up to 8 lines of of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.5µs conversion time and 6-bit guaranteed resolution.

Figure 2.ST92E93 Block Diagram



Note : Refer to Table 1 for ST92E94 I/O Port Summary

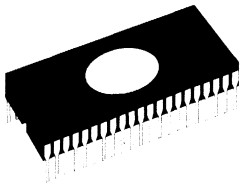
SGS-THOMSON MICROELECTRONICS

ST92E94
ST92T94

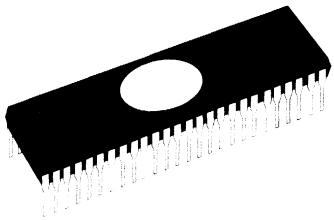
24K EPROM HCMOS MCUs WITH ON SCREEN DISPLAY AND CLOSED-CAPTION DATA SLICER

PRELIMINARY DATA

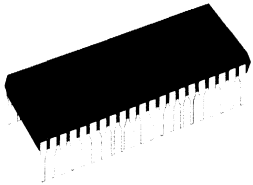
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 24K bytes of EPROM, 640 bytes of RAM, 224 general purpose registers available as RAM, accumulators or index registers (Register File)
- 42-lead or 56-lead Window Ceramic Shrink DIP package for ST92E94
- 42-lead or 56-lead Plastic Shrink DIP package for ST92T94
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 (42 pin package) / 42 (56 pin package) fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- Digital Data Slicer extracting closed caption data from video
- 8 8-bit PWM D/A outputs with repetition frequency 2 to 32kHz and 12V Open Drain Capability
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 3 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9294 ROM device



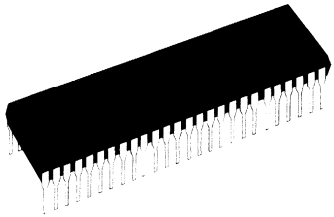
CSDIP42-W



CSDIP56-W



PSDIP42



PSDIP56

May 1993

This is Preliminary Information from SGS-THOMSON. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST92E94 are EPROM members in windowed ceramic (E) and plastic OTP (T) packages, completely of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

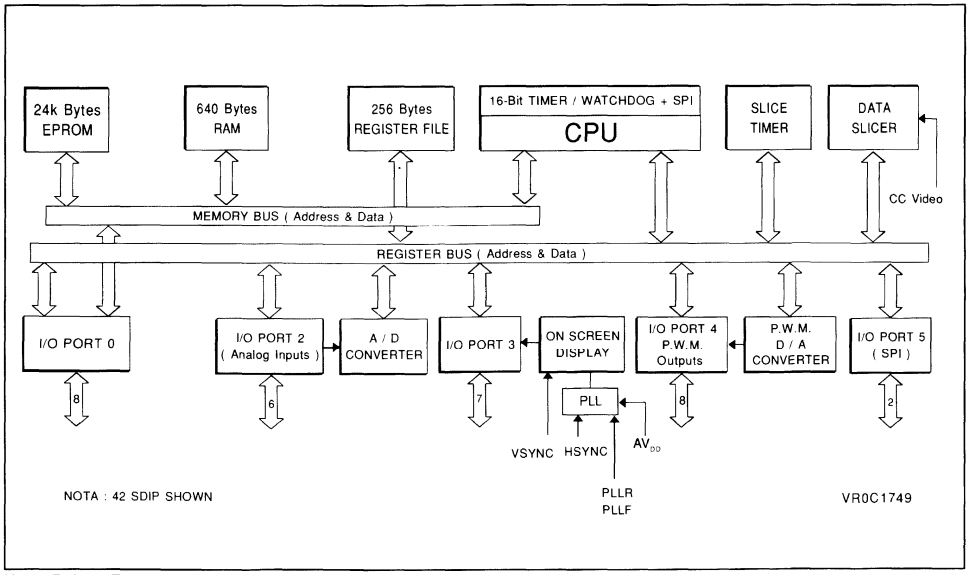
THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9294 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST92E94 may be used for the prototyping and pre-production phases of development.

The nucleus of the ST92E94 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92E94 with up to 31/42 I/O lines dedicated to digital Input/Output. These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

Figure 2.ST92E94 Block Diagram



Note : Refer to Table 1 for ST92E94 I/O Port Summary

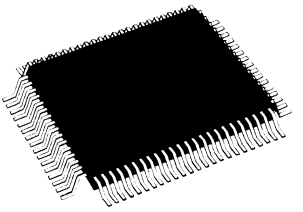
SGS-THOMSON MICROELECTRONICS

ST90R51

ROMLESS HCMOS MCU WITH BANKSWITCH

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time : 500ns (12MHz internal)
- 224 general purpose registers available as RAM, accumulators or index pointers (register file)
- ROMless to allow maximum external memory flexibility
- Bankswitch logic allowing a maximum addressing capability of 8Mbytes for Program and Dataspace (16Mbytes total)
- 80-pin Plastic Quad Flat Pack package
- DMA controller, Interrupt handler and a Serial Peripheral Interface as standard features
- 54 fully programmable I/O ports
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Three 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- Two Serial Communication Interfaces with asynchronous and synchronous capability
- Rich Instruction Set with 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development Tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9054, 32K ROM device (also available in windowed and One Time Programmable EPROM packages).



PQFP80

March 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1.1 GENERAL DESCRIPTION

The ST90R51 is a Romless member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The Romless part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility

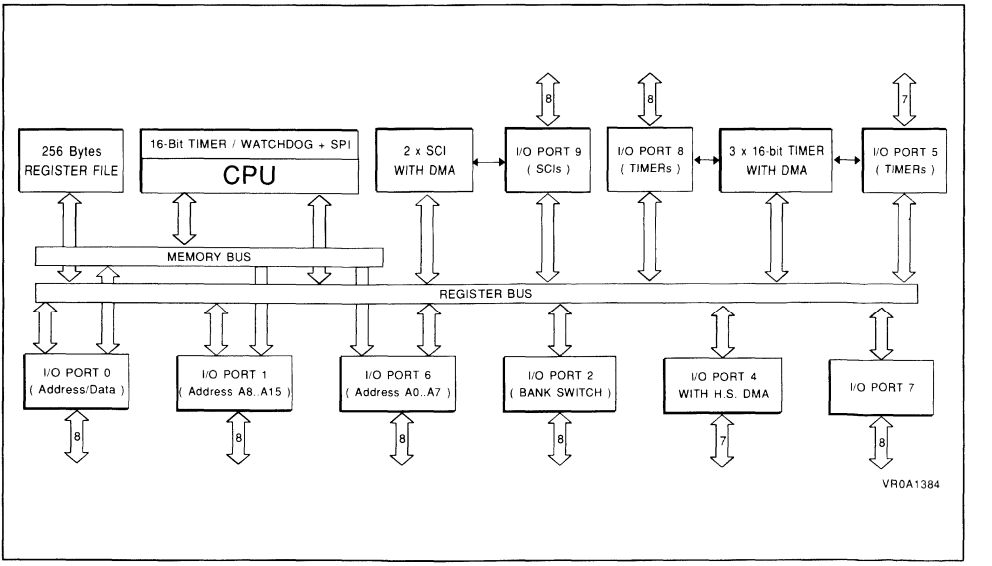
The nucleus of the ST90R51 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R51 with 54 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing to the external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the internal Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device are 2 full duplex Serial Communications Interfaces with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 2.ST90R51 Block Diagram



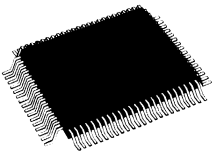
SGS-THOMSON MICROELECTRONICS

ST90R91

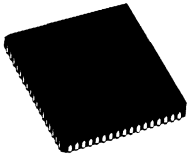
ROMLESS HCMOS MCU WITH BANKSWITCH AND A/D CONVERTER

PRELIMINARY DATA

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time : 500ns (12MHz internal)
- ROMless to allow maximum external memory flexibility
- 1536 bytes of internal RAM
- 224 general purpose registers available as RAM, accumulators or index pointers (register file)
- Bankswitch logic allowing a maximum addressing capability of up to 2Mbytes for Program and Dataspace
- 80-pin PQFP package for ST90R91Q
- 68-pin PLCC package for ST90R91C
- DMA controller, Interrupt handler and a Serial Peripheral Interface as standard features
- Up to 32 fully programmable I/O ports
- Up to 7 external plus 1 non-maskable interrupts
- 16-bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit Slice Timer with 8 bit Prescaler
- 16-bit Multifunction Timer, with 8 bit prescaler and 13 operating modes
- 4 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Rich Instruction Set with 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development Tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System



PQFP80



PLCC68

September 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

1.1 GENERAL DESCRIPTION

The ST90R91 is a Romless member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The Romless part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility

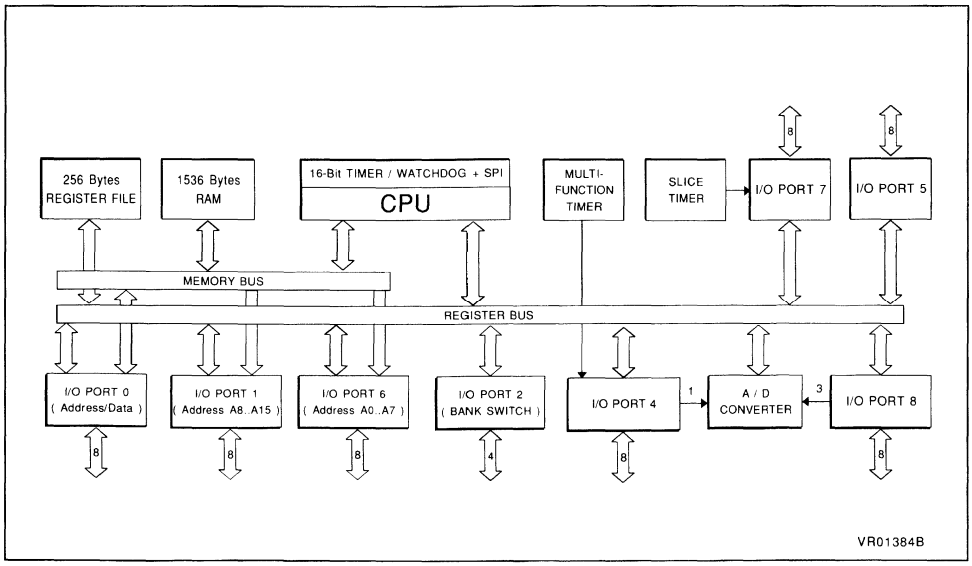
The nucleus of the ST90R91 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R91 with up to 32 I/O lines dedicated to digital Input/Output. These lines are grouped into nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing to the external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the internal Register File, which includes the control and status registers of the on-chip peripherals.

A 16 bit MultiFunction Timer, with an 8 bit Prescaler and 13 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 4 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is the Slice Timer, capable of generating PWM signals and simple timing functions.

Figure 1-3. ST90R91 Block Diagram



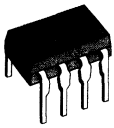
PACKAGES

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DDIP8.TBL

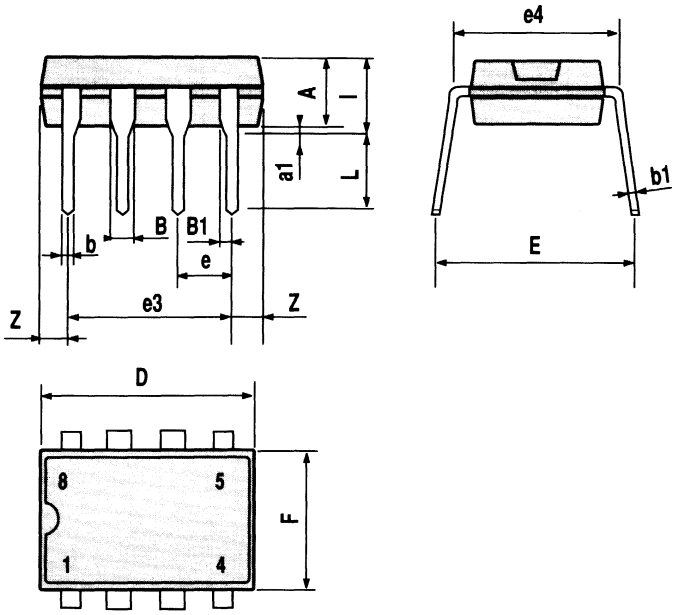
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP8.EPS

DIP8



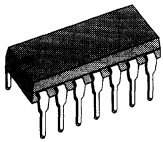
PM-DIP8.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DDIP14.TBL

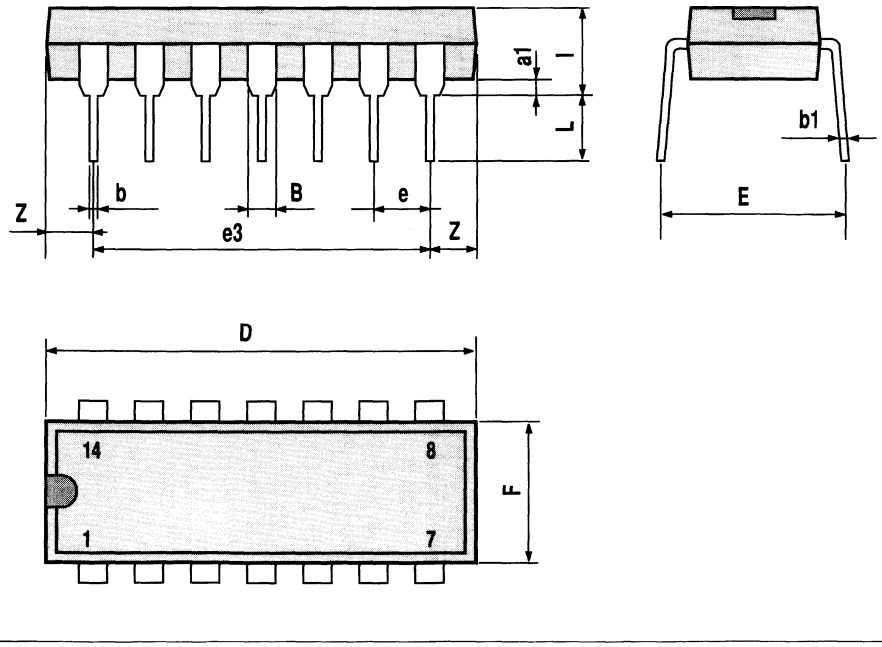
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP14.EPS

DIP14



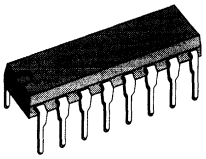
PM-DIP14.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DDIP16.TBL

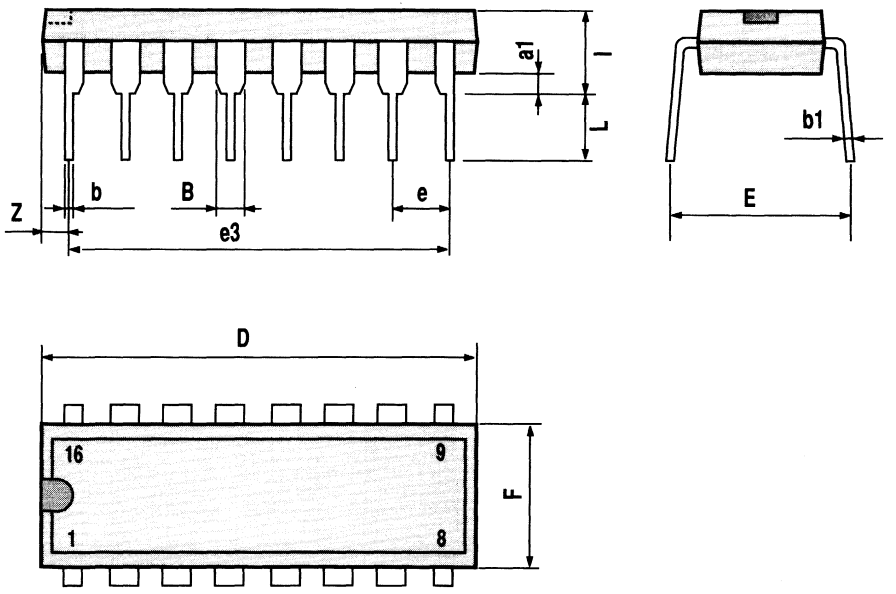
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP16.EPS

DIP16 / BATWING DIP16



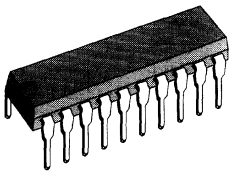
PM-DIP16.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.064
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.914
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
i			3.93			0.155
L		3.3			0.130	

DDIP18.TBL

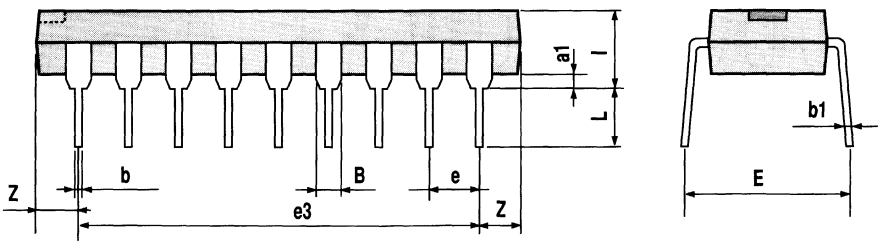
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18.EPS

DIP18



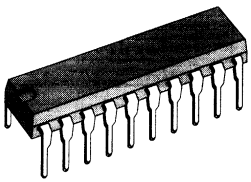
PM-DIP18.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

DDIP20.TBL

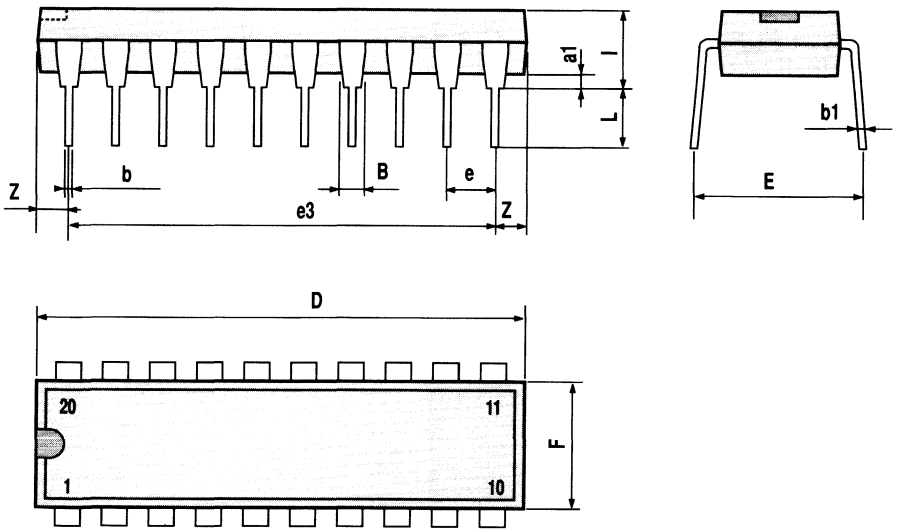
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20.EPS

DIP20



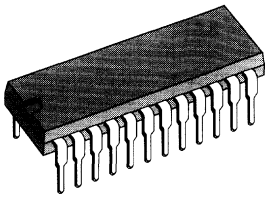
PM-DIP20.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DDIP24.TBL

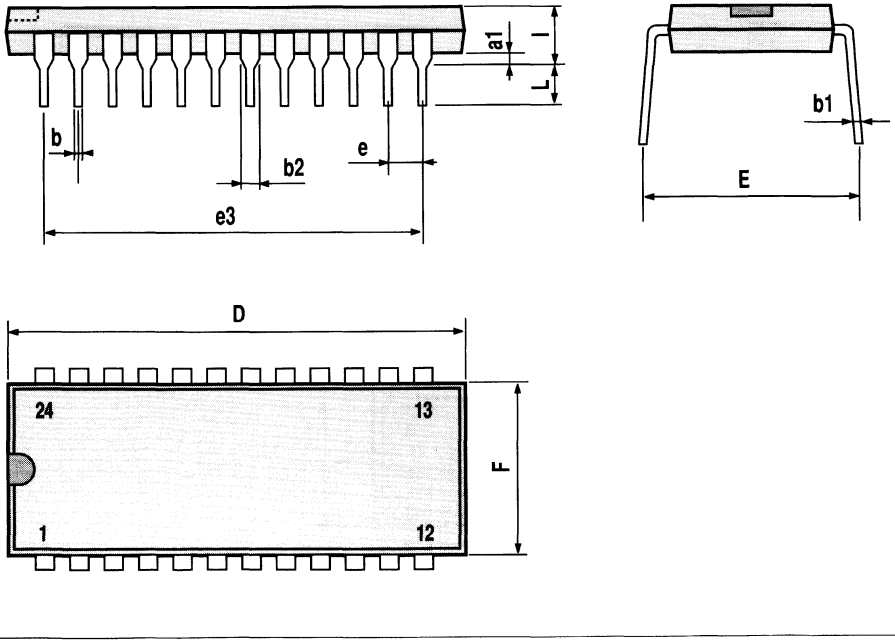
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP24.EPS

DIP24



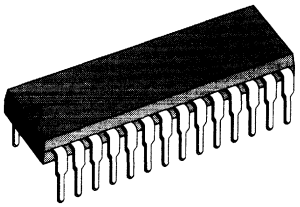
PM-DIP24.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.4			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DDIP28.TBL

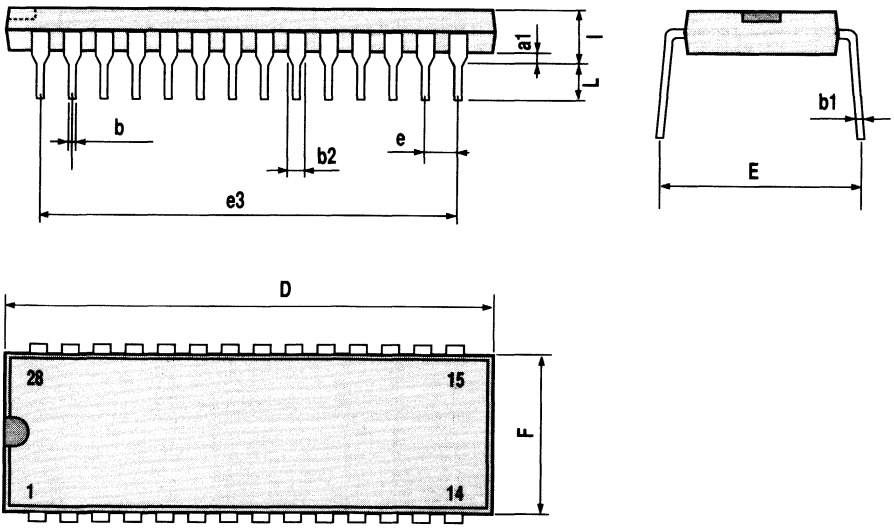
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP28.EPS

DIP28



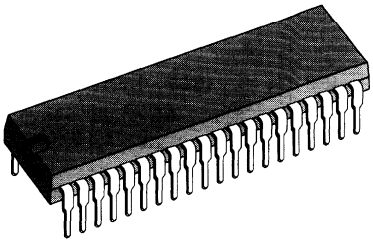
PM-DIP28.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DDIP40.TBL

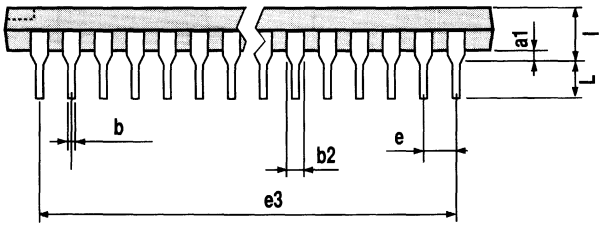
SGS-THOMSON MICROELECTRONICS

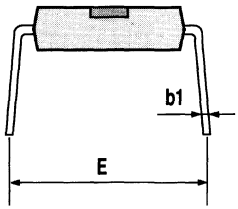
OUTLINE AND MECHANICAL DATA

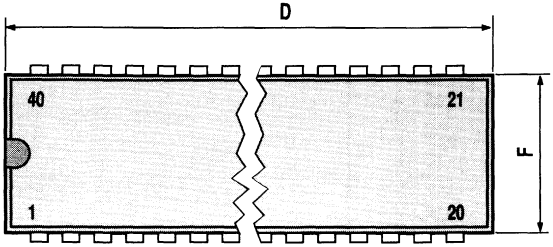


DIP40.EPS

DIP40







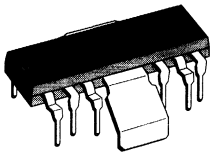
PM-DIP40.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.8		4.05	0.150		0.159
a1	1.5		1.75	0.059		0.069
b	0.55		0.6	0.022		0.024
b1	0.3		0.35	0.012		0.014
c		1.32			0.052	
c1		0.94			0.037	
D	19.2		19.9	0.756		0.783
E	16.8	17.2	17.6	0.661	0.677	0.693
E1	4.86		5.56	0.191		0.219
E2	10.11		10.81	0.398		0.426
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	17.43	17.78	18.13	0.686	0.700	0.714
e4		7.62			0.300	
e5	7.27	7.62	7.97	0.286	0.300	0.314
e6	12.35	12.7	13.05	0.486	0.500	0.514
F	6.3		7.1	0.248		0.280
G		9.8			0.386	
I	7.8		8.6	0.307		0.339
K	6.1		6.5	0.240		0.256
L	2.5		2.9	0.098		0.114

DFINDIP-TBL

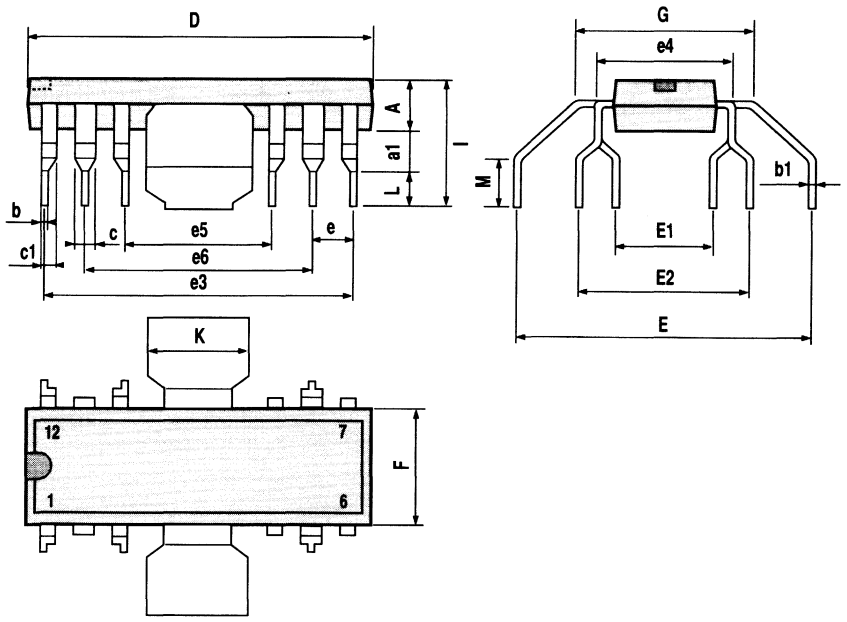
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



FINDIP

FINDIP.EPS



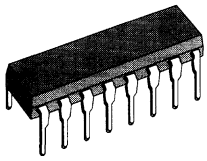
PM-FDIP.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DDIP16W.TBL

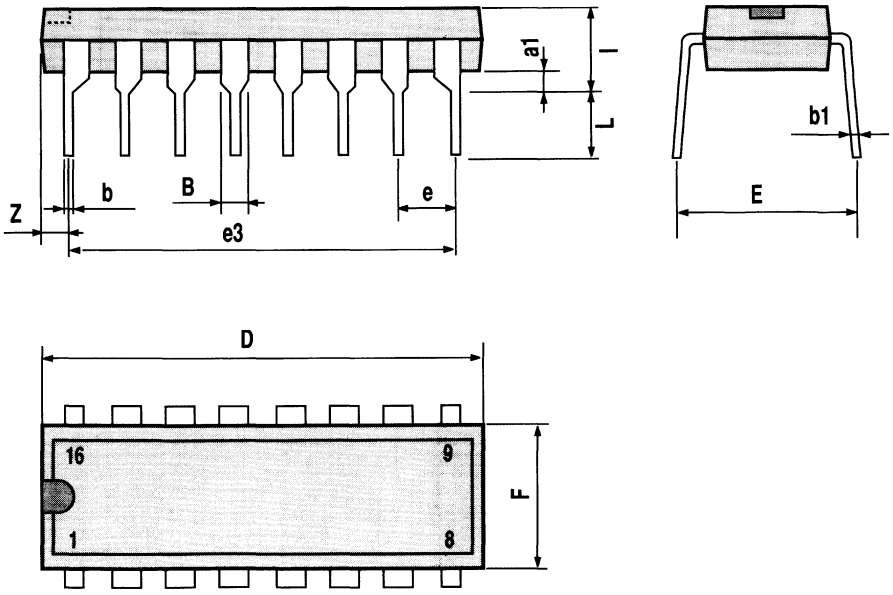
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP16.EPS

POWERDIP (8+8)



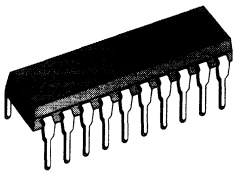
PMDIP16W.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

DDIP18W.TBL

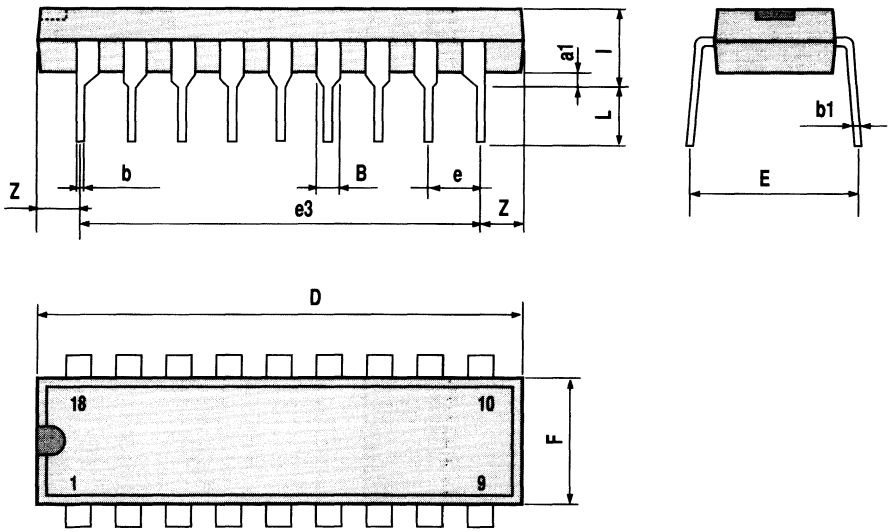
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP18.EPS

POWERDIP (9+9)



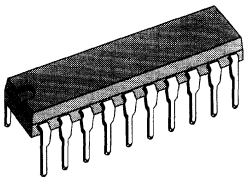
PMDIP18W.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DDIP20W.TBL

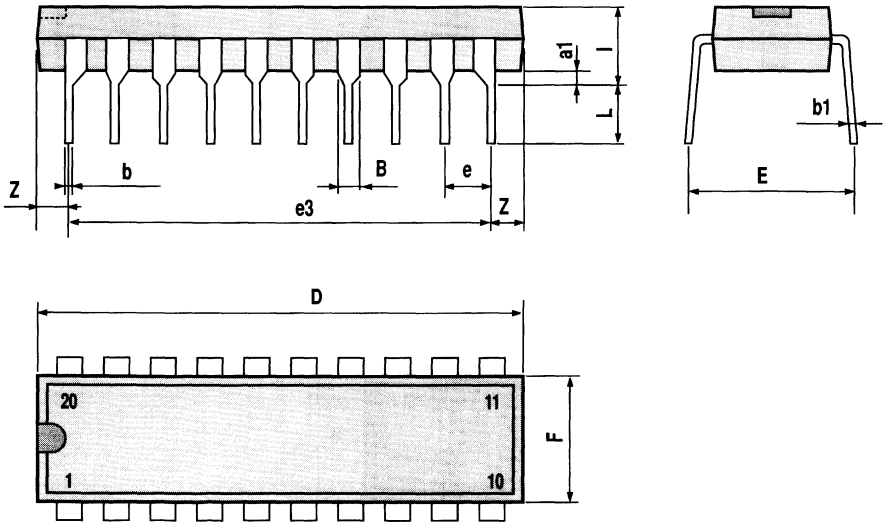
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20.EPS

POWERDIP (16+2+2)



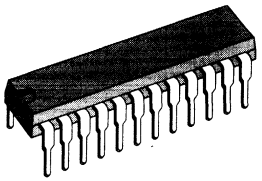
PMDIP20W.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.51			0.020		
b	0.35		0.59	0.014		0.023
b1	0.2		0.36	0.008		0.014
b2	0.75		1.42	0.030		0.056
b3	0.75			0.030		
D			23.11			0.910
E	7.95		9.73	0.313		0.383
e		1.778			0.070	
e3		19.558			0.770	
e4		7.62			0.300	
F			6.86			0270
i			5.08			0.200
L	2.54			0.100		

DSDIP24 TBL

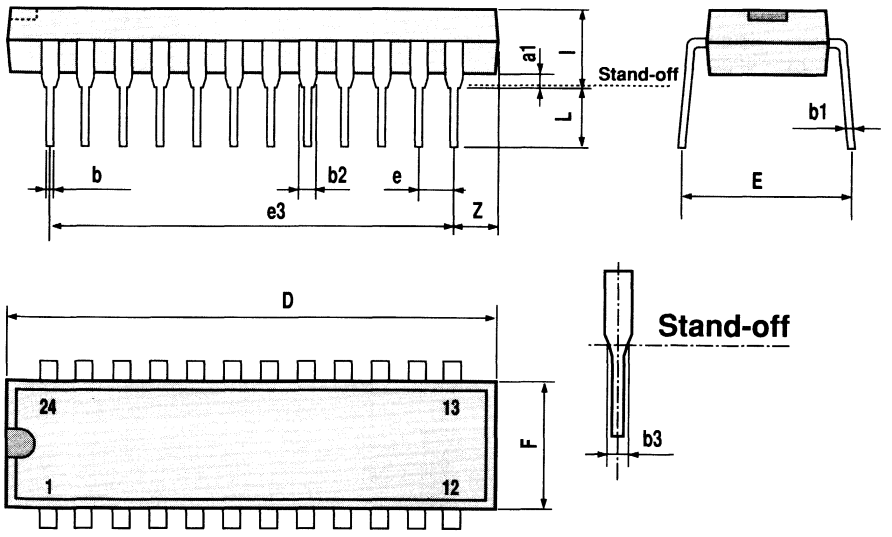
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SDIP24.EPS

SHRINK24



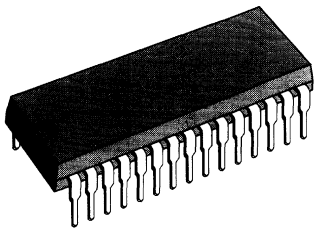
PMSDIP24.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.78			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0^o (min.), 15^o (max.)					
S	0.31			0.012		

DSDIP30.TBL

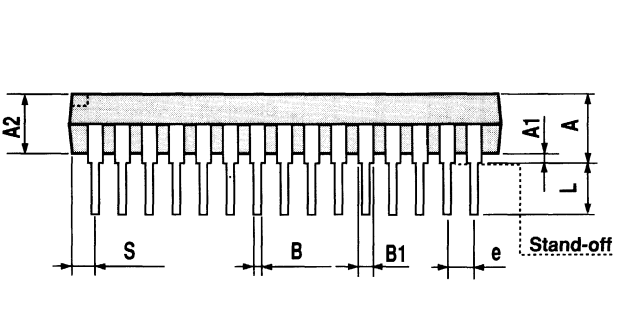
SGS-THOMSON MICROELECTRONICS

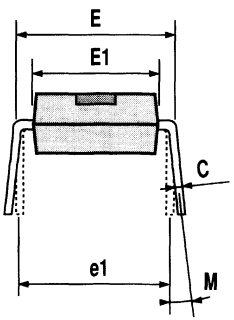
OUTLINE AND MECHANICAL DATA

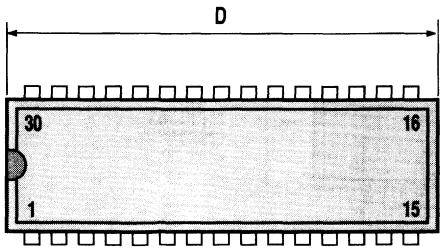


SDIP30.EPS

SHRINK30







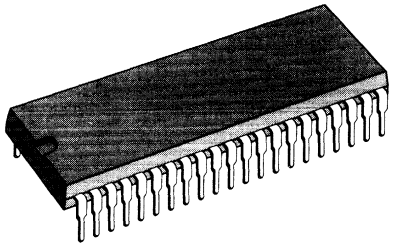
PMSDIP30.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

DSDIP42.TBL

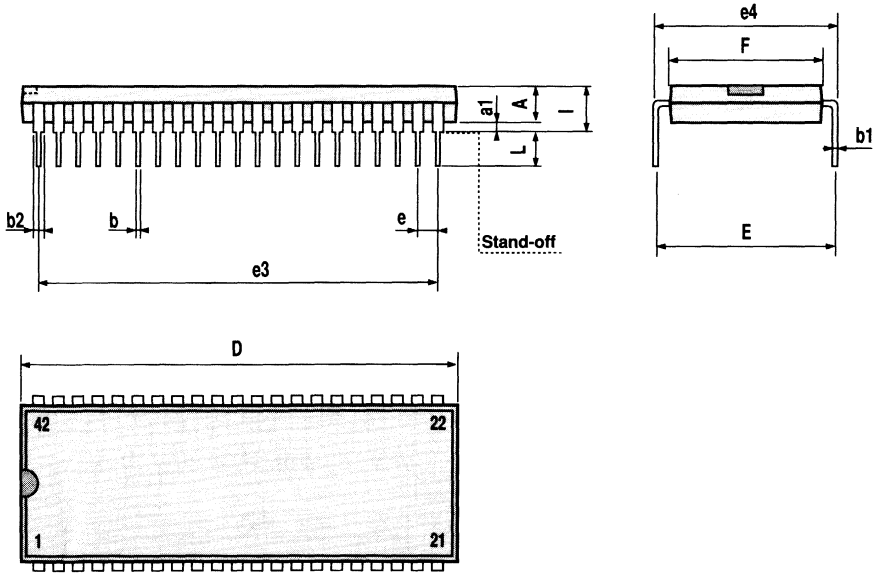
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SDIP42.EPS

SHRINK42



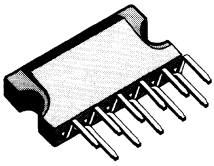
PMSDIP42.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.10			0.122
B			1.10			0.04
C		0.15			0.006	
D		1.50			0.059	
E		0.52			0.02	
F		0.80			0.03	
G		1.70			0.066	
G1		17			0.66	
H1		12.00			0.48	
H3		20.00			0.79	
L		17.90			0.70	
L1		14.40			0.57	
L2		11.00			0.43	
M		2.54			0.1	
M1		2.54			0.1	

DCPW11.TBL

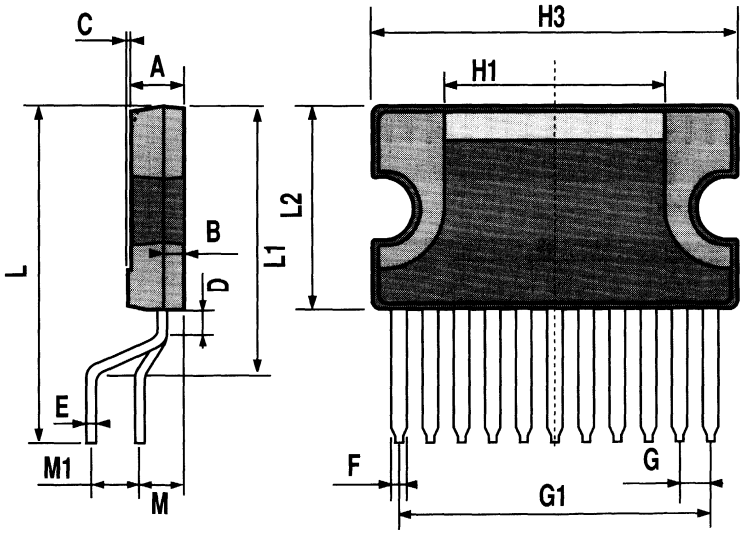
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



CPW11.EPS

CLIPWATT11



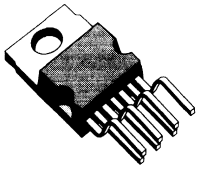
PM.CPW11.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		08	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

DHEPTV.TBL

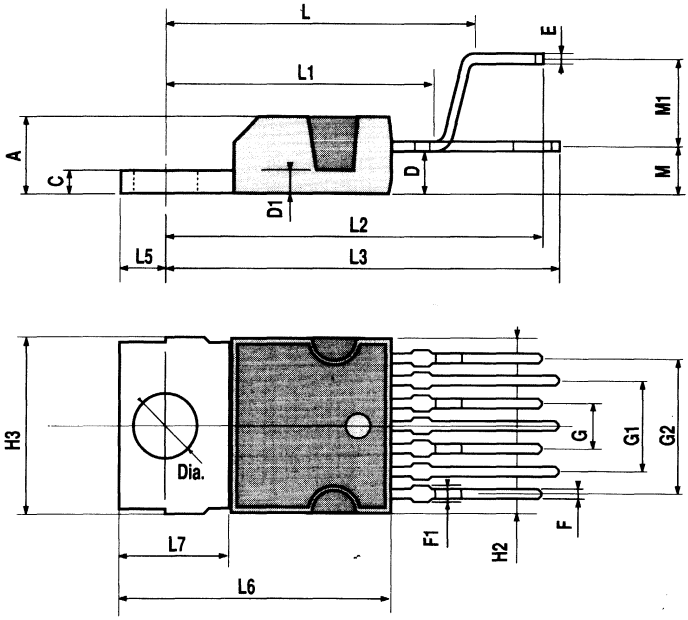
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



HEPTV.EPS

HEPTAWATT V



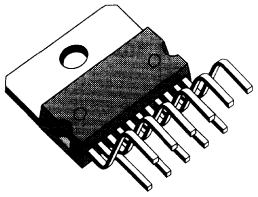
PM-HEPTV.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia. 1	3.65		3.85	0.144		0.152

DMUL15V.TBL

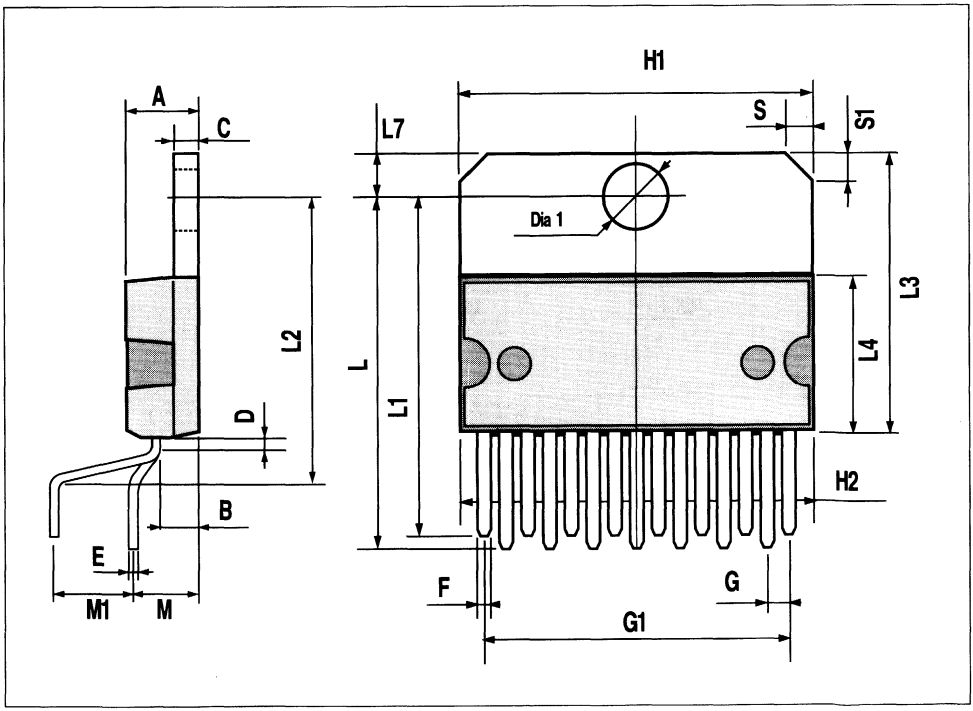
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



MUL15V.EPS

MULTIWATT 15V



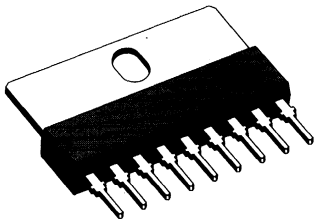
PMMUL15V.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

DSIP9.TBL

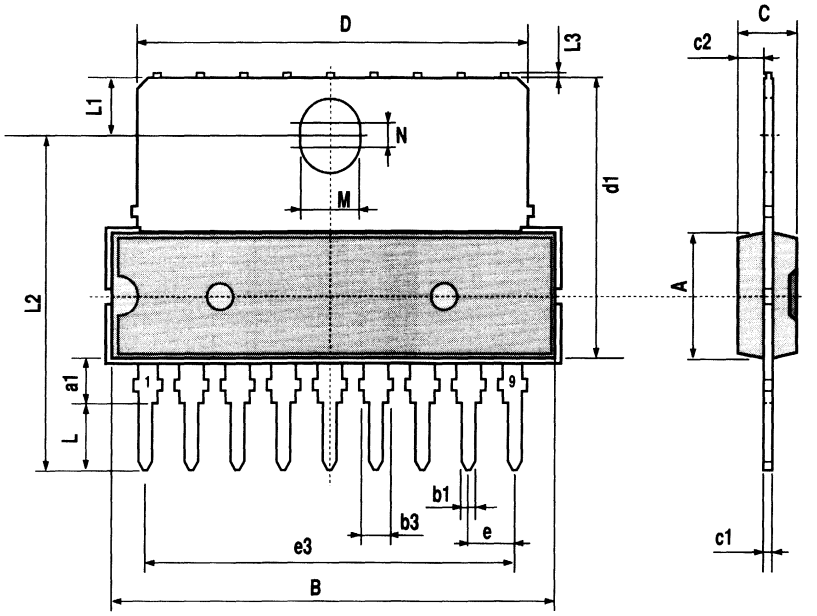
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SIP9

SIP9.EPS



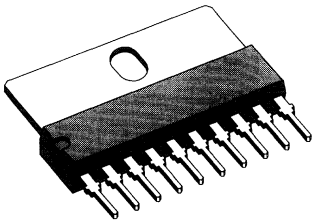
PM-SIP9.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			23.7			0.933
d1		14.5			0.571	
e		2.54			0.100	
e3		22.86			0.900	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

DSIP10.TBL

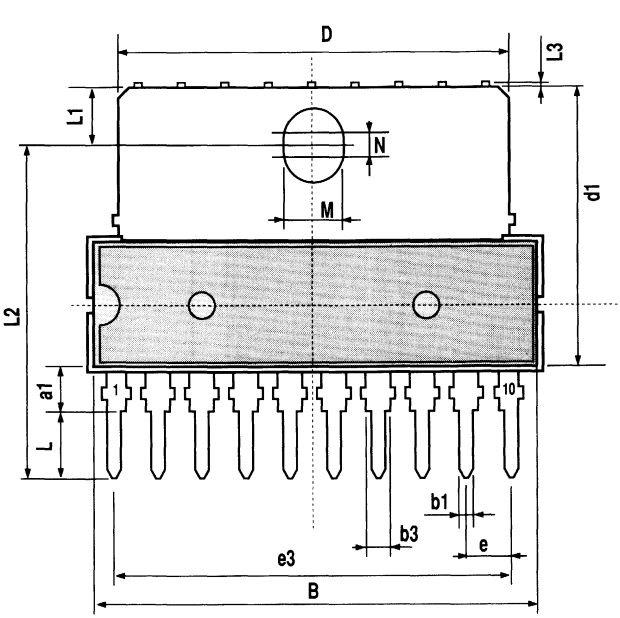
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SIP10.EPS

SIP10



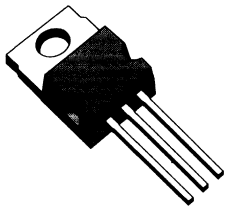
PM-SIP10.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F2	1.15		1.4	0.045		0.055
G	4.95	5.08	5.21	0.195	0.200	0.205
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L2		16.2			0.638	
L3	26.3	26.7	27.1	1.035	1.051	1.067
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
Dia.	3.65		3.85	0.144		0.152

DTO220.TBL

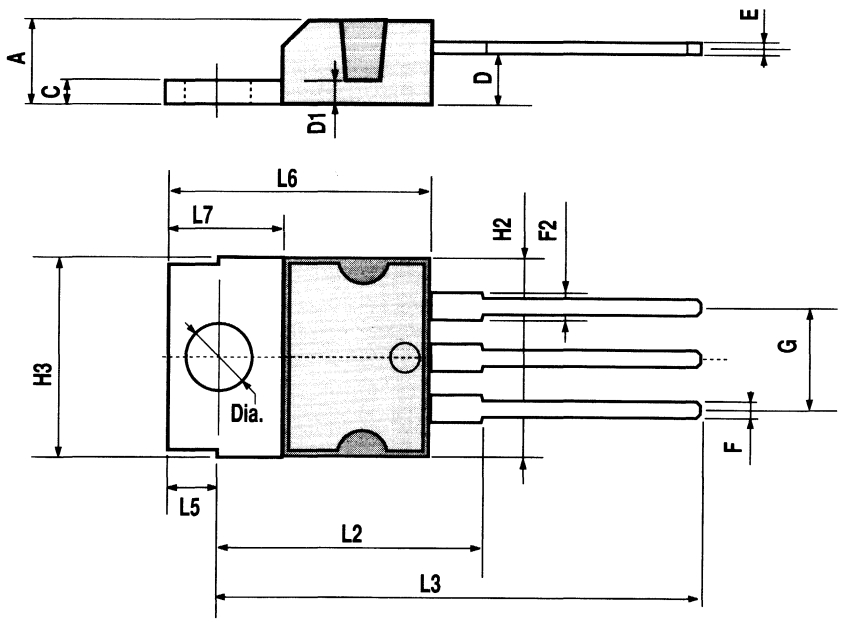
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



TO220.EPS

TO220



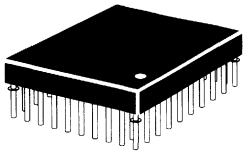
PM-TO220.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	22.05		22.31	0.868	0.878	
B	25.04		25.54	0.985	0.1000	
C	2.54			0.100		
D	2.54			0.100		
E	1.2		1.3	0.047	0.051	
F	0.46		0.51	0.018	0.020	
G	25.40		25.90	0.996	0.1007	
H	4.2			0.165		
I	3.8			0.149		

DPGA37.TBL

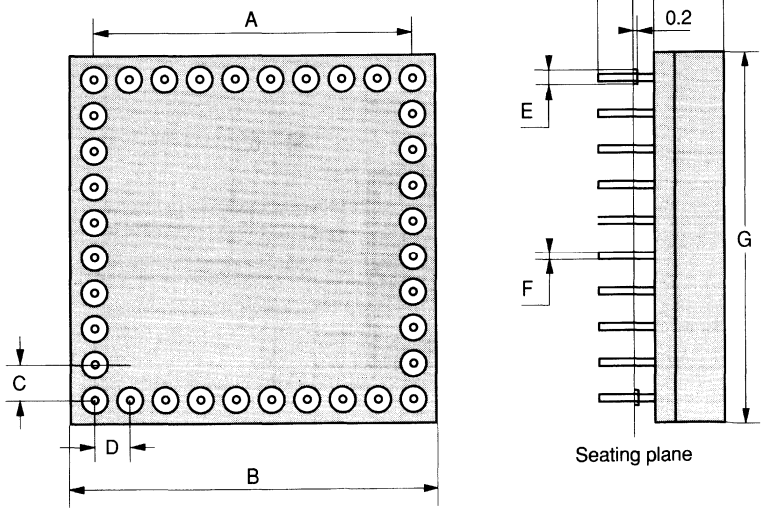
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PGA37.EPS

PGA37



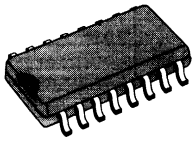
PM-PGA37

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.209
L	0.5		1.27	0.020		0.050
M			0.62			0.024
S	8° (max.)					

DSO16.TBL

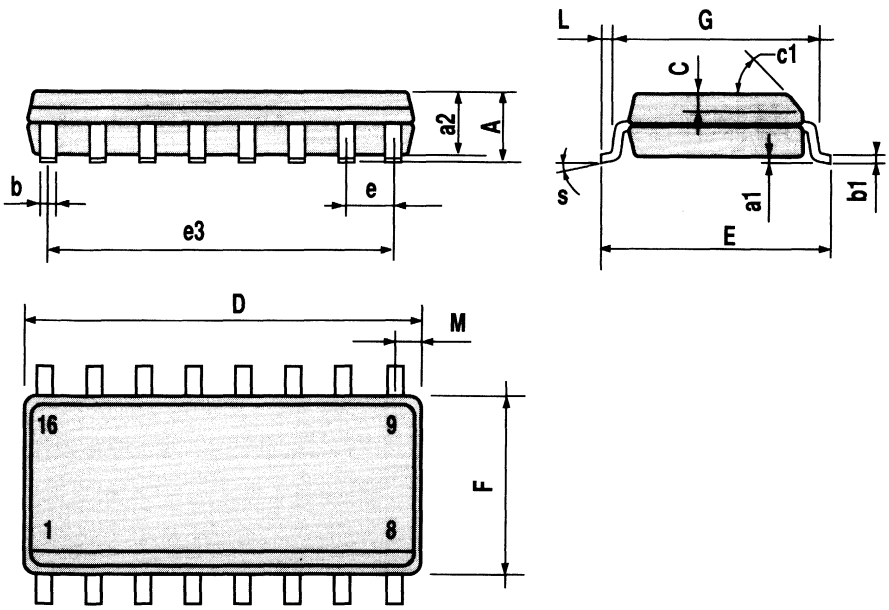
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16.EPS

SO16 J / SO16 Narrow



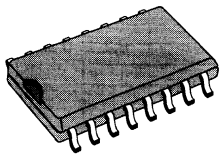
PM-SO16.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.19		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	10.1		10.5	0.397		0.413
E	10.0		10.65	0.393		0.419
e		1.27			0.050	
e3		8.89			0.350	
F	7.4		7.6	0.291		0.300
G	8.8		9.15	0.346		0.360
L	0.5		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					

DSO16L.TBL

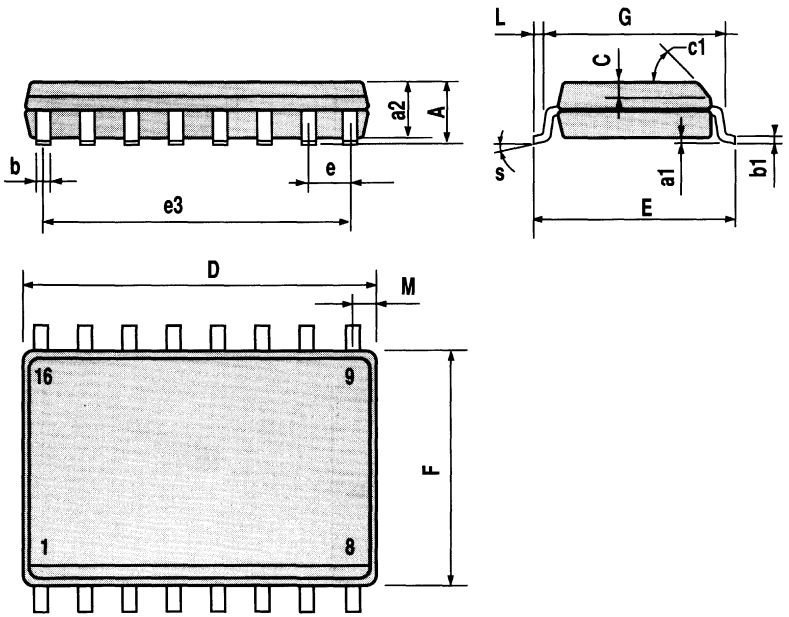
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO16L.EPS

SO16 Large



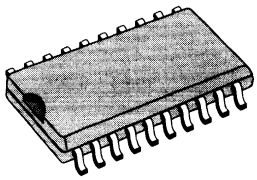
PM-SO16L.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

DSO20L.TBL

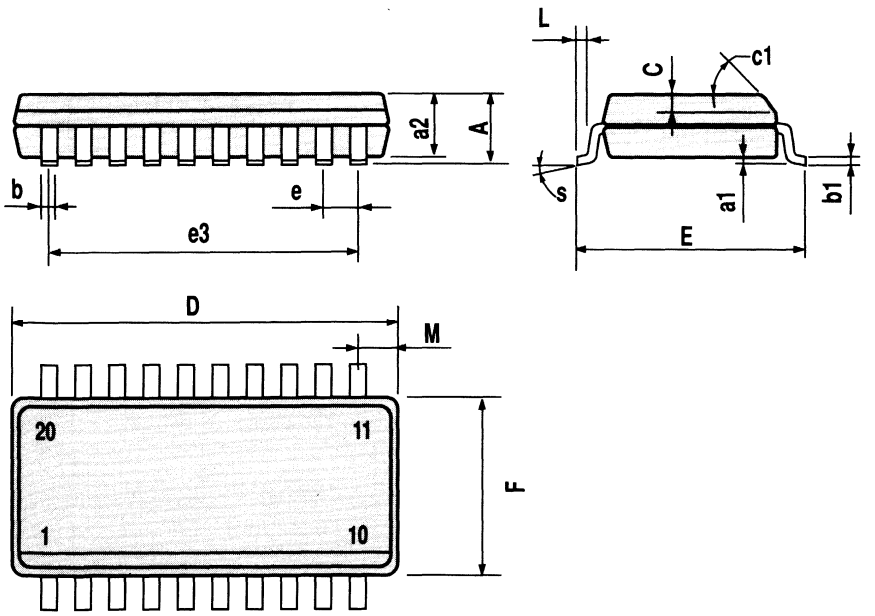
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20L.EPS

SO20 Large



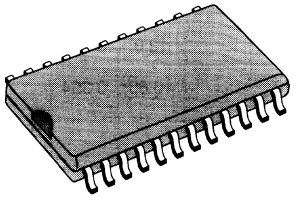
PM-SO20L.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	15.2		15.6	0.598		0614
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

DSO24.TBL

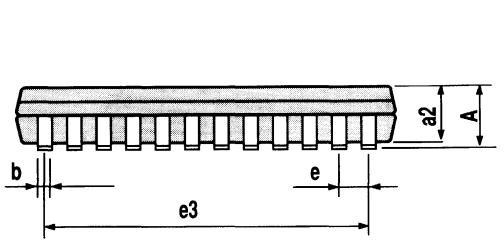
SGS-THOMSON MICROELECTRONICS

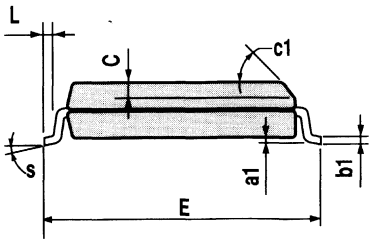
OUTLINE AND MECHANICAL DATA

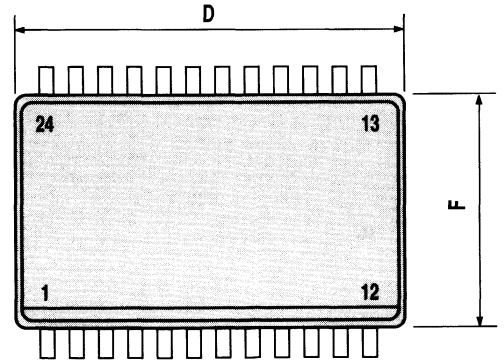


SO24.EPS

SO24 Large







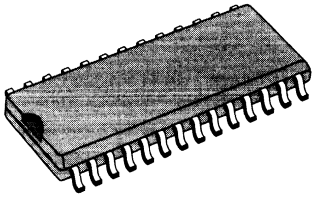
PM-SO24.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					

DSO28L.TBL

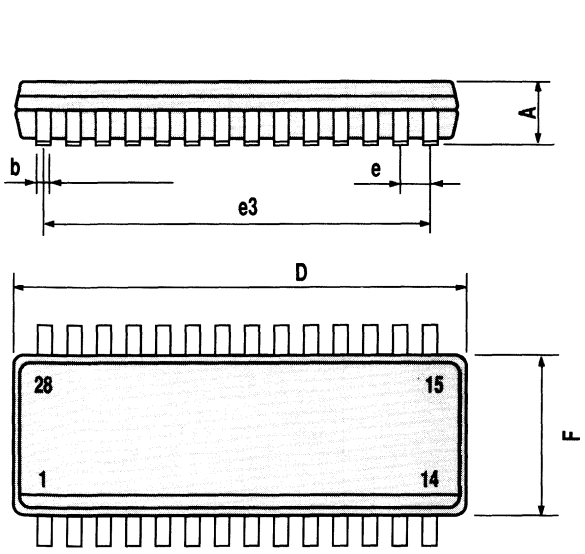
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28L.EPS

SO28 Large



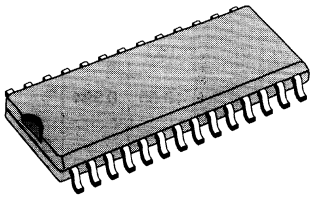
PM-SO28L.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.59			0.102
a1	0.05		0.20	0.002		0.008
b	0.31	0.41	0.51	0.012	0.016	0.020
b1	0.15		0.25	0.006		0.010
C		0.33			0.013	
D			18.13			0.714
E	10.11	10.31	10.51	0.399	0.406	0.414
e		1.27			0.050	
e3		16.51			0.65	
F	7.42	7.52	7.62	0.292	0.296	0.300
L	0.48	0.58	0.68	0.019	0.023	0.027
S	8^o (max.)					

DSO28B.TBL

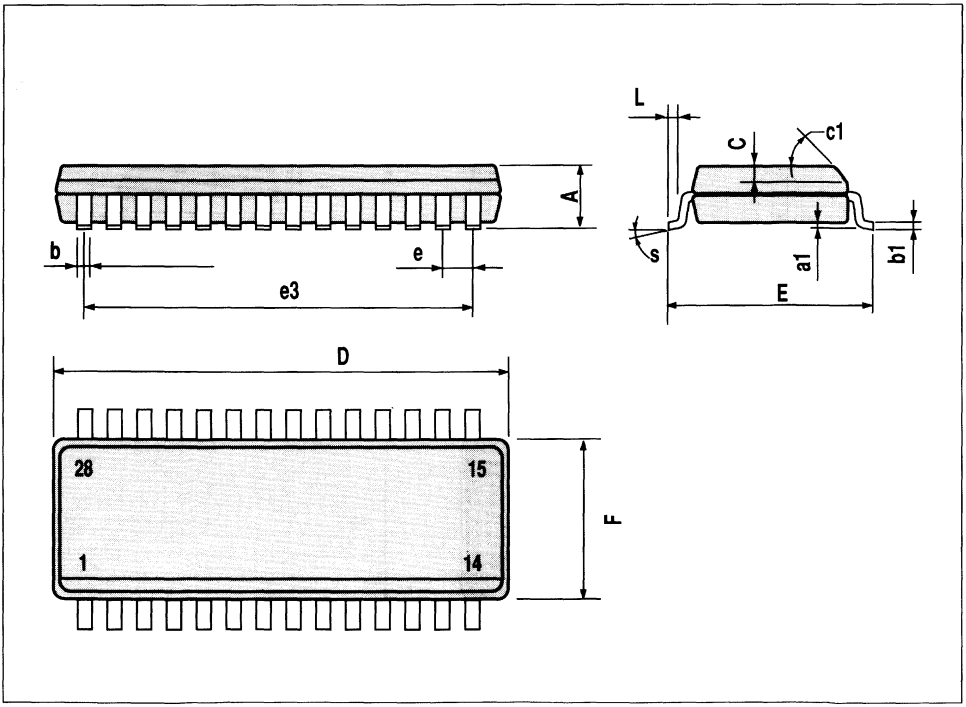
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO28L.EPS

SO28 Large version B



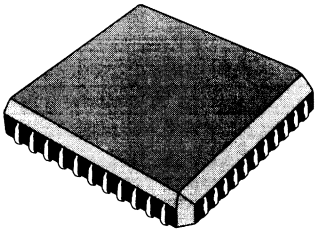
PM-SO28L.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

DPLCC44.TBL

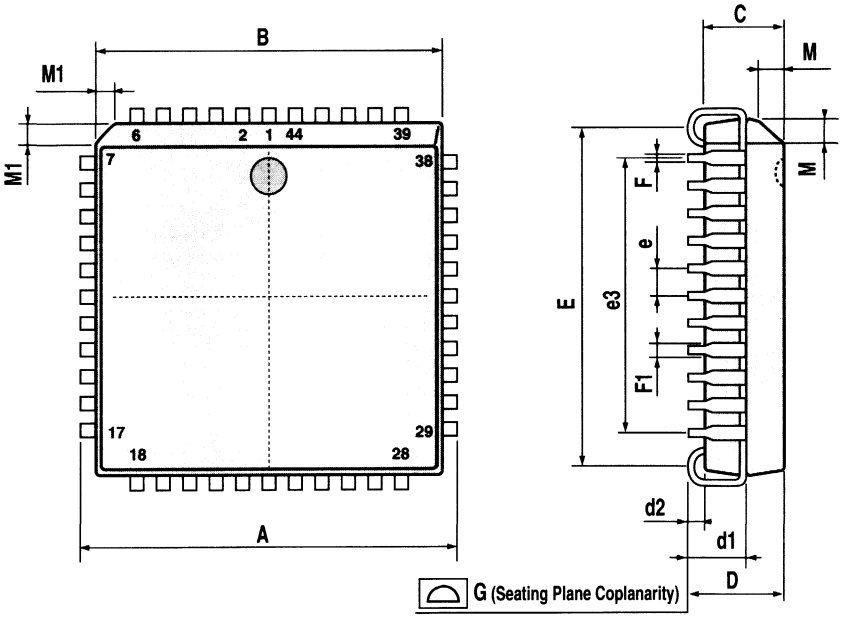
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC44.EPS

PLCC44



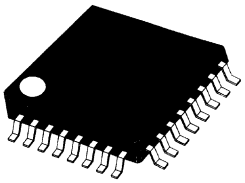
PMPLCC44.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.0145	0.0177
C	0.09		0.20	0.004		0.0078
D		9.00			0.354	
D1		7.00			0.276	
D3		5.60			0.220	
e		0.80			0.0314	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.60			0.220	
L	0.45	0.60	0.75	0.177	0.024	0.028
L1		1.00			0.039	
K	0^o (min.), 7^o (max.)					

DPQFP32.TBL

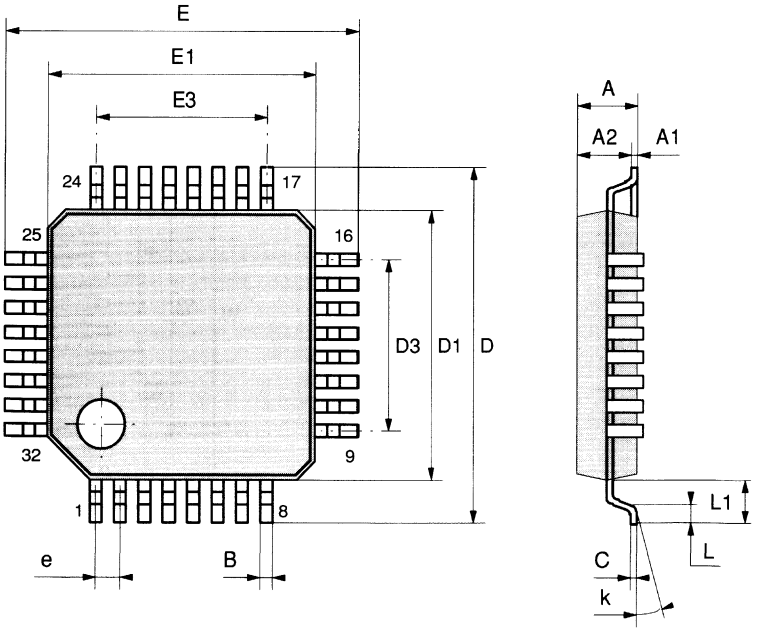
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP32.EPS

PQFP32



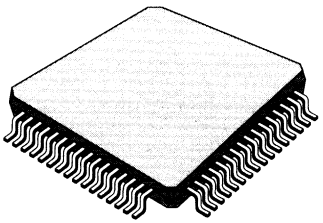
PMPQFP32.EPS

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.10	0.11	0.12
B	0.30		0.45	0.012		0.018
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D2		12.00			0.472	
e		0.80			0.031	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E2		12.00			0.472	
F		1.60			0.063	
K	0^o (min.), 7^o (max.)					
L	0.65	0.80	0.95	0.025	0.031	0.037

DPQFP64.TBL

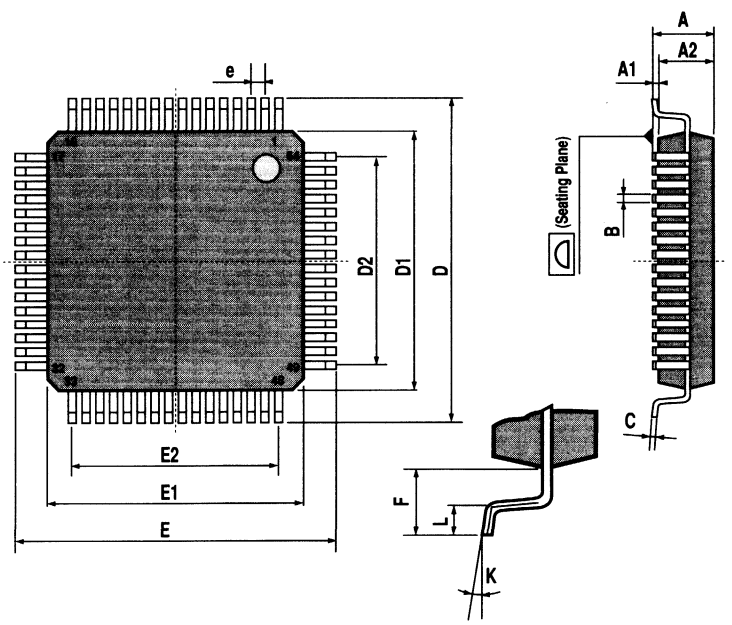
SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PQFP64.EPS

PQFP64



PMPQFP64.EPS

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